

1024-BIT STATIC RAM

2102L

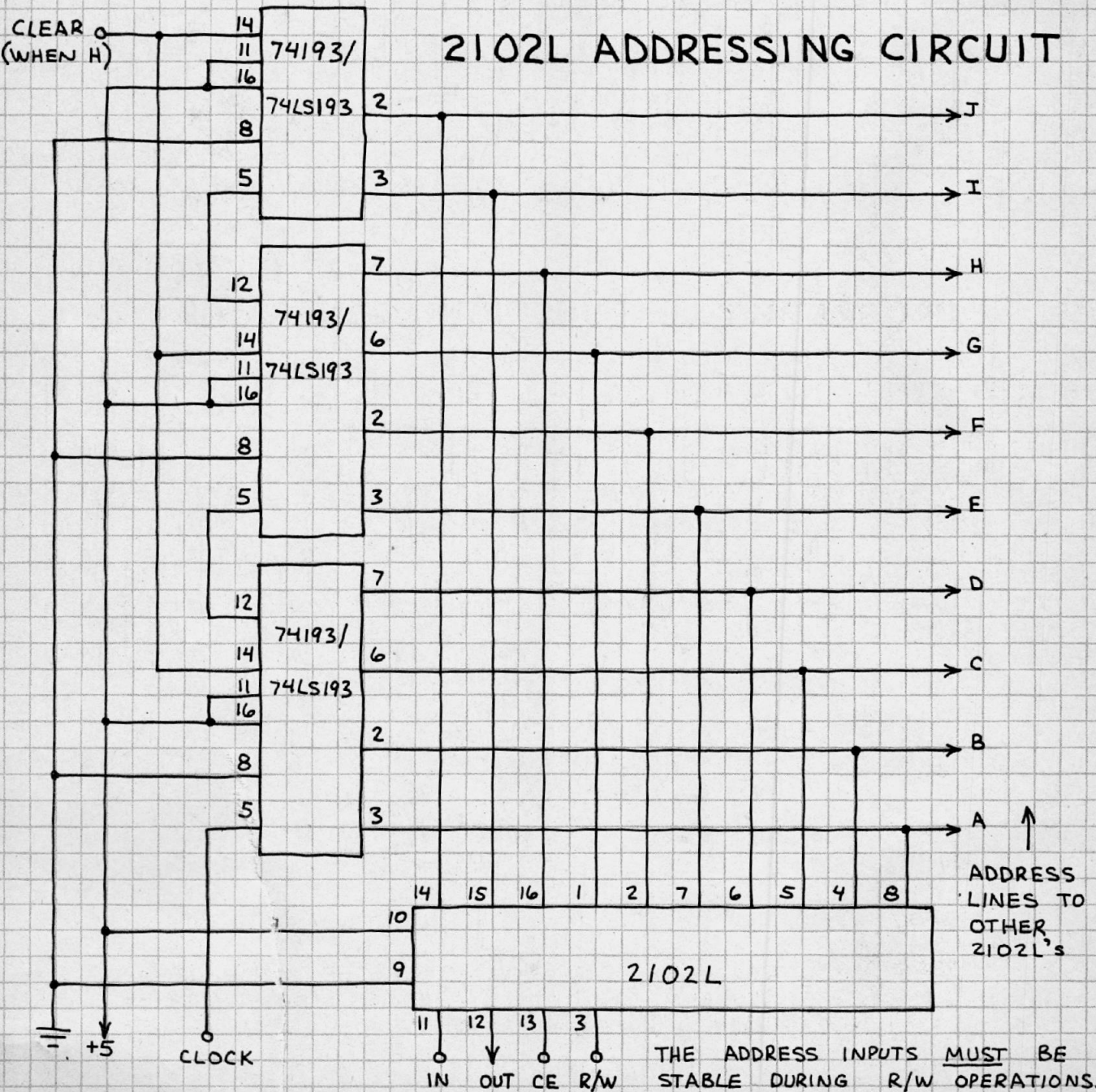
1024 1-BIT STORAGE LOCATIONS ADDRESSED BY PINS A0-A9. TTL/LS COMPATIBLE. CE (CHIP ENABLE) INPUT CONTROLS R/W (READ/WRITE) OPERATIONS). 3-STATE OUTPUTS.

A7	A8	A9	CE	OUT	IN	+5	GND
16	15	14	13	12	11	10	9

NOTE UNUSUAL LOCATION OF POWER SUPPLY PINS.
(A0-A9: ADDRESS INPUTS)

CE	R/W	OPERATION
L	L	WRITE (LOADS BIT AT PIN 11)
L	H	READ (OUTPUTS BIT AT PIN 12)
H	X	HI Z (OUTPUT ENTERS THIRD STATE)

1	2	3	4	5	6	7	8
A6	A5	R/w	A1	A2	A3	A4	A0



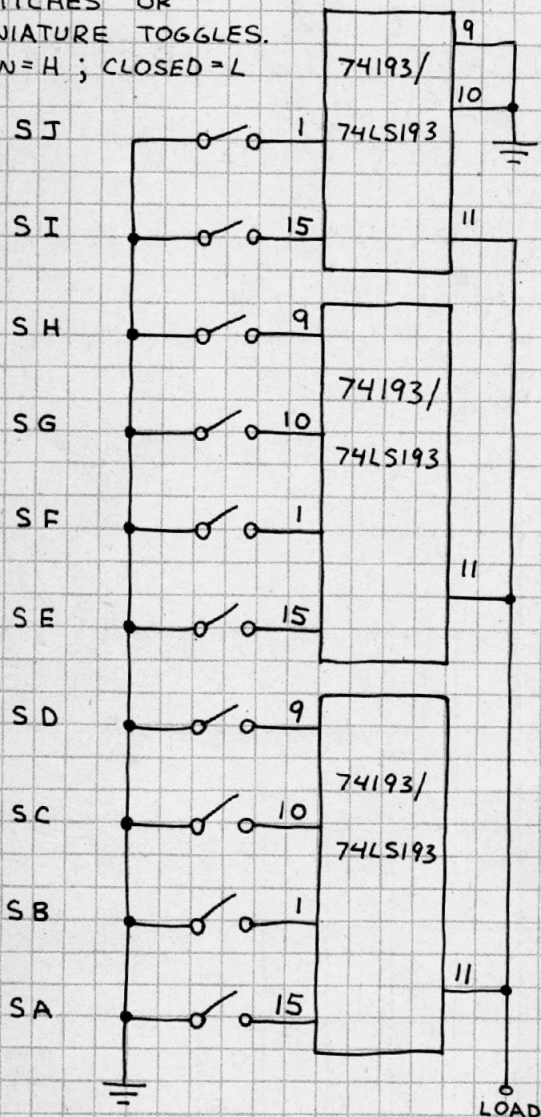
1024-BIT STATIC RAM (CONTINUED)

2102L

ADDING PROGRAMMED OR MANUAL JUMP

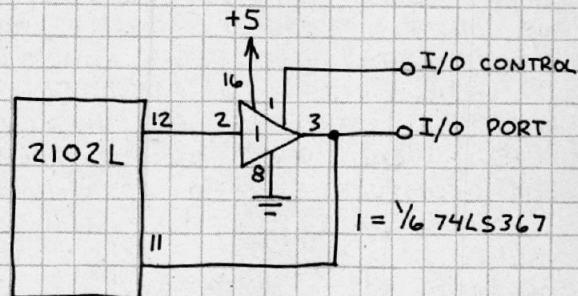
ADD THESE CONNECTIONS TO THE ADDRESSING CIRCUIT ON FACING PAGE.

SA-SJ: USE 8-POSITION DIP SWITCHES OR MINIATURE TOGGLES. OPEN=H; CLOSED=L



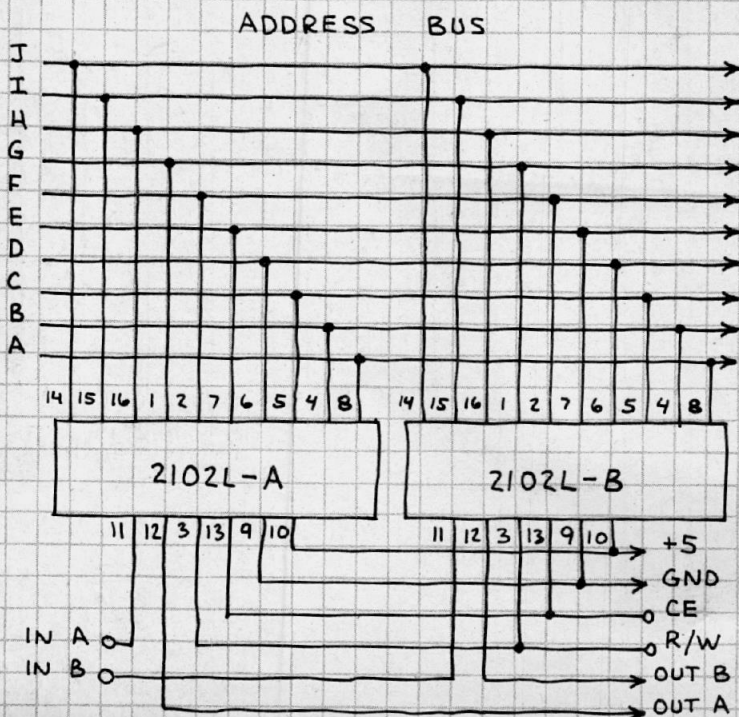
NORMALLY THE LOAD INPUT IS HIGH. MAKING LOAD LOW LOADS THE ADDRESS PROGRAMMED IN SWITCHES SA-SJ INTO THE 74193'S. THIS PERMITS A PROGRAMMED JUMP OR A MANUAL JUMP TO ANY ADDRESS.

SINGLE I/O PORT



ADD THIS CIRCUIT TO THE ADDRESSING CIRCUIT ON FACING PAGE. WHEN I/O (INPUT/OUTPUT) CONTROL IS H, PIN 3 OF THE 74LS367 ENTERS THIRD STATE (HI-Z) AND I/O PORT ACCEPTS INPUT DATA. WHEN PIN 3 OF THE 74LS367 IS L, I/O PORT OUTPUTS DATA. BOTH THESE OPERATIONS ARE DEPENDENT UPON THE STATUS OF THE 2102L CONTROL INPUTS.

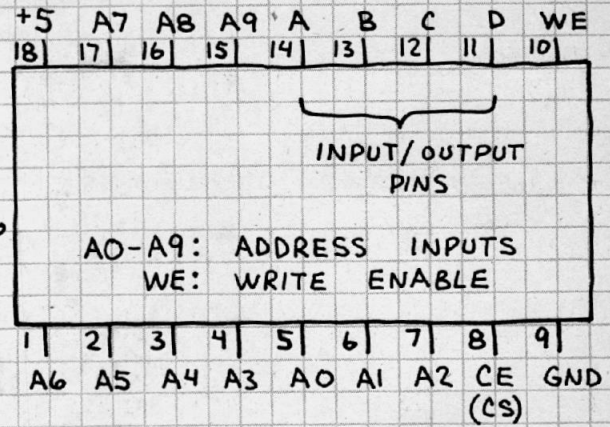
CASCADING 2102L'S



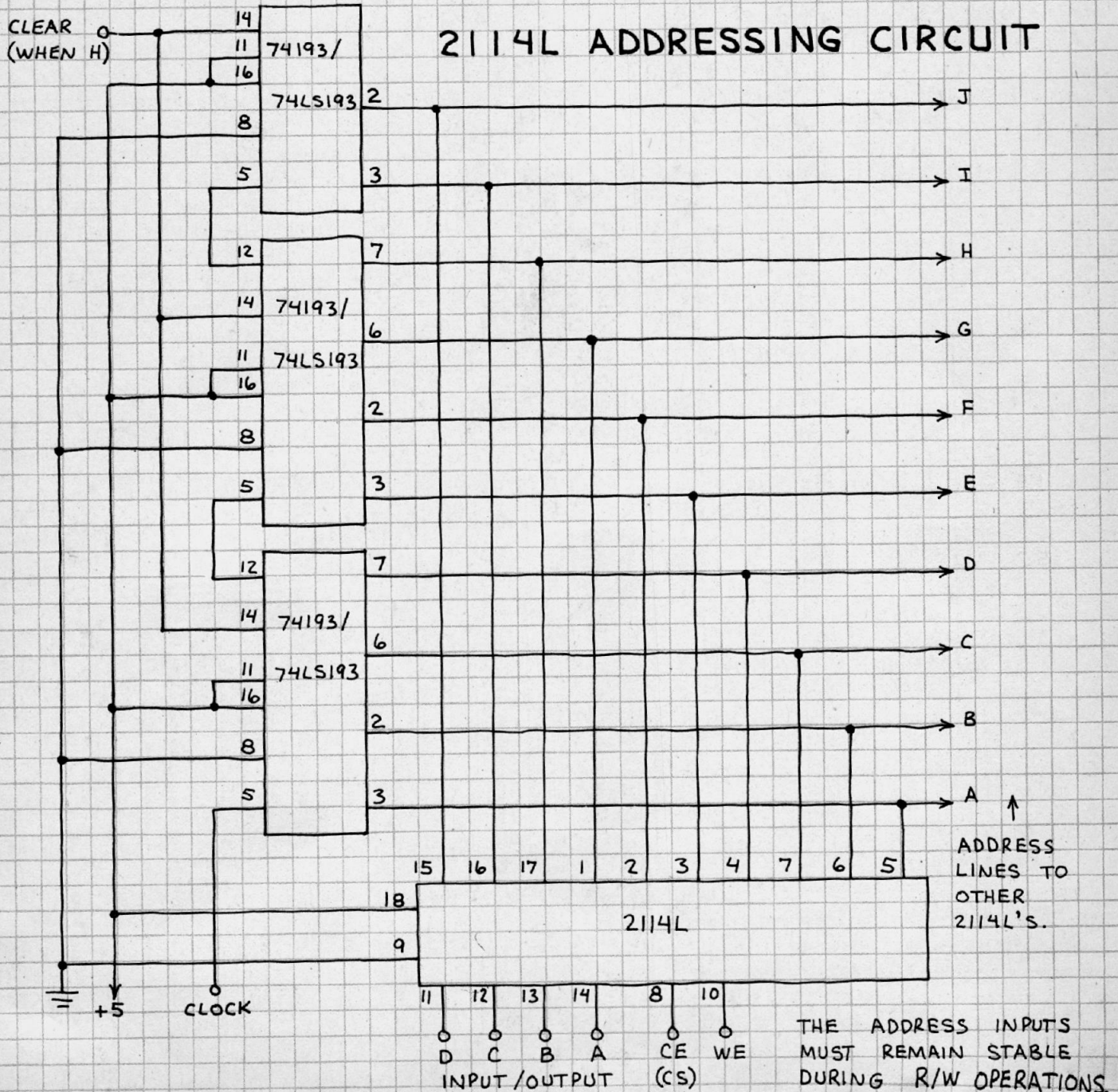
1024 x 4-BIT RAM

2114L / 4045

1024-4-BIT STORAGE LOCATIONS ADDRESSED BY PINS A0-A9. TTL/LS COMPATIBLE. FOR READ/WRITE OPERATIONS, CE (CHIP ENABLE, ALSO CALLED CHIP SELECT) MUST BE LOW. WE INPUT MUST BE LOW TO WRITE (LOAD) DATA INTO CHIP. WHEN WE IS HIGH, DATA IN ADDRESSED LOCATION APPEARS AT INPUT/OUTPUT PINS. IDEAL CHIP FOR DO-IT-YOURSELF MICROCOMPUTERS AND CONTROLLERS.



2114L ADDRESSING CIRCUIT



1024 x 4-BIT RAM (CONTINUED)

2114L/4045

1024-NIBBLE

MANUAL JUMP: 1. SET SWITCHES A-J TO DESIRED ADDRESS; 2. PRESS S6.

DATA LOADING CIRCUIT

(NIBBLE = 4-BIT WORD OR 1/2 8-BIT WORD)

