Designer's casebook

Nonmaskable interrupt saves processor register contents

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Linking a battery-powered random-access memory to the nonmaskable interrupt input available on many microprocessors will save the contents of the memory registers in a microprocessor system during power loss. The NMI input is used to initiate a software routine that, when alerted to a power loss by such means as a power-line relay, stores the contents of the registers in the RAM and then disables the RAM's inputs. These registers require such protection of their status if the microprocessor is to continue execution of the program at the point at which it left off when power failure occurred.

The data-save circuit may be implemented as shown in the figure, using two 5101 complementary-metal-oxide-semiconductor RAMs in conjunction with the 6800/6820 combination of microprocessor and peripheral interface adapter. Since each RAM is organized as a 256-word-by-4-bit array, this 8-bit system requires two of them, configured as a 256-word-by-8-bit device. A set-reset flip-flop, built by cross-connecting two C-MOS two-input NAND gates, controls the data-enable port of the RAMs. The flip-flop and the RAMs are powered by a 4.5-volt battery if the main power is lost.

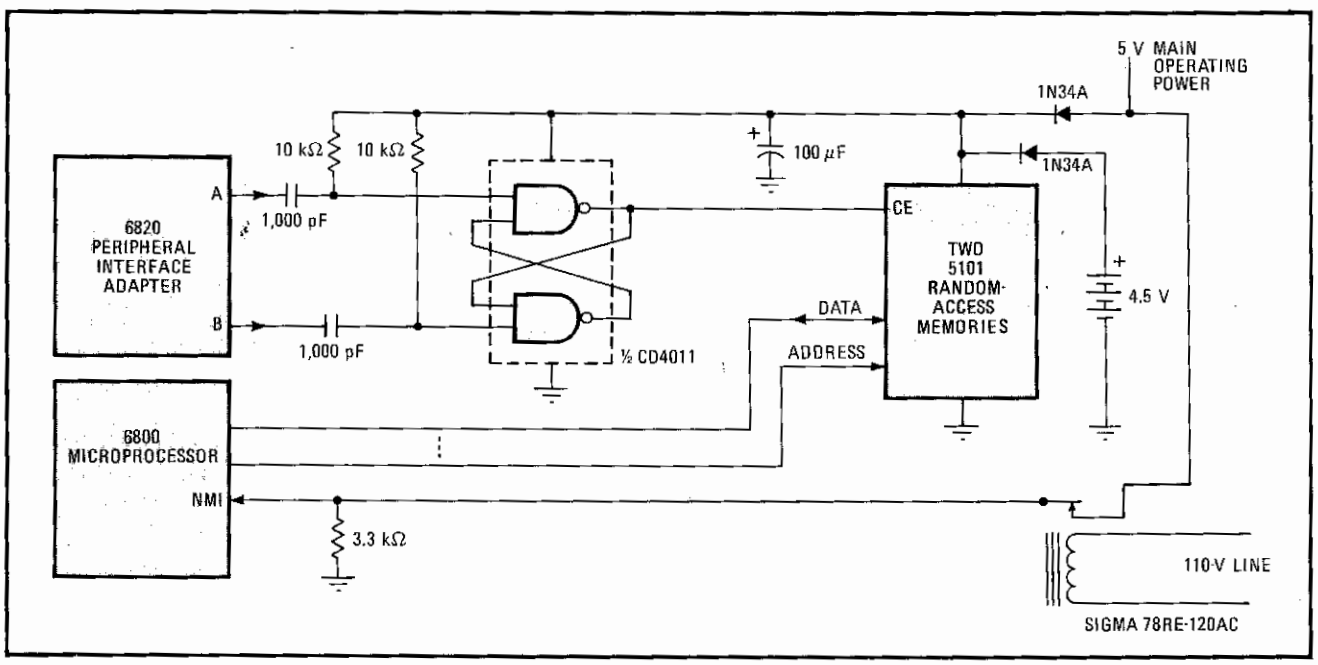
During system startup, a pulsed logic 1 signal is generated at the A output of the PIA through software control. The negative-going edge of this pulse sets the flip-flop and drives the control-enable lead (CE) of the RAMs. This allows desired system parameters, which may have taken hours to determine initially, to be stored in the RAM for protection from power failure.

During a power-down cycle, the address and data lines of the RAM will usually assume random logic states for several milliseconds. This condition is likely to destroy or modify the contents of the RAM unless a logic 0 is applied to the CE input at least a few microseconds before the main power is lost.

A loss of line voltage causes the relay to open; once the operating voltage drops below 4.5 V the battery immediately assumes the power-delivery chores to the RAM and flip-flop. Loss of voltage to the microprocessor and PIA occurs approximately 25 ms later; a pulse must be delivered to the CE port of the RAM before that time.

Relay dropout initiates the NMI sequence. The NMI input, which was at 5 V, drops rapidly. The negative-going transition terminates normal program execution and initiates the interrupt sequence. During this time, an output pulse is generated at port B or the PIA. Its negative edge clears the flip-flop, disabling the RAM by removing its CE signal. This occurs before operating power collapses; thus the RAM's content is not upset. Capacitive coupling between the PIA and the flip-flop is employed to prevent false triggering which may occur during power loss.

This circuit is exceptionally reliable and consumes little power. A small 4.5-v battery will store 256 8-bit words for more than a year if necessary. □



To the rescue. Should power to microprocessor or PIA fail, data in their registers is stored in battery-powered RAMs for protection. Control-enable line of RAMs is enabled during normal operation, disabled on power-down to prevent modification of RAM contents.