FEATURE

Introducing Microprocessors Part 5

This month we examine the different types of computer memories.

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The general learning objectives for Part 5 are that readers should be able to:
(a) Understand the characteristics and applications of semiconductor read-only memory (3.1).
(b) Understand the characteristics and applications of semiconductor random-access memory (3.2).
(c) Understand memory maps for typical 8-bit microprocessor based systems (3.3).
The specific objectives for Part 5 are as follows:

3.1 Semiconductor Ready-Only Memory

3.1.1 State why read-only memory is needed.
3.1.2 Give examples of the use of ROM devices to implement read-only memories.
3.1.3 Explain, in simple terms, the arrangement of a semiconductor read-only memory cell matrix.
3.1.4 Distinguish between mask-programmed or fusible-link (PROM) and erasable-programmable (EPROM) devices, state typical applications and give relative costs.
3.1.5 Explain, in simple terms, the process of programming mask- programmed, fusible-link, and erasable-programmable ROM devices and explain the process of erasure.

3.2 Semiconductor Random-Access Memory

3.2.1 State the need for read/write memory and distinguish between read/write memory and read-only memory.
3.2.2 State that semiconductor random-access memory (RAM) provides read-write memory of a transient nature.
3.2.3 State typical applications of random-access memory.
3.2.4 Explain, in simple terms, the arrangement of a semiconductor random-access memory cell matrix, and how it is accessed.
3.2.5 Distinguish between static and dynamic RAM.

Memory Maps

3.3.1 Explain the need for a memory map.
3.3.2 Draw and interpret the memory map for a representative microcomputer system showing addresses in both decimal and hexadecimal form.
3.3.3 Explain the allocation of total memory space available in a representative microprocessor-based system.

Storage

All microprocessor-based systems require a means of storing their control programs (or operating systems), applications programs and data. Furthermore, the microprocessor itself will require some means of storing transient data (e.g. variables used in a program) and implementing a stack.

Storage may take a variety of different forms including magnetic tape, magnetic disk, and semiconductor memories. Indeed, microprocessor-based systems are often designed so that they can take advantage of more than one storage method. A simple home computer, for example, will contain semiconductor memory devices to satisfy the needs of the microprocessor and to provide storage for a BASIC interpreter. The computer may also be able to save and load programs and data using an external cassette tape recorder or disk drive.

The types of storage device which are relevant are the semiconductor read-only memory (ROM) and semiconductor random access memory (RAM). These devices are both simple and compact. Furthermore, when compared with magnetic disk and tape storage, they offer very fast access times.

Ready-only versus read/write memory

The term "read-only" applies to a wide variety of memory types and all provide permanent or semi-permanent storage and, whilst the contents of a read-only memory cannot normally be changed, certain types of read-only memories may be re-programmed. Read/write memories, on the other hand, allow both reading and writing to take place and their contents can be modified at will.
Unlike magnetic disk and tape (which both exhibit read/write characteristics), the data stored in a semiconductor read/write memory will, unless special precautions are taken in the form of a battery-backed supply, be lost when the power is switched off. Such memories are thus often said to be "volatile". Semiconductor read-only memories, on the other hand, are permanently programmed and thus are said to be "non-volatile".

Random access memory

Semiconductor read/write memory is usually implemented by so- called "random access" memories (RAM). The term "random access" simply indicates that one can access stored data anywhere within the memory with equal ease. Readers should contrast this form of memory with the "sequential access" form of read/write memory provided by magnetic tape in which data is stored one item after another.

Semiconductor Read-Only Memory (ROM)

Microprocessors require non-volatile storage for their control programs and, where appropriate, operating systems and

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high-level language interpreters. Since its contents will not be lost when the power is disconnected, this is an ideal application for a semiconductor ROM. Furthermore, if it becomes necessary to update the control program, operating system or high-level language interpreter, it is possible to remove the ROM and replace it with a later version.

We shall now briefly consider the characteristics of each of the most popular types of semiconductor ROM device:

Mask programmed read-only memories

When large-scale production of a microprocessor based system is envisaged (as is the case with a home computer, for example), the most cost-effective method of implementing read-only memory is with the aid of a mask programmed device. Such devices are programmed by the semiconductor manufacturer who uses a mask to determine the data that will be permanently stored within the chip. The programming information (used to generate the mask) is supplied to the semiconductor manufacturer by the manufacturer of the microprocessor-based system.

Since the process is only cost-effective for quantities in the tens of thousands, it should be obvious that the manufacturer of the microprocessor system needs to be very confident that the stored data and program is free from errors and will require no further modification (which never happens).

Fusible-link programmable read-only memories

Fusible-link programmable read-only memories (PROM) are cost-effective for medium scale production and are programmed by the equipment manufacturer rather than the semiconductor manufacturer. The PROM consists of an array of nichrome or polysilicon fuses (see Fig. 5.1(a)). These fuse links may be "blown" by applying a current pulse of sufficient magnitude to rupture the link. Programming takes a considerable time but the equipment required is simple and relatively inexpensive equipment.

Often, early variants of microprocessor-based systems are supplied with PROM devices which are later replaced with mask ROM devices as soon as teething troubles and bugs have been eliminated and large scale production commences.

An alternative to the fusible-link ROM is the "blown junction" ROM shown in Fig 5.1(b). The operation of this type of ROM is similar to that of the fusible-link type but with the important difference that the diode junction is short-circuited rather than open-circuited during programming.

Erasable-programmable read-only memories

The programming of mask-programmed and fusible-link memories is irreversible. Once programmed, devices cannot be erased in preparation for fresh programming. The erasable-programmable read-only memory (EPROM) can, however, be "wiped clean" allowing the device to be programmed and re-programmed many times over.

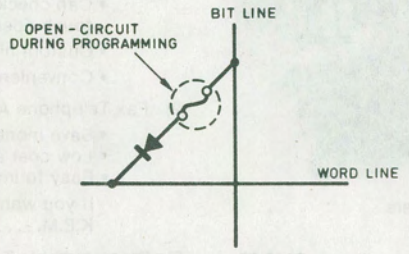

Fig. 5.1(a). Principle of the fusible link PROM.

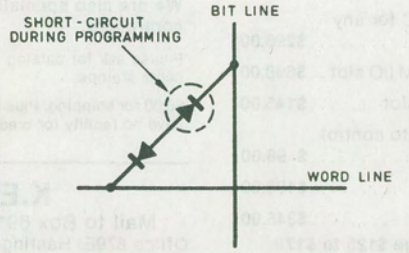

Fig. 5.1(b). Principle of the blown-diode PROM.

EPROM devices are fitted with a window which allows light to fall upon the memory cell matrix. When this area is exposed to strong ultra-violet (UV) light over a period of several minutes, the stored data is erased. The EPROM may then be reprogrammed using a low-cost device which supplies pulses of current to establish the state of individual memory cells. This process takes several minutes though some EPROM programmers can program several devices at once.

EPROMS are ideal for small-scale production and software development. They are, however, relatively expensive and thus are inappropriate for large-scale production. Typical capacities for EPROMs are within the range 2K to 32K bytes.

Readers may be forgiven for thinking that EPROM devices are really forms of read/write memory. In a sense they are: but it is rather more important to make a distinction between these memories and "true" read/write memories (e.g. semiconductor RAM) in which individual bytes can be changed at will.

Another important point is the time and ease with which a device may be reprogrammed with data. A single byte of data can be accessed from a semiconductor RAM in a typical time interval of 150ns. An entire 8K byte RAM can have its data changed in a time interval of 8192 x 150ns (plus an additional overhead for the processor). This results in a total programming time which can be measured in milliseconds. An 8K byte EPROM, on the other hand, may require several minutes of programming, not to mention the time taken for removal and erasure under UV-light.

Semiconductor Random Access Memory (RAM)

Microprocessors require access to read/write memory to implement stacks on which register contents can be stored during processing. Control programs and operating systems also require access to RAM for temporary storage of data and system variables. A further area must be made available for the user to store his or her own programs and data. In addition, where a faster scanned display is used, an area of RAM is usually devoted to a "screen memory". With modern systems, this reserved area of memory is invariably "bit mapped" (i.e. each bit of "screen RAM" corresponds to a particular pixel). The typical allocation of RAM on an 8-bit microcomputer might be as follows:

Function	Storage capacity	Notes
System variables	512 bytes	A fixed address is used for each system variable
Stacks	0–256 bytes	Changes in size during program execution
Screen memory	16K	Bit-mapped screen
User's program and data	Up to 31.5K	Amount used depends upon individual program

Static RAM

Static memories are based upon bistable cell configuration as shown in Fig. 5.2(a). This configuration will remain in a "set" or "reset" state (storing a 1 or 0) until changed or until the power supply is

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removed. The use of NMOS or CMOS (rather than conventional bipolar) technology ensures that each cell consumes very little current and thus a very large number of cells can be present within a small area of integrated circuit.

Dynamic RAM

Dynamic RAM utilises the principle of charge storage within a capacitor. The simplified circuit of an NMOS dynamic memory cell is shown in Fig. 5.2(b). The charge stored in the capacitor, C, inevitably leaks away and thus dynamic memories require periodic "refreshing". The process of refreshing a dynamic memory involves periodically reading the data stored and then writing it back to the memory. Some microprocessors (such as the Z80) incorporate a means of refreshing dynamic memories, alternatively the task can be consigned to a dedicated dynamic memory controller chip.

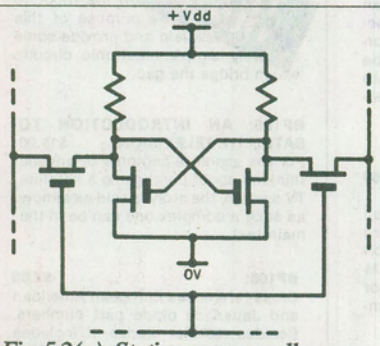


Fig. 5.2(a). Static memory cell configuration.

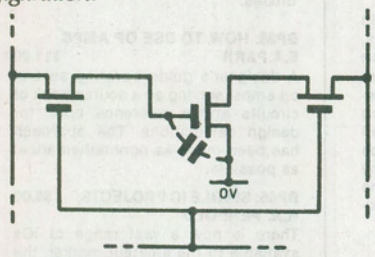


Fig. 5.2(b). Dynamic memory cell configuration.

Memory organization and storage capacity

Read-only memories are, for obvious reasons, "byte wide" (i.e. all eight bits stored at each location are contained within the same semiconductor device). Thus, a 4K byte EPROM would be organized as 4096 words each of 8 bits and its total storage capacity would be 32768 bits.

A wide variety of semiconductor RAM devices is currently available with storage capacities ranging from as little as 4096 bits (1K words x 4 bits) to as much as 262144 bits (256K words x 1 bit.

Each location within a semiconductor memory, whether it be ROM or RAM, comprises a "cell" at which a single bit of data (either a 1 or a 0) is stored. The memory cell matrix for a semiconductor RAM is shown in Fig. 5.3. The matrix comprises 64 rows and 64 columns and thus has a total of (64 x 64) = 4096 individual cells.

The six least-significant address lines (A0 to A5) are used to form the column address whilst the six most significant address lines (A6 to A11) are used to from the row address. Note that the action of the column and row decoders is that of selecting only ONE of the column and row lines at a time hence a unique cell is addressed which corresponds to the binary pattern placed on the address lines.

Fig. 5.3 also shows how data is transferred into and out of the memory cell matrix (by means of the column I/O and how the active-low chips select (CS) and write enable (WE) lines are connected.

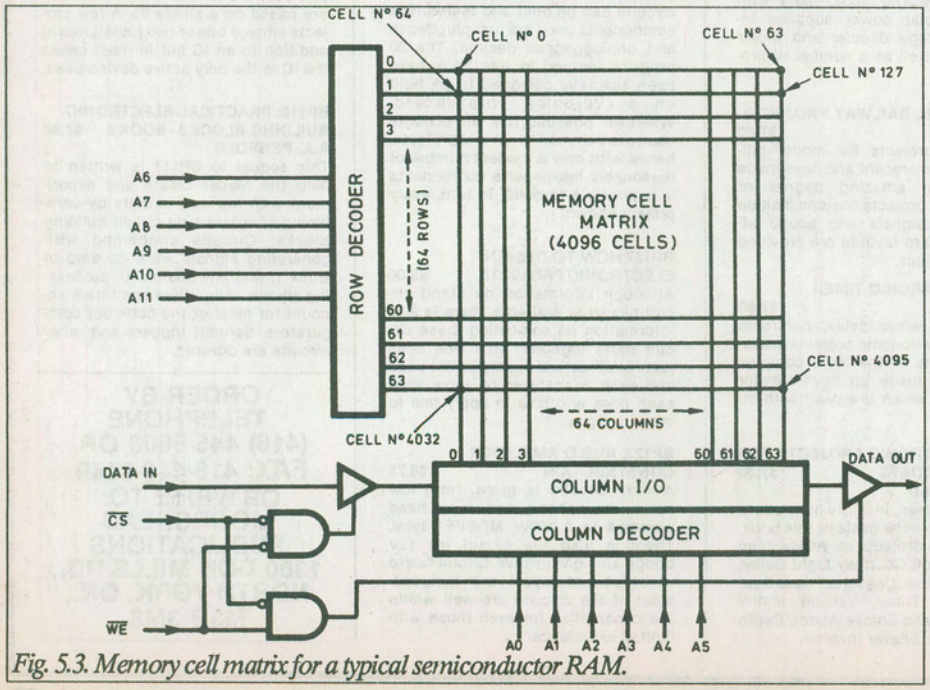


Fig. 5.3. Memory cell matrix for a typical semiconductor RAM.

Problem 5.1

The data sheet for a semiconductor memory device is shown in Fig. 5.4.
(a) State the type number of the device.
(b) State the manufacturer's name.
(c) State the type of device.
(d) State the storage capacity of the device.
(e) State the organization of the memory.
(f) State the number of the pin which is connected to the:
(i) positive supply
(ii) GND or 0V
(iii) least significant address line
(iv) most significant address line
(v) programming supply voltage

Problem 5.2

The data sheet for a semiconductor memory device is shown in Fig. 5.5
(a) State the type number of the device.
(b) State the manufacturer's name.
(c) State the type of device.
(d) State the organization of the memory.
(e) State the number of the pin which is connected to the:
(i) positive supply
(ii) GND or 0V
(iii) least significant address line
(iv) most significant address line
(v) active-low write (WR) line
(iv) address decoding logic

A practical semiconductor read/write memory

Fig. 5.6 shows the basic arrangement of a practical 16K byte semiconductor read/write memory based on eight 6167 CMOS static RAM devices. Each 6167 RAM is organized on the basis of 16384 words x 1 bit and thus eight 6167 devices will be required (one for each data bit). Note that address lines A0 to A13 are common to all of the RAM devices and that the active-low chip select (CS) line is driven from the address decoder (not shown) which uses the two most significant address lines (A15) and (A14) as inputs to determine which of the four 16K byte blocks of memory is actually being used.

Fig. 5.5 See problem 5.2.

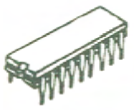
HM6147, HM6147-3
HM6147P, HM6147P-3

4096-word×1-bit High Speed Static CMOS RAM

■FEATURES

- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 55ns/70ns Max.
- Low Power Standby and Low Power Operation, Standby: 100μW typ., Operation: 75mW typ.
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power–On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Pin-out Compatible with Intel 2147 NMOS STATIC RAM

HM6147, HM6147-3

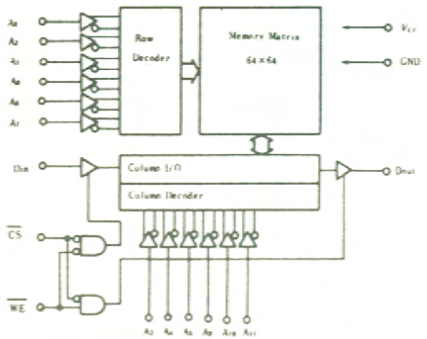


(DG-18)

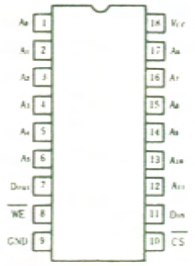
HM6147P, HM6147P-3

(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C

* V_{IN} min = −1.0V (Pulse Width ≤ 20ns)

■RECOMMENDED DC OPERATING CONDITIONS (0°C ≤ Ta ≤ 70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.3*	—	0.8	V

* V_{IL} min = −1.0V (Pulse width ≤ 20ns)

Fig. 5.4 See problem 5.1.

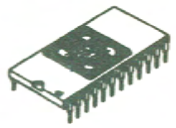
HN462716, HN462716G

2048-word × 8-bit U.V. Erasable and Electrically Programmable Read Only Memory

The HN462716 is a 2048 word by 8 bit erasable and electrically programmable ROMs. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

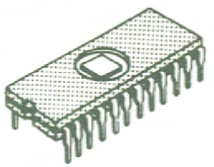
- Single Power Supply ···· +5V ±5%
- Simple Programming ···· Program Voltage: +25V DC
  Programs with One 50ms Pulse
- Static ····· No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded-on Chip Address Decode
- Access Time ····· 450ns Max.
- Low Power Dissipation ·· 555mW Max. Active Power
  161mW Max. Standby Power
- Three State Output ····· OR-Tie Capability
- Interchangeable with Intel 2716

HN462716



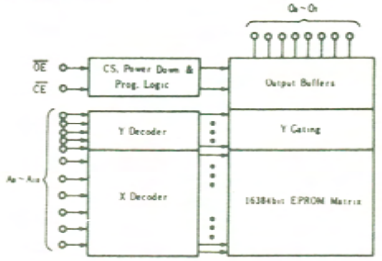
(DC-24C)

HN462716G



(DG-24B)

■BLOCK DIAGRAM



■PROGRAMMING OPERATION

Mode \ Pins	CE (18)	OE (20)	VPP (21)	VCC (24)	Outputs (9~11, 13~17)
Read	VIL	VIL	+5	+5	Dout
Deselect	Don't Care	VIH	+5	+5	High Z
Power Down	VIH	Don't Care	+5	+5	High Z
Program	Pulsed VIL to VIH	VIH	+25	+5	Din
Program Verify	VIL	VIL	+25	+5	Dout
Program Inhibit	VIL	VIH	+25	+5	High Z

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
All Input and Output Voltages*	V_T	−0.3 to +7	V
V_{PP} Supply Voltage*	V_{PP}	−0.3 to +28	V

* With respect to Ground

■PIN ARRANGEMENT

(Top View)

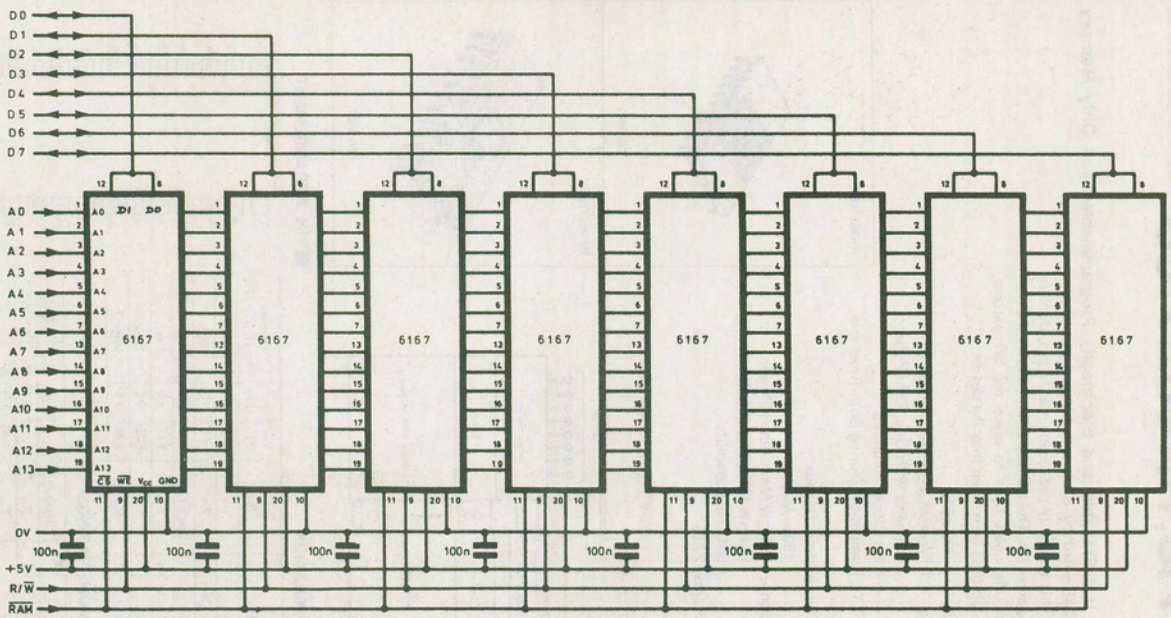


Fig. 5.6. Apractical 16K byte semiconductor read/write memory.

provide decoupling of the +5V supply rail.

Memory Maps

Each location in semiconductor ROM and RAM must have its own unique address. At each address a byte (comprising eight bits) is stored. Each ROM, RAM (or bank of RAM devices) accounts for a particular block of memory, its size depending upon the capacity of the ROM and RAM in question. Furthermore, I/O devices such as keyboards, VDU displays, parallel and serial ports may also be memory mapped into the microprocessor's address space. As an example, a simple home computer may have 12K byte ROM, 4K bytes reserved for I/O, and 16K bytes of RAM allocated to addresses shown in the following table:

Device	Capacity	Address	Range
	(bytes)	Hexadecimal	Decimal
ROM	12K	0000-2FFF	0-12287
I/O	4K	3000-3FFF	12288-16383
RAM	16K	4000-7FFF	16384-32767
unused	32K	8000-FFFF	32768-65535

A more meaningful way of expressing the allocation of addresses to RAM, ROM and I/O is by means of a memory map along the lines of that shown in Fig. 5.7. Note that the map is drawn to scale with addresses ranging from 0000H (at the bottom) to FFFFH (at the top) and that not all of the address space is populated (the upper 32K bytes of memory is unused and any attempt to read or write to this area would be unproductive).

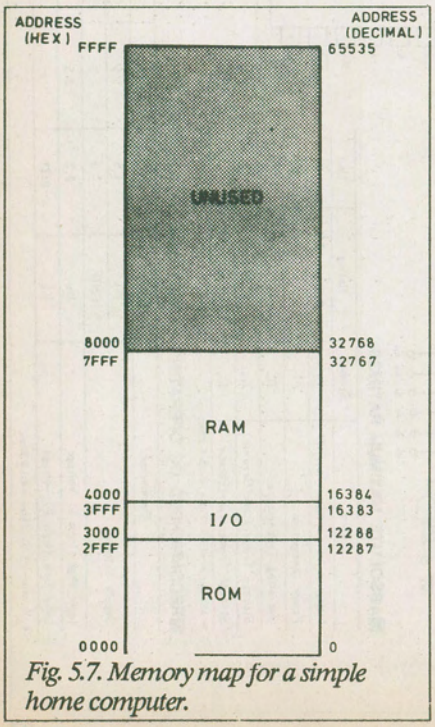


Fig. 5.7. Memory map for a simple home computer.

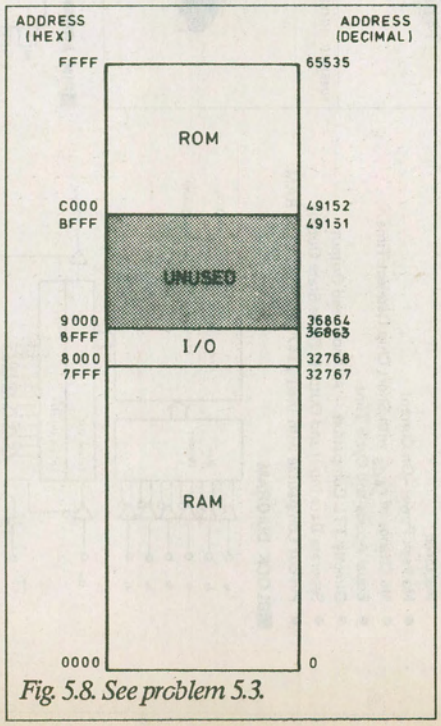


Fig. 5.8. See problem 5.3.

Problem 5.3

Fig. 5.8 shows the memory map for a microprocessor based system.

(a) State the total amount of ROM available.

(b) State the total amount of RAM available.

(c) If the ROM space is populated by devices each organized on the basis of 4096 words of 8 bits, how may ROM device will be present?

(d) If the RAM space is populated by devices each organized on the basis of 16384 words of 4 bits, how many RAM devices will be present?

(e) What is present at each of th of the following memory addresses?

(i) 007F hexadecimal

(ii) 32767 hexadecimal

(iii) 8001 hexadecimal

(iv) 49150 decimal

(v) 1111111110101000 binary

Glossary For Part Five

Address decoder

A decoder which selects a specific address

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or field of addresses to enable unique devices.

Erasable programmable read only memory (EPROM)
A programmable read-only memory that can be erased and reprogrammed. Most EPROM devices can be erased by exposing them to ultraviolet (UV) light.

Memory map
A drawing or table which shows the address assignments for each device in the system.

Memory mapped I/O
Input/output devices that are accessed using the same group of instructions and control signals as used by the memory devices (RAM and ROM) present in the system. The memory and I/O devices thus share the same address space.

Non-volatile
Property of a memory in which data is not lost when the power supply is removed or disconnected.

Answers to Problems

5.1 (a) 2716 (HN462716, HN462716G)
(b) Hitachi
(c) EPROM
(d) 2K bytes
(e) 2048 words x 8 bits
(f) (i) 24
(ii) 12
(iii) 8
(iv) 19
(v) 21

5.2 (a) 6147 (HM6147, HM6147-3, HM6147P, HM6147P-3)
(b) Hitachi
(c) CMOS static RAM
(d) 4096 words x 1 bit
(e) (i) 18
(ii) 9
(iii) 1
(iv) 12
(v) 8
(vi) 10

5.3. (a) 16K bytes
(b) 32K bytes
(c) 4
(d) 4
(e) (i) RAM
(ii) RAM
(iii) I/O
(iv) nothing (i.e. unpopulated)
(v) ROM ■