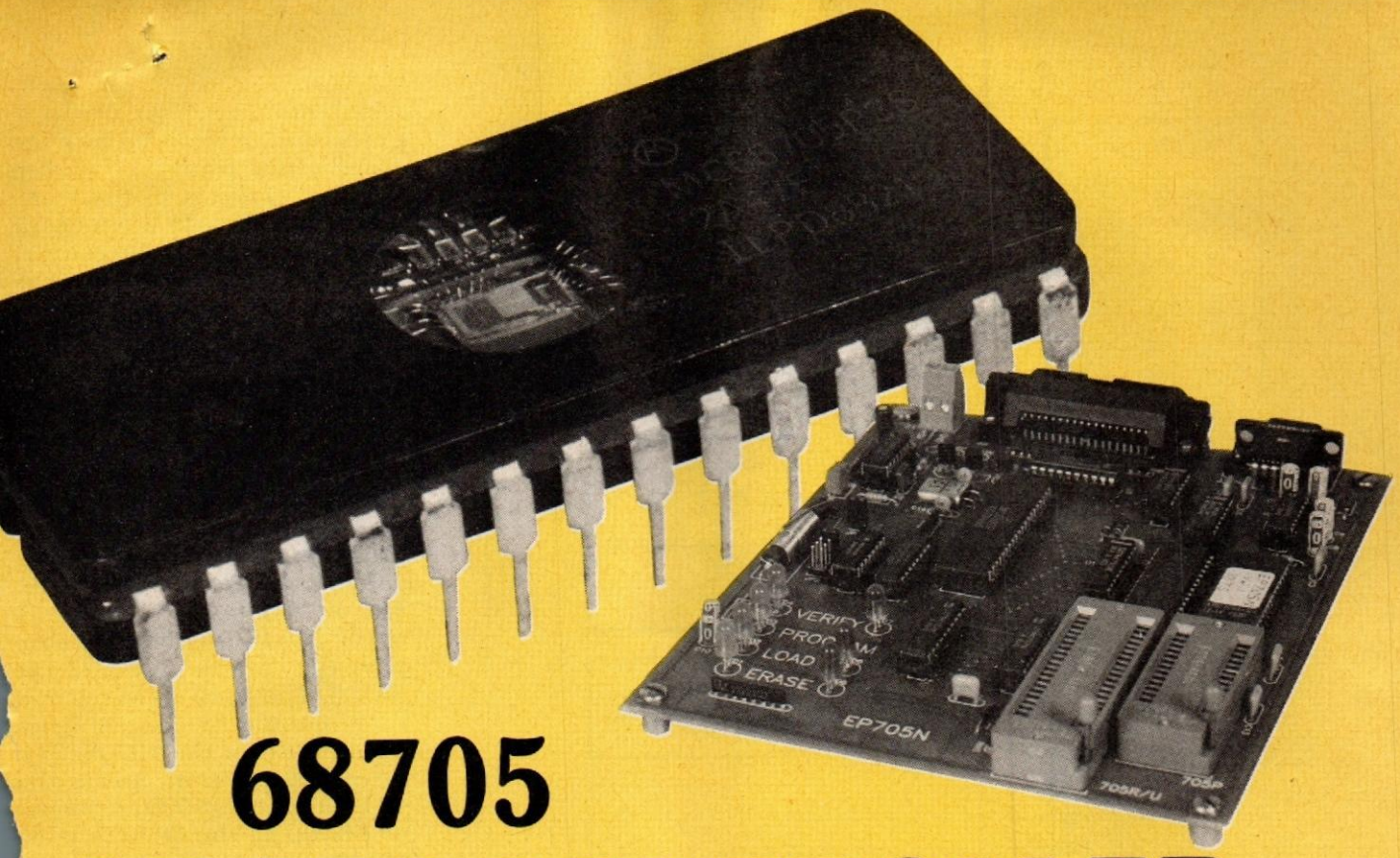


68705 MICROCONTROLLER PROGRAMMER

Now you can program your own 6805 microcontrollers with this inexpensive programmer.

BRIAN BEARD

THIS ARTICLE WILL DESCRIBE THE design of a programmer for the 68705 called the EP705N. The 68705 microcontroller differs from the 6805 in that it has EPROM in place of masked ROM, so that it can be erased and reprogrammed again and again.

The microcontrollers in Motorola's 6805 family are some of the most widely used microcontrollers on the market today. They are optimized for control applications, rather than general-purpose data processing and, are imbedded inside such products as VCRs, printers, modems, toys, and appliances. Today there are over 30 devices in the 6805 family with new ones being added every year. Every member of the family has the same 8-bit CPU core, so if you can program one device you can program any member of the family.

The 68705 is ideal for small control projects because it is easy to program and because it is available to hobbyists for less than $17. The EP705N can program the P3, P5, R3, R5, U3, and U5 versions of the 68705. The "5" parts are identical to the "3" parts except for the addition of an EPROM security feature that prevents the viewing of code in a programmed device. Table 1 compares the features of the various versions.

The EP705N is flexible, quick, and easy to use. It operates from a single 5-volt supply thanks to its own DC-to-DC converter which provides the 21 volts required for programming. LED indicators show the status of the programming process. A parallel printer port and a serial port allow it to be connected to most personal computers. Figure 1 shows the functional blocks that make up the EP705N and how they are interconnected.

Theory of operation

Because the HMOS (high-density NMOS) 68705 processors have no external address or data bus, they cannot access external programs. They can be programmed, however, because of a bootstrap program in a small section of ROM in each 68705. Normally, when the

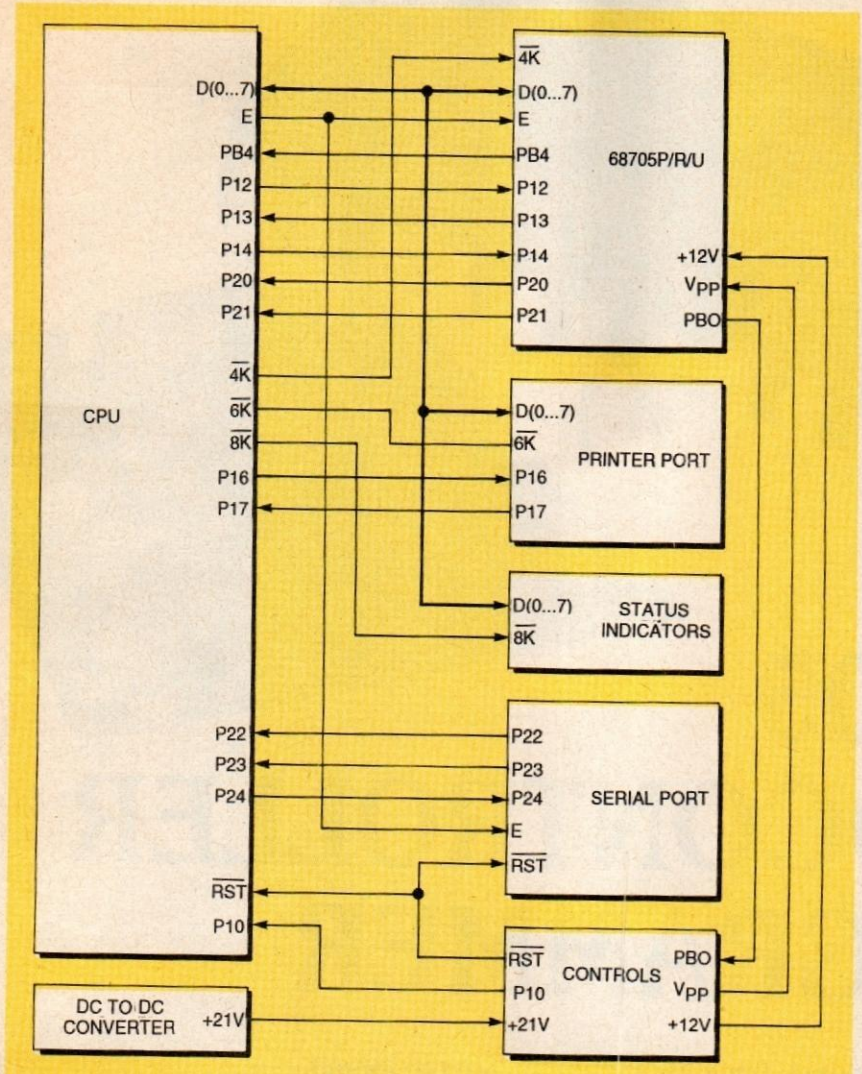


FIG. 1—THE FUNCTIONAL BLOCKS that make up the EP705N and how they are interconnected.

TABLE 1—CHIP FEATURES

	68705P	68705R	68705U
Number of pins	28	40	40
On-chip RAM (bytes)	112	112	112
On-chip ROM (bytes)	115	120	120
On-chip EPROM (bytes)	1804	3776	3776
Bidirectional I/O lines	20	24	24
Input only I/O lines	0	8	8
A/D	No	Yes	No
Timer	Yes	Yes	Yes
External Interrupts	1	2	2

TABLE 2—MEMORY MAP FOR THE EP705N

$0000–$001F	MPU REGISTERS, 6803, IC9
$0020–$3FFF	UNUSED
$4000–$5FFF	DATA OUTPUT TO 68705
$6000–$7FFF	PRINTER PORT INPUT
$8000–$9FFF	LED OUTPUT PORT
$A000–$BFFF	ADDRESS 000 LATCH SET
$C000–$DFFF	RAM, 6264, IC11
$EC00–$FFFF	EPROM, 2764, IC12

RESET pin goes high, the program counter is loaded with the reset vector from the on-chip EPROM. However, if the TIMER pin is at +12 volts when RESET goes high, the program counter is loaded with the starting address of the bootstrap program instead.

The bootstrap program is designed to work with the hardware shown in Motorola Application Note 857 (AN857) consisting primarily of a 2764 EPROM and a 4040, 12-bit ripple counter. The 2764 is preprogrammed with the object code destined for the 68705. The 4040 supplies the address to the 2764 which in turn supplies the data to port A of the 68705. The 4040 is cleared and incremented by control lines from port B of the 68705. The bootstrap program starts the 4040 at address $000 and increments up to the 68705's maximum address: $7FF for the P3/P5, and $FFF for the R3/R5/U3/U5. At each address corresponding to EPROM in the 68705, the bootstrap program takes the data from port A and programs it into the EPROM.

After reaching the maximum address, the bootstrap program clears the 4040 and makes one more pass through the address space to compare the data at port A with the contents of its on-chip EPROM. The +21 volts required to program the 68705's EPROM (V_{PP}) is switched by PBO. Additional lines from port B are used to signal that the EPROM is programmed and the program is verified.

The 68705 being programmed expects to interact with the hardware specified in AN857. The circuitry of the EP705N emulates the functions of that hardware. The programming data comes from the RAM buffer via a latched port (IC14 in Fig. 2) instead of from a 2764 EPROM. A 6803 monitors the count (PB3) and clear (PB4) lines from the 68705 and modifies its pointer into the RAM buffer, which replaces of the 4040 counter. The control line from the 68705 that switches V_{PP} to the chip is still controlled directly by the 68705.

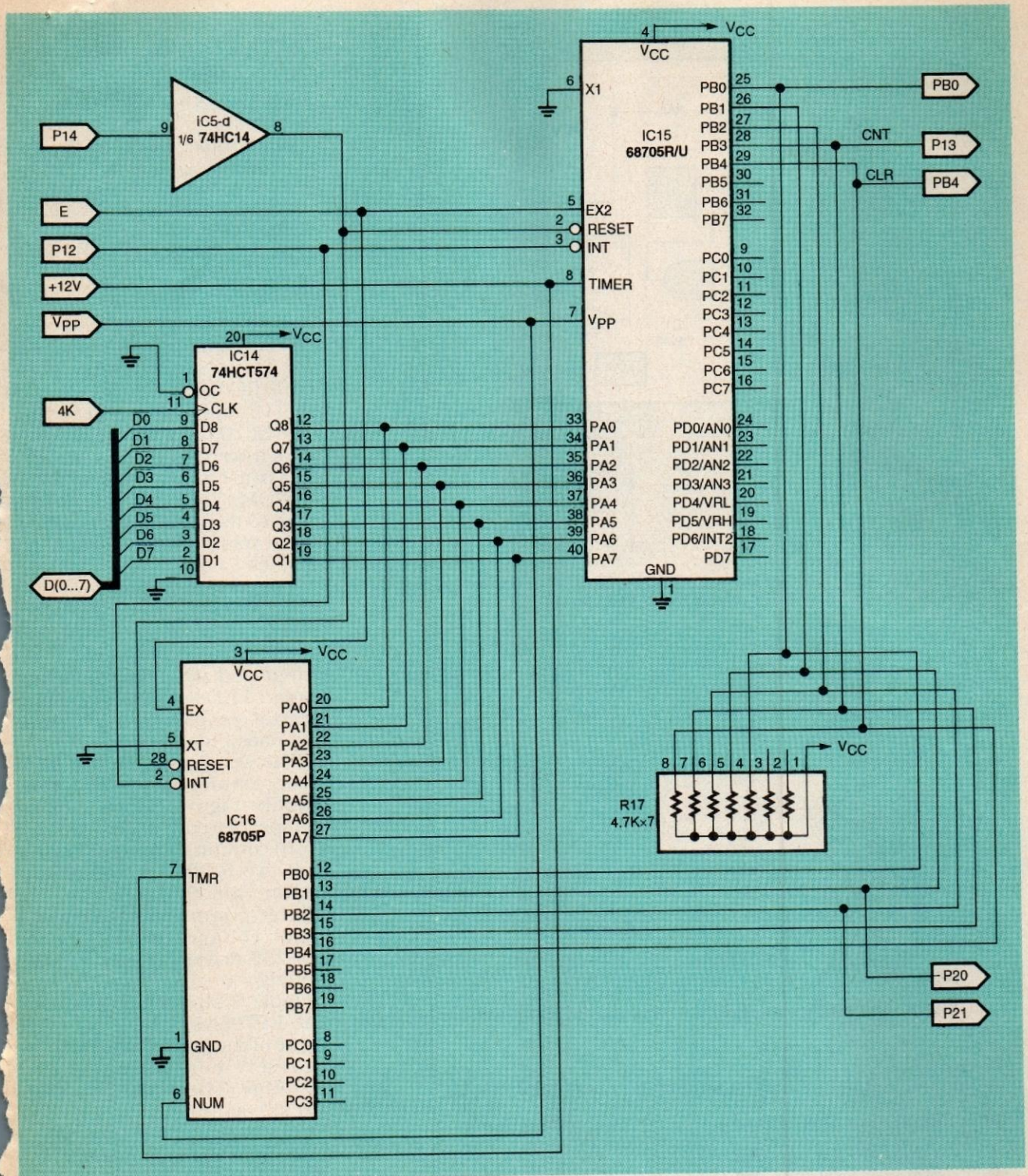


FIG. 2—28-PIN 68705's are programmed in the IC16 socket and the 40-pin chips in IC15. Only one 68705 can be programmed at a time.

Figure 2 shows the sockets for the 68705 chips. There are two 68705 sockets because of the different pinouts on the chips. The 28-pin 68705s are programmed in the IC16 socket and the 40-pin chips in IC15. Only one 68705 can be programmed at a time even though there are two sockets. Note that the RESET and INT lines to the 68705 are controlled by the 6803 processor. The 6803 uses the RESET line to keep the 68705 inactive until programming begins. The INT line serves as a "data ready" handshake line to the 68705.

The EP705N requires a supply of 5-volts DC at 500 milliamperes. The 21 volts (V_{PP}) needed to program the microcontroller is supplied by the DC-to-DC converter circuit shown in Fig. 3. Trimmer R4 adjusts the 21-volt supply, which is applied to the V_{PP} pin of the 68705 by the

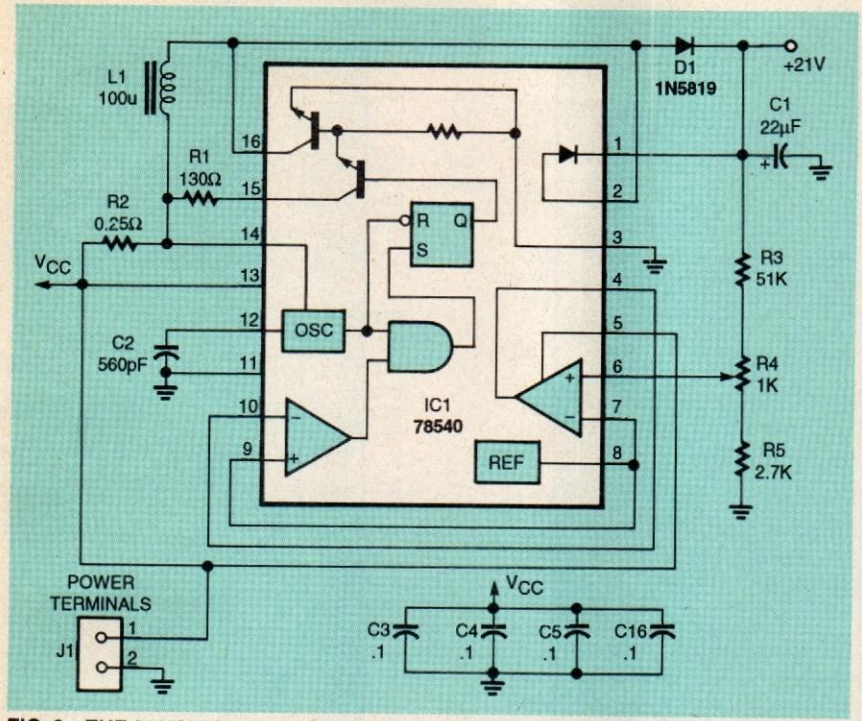


FIG. 3—THE 21 VOLTS (V_{PP}) needed to program the EPROM is supplied by this DC-to-DC converter circuit. Trimmer R4 adjusts the 21-volt supply.

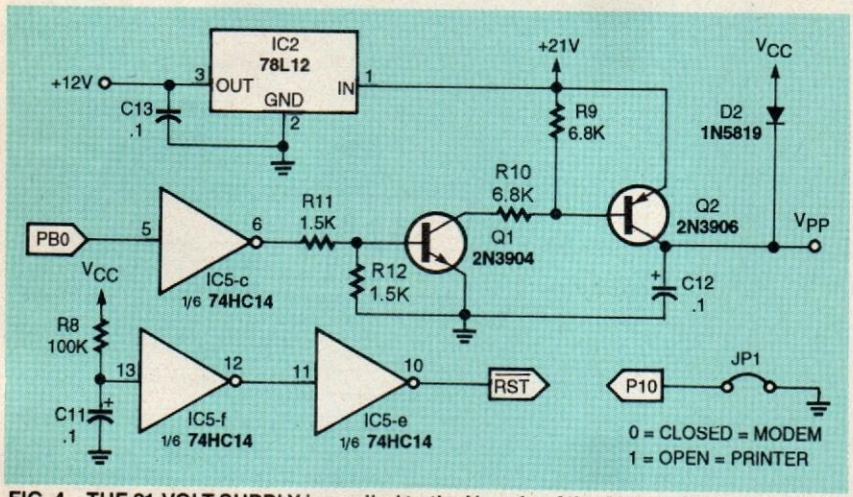


FIG. 4—THE 21-VOLT SUPPLY is applied to the V_{PP} pin of the 68705 with this switching circuit.

TABLE 3—EP705N SERIAL CONNECTOR

Pin	Circuit	Description	Direction
1	CF	Carrier detect. DCD	from EP705N
2	BB	Receive data, RD	from EP705N
3	BA	Transmit data, TD	to EP705N
4	CD	Data Terminal ready, DTR	to EP705N, n/c
5	AB	Signal ground, SG	—
6	CC	Data set ready, DSR	to EP705N
7	CA	Request to send, RTS	to EP705N
8	CB	Clear to send, CTS	from EP705N
9	CE	Ring indicator, RI	from EP705N, n/c

switching circuit shown in Fig. 4. The 21-volt supply also serves as the source for the 12-volt regulator, IC2.

Table 2 shows the memory map of the EP705N. Note that this is the memory map for the 6803 processor in the EP705N,

TABLE 4—MODEM MODE MENU SCREEN

[U] Upload ASCII S19 file to buffer
[P] Program 705 from buffer and verify
[C] Generate buffer checksum
[H] Buffer display, HEX × ASCII
[M] Modify buffer
[D] Download buffer to S19 file
?

and not the memory map of the 68705 being programmed. Figure 5 shows the circuitry for the 6803 (IC9), EPROM (IC12), RAM (IC11), and address decoding. The EP705N operating program and interrupt vectors are programmed into the 2764 EPROM. The 6264 8K × 8 RAM is used as a buffer for uploaded programs, variable storage, and a stack.

The status of the programming process is indicated by the seven LEDs on the board. Figure 6 shows how LEDs 1–7 are wired and what they indicate. Green LEDs indicate the successful completion of a step and red ones indicate a failure.

The serial port on the 6805 programmer is RS-232 compatible. Figure 7 shows the serial-port circuitry. The MAX232 (IC6) contains two RS-232 drivers, two RS-232 receivers, and an on-chip charge-pump. The charge-pump generates the bipolar voltages needed by the RS-232 drivers from the 5-volt supply.

Table 3 shows the pinout of the EP705N's serial connector. None of the handshake lines are actively controlled by the EP705N. The DTR (DATA TERMINAL READY) line is not connected. Lines DSR (DATA SET READY) and DCD (DATA CARRIER DETECT) are wired to a logic-high condition at all times. The RTS line is received, buffered, and looped back to the host as CTS, so that CTS (CLEAR TO SEND) tracks RTS (REQUEST TO SEND). The baud rate is selected with jumper block JP2 (Fig. 7). All of the standard baud rates from 600 to 9600 baud are available.

The parallel printer port circuitry is shown in Fig. 8. Each byte sent to the port from a per-

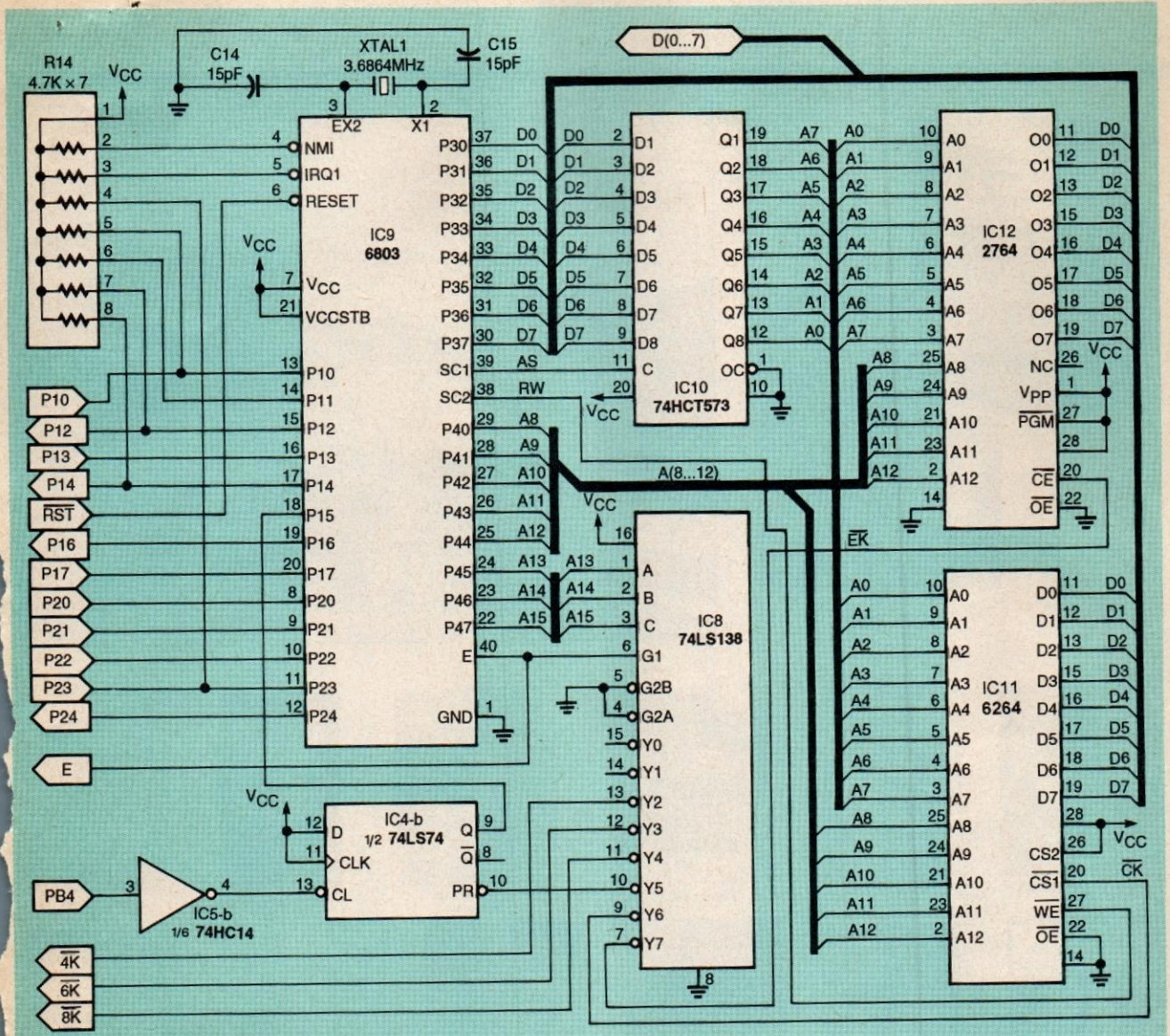


FIG. 5—THE EP705N OPERATING PROGRAM and interrupt vectors are programmed into the 2764 EPROM. The 6264 8K × 8 RAM is used as a buffer.

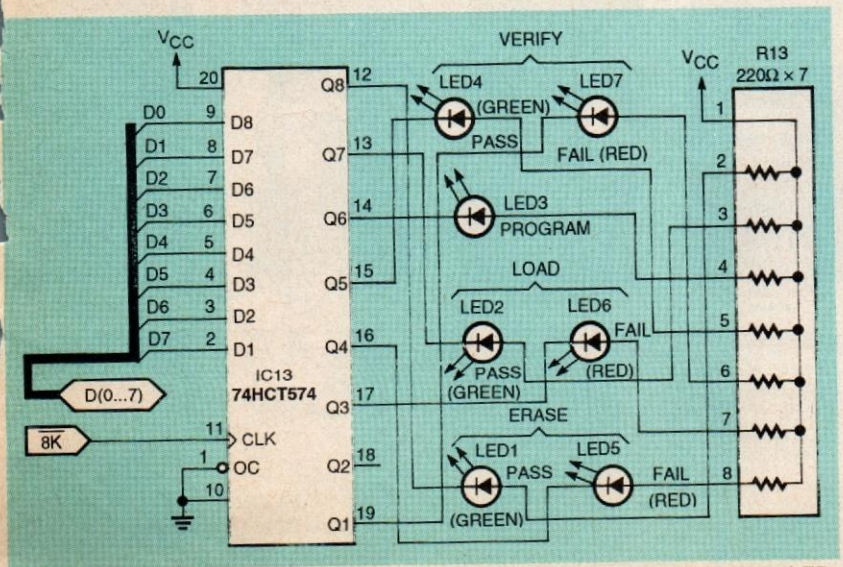


FIG. 6—THE STATUS OF THE PROGRAMMING PROCESS is indicated by seven LEDs. Green LEDs indicate success, and red ones indicate failure.

sonal computer is signaled by DST (DATA STROBE) strobing low. DST sets flip-flop IC4-a, which sets the BUSY line and latches the new byte into IC3. The 6803 monitors the BUSY line (P17), and when it detects activity it reads the new byte from IC3. After processing the new byte, the 6803 strobes ACK (ACKNOWLEDGE) (P16) low. The rising edge of ACK clears the flip-flop which clears the BUSY line allowing the host computer to send the next byte.

The EP705N can operate in two different modes. If jumper block JP1 in Fig. 4 is open, the EP705N acts like a printer. It monitors the parallel and serial ports and accepts data from whichever one is active. The S19 output of an assembler can

be sent from a computer to the EP705N just as if it were a printer. For example, on an MS-DOS system, you would simply connect the EP705N in place of your printer and type in the normal print command "PRINT (FILENAME).S19."

In the printer mode the EP705N performs all operations automatically. The result of each step in the programming process is marked by the appropriate LED. If any step fails, a red LED will light up and the process will cease. When programming is complete and successful, there will be four green LEDs glowing.

When power is first applied to the EP705N, all LEDs come on for one second to verify that they are operational. The EP705N then checks the 68705's internal EPROM to determine if it is completely erased. If it is erased, the chip is ready to be programmed and the green ERASE LED comes on. The EP705N will now wait for you to send it an object file via either the parallel or serial port.

The object file must be in the Motorola standard S19 format. Any 6805 assembler will generate this type of output. As the object file is sent to the EP705N, it is converted to binary code and stored in the RAM buffer. If there is an error in the conversion, such as a non-hex character or a bad checksum, the red LOAD LED lights.

If the entire S19 file is received successfully, the green LOAD LED comes on. After an object file is loaded, programming of the 68705 begins. Completion of the programming step is marked by the program LED. The last step is to verify the pro

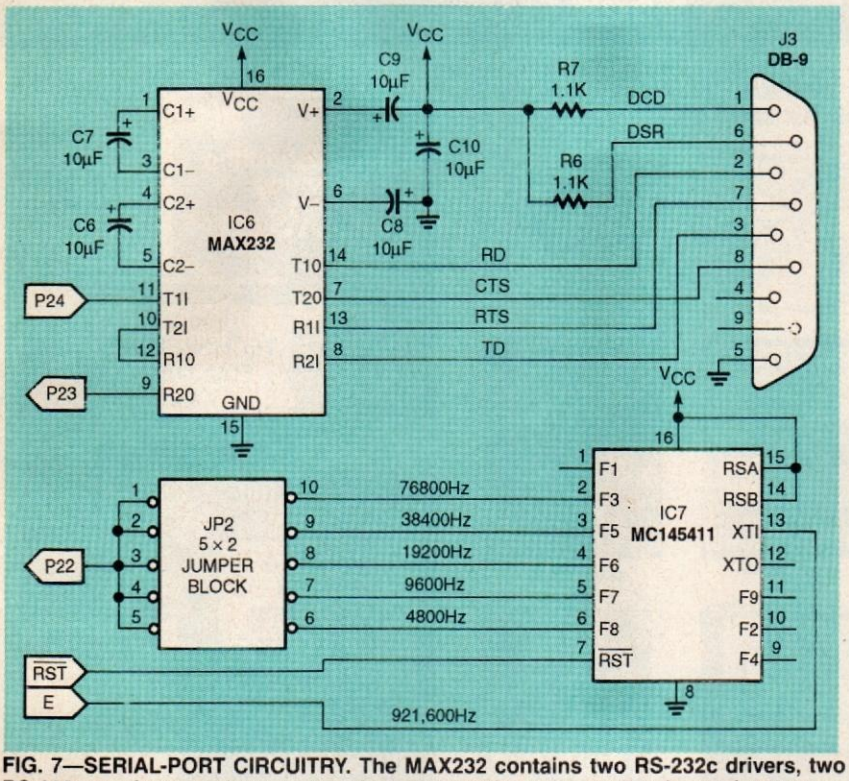
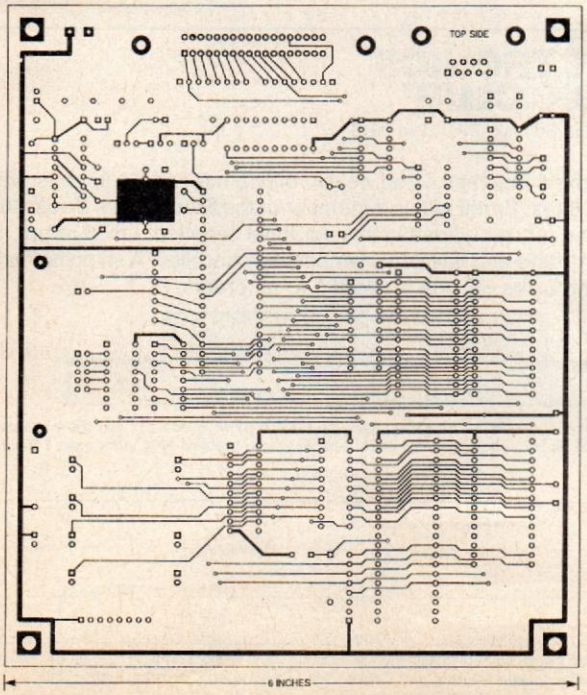
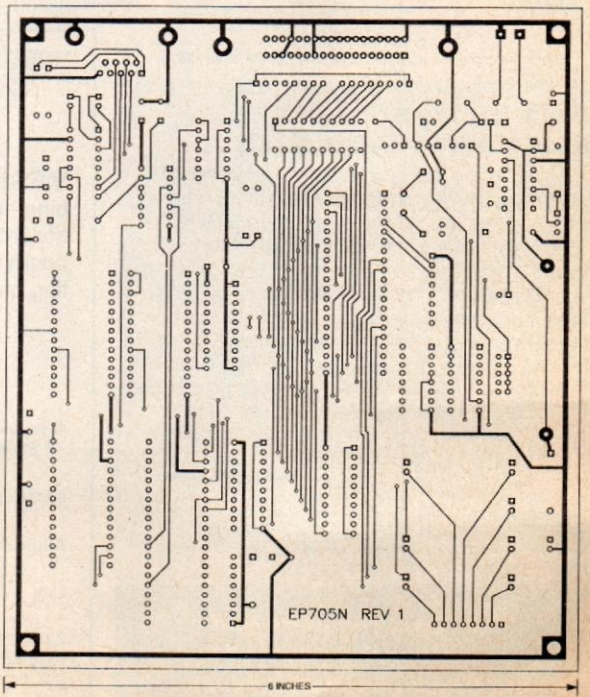


FIG. 7—SERIAL-PORT CIRCUITRY. The MAX232 contains two RS-232c drivers, two RS-232c receivers, and an on-chip charge-pump that uses the 5-volt supply to generate the bipolar voltages needed by the RS-232c drivers.



COMPONENT SIDE of the 6805 programmer board.



SOLDER SIDE of the 6805 programmer board.

PARTS LIST

All resistors are¼-watt, 5%, unless otherwise noted.

R1—130 ohms
R2—0.25 ohm or less
R3—51,000 ohms
R4—1000 ohms, ⅜-inch upright trimmer
R5—2700 ohms
R6, R7—1100 ohms
R8—100,000 ohms
R9, R10—6800 ohms
R11, R12—1500 ohms
R13—220 ohms × 7, 8-pin SIP (pin 1 common)
R14–R17—4700 ohms × 7, 8-pin SIP (pin 1 common)

Capacitors

C1—22 µF, 50 volts, electrolytic
C2—560 pF, Mylar
C3–C5, C11, C13, C16—0.1 µF, ceramic disc
C6–C10—10 µF, 16 volts, radial electrolytic
C12—0.1 µF, 50 volts, ceramic disc
C14, C15—15 pF, ceramic disc

Semiconductors

IC1—78S40 switching regulator
IC2—78L12 12-volt regulator (TO-92 case)
IC3, IC13, IC14—74HCT574 octal D-type flip-flop
IC4—74LS74 dual D-type flip-flop
IC5—74HC14 hex inverter
IC6—MAX232 RS-232 interface
IC7—MC145411 bit rate generator
IC8—74LS138 3-to-8 decoder
IC9—MC6803 microcomputer
IC10—74HCT573 octal latch
IC11—6264 8K × 8 CMOS RAM
IC12—2764 8K × 8 EPROM (preprogrammed)
D1, D2—1N5819 Schottky diode
Q1—2N3904 NPN transistor
Q2—2N3906 PNP transistor
LED1–LED4—Green light-emitting diode
LED5–LED7—Red light-emitting diode

Other components

J1—2-contact terminal block
J2—25-pin female right-angle Centronics connector
J3—9-pin female DB-9 connector
JP1—1 × 2 jumper header and one shorting jumper, 0.1-inch spacing
JP2—5 × 2 jumper header and one shorting jumper, 0.1-inch spacing
L1—100 µH coil
XTAL1—3.6864 MHz crystal

Miscellaneous: PC board, two 14-pin IC sockets, four 16-pin IC sockets, four 20-pin IC sockets, two 28-pin IC sockets, one 40-pin IC socket, one 40-pin ZIF socket, and one 28-pin ZIF socket.

Note: The following items are is available from Lucid Technologies, 7439 Highway 70 South, Unit 297, Nashville, TN 37221:

- **Partial EP705N kit (includes PC board, programmed 2764 EPROM (IC12), MC145411 bit-rate generator (IC7), documentation disk (5.25", 360K IBM format), and schematics)—$45**
- **Same kit as above but without PC board—$25**

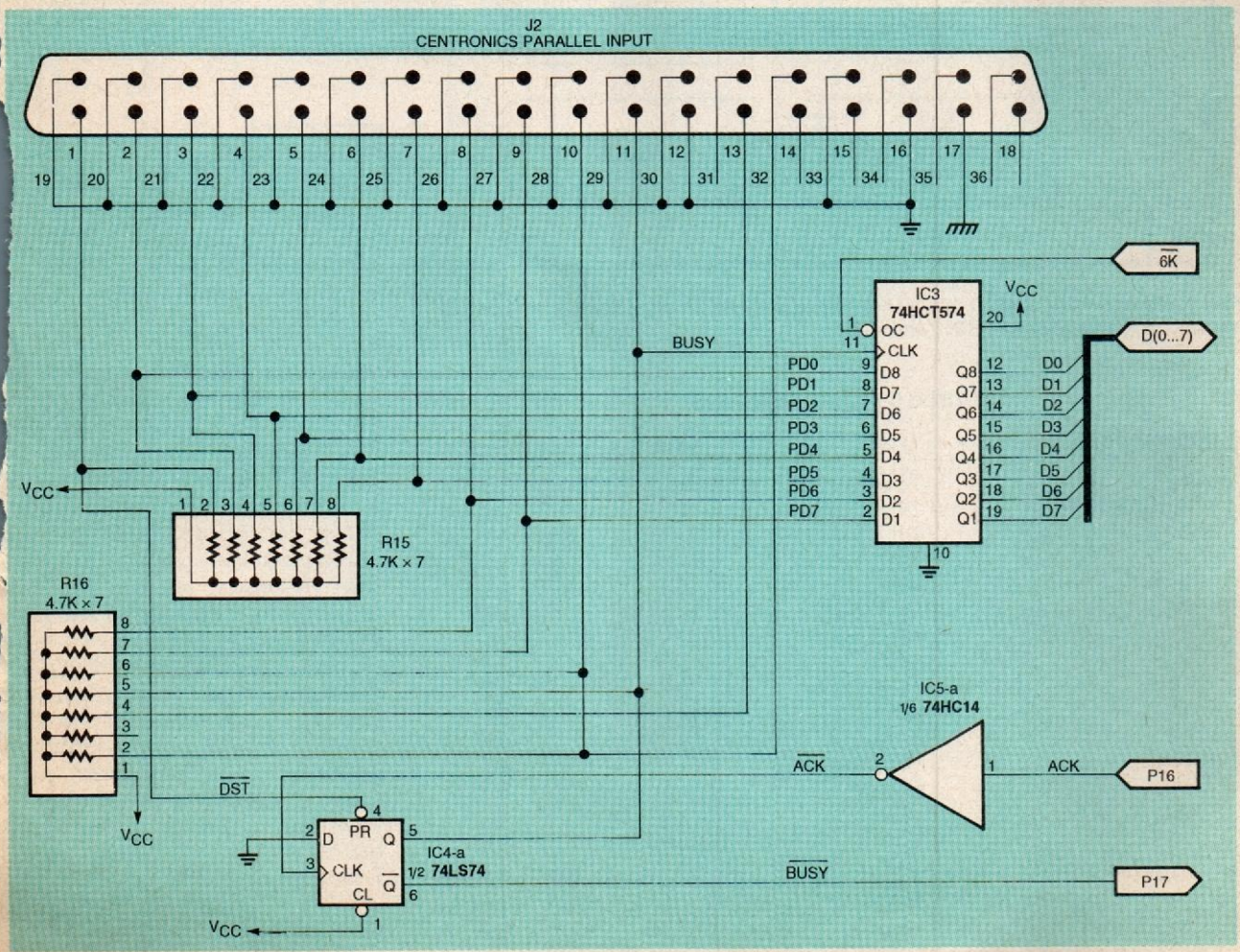


FIG. 8—PARALLEL PRINTER PORT CIRCUITRY. Each byte sent to the EP705N is signaled by scdst strobing low.

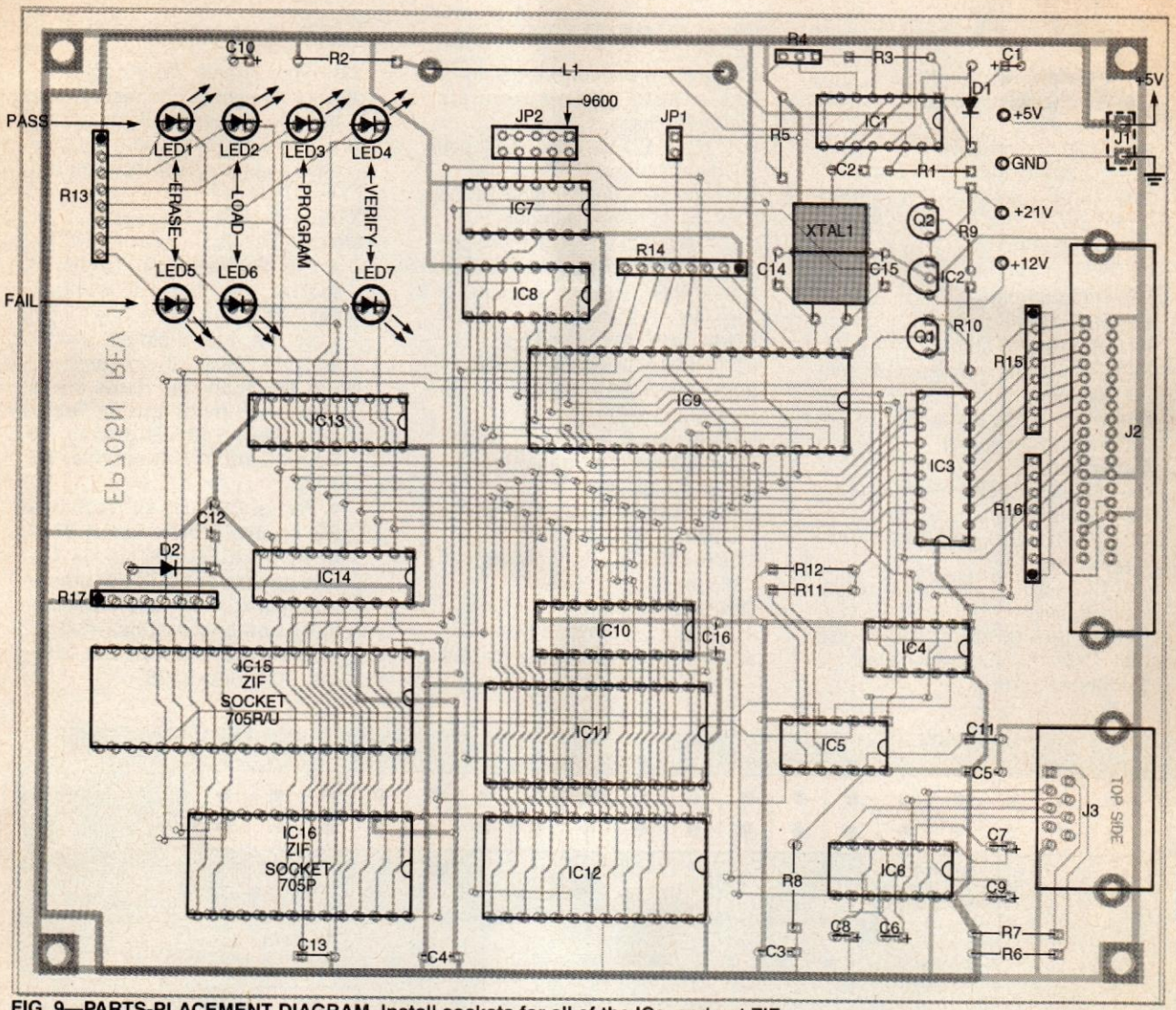


FIG. 9—PARTS-PLACEMENT DIAGRAM. Install sockets for all of the ICs, and put ZIF sockets in the locations for IC15 and IC16.

TABLE 5—IC POWER PINS

Reference	Type	Gnd	V_{CC}
IC1	78S40	3	13
IC3, IC13, IC14	74HCT574	10	20
IC4	74LS74	7	14
IC5	75HC14	7	14
IC6	MAX232	15	16
IC7	MC145411	8	16]
IC8	74LS138	8	16
IC9	6803	1	7,21
IC10	74HCT573	10	20
IC11	6264	14	28
IC12	2764	14	28
IC15	68705R/U	1	4
IC16	68705P	1	3

grammed EPROM against the object file loaded in the RAM buffer. If verification is successful, the green LED comes on; if not, the red one does.

If jumper block JP1 is short-circuited, the EP705N acts like a modem and uses only the serial port. To use this option your computer must have a communications program capable of ASCII file transfer. This mode allows you to interact with the EP705N via the menu shown in Table 4. The modem mode is not a completely automatic mode; the erase check is still done when power is applied, but after that you must tell the EP705N to perform each step of the programming process. In the printer mode, if something goes wrong, the only indication is a red LED. However, in the modem mode, a problem will generate a specific error message. The modem mode also allows the contents of the RAM buffer to be examined, modified, and downloaded.

Construction

The design of the EP705N is complex enough to make point-

Last Page — See Radar Monitor.