# C-MOS reset circuit ignores brief outages

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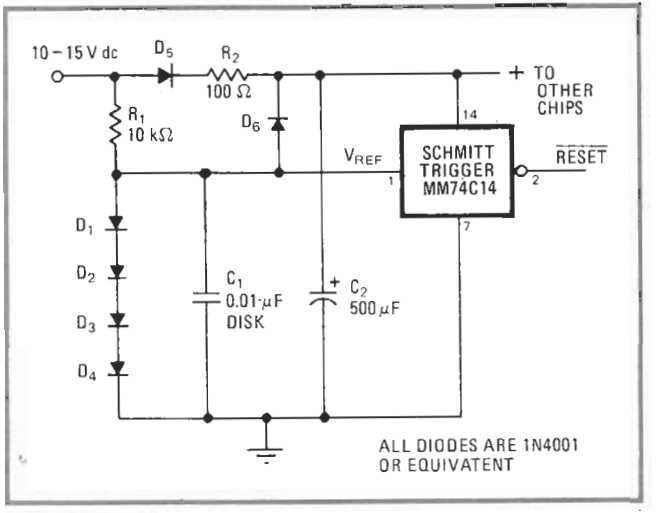
If the voltage supply to a C-MOS circuit drops much below 3 volts during a power failure, a reset signal is necessary to initialize the logic and perhaps also to indicate that the power has failed. But, unlike conventional power-fail circuits, the reset should ignore transient interruptions that do not drop the supply below 3 volts, the level at which the logic states of the latches, counters, and the like may change randomly.

Such a reset signal can readily be derived. An isolated reference voltage is applied to the input of a Schmitt trigger having threshold voltages that are a function of the logic-supply voltage.

In the complementary-metal-oxide-semiconductor circuit shown, the Schmitt trigger is a National MM74C14. Diodes $D_1$ through $D_4$ and resistor $R_1$ establish a reference voltage of approximately 2.5 volts across capacitor $C_1$. $D_5$ isolates the energy-storage capacitor $C_2$ from the supply and from any higher-current loads such as relays and displays that are not needed during a power failure. $D_6$ assures that the reference cannot exceed the supply voltage by more than one diode drop.

When power is first applied, $C_2$ is at zero volts. As $C_2$ charges through $D_5$ and $R_2$, the reference at first exceeds the high threshold of the Schmitt trigger, causing its output to go low and thus resetting associated circuits. This signal remains low until the logic supply voltage (across $C_2$) is high enough (about 8 V) for the low threshold to exceed the reference and to switch the Schmitt high. During subsequent power failures—provided the logic supply voltage across $C_2$ remains above 3 V—the high threshold (about 80% of supply at low voltages) will remain above the reference, so that the Schmitt output will not switch when power is reapplied. However, should the supply fall so low that the high threshold is lower than the reference when power is restored, the Schmitt output will go low, thus resetting




**Resets if necessary.** During brief interruptions of dc power, the charge on $C_2$ maintains voltage to C-MOS digital circuits, preserving their logic states. But if the power failure lasts so long that the voltage across $C_2$ drops below 3 V, the Schmitt trigger resets the logic circuits when power is restored.