Timer circuit generates precision power-on reset

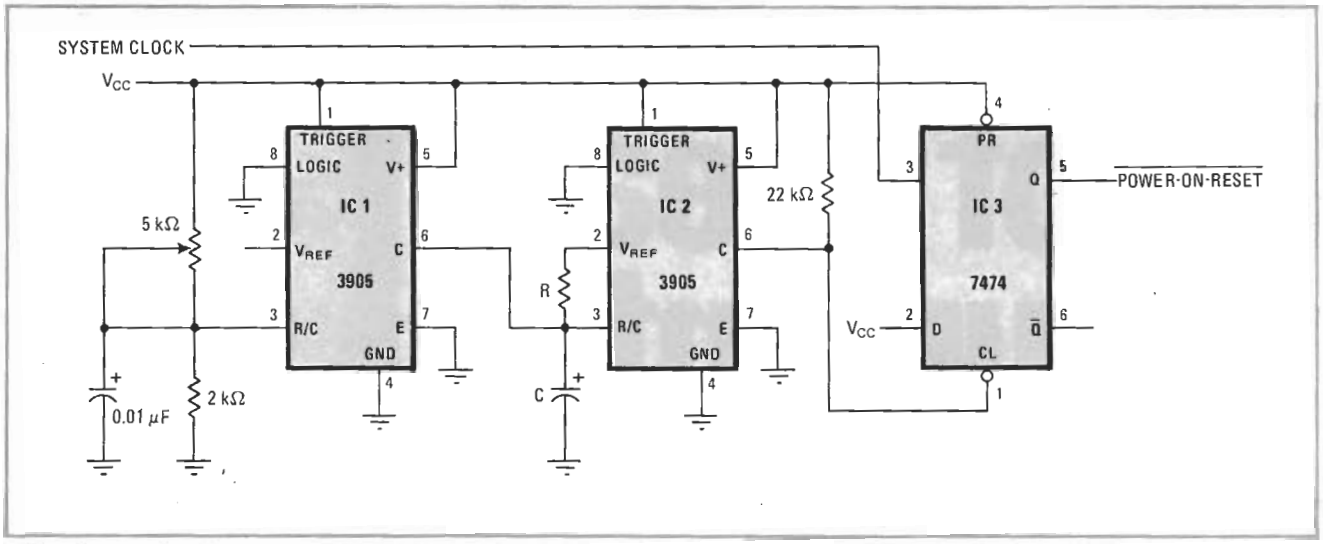
by Jim Felps
Texas Instruments Inc., Austin, Texas

Digital systems are commonly initialized with a power-on reset, generated automatically when the power switch is turned on, but at no other time. A typical circuit simply holds a reset line long enough for all the power transients to die out, then drops it. Its duration isn't well defined, and it doesn't respond to dips or glitches in the primary power line.

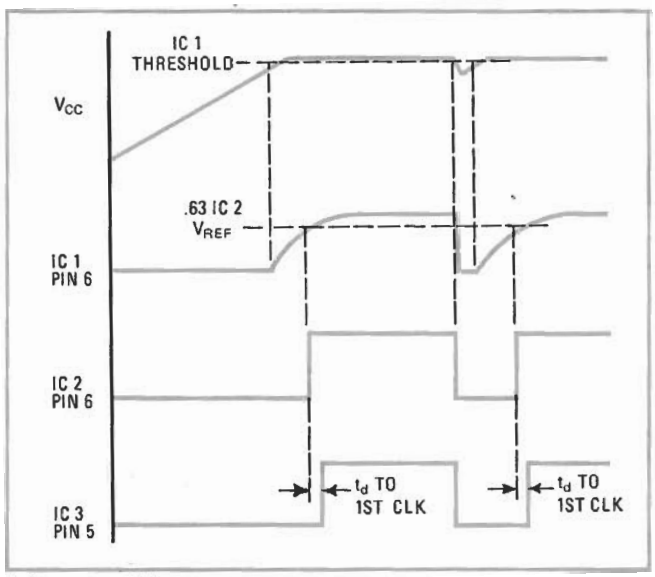
Until recently, a more precise power-on reset circuit would have been too complex and too costly to be justified. Now, however, new integrated circuits are available that contain voltage comparators and references that work at supply voltages as low as 4.5 volts. One such IC is the National Semiconductor LM 3905 N—a comparator, reference, and precision timer all in one eight-lead package.

In a power-on reset circuit based on the 3905 (Fig. 1), the timing begins only when the incoming V_{cc} has reached a suitable level, which can be very precisely established, and it is repeated if V_{cc} later drops even momentarily below that level. As a result, all logic circuits in the system are properly reset, even if the power reaches its nominal level only after an exceptionally long rise time, and no random logic failures can be caused by a power-line glitch.

IC 1 is a 3905 used as a comparator, which monitors the level of V_{cc} (nominally 5 volts for transistor-transistor logic). It keeps the reset on whenever V_{cc} is less than



1. Reset generator. One comparator, one timer and a flip-flop join forces to produce a precisely timed power-on reset.



2. Sequence. When V_{cc} reaches a threshold defined by the setting of the 5-kilohm potentiometer, IC 1 turns on. Its rise is delayed by the RC network on IC 2. After one time constant, the clear input to IC 3 is released, and the flip-flop is set by the next clock pulse.

4.75 V; its triggering level is established by setting V_{cc} at 4.75 and adjusting the 5-kilohm potentiometer at the point where the circuit's output (pin 5 of IC 3) just switches. Thereafter, when power is turned on and V_{cc} rises above this 4.75-v threshold (Fig. 2), IC 2, a 3905 used as a timer, is released. One time constant later, as determined by the RC network connected to pins 2 and 3 of IC 2, an ordinary 7474 D-type flip-flop, IC 3, is released. By this time the system clock should be running smoothly; at the next positive-going clock pulse the flip-flop is set, thus removing the power-on reset.

If the level of V_{cc} drops below 4.75 v at any time, both timers and the flip-flop immediately go down, generating another reset to the rest of the system. Restoration of V_{cc} initiates the power-on sequence again.

If less precise reset timing is necessary, IC 2 may be omitted. The output of IC 1 then rises as soon as the threshold has been passed, and the flip-flop is set by the next clock pulse. If several power supplies have to reach their nominal levels before the reset terminates, a separate 3095 as comparator can be connected to each supply and all the outputs (pin 6) connected to each other as a wired OR. □

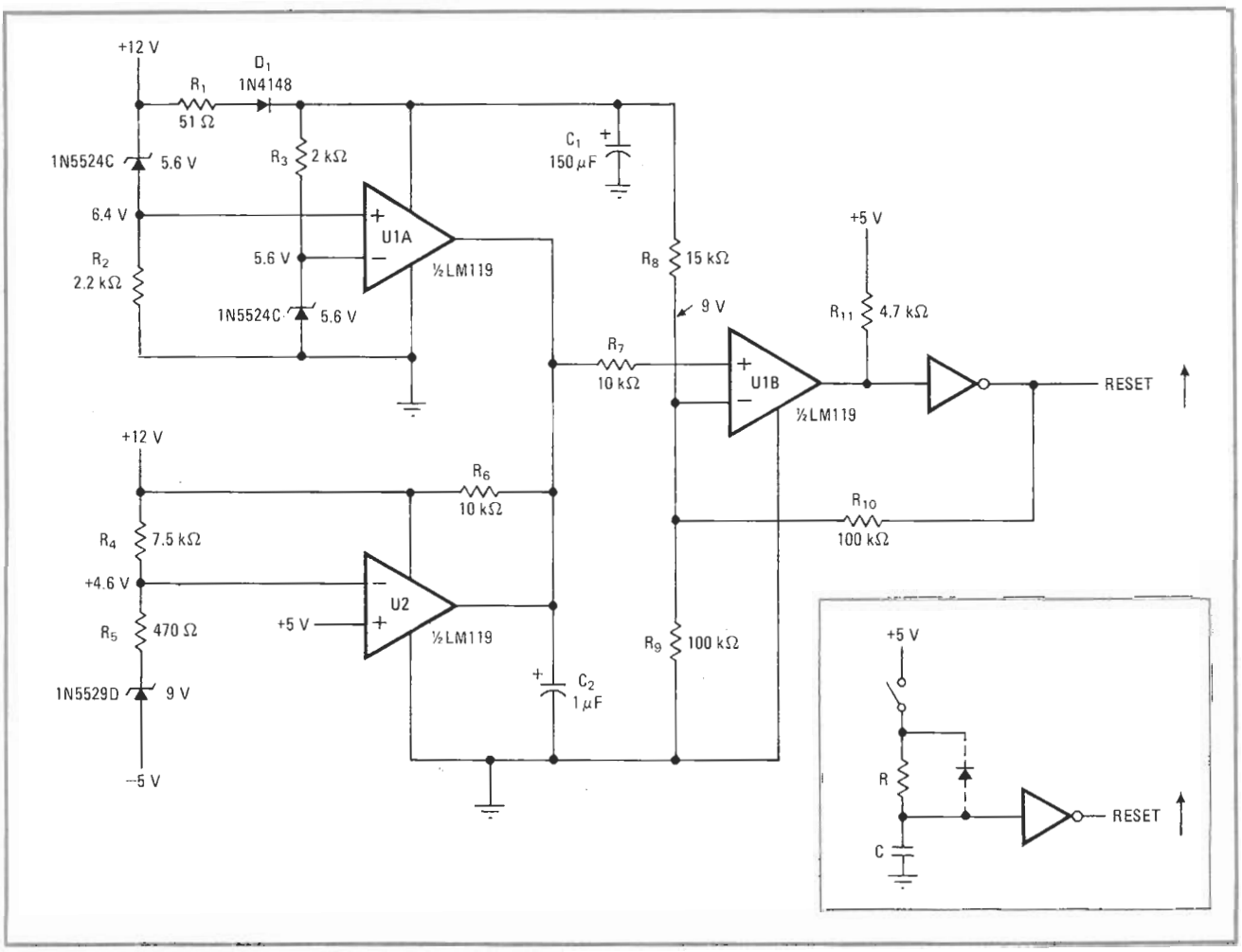
Fail-safe reset circuit initializes processor

by C. Gyles
Canadian Marconi Co., Montreal, Canada

No matter how unreliable the power source or troublesome the switch-on transients may be, this circuit will successfully initialize any circuit either during normal power-up conditions or after a power failure or glitch. This virtually fail-safe circuit was designed for a microprocessor with multiple power-source requirements (12, 5, and −5 volts), where transients could occur on one or more supplies, thus causing loss of data or other disasters in stringent control applications.

The most common reset circuit used to initialize microprocessors, one that is suggested by many manufacturers, is shown in the lower right-hand corner of the figure. When power is switched on, all microprocessor circuits are energized, but capacitor C charges slowly, meanwhile maintaining a reset condition (logic 1) at the output until all circuits stabilize. At stabilization, the capacitor is nearly charged and the reset signal is removed.

This circuit will not function satisfactorily if a momentary glitch should occur, because the capacitor voltage will not go below the 1 threshold before it again charges to the value of the supply voltage. Thus the circuits in the microprocessor may fail to function, but the circuits will not be reinitialized. Placing a diode permanently across the resistor to quickly discharge the capacitor is not always satisfactory, as the voltage could fall sufficiently to destroy processor operation but not enough to discharge the capacitor below the logic threshold. There is a cure—fully discharge the capacitor before the voltage has fallen below the component's threshold, thus assuring a reset signal if there is a power failure.



Fail-safe and foolproof. Simple RC circuit to the right cannot reliably initialize microprocessors under power-up or power-glitch conditions, even with addition of diode. Circuit using threshold detectors is more expensive but dependable.

Three threshold detectors using LM119 open-collector operational amplifiers overcome the inherent faults of the usual reset circuit. Comparator U_{1A} and its associated components form the 12-v detector, and U_2 is the ±5-v detector. Comparator U_{1B} monitors the voltage across a capacitor, C_2, in order to determine the state of the reset signal.

During power-up conditions, the inverting input of the op amp rises almost immediately to 9 v through a resistor divider consisting of R_1, D_1, R_8, and R_9. The noninverting input rises slowly to 12 v through R_6 and C_2. Thus U_{1B} is turned on and a reset signal is generated until the voltage on the noninverting input, which is the voltage across C_2, exceeds 9 v. The period of the reset signal is about 15 milliseconds, enough time for the microprocessor circuits to settle and be successfully initialized. During the switch-on transient, the internal operation U_{1B} is not defined; R_7 is therefore added to prevent premature charging of C_2 by current supplied from the noninverting input of the op amp.

In the steady state, voltages on the input ports to U_{1A} are within 0.8 v of one another, as shown. The voltage differences at the inputs to U_2 differ by only 0.4 v. These differences are arbitrarily set, and any value may be selected by the appropriate choice of zener diodes and divider resistors. A glitch on the 12-v line that causes a 0.8-v drop will cause U_{1A} to turn on, discharging C_2 and generating a reset signal. C_1 maintains voltage to the comparator's supply line to assure that the comparator fully discharges C_2 under conditions where the 12-v line voltage drops rapidly. D_1 prevents discharge into the collapsing 12-v line. In the event of a failure in either 5-v supply and not in the 12-v line, the 0.4-v threshold is exceeded, and comparator U_2 turns on, again discharging C_2 and producing a reset signal. R_{10} provides hysteresis to ensure a clean transition into the reset state. R_1 reduces the initial current surge through C_1.

The required length of the reset signal in any system depends on the settling time of the microprocessor circuits. Combinational logic will settle very fast, whereas divider chains or circuits that use large capacitors (one-shots) need a sufficiently long reset signal. □

Circuit guarantees logic system is reset when switched on

Two resistors, a capacitor, and a logic inverter are all it takes to assure that your logic system is reset when you switch on the power supply, say Emilio Bernstein and Marc Javnoozon of Jerusalem, Israel. The two resistors are connected as a voltage divider between the supply and ground. Let's call the resistor to the supply R_1, and the resistor to ground R_2. The capacitor is placed across R_2, and the input to the inverter is taken from the junction of R_1, R_2, and the capacitor.

When the supply is turned on, the inverter's output at first is high, but the capacitor starts charging until its voltage reaches the switching threshold of the inverter. When this happens, the inverter's output goes low, **producing a pulse that is suitable for resetting subsequent digital circuitry.** When the supply is shut off, the capacitor discharges to ground through R_2. R_1 determines the capacitor's charging time and charging current.

—Laurence Altman

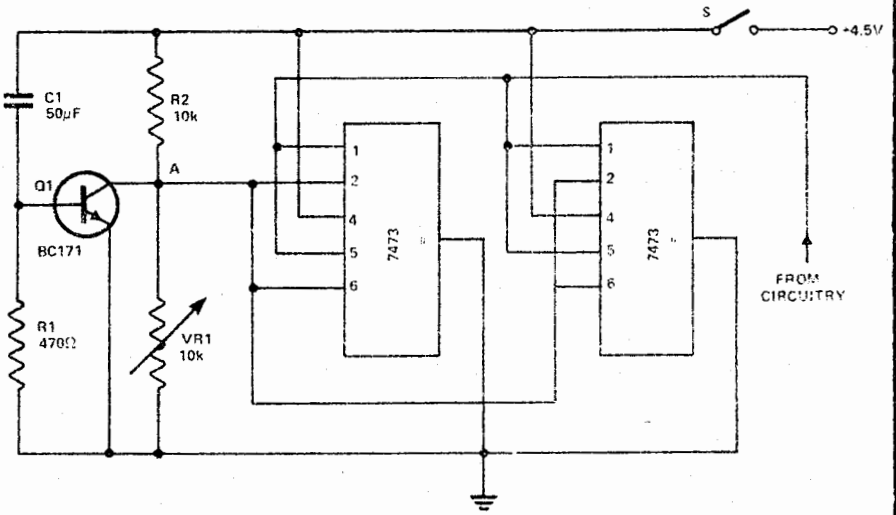
SELF–CLEAR

The network consists of two resistors R2 and VR1 arranged as a potential divider, the latter being shunted with a non linear load Q1 whose value depends on the voltage developed across R1. This is related to the charge of the capacitor C1. The resistor VR1 was made variable to make the design less critical.

As soon as S is closed, C1 starts charging; at the same time the base-emitter junction is being forward biased and Q1 conducts, bypassing VR1. Voltage at point A is "low" and a set pulse is produced, therefore.

When the charge on C1 reaches a given value, Q1 stops conducting and voltage at point A rises to a stabilized value which is approx. 4.5 VR1/(R2 + VR1).

Component values are not critical although R1 and R2 must be close to the indicated values.



Any NPN silicon transistor will work the prototype being assembled with the BC171.

VR1 adjustment depends, amongst other things, on the number of flip-flops and must be adjusted in each particular case to give best results.

Counter/monostable combo gets back to 0 easily

Getting a decade counter to initialize to 0 when the power goes on is easy, says Barton A. Gravatt of Newfield, N.Y. Simply connect the counter's reset input to the Q output of a retriggerable monostable, such as the 74123. Then connect the +5-volt supply to the monostable's positive-transition triggering input. Use a 1-second RC time constant at the monostable's external R and C terminals. **When power is applied to both devices, the Q output will not go high for a second, avoiding contact bounce and resetting the counter.**

Power-up relays prevent meter from pinning

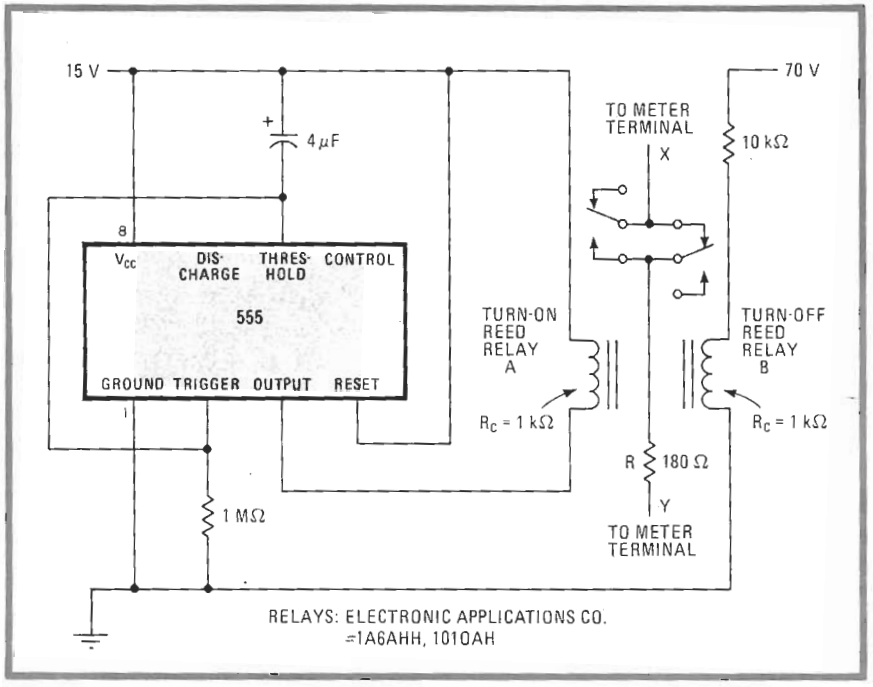
by Michael Bozoian
Ann Arbor, Mich.

Sensitive microammeters with d'Arsonval movements are still manufactured and used widely today, but surprisingly, there has been little attempt to correct one defect in their design—they are still very prone to pointer damage from input-signal overload and turn-on/turn-off transients. Although ways of protecting the meter movement from input signals of excessive magnitude are well known and universally applied, no convenient means of preventing the pointer from slamming against the full-scale stop during power-up or power-off conditions has so far been introduced or suggested in the literature. However, the problem may be easily solved by the use of a 555 timer and two relays to place a protective shunt across the meter during these periods.

Basically, the 555 timer closes reed relay A's normally open contacts on power up and puts shunt resistor R across the meter for 5 or 6 seconds until the turn-on transients have subsided, as shown in the figure. The normally closed contacts of relay B are also opened at this time.

On power-down, relay B reintroduces the shunt to protect the meter from turn-off transients. Such a scheme is more effective than placing a diode across the meter, as is often done and is much more elegant and less bothersome than manually activating an auxiliary mechanical switch for placing R across the meter each time it is used.

R has been selected for a meter movement having a full-scale output of 200 microamperes and an internal resistance of 1,400 ohms. The complete circuit may be mounted on a 2-by-2¼-inch printed-circuit board. The only design precaution is to ensure that relay B is energized from a source that has a fast decay time during power-off conditions. Here, the voltage has been tapped from the meter's power-supply rectifier. □

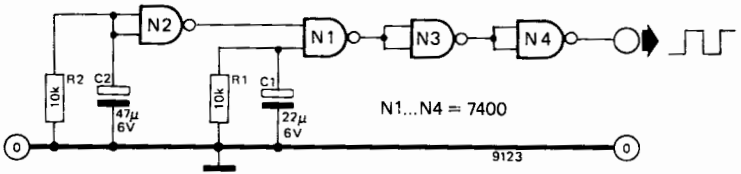


Shunted. Reed relays and 555 timer prevent d'Arsonval movement from slamming against microammeter's full-scale stop during power-up and power-down conditions by introducing shunt resistor across meter terminals until transients die out. Method does not degrade meter's accuracy or its transient response to input signals.

29

automatic reset for TTL circuits

W. Hollevoet



When the supply voltage is switched off, TTL counters and memories lose their information. To prevent them from assuming a random position when the supply voltage is switched on again, we can use the circuit described in this article for a complete automatic resetting or presetting to a certain position.
The auto reset circuit functions as follows:
When the supply voltage is switched on, the output of N1 will become logic '1', because capacitor C1 is not yet charged. Since C2 will not be charged either, the output of N2 will also be logic '1'.
The time constants are chosen so that the charging time of C1 is shorter than that of C2. This means that at a certain moment C1 is sufficiently charged for both inputs of N1 to be logic '1', so that the output will be '0'.
A short time later, when C2 has charged sufficiently, the output of N2 will become logic '0', with the result that the output of N1 will immediately return to logic '1'. From then on the circuit is stable.
The resistors R1 and R2 serve to discharge the electrolytic capacitors C1 and C2 when the supply voltage cuts out. The moment of switching, and also the pulse duration, can be modified by experimenting with the values of the two resistors and capacitors; the charging time of C1 must, however, always be shorter than that of C2! The values given here will be suitable in most cases.