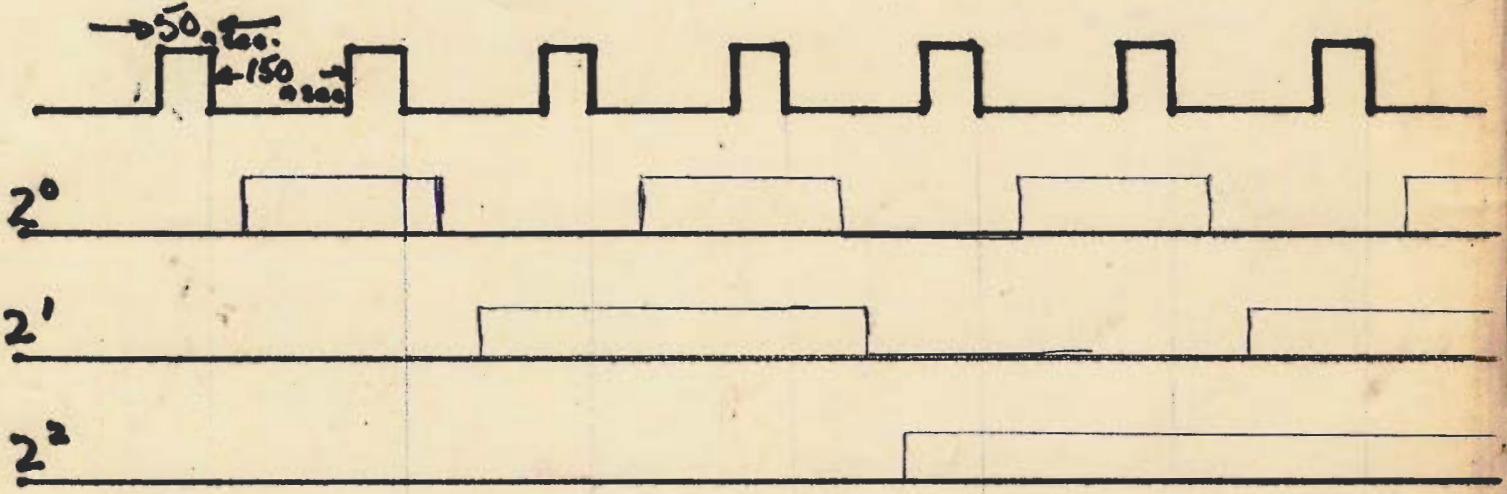
ET 771/72 ASSIGNMENT # 6-7 NAME _____

NOTE: Only logic functions as per computer lab to be used. Some assignment problems to be completed using logic labs.

1. Given the following clock pulse train for a three bit asynchronous counter, draw the timing diagram assuming that the delay for each flip-flop is 35 nsec. Assume that the register is reset prior to the first clock pulse.



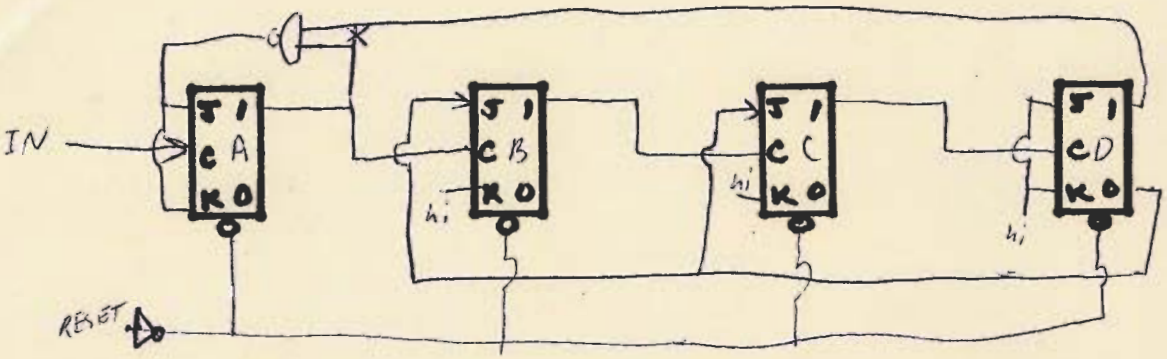
2. Connect a basic 4 Bit Asynchronous (ripple) up counter using feedback from the $\overline{Q}$ of the last stage to disable the J & K inputs of the first stage. Using the reset to start the counter determine the maximum frequency of operation. Determine the average PROPAGATION DELAY of the J-K flip flops used.

MAXIMUM FREQUENCY = 7.15 MHz $= \frac{1}{140ns}$

PROPAGATION DELAY = 140ns

ASSUMING DELAY/F.F. = 35ns.

3. Design a Modulo 10 (0-9) self-stopping asynchronous up-counter.



on gate B & C both JK FFs CAN BE LEFT HI but if circuit is hooked up as shown we have redundant circuitry for extra reliability.

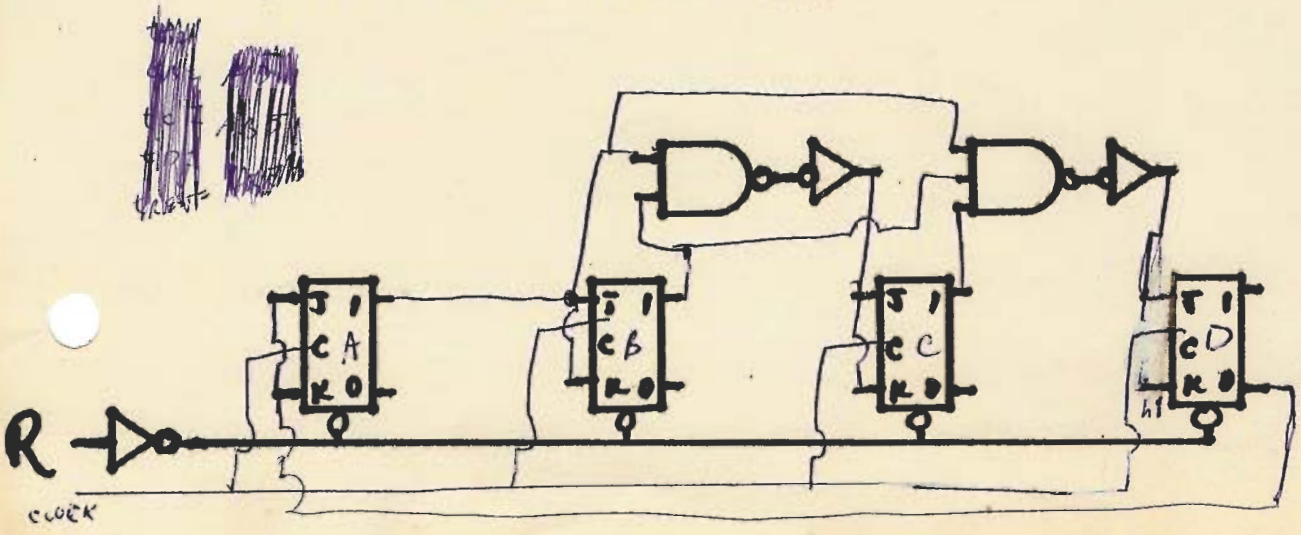
4. Describe two ways in which an up counter (either synchronous or asynchronous) can be modified to convert it to a down counter.

a. Place lights on $\overline{Q}$ outputs rather than Q outputs

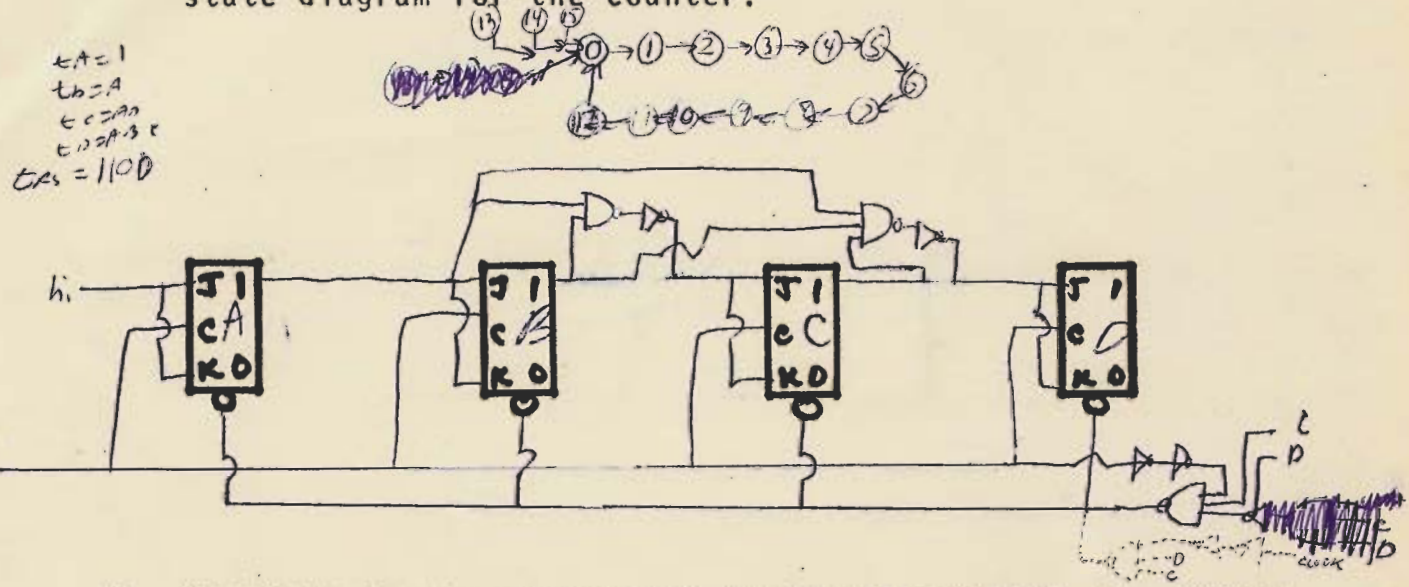
b. Drive the following clock input from the $\overline{Q}$ output (asynchronous counter).

$\overline{A}B$ rather than $A\overline{B}$ for asynchronous.

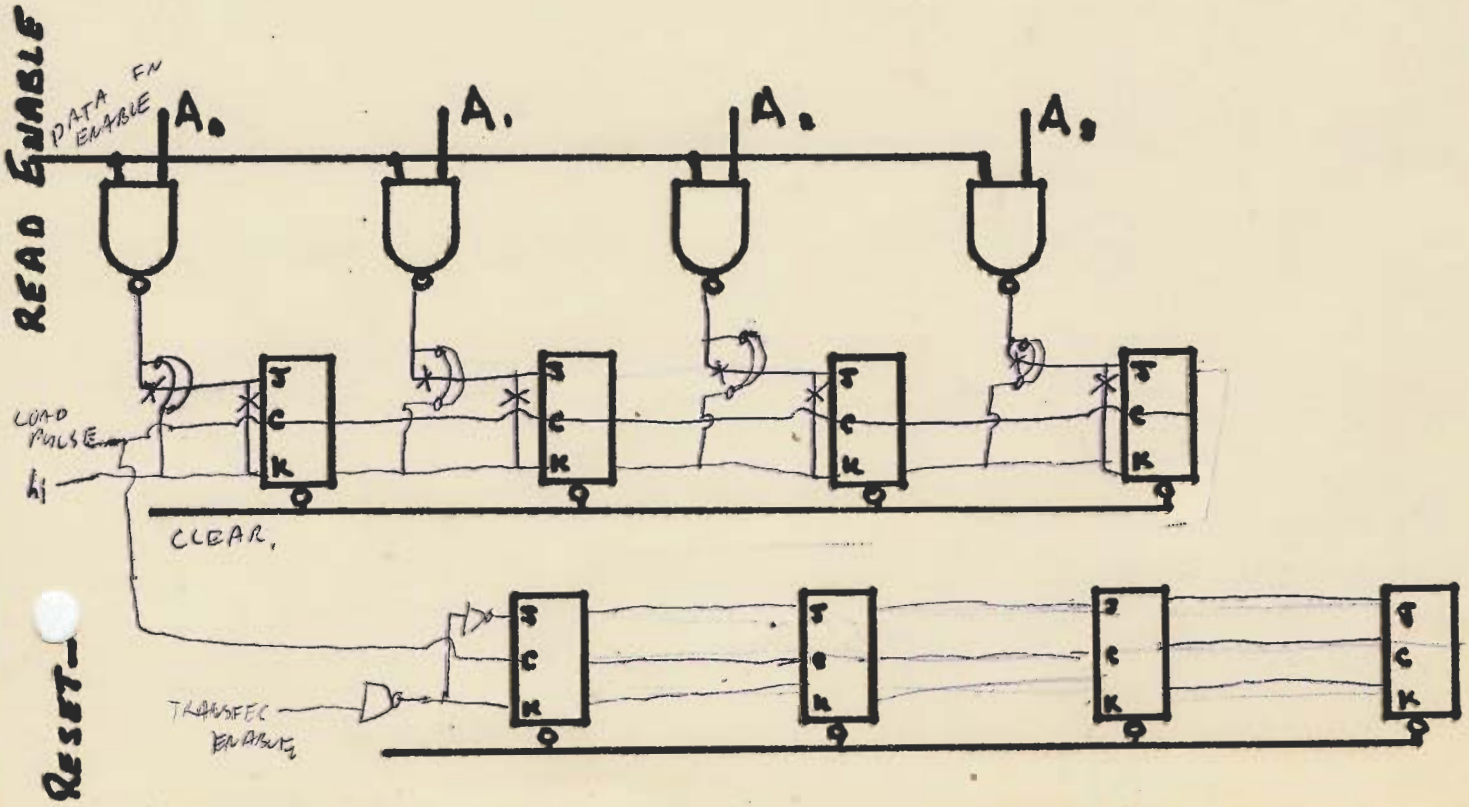
5. Design a modulo 9 (0-8) synchronous up-counter. No additional gates to be used for feedback.



6. Design a Modulo 13 synchronous counter. Draw the complete state diagram for the counter.



7. Complete the design for the following PARALLEL IN - SERIAL OUT REGISTERS. Use a READ ENABLE etc. to BLOCK SHIFT and READ DATA IN. Design the circuitry necessary to fill the register up with zeros as the shifting takes place so that a READ rather than a JAM TRANSFER is sufficient for parallel read in. Determine the number of unit loads on the clock and reset.



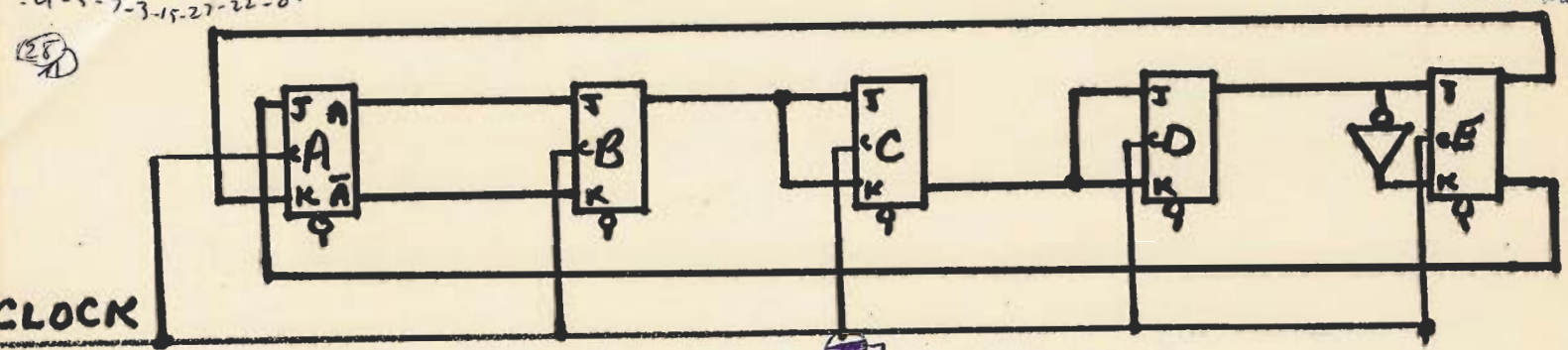
8. Develop the complete state diagram for the following circuit. Start in ØØØØ. Write eqn's for each flip flop. Determine a second name for the output sequence of this type of circuit.

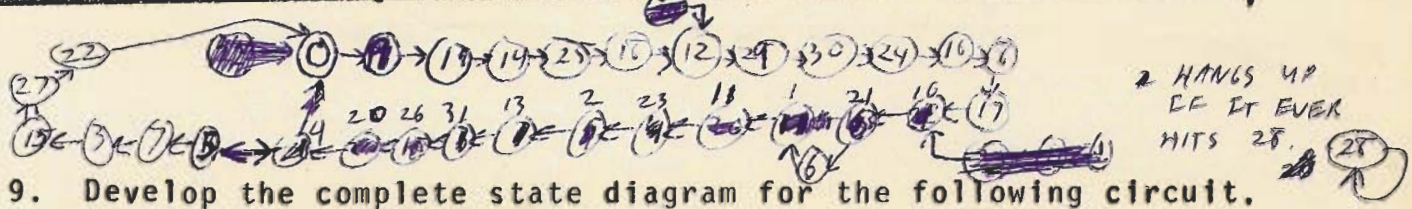
0-9-14-14-25-18
-12-29-30-24-16-8
-17-10-21-6-1-11
-23-2-13-31-26-20
-4-5-7-3-15-27-22-0.

Powers Random number generator

Maximal Length Sequence generator

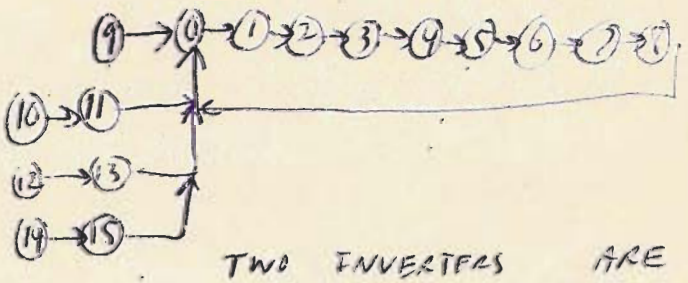
$A(t+1) = \bar{E}$ $\quad B(t+1) = A$ $\quad C(t+1) = \bar{C}B + C\bar{B} = C \oplus B$ $\quad D(t+1) = \bar{D}\bar{C} + DC = \overline{C \oplus D}$ $\quad E(t+1) = D$





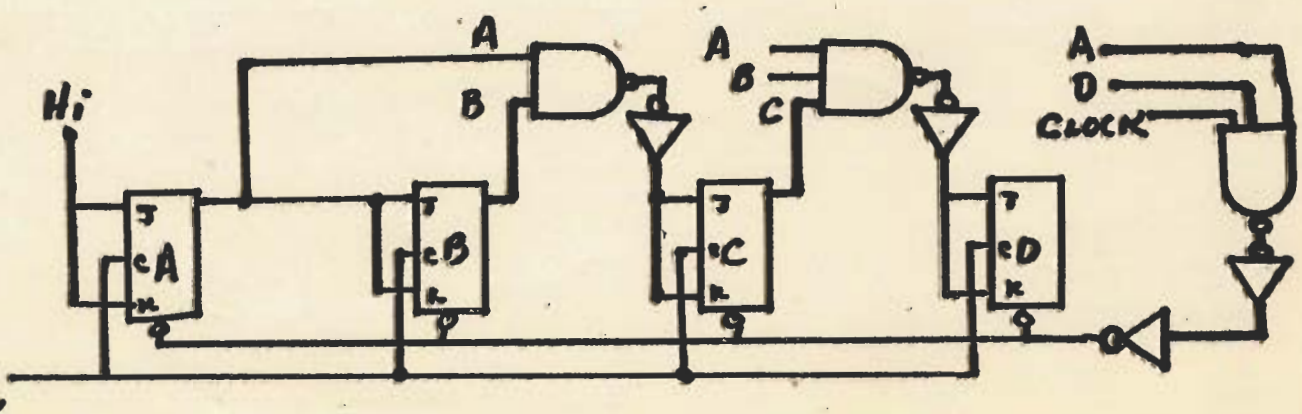
2 HANGS UP IF IT EVER HITS 28.

9. Develop the complete state diagram for the following circuit. Explain why two inverters are needed. Be Precise.
Propagation delay of flip-flop = 35 nsec.
Propagation delay of gate = 15 nsec.

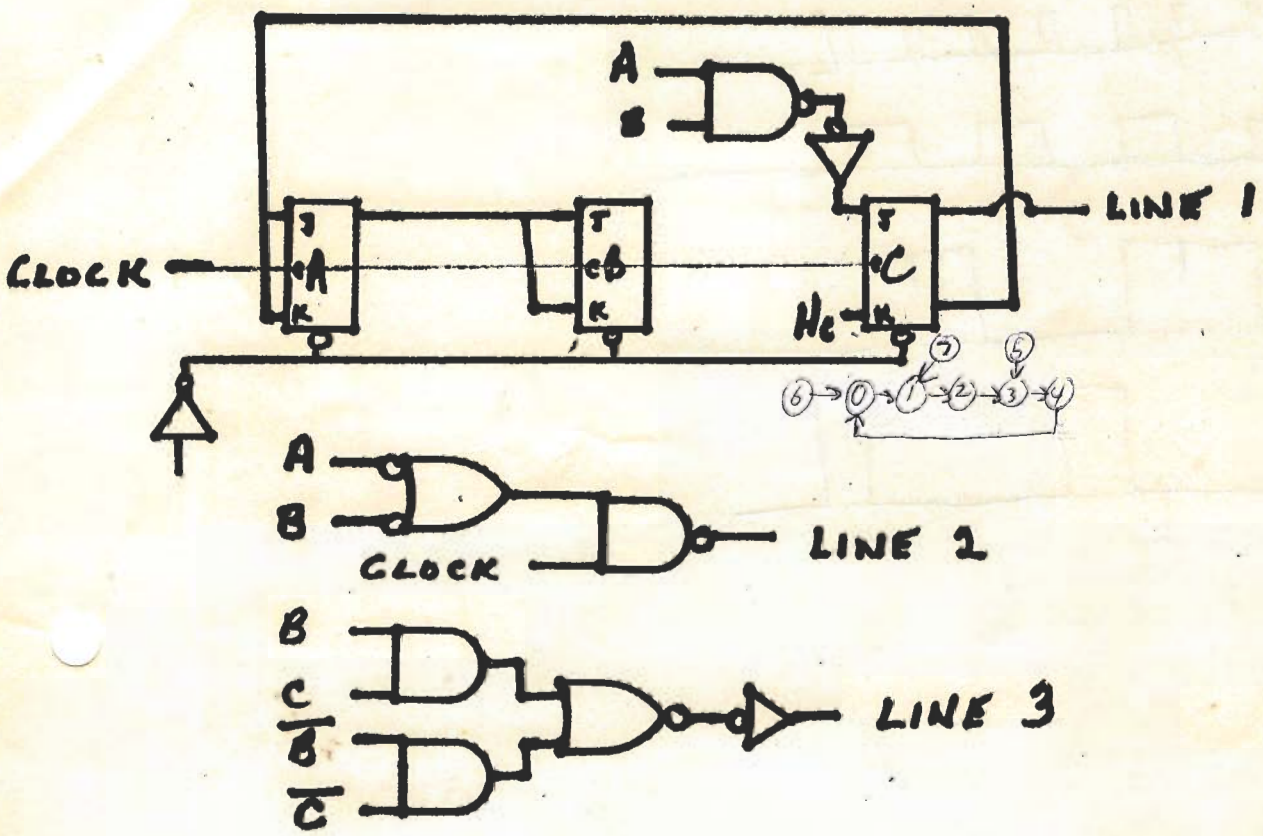


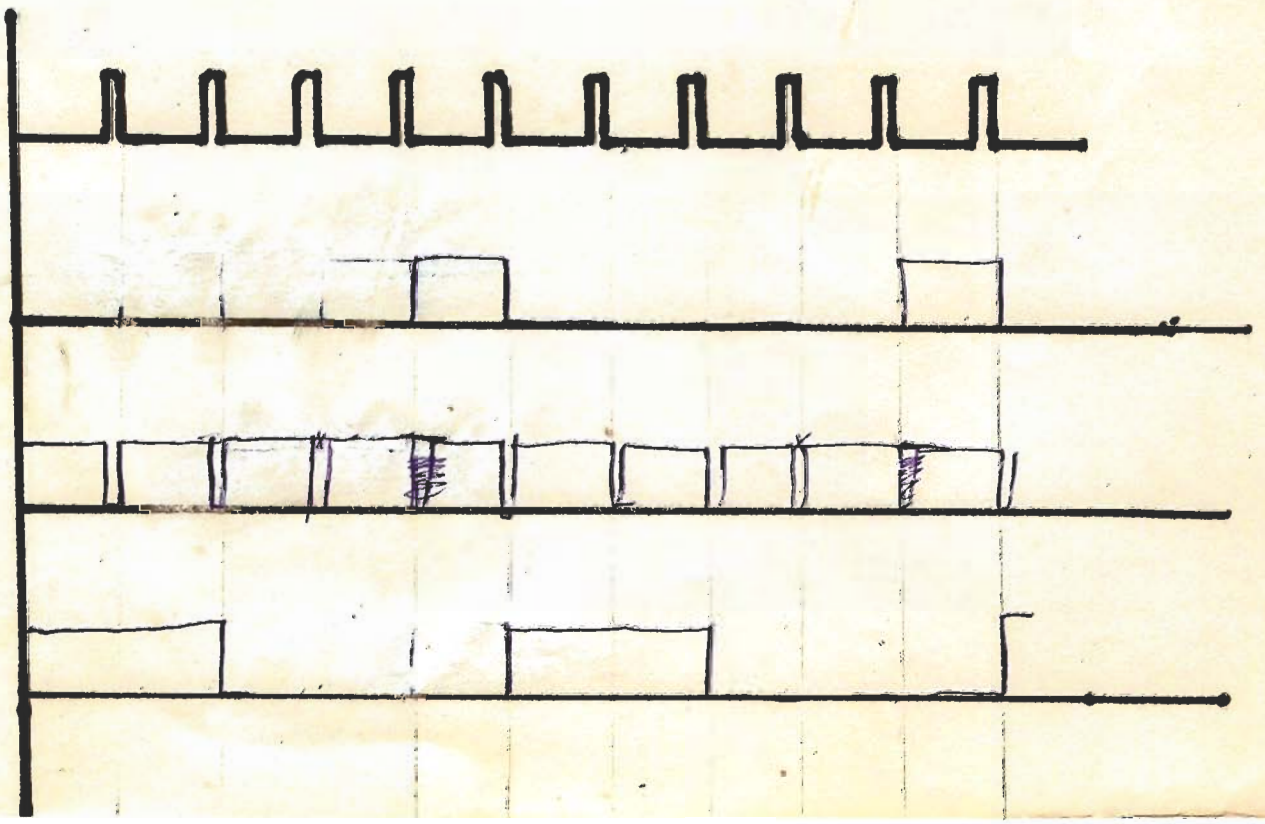
0-1-2-3-4-5-6-7-8-9-1
0 appears for a very short time

TWO INVERTERS ARE USED SO THE RESET PULSES ARRIVE AFTER THE CLOCK PULSE SO THERE IS NO ACCIDENTAL DOUBLE TRIGGERING.

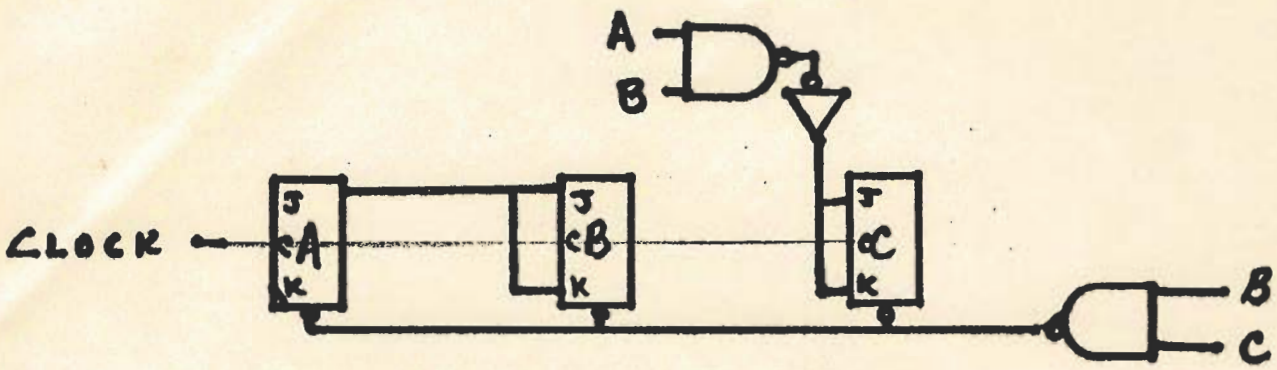


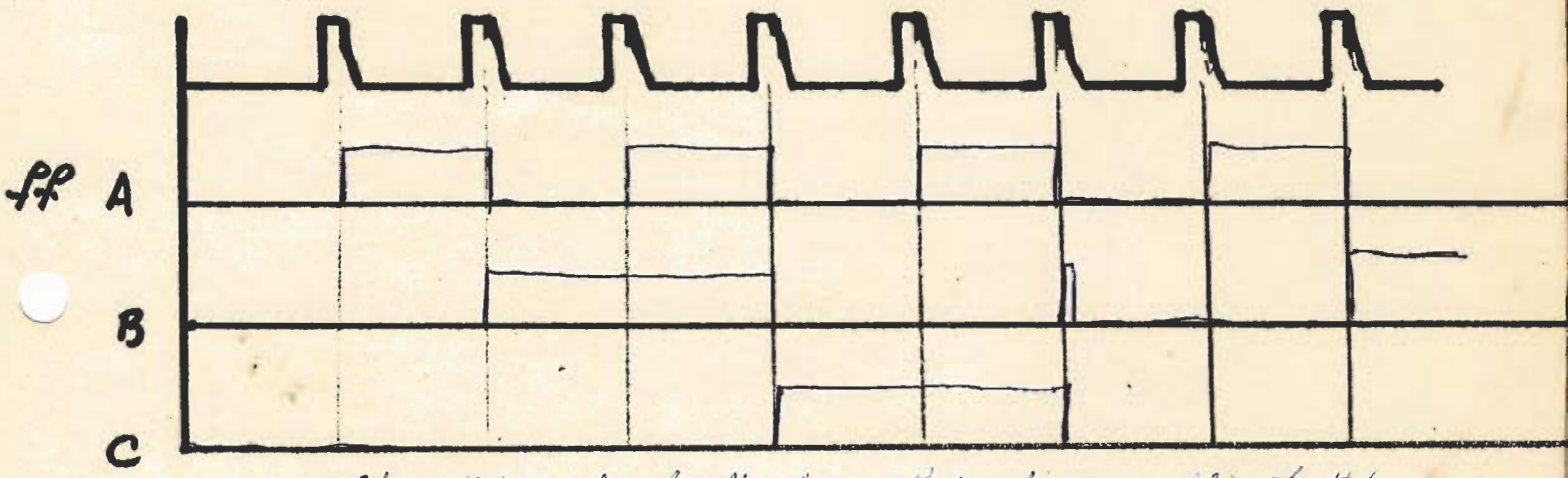
10. Determine the complete state diagram for the following circuit. Show output waveforms on lines as indicated. (Flip-flops reset to zero before first pulse applied).





11. Draw the waveforms for the following circuit. Explain why a Glich is obtained.



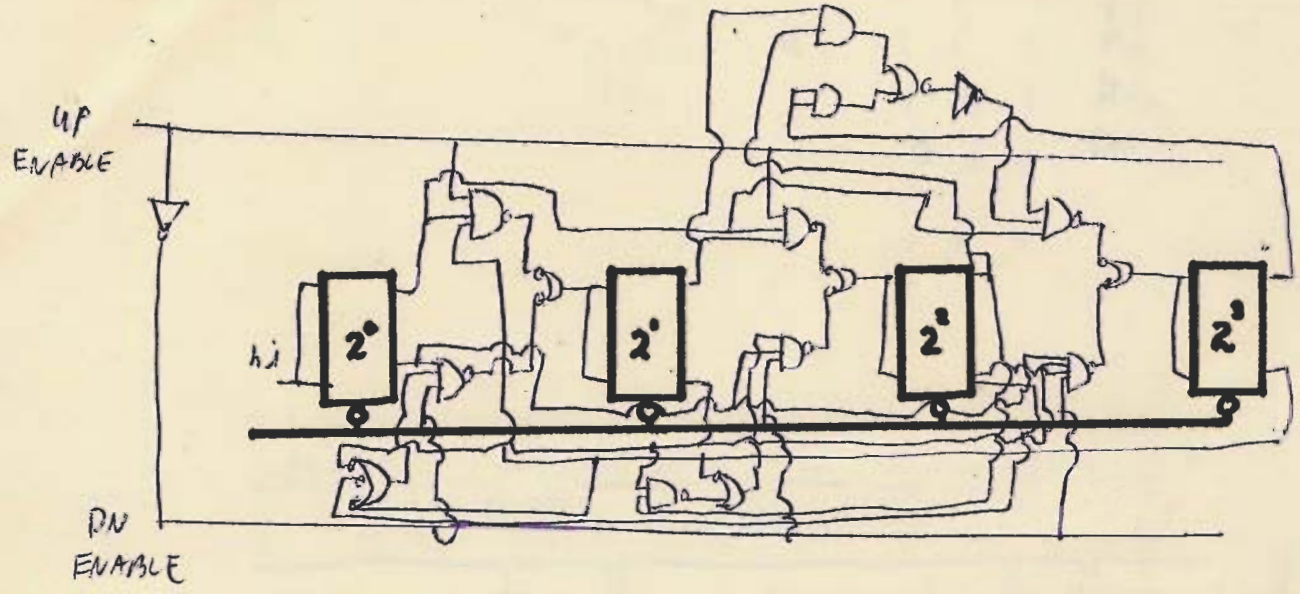


The Glich is due to the fact that the CCT flips to #6 then resets to 0 after the delay time of the gate is passed. Reset delay is the the F.F delay + the gate delay while only F.F delay matters in counting.

12. Considering the circuit to be designed for question 13. What happens if both the up enable and down enable lines of the synchronous BCD up/down counter are simultaneously enabled with a HI level when a clock pulse occurs? Why?:

ALL F.F's WILL FLIP AS ALL FF's INPUTS (J&K INPUTS) WILL BECOME HIGH ~~STAT~~ AT ONCE & THE NEXT CLOCK PULSE will FLIP EVERY F.F.

13. Design a synchronous Modulo 10 (BCD) up/down (0-9) counter.



ASSUME CLOCK ATTACHED TO ALL F/F'S.

14. Design the circuitry around the following register to give the waveforms as indicated.