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CHAPTER 13: DESIGN DEVELOPMENT TOOLS

Introduction

There are several tools available to help in the design and verification of a design. From software that helps in the part selection to circuit simulation and error budget analysis, these tools make the process of design faster, easier, and more exact.

The first section covers the simulation software. Primary among these is Spice. Originally developed for analysis of linear circuits for the integrated circuit industry (Spice is an acronym for *Simulation Program with Integrated Circuit Emphasis*), it has expanded to become the primary linear simulation engine. It has become available in many versions, such as Pspice®, Hspice®, as well as others. The original Spice was developed in the mid-1970s. It originally ran on mainframes, obviously without the benefit of a graphical user interface (GUI). Most of the proprietary versions use front end and back end processing to make the human interface easier. Some add other features, such as Monte-Carlo analysis. All handle the basic Spice functions the same, however. At Analog Devices, we have settled on Pspice as our standard, but we use only the basic SPICE2-G functions. This makes the files more transportable.

For very large circuits, such as a data converter, Spice becomes increasingly harder to use. For this reason, we shift from component level modeling to behavioral modeling. An example of this is the ADIsimADC program, which is also discussed in this section.

In the second section we discuss the family of on-line tools developed by Analog Devices. These range from relatively simple tools, such as the settling time calculator to "wizards," such as the filter design wizard. Wizards help design the circuits as well as assist in part selection.

No matter how much simulation and design tools may help with the design of the circuit, there is absolutely no substitute for actually building the circuit. The last section discusses evaluation boards and prototyping techniques.

BASIC LINEAR DESIGN

SECTION 13.1: SIMULATION

Spice

In the past decade, circuit simulation has taken on an increasingly important role within analog circuit design. The most popular simulation tool for this is Spice, which is available in multiple forms for various computer platforms (see References 1 and 2). However, to achieve meaningful simulation results, designers need accurate models of many system components. The most critical of these are realistic models for ICs, the active devices that drive modern designs. In the early 1990s, Analog Devices developed an advanced op amp Spice model, which is in fact still in use today (see References 3 and 4). Within this innovative open amplifier architecture, gain and phase response can be fully modeled, enabling designers to accurately predict ac, dc, and transient performance behavior. This modeling methodology has also been extended to include other devices such as in-amps, voltage references, and analog multipliers.

The popularity of Spice simulation has led to many op amp macromodel releases, which (ideally) software-mimic amplifier electrical performance. With numerous models available, several confusions are possible. There may be uncertainty as to what is/isn't modeled, plus a basic question of *model accuracy*. All of these points are important, in order to place confidence in simulation results. So, *verification* of a model is important, checking it by comparison to the actual device performance conditions, before trusting it for serious designs.

Of course, a successful first design step using an accurate op amp model by itself doesn't necessarily guarantee totally valid simulations. A simulation based on incomplete information has limited value. All parts of a target circuit should be modeled, including the surrounding passive components, various parasitic effects, and temperature changes. Then, the circuit needs to be verified in the lab, by breadboarding and prototyping. A breadboard circuit is a quickly executed mockup of a circuit design using a semi-permanent lab platform, i.e., one which is less than final physical form. It is intended to show real performance, but without the total physical environment. A good breadboard can often reveal behavior not predicted by Spice, either because of an incomplete model, external circuit parasitics, or numerous other reasons. However, by using Spice along with intelligent breadboarding techniques, a circuit can be efficiently and quickly designed with reasonably good assurance of working properly on a prototype version, or even a final PCB. The following prototype phase is just one step removed from a final PCB, and may in fact be an actual test PCB, with nearly all design components incorporated, and with close to full performance.

The breadboard/prototype design steps are closely allied to simulation, usually following it in the overall design process. These are more fully discussed in subsequent sections.

Macromodel vs. Micromodel

The distinction between *macromodel* and *micromodel* is often unclear. A micromodel uses the actual *transistor level* and other Spice models of an IC device, with all active and passive parts fully characterized according to the manufacturing process. In differentiating this type of model from a macromodel, some authors use the term *device level model* to describe the resulting overall op amp model. Typically, a micromodel is used in the actual design process of an IC.

	METHODOLOGY	ADVANTAGES	DISADVANTAGES
MACROMODEL	IDEAL ELEMENTS MODEL DEVICE BEHAVIOR	FAST SIMULATION TIME, EASILY MODIFIED	MAY NOT MODEL ALL CHARACTERISTICS
MICROMODEL	FULLY CHARACTERIZED TRANSISTOR LEVEL CIRCUIT	MOST COMPLETE MODEL	SLOW SIMULATION, CONVERGENCE DIFFICULTY, NON-AVAILABILITY

Figure 13.1: *Differentiating the Macromodel and Micromodel*

A macromodel goes another route in emulating op amp performance. Taking into consideration final device performance, it uses ideal native Spice elements to model observed behavior—as many as necessary. In developing a macromodel, a real device is measured in terms of lab and data sheet performance, and the macromodel is adjusted to match this behavior. Some aspects of performance may be sacrificed in doing this. Figure 13.1 compares the major pros and cons between macromodels and micromodels.

There are advantages and disadvantages to both approaches. A micromodel can give a complete and accurate model of op amp circuit behavior under almost all conditions. But, because of a large number of transistors and diodes with nonlinear junctions, simulation time is very long. Of course, manufacturers are also reluctant to release such models, since they contain proprietary information. And, even though all transistors may be included, this isn't a guarantee of total accuracy, as the transistor models themselves don't cover all operational regions precisely. Furthermore, with a high node count, Spice can have convergence difficulties, causing a failed simulation. This point would make a micromodel virtually useless for multiple amplifier active filters, for example.

On the other hand, a carefully developed macromodel can produce both accurate results and simulation time savings. In more advanced macromodels such as the ADSpice model described below, transient and ac device performance can be closely replicated. Op amp nonlinear behavior can also be included, such as output voltage and current swing limits.

However, because these macromodels are still simplifications of real devices, all nonlinearities aren't modeled. For example, not all ADSpice models include common-mode input voltage range, or noise (while more recent ones do). Typically, in model

development parameters are optimized as may be critical to the intended application—for example, ac and transient response. Including every possible characteristic could lead to cumbersome macromodels that may even have convergence problems. Thus, ADSpice macromodels include those op amp behavior characteristics critical to intended performance for normal operating conditions, but not necessarily all nonlinear behavior.

The ADSpice Op Amp Macromodels

The basic ADSpice model was developed as an op amp macromodeling advance, and as an improved design tool for more accurate application circuit simulations. Since being introduced in 1990, it has become a standard op amp macromodel topology, as evidenced by industry adoption of the frequency shaping concepts.

Prior to about 1990, a dominant op amp model architecture was the Boyle model. This macromodel, developed in the early ’70s, cannot accurately model higher speed amplifiers. The primary reason for this is that it has limited frequency shaping ability—only two poles and no zeroes. In contrast, the ADSpice model topology has a flexible and open architecture, allowing virtually unlimited pole and zero frequency shaping stages to be cascaded. This key difference provides much more accurate ac and transient response, vis-à-vis the more simplistic Boyle model topology.

An ADSpice model is comprised of three main portions, described as follows. The first of these is a combined input and gain stage, which will include transistor models as appropriate to the device being modeled (NPN or PNP bipolar, JFET, MOSFET, etc.). Next are the synthetic pole and zero stages, which are comprised of ideal Spice native elements. There may be only a few of these or there may be many, dependent on the complexity of the op amp’s frequency response. Finally, there is an output stage, which couples the first two sections to the outside world.

Before describing these sections in detail, it is important to realize that many variations upon what is shown below do in fact exist. This is due to not just differences from one op amp model to another, but also to evolutionary topology developments in op amp hardware, which in turn has led to corresponding modeling changes. For example, modern op amps often include either rail-to-rail output or input stages, or both. Consequently more recent developments in the ADSpice models have addressed these issues, along with corresponding model developments.

Furthermore, although the Boyle model and the original ADSpice models were designed to support *voltage feedback* op amp topologies, subsequent additions have added *current feedback* amplifier topologies. In fact, Reference 9 describes an ADSpice current feedback macromodel which appeared just shortly after the voltage feedback model of Reference 3. These current feedback macromodels are discussed in more detail below.

Input and Gain/Pole Stages

A basic ADSpice voltage feedback op amp macromodel input stage is shown in Figure 13.2. As noted, it uses what are (typically) the only transistors in the entire model, in this example the Q1-Q2 NPN pair, to the left on the diagram. These are needed to properly model an op amp's differential input stage characteristics. A basic tenet of this model topology is that this stage is designed for unity gain, by the proper choice of Q1-Q2 operating current and gain-setting resistors R3-R4 and R5-R6.

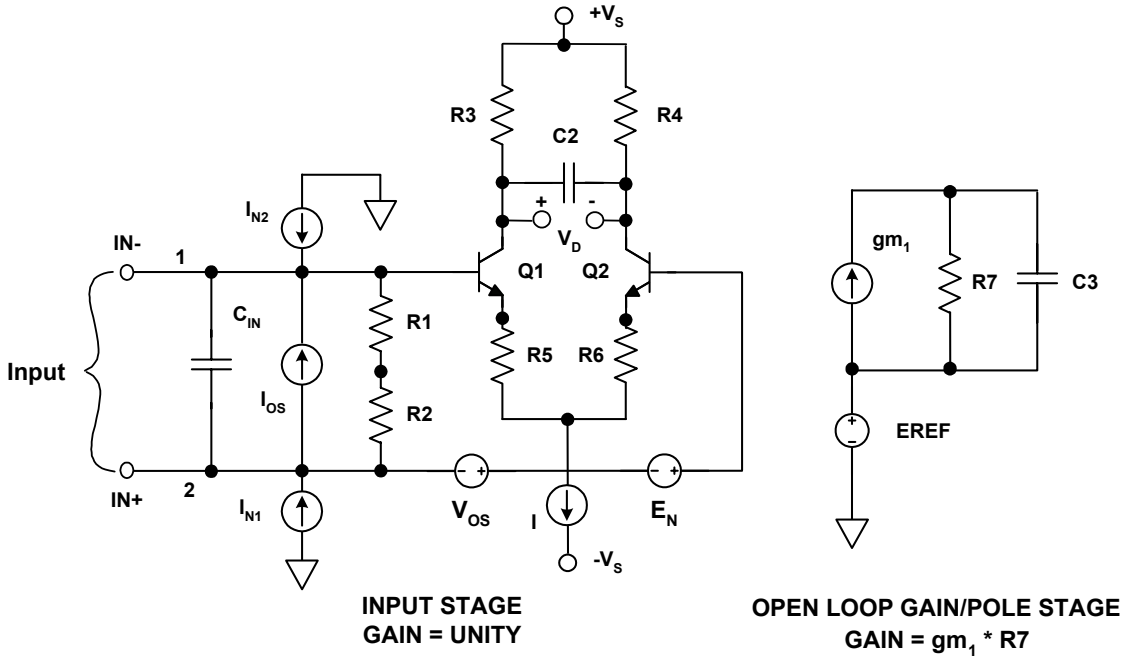


Figure 13.2: *Input and Gain/Pole Stages of ADSpice Macromodel*

Although this example uses NPN transistors, the input stage is easily modified to use PNP bipolars, JFET, MOSFET devices, or even the NPN-PNP combination typically found in rail-to-rail input op amps. The rest of the input stage uses simple Spice elements such as resistors, capacitors, and controlled sources.

The open-loop gain vs. frequency characteristics of the modeled op amp is provided by the gain stage, to the right in the diagram. Here controlled source gm_1 senses the differential collector voltage V_D from the input stage, converting this voltage to a proportional current. The gm_1 output current flows in load resistor R7, producing a single ended voltage referenced to an internal voltage, EREF. Typically, this voltage is derived as a supply voltage midpoint, and is used throughout the model.

By simply making the gm_1-R7 product equal to the specified gain of the op amp, this stage produces the entire open-loop gain of the macromodel. This design factor means that all other model stages operate at unity gain, a feature leading to significant flexibility in adding and deleting subsequent stages. This approach allows the quick synthesis of the

complex ac characteristics typical of high performance, high speed op amps. In addition, this stage also provides the dominant pole of the amplifier's ac response. The open-loop pole frequency is set by selection of capacitor C3, as noted in the diagram.

Frequency Shaping Stages

Following the gain stage of the macromodel is a variable but unlimited number of pole and/or zero stages, which in combination provide frequency response shaping. Typical topologies for these stages are as shown in the Figure 13.3 diagram. The stages can be either a single pole or a single zero, or combined pole/zero or zero/pole stages. All such stages have a dc transfer gain of unity, and a given amplifier type can have all or just a few of these stages, as may be required to synthesize its response.

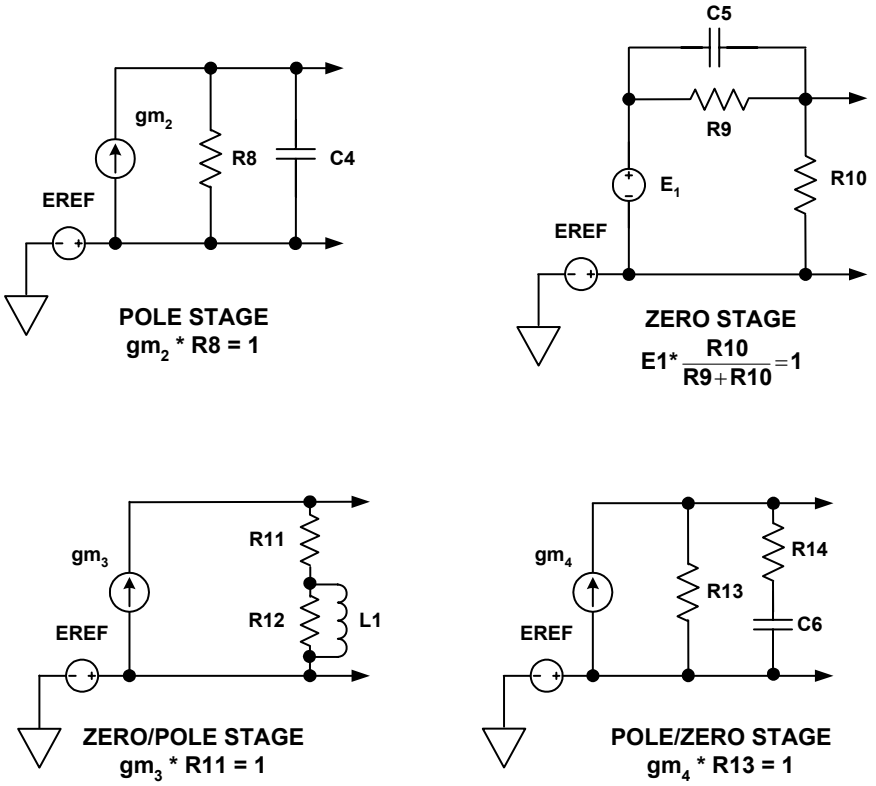


Figure 13.3: *The Frequency Shaping Stages Possible Within the ADSpice Model*

The pole or zero frequency is set by the combination of the resistor(s) and capacitor, or resistor(s) and inductor, as may be the case. Because an infinite number of values are possible in Spice, choice of RC values is somewhat arbitrary, and a wide range work. Early ADSpice models used relatively high values, while later ones employ lower values to reduce noise (described in more detail later). In all instances, it is assumed that each

stage provides zero loading to the driving stage. The stages shown reflect no particular op amp, but example principles can be found within the OP27 model.

Because all of these frequency-shaping stages are dc-coupled and have unity gain, any number of them can be added or deleted, with no affect on the model's low frequency response. Most importantly, the high frequency gain and phase response can be precisely tailored to match a real amplifier's response. The benefits of this frequency-shaping flexibility are especially apparent in performance comparisons of the ADSpice model closed loop pulse response and stability analysis, versus that of a more simplistic model. This point is demonstrated by a later example.

Macromodel Output Stages

A general form of the output stage for the ADSpice model, shown in Figure 13.4, models a number of important op amp characteristics. The Thevenin equivalent resistance of R_{O1} and R_{O2} mimics the op amp's dc open loop output impedance, while inductor L_O models the rise in impedance at high frequencies. A unity gain characteristic for the stage is set by the g_7-R_{O1} and g_8-R_{O2} products.

Additionally, output load current is correctly reflected in the supply currents. This feature is a significant improvement over the Boyle model, because the power consumption of the loaded circuit can be analyzed accurately. Furthermore, circuits using the op amp supply currents as part of the signal path can also be correctly simulated. The output stage shown is not intended to reflect any particular op amp, but close similarity is found within the AD817 model.

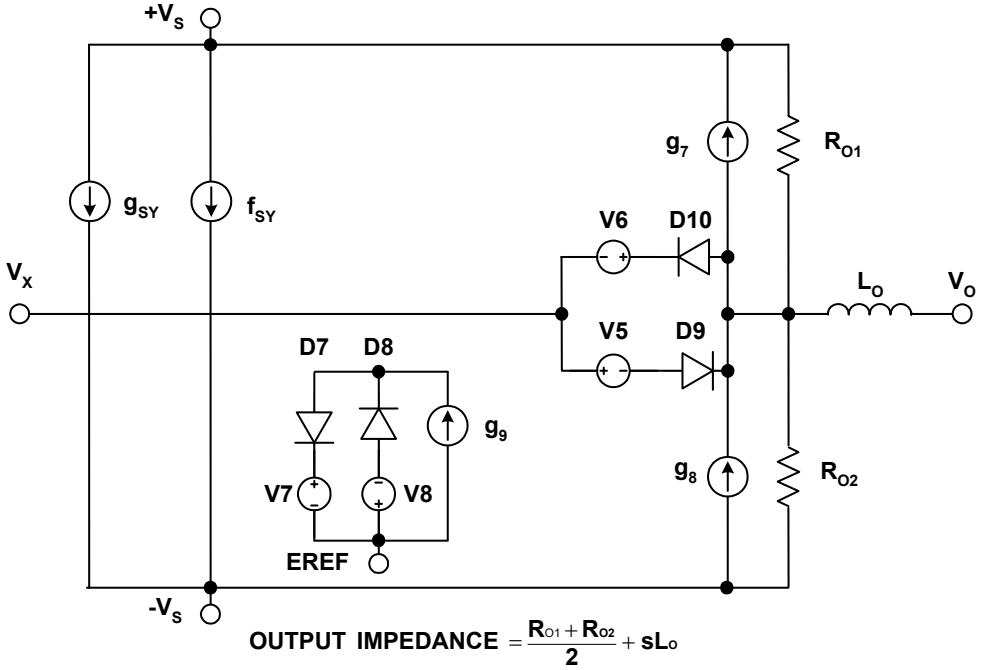


Figure 13.4: *General-Purpose Macromodel Output Stage*

With the recent advent of numerous rail-to-rail output stage op amps, a number of customized model topologies have been developed. This expands the ADSpice library to include rail-to-rail model behavior, matching op amp architectures using P and N MOSFET devices, as well as bipolar devices. Characteristically, a rail-to-rail output stage includes several key differentiating performance points. First and foremost is the ability to swing the op amp output to within a few mV of both supplies. A second point is the fact that such an output stage has a voltage gain greater than one, and a third is the relatively high output impedance (high as contrasted to traditional emitter follower outputs).

In addition to rail-rail output operation, many modern op amps also feature rail-to-rail *input stages*. Such stages essentially duplicate, for example, an NPN-based differential stage with a complementary PNP stage, both stages operating in parallel. This allows the op amp to provide a CM range that includes both supply rails. This performance feature can also be accomplished within CMOS op amps, using both a P and N type MOS differential pairs.

Model Transient Response

The performance advantage of the multiple pole/zero stages is readily demonstrated in a transient pulse response test, as in Figure 13.5. This figure compares an actual OP249 op amp, the ADSpice model, and the Boyle model. It reveals the improved execution resulting from the unlimited number of poles and zeros in this model.

The difference is easily apparent from this transient analysis plot for a unity gain follower circuit. An OP249 amplifier was used, with the output connected to the inverting input, and a 260 pF capacitive load.

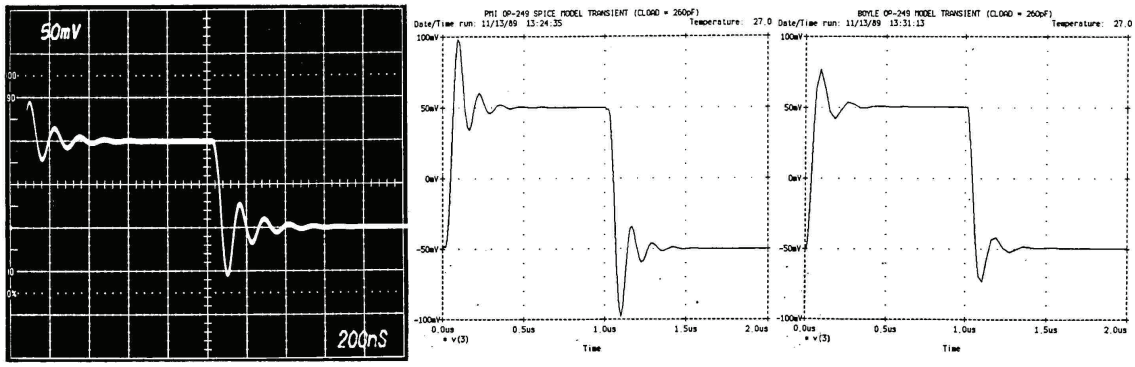


Figure 13.5: *A Pulse Response Comparison of an OP249 Follower (left) and the ADSpice Model (center) and the Boyle Model (right)*

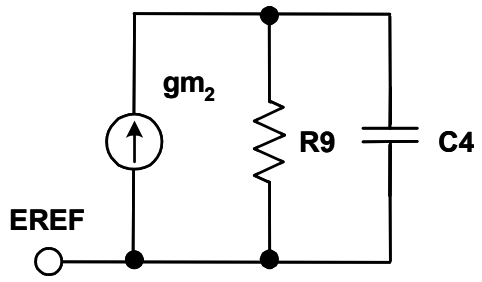
As can be noted, this results in ringing, as seen in the op amp response (left). Note that the ADSpice model accurately predicts the amount of overshoot and frequency of the damped ringing (center). In contrast, the Boyle model (right) predicts about half the overshoot and significantly less ringing.

The Noise Model

An important enhancement to the ADSpice model is the ability to realistically model noise performance of an op amp. The capability to model a circuit's noise in Spice can be appreciated by anyone who has tried to analyze noise by hand. A complete analysis is an involved and tedious task that involves adding all the individual noise contributions from all active devices and all resistors, and referring them to the input.

To aid this task, the ADSpice model was enhanced to include noise generators that accurately mimic the broadband and 1/f noise of an actual op amp. Conceptually, this involves first making an existing model noiseless, and then adding discrete noise generators, so as to emulate the target device. As noted earlier, all ADI models aren't necessarily designed for this noise-accurate performance. Selected device models are designed for noise, however, when their typical uses include low noise applications.

The first step is an exercise in scaling down the model internal impedances. For example, by reducing the resistances in the pole/zero stages from a base resistance of 1 MΩ to 1 Ω, total noise is reduced dramatically, as figure 13.6 illustrates.



	CASE	
	"Noisy"	"Noiseless"
R9	1 MΩ	1 Ω
gm_2	$1x10^{-6}$	1.0
C4	.159 pF	159 pF
Noise	129 nV/√Hz	129 pV/√Hz

Figure 13.6: *A First Design Step in Achieving Low Noise Operation, is the Reduction of Pole/Zero Cell Impedances to Low Values*

For the "Noisy" column of the table, the noise from the pole stage shown with a large R9 resistor value is 129 nV/$\sqrt{Hz}$. But when this resistor is scaled down by a factor of 10^6, to 1 Ω as in the "Noiseless" column, stage noise is 129 pV/$\sqrt{Hz}$. Note also that transconductance and capacitance values are also scaled by the same factor, maintaining the same gain and pole frequency. To make the model's input stage noiseless, it is operated at a high current and with reduced load resistances, making noise contributions negligible. Extending these techniques to the entire model renders it essentially noiseless.

Once global noise reduction is achieved, independent noise sources are added, one for voltage noise and two for current noise. The basic noise source topology used is like Figure 13.7, and it can be set up to produce both voltage and current noise outputs.

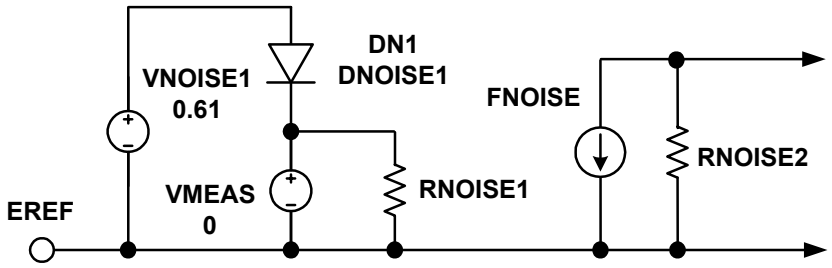


Figure 13.7: *A Basic Spice Noise Generator Is Formed with Diodes, Resistors, and Controlled Sources*

Note that, within Spice, semiconductor models can generate 1/f (flicker) noise. The noise generators use diodes such as DN1 to produce this portion of the noise, modeling the 1/f noise of the op amp. By properly specifying diode model parameters and bias voltage VNOISE1, the 1/f noise is tailored to match the op amp. The noise current from DN1 passes through a zero voltage source. Here VMEAS is being used as a measurement device, combining the 1/f noise from DN1 and the broadband noise from RNOISE1.

RNOISE1 is selected for a value providing an appropriate broadband noise. The combined noise current in VMEAS is monitored by FNOISE, and appears as a voltage across RNOISE2. This voltage is then injected in series with one amplifier input via a controlled voltage source, such as E_N of Figure 13.2. Either FNOISE or a controlled voltage source coefficient can be used for overall noise voltage scaling.

Current noise generation is similar to the above, except that the RNOISE2 voltage producing resistor isn't used, and two current-controlled sources drive the amplifier inputs. With all noise generators symmetrical about ground, dc errors aren't introduced.

Current Feedback Amplifier Models

As noted previously, a new model topology was developed for current feedback amplifiers, to accommodate their unique input stage structure. The model uses a topology as shown in Figure 13.8 for the input and gain stages. The remaining model portions (not shown) contain multiple pole/zero stages and the output stage, and are essentially the same as voltage feedback amplifiers, described above.

The four bipolar transistor input stage resembles actual current feedback amplifiers, with a high impedance noninverting input (+IN) and a low impedance inverting input (−IN). In current feedback amplifiers, the maximum slew rate is very high, because dynamic slew current isn't limited to a differential pair tail current (as in voltage feedback op

amps). In current feedback op amp designs, much larger amounts of error current can flow in the inverting input, as developed by the feedback network. Internally, this current flows in either Q3 or Q4, and charges compensation capacitor C3 via current mirrors.

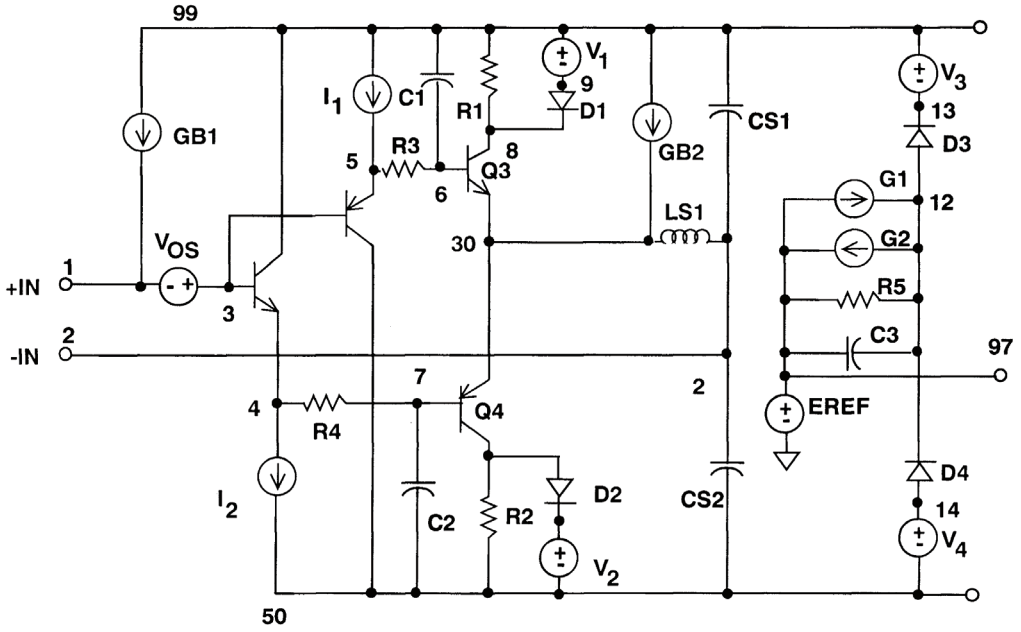


Figure 13.8: *Input and Gain Stages of Current Feedback Op Amp Macromodel*

The current mirrors of the ADSpice model are actually voltage controlled current sources in the gain stage, G1 and G2. They sense voltage drops across input stage resistors R1 and R2, and translating this into a C3 charging current. By making the value of G1 and G2 equal to the R1-R2 reciprocal, the slew currents will be identical. By clamping the R1-R2 voltage drops via D1-V1 and D2-V2, the maximum current is limited, which thus sets the highest slew rate. Open-loop gain or transresistance of the model is set by R5, and the open-loop pole frequency by C3-R5 (as described previously, Figure 13.2). The output from across R5-C3 (node 12) drives the model's succeeding frequency shaping stages, and EREF is again an internal reference voltage.

One of the unique properties of current feedback amplifiers is that bandwidth is a function of the feedback resistor and the internal compensation capacitor, C3. The lower the feedback resistor, the greater the bandwidth, until a practical lower limit is reached, i.e., the value at which the part oscillates. As the model includes a low impedance inverting input, it accurately mimics real part behavior as R_F is altered. Figure 13.9 compares the ADSpice model to the actual device for an AD811 video amplifier. As shown, the model accurately predicts the gain roll off at the much lower frequency for the 1 kΩ feedback resistor as opposed to the 500 Ω resistor.

The current feedback amplifier input and gain stage is an enhancement to the ADSpice model that increases flexibility in modeling different op amp devices, and provides a net increase in design cycle speed.

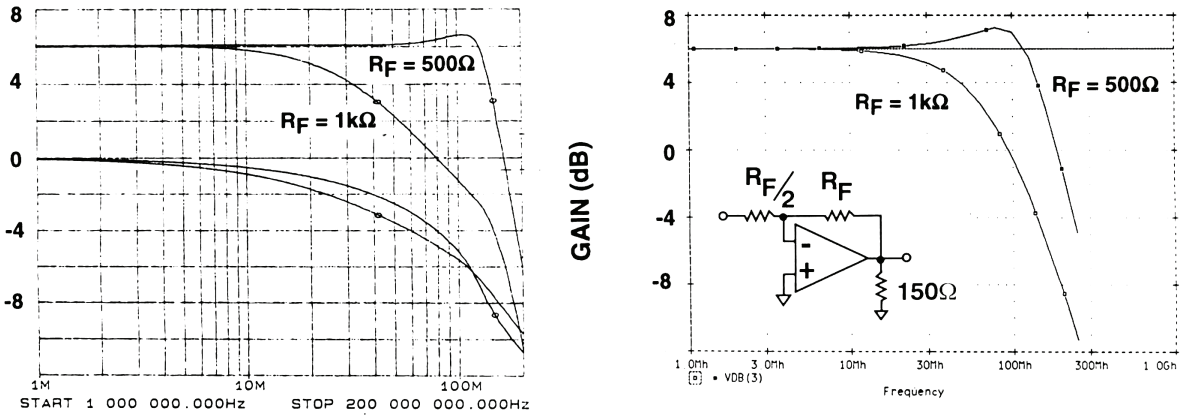


Figure 13.9: *Comparison of a Real AD811 Current Feedback Op Amp (left) with Macromodel (right) as Feedback Resistance Is Varied*

Simulation Must Not Replace Breadboarding!

No matter how accurate your models are, or how much confidence you have with simulations, Spice *analysis alone should never totally replace breadboarding*. As part of a layout and the actual devices existing within a real world PCB assembly, there are second and third order effects which can easily become relevant to performance. By and large, Spice will never ever "know" of such things, unless you explicitly enter them into the Spice netlist. However, this may be either difficult or outright impossible. You may not even be aware of some things before a PCB is built and tested within the final system—spurious signal coupling, the effects of crosstalk, the inevitable parasitic capacitance, inductance, and resistance—on and on goes the list. Let's face it, it is all but impossible to include all of these effects in a simulation. Even if generally aware of their existence, you simply won't have any data whatsoever on the magnitudes involved without actually building a PCB, and operating it under the intended conditions.

Furthermore, remember the fact that no macromodel includes all op amp characteristics. For example, exceeding the input voltage range can cause nonlinear behavior in an op amp, which is not necessarily included in its model. Because of such effects that a simulation might not predict, it is necessary to breadboard the circuit.

Even with models as comprehensive as those of the ADSpice library, external effects can easily cause a circuit to work improperly. As noted, PCB parasitics can significantly alter the frequency performance in high speed designs. Such parasitics are easily overlooked in a Spice simulation, but a breadboard will reveal the problems.

Ultimately, simulation and breadboarding should be used together to maximize the design efficiency. It is necessary to understand the abilities and limitations of simulation and have reasonable expectations as to what spice simulation will tell you.

Simulation Is a Tool to be Used *Wisely*

It must be remembered that while simulation is an extremely powerful tool, it must be used wisely to realize its full benefits. This includes knowing models well, understanding PCB and other parasitic effects, and anticipating the results. For example, consider a simple differential amplifier comprised of an op amp and four equal resistors, to be analyzed for common mode rejection ratio (CMRR) performance. At low frequencies, CMRR will be dominated by resistor mismatch, while at higher frequencies it is dominated by op amp CMRR performance. However, a Spice simulation will only show this if the external resistors are realistically mismatched, and the op amp model used also properly treats not only dc CMRR, but also CMRR reduction at higher frequencies. If these critically important points are overlooked in the analysis, then an optimistic result will shows excellent CMRR performance over the entire circuit bandwidth. Unfortunately, this is simply wrong. Alternatively, substituting into the netlist resistors mismatched by their specified tolerances as well as an ADSpice model (which *does* have CMRR frequency effects modeled) the end results will be quite different. CMRR performance at low frequencies will be limited by resistor mismatch errors, and it will degrade at higher frequencies, as would a real op amp device with CMRR versus frequency effects.

Know the Models

Using various dc and ac tests, any op amp macromodel can be checked for accuracy and functional completeness. Specialized test simulations can also be devised for other op amp parameters important for a particular analysis. All this is critically important, as knowing a model's capabilities ahead of time can help prevent many headaches later.

Understand PCB Parasitics

Even if the model passes all preliminary tests, caution still should be exercised. As noted, PCB parasitics can have significant impact on a circuit's performance. This is especially true for high speed circuits. A few picofarads of capacitance on the input node can make the difference between a stable circuit and one that oscillates. Thus, these effects need to be carefully considered when simulating the circuit to achieve meaningful results.

To illustrate the impact of PCB parasitics, the simple voltage follower circuit of Figure 13.10 (left) was built twice. The first time this was on a carefully laid out PCB, and the second time on a component, plug-in type of prototype board. An AD847 op amp is used because of its 50 MHz bandwidth, which makes the parasitic effects much more critical (smaller C values will have a greater effect on results).

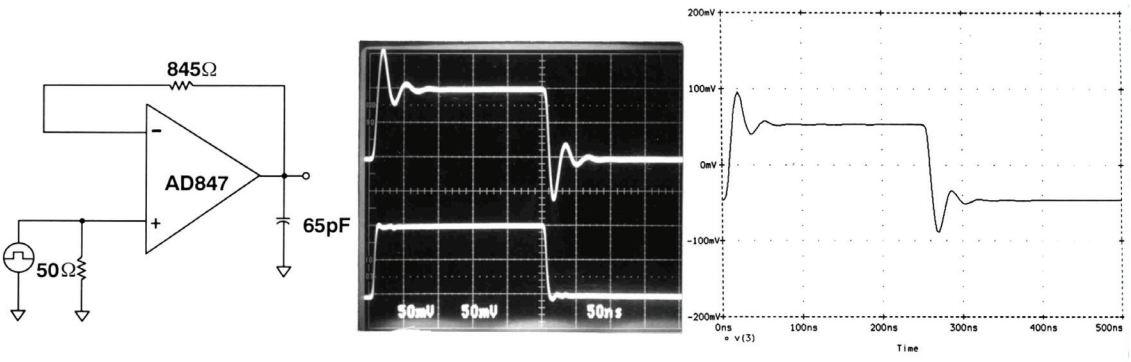


Figure 13.10: *Parasitic Effects in the PCB Layout, Results of Lab Testing (center) and Simulation (right)*

As the results above indicate, this circuit executed on a properly laid out PCB has a clean response with minor overshoot and ringing (center picture). The Spice model results also closely agree with the real part, showing a corresponding simulation (right picture).

On the other hand, the same circuit built on the plug-in prototype board shows distinctly different results. In general it shows much worse performance, due to the relatively high nodal capacitances around the op amp inputs, which degrade the square wave response to severe ringing, much less than full capability of the part.

This is shown in Figure 13.11 in the center and right pictures, respectively. The voltage follower circuit on the left shows the additional capacitances as inherent to the prototype board. With this test circuit and corresponding analysis, there was (initially) no agreement between the poor lab test, and the parallel Spice test. However, when the relevant PCB parasitic capacitances are included in the Spice file, then the simulation results do agree with the real circuit, as noted in the right picture.

This example illustrates several key points. One, PCB parasitics can easily make a high speed circuit behave much differently from a simplistic Spice analysis. Secondly, when the Spice netlist is adjusted to more reasonably reflect the parasitic elements of a PCB, then the simulation results do compare with the actual lab test. Finally, a point that should be obvious, a clean PCB layout with minimal parasitics is critically important to high speed designs. To put this in a broader perspective, op amps of today are capable of operating to 1 GHz or more!

Another interesting point is that the simulation can be used as a rough measure of the PCB layout design. If the simulation, without any parasitics, agrees with the PCB, then there is a reasonable assurance that PCB is well laid out.

Parasitic PCB elements are not the only area that may cause differences between the simulation and the breadboard. A circuit may exhibit nonlinear behavior during power-on that will cause a device to lock up. Or, a device may oscillate due to insufficient power

supply decoupling or lead inductance. Spice circuits need *no* bypassing, *but real world ones always do*! It is, practically speaking, impossible to anticipate all normal or abnormal operating conditions to which an amplifier might be subjected.

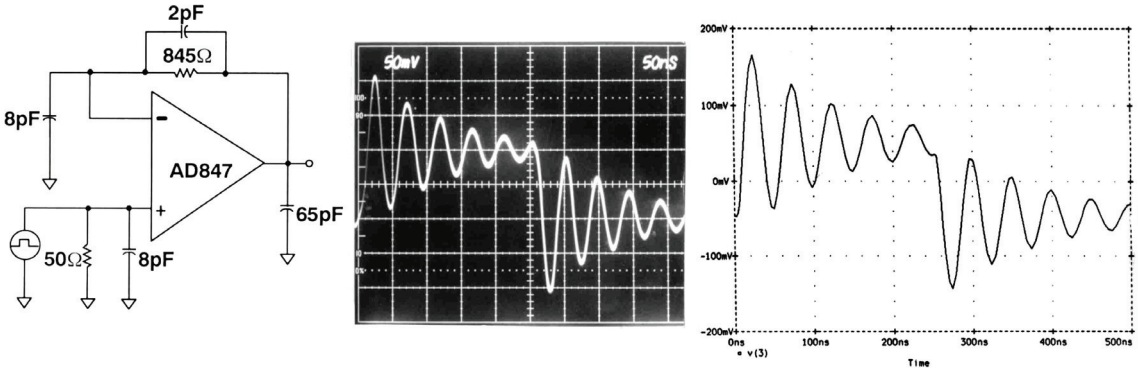


Figure 13.11: *Lab Testing Results (center) and Simulation (right) Show Convergence—with a Poorly Damped Response*

Thus, it is always important that circuits be breadboarded and thoroughly checked in the lab. Careful forethought in these stages of design helps minimize any unknown problems from showing up when the final PCBs are manufactured.

Simulation Speeds the Design Cycle

Simulation is very effective in the initial design phase, to try out different ideas and circuit configurations. When a circuit topology has been decided upon and tested in Spice, then a breadboard can be built. If the simulation was done carefully, the breadboard has good likelihood of working correctly without significant modifications.

When the simulation and the actual results correlate, then the circuit can be easily altered in Spice to perform many different types of analysis. For example, it is much easier to try to optimize the circuit while working within in Spice, as opposed to repeatedly modifying a breadboard. Quick substitutions of the op amps and components can be made in Spice and the results immediately viewed.

Worst-case and sensitivity analyses are also done in Spice much easier than on paper, and with multiple Spice runs, the sensitivity to a certain parameter can be determined. Consider for example an analysis of a multistage active filter, for all possible combinations of component values. This is a nightmare if not impossible either by hand or in the lab, but valid results for response extremes can be obtained relatively easily via a Spice Monte Carlo option, providing greater design confidence.

While simulation cannot reasonably be allowed to replace breadboarding, the two can and should be used together, to increase the efficiency of a design cycle.

Spice Support

A variety of industry vendors offer Spice analysis packages for various computer platforms, including the PC. The first of these and among the most popular is PSpice®, a commercial program which now includes allied packages for both schematic capture and PCB layout. In addition, many vendors also offer low or no cost limited capability student versions of their Spice programs.

Model Support

The ADSpice model library is available in several different forms. Included within it are models of several IC device types, in addition to the op amps discussed above. These are for in-amps, analog multipliers, voltage references, analog switches, analog multiplexers, matched transistors, and buffers. Individual op amp models are available as listings on many data sheets. Electronic ASCII text files of the model library are found from either the ADI website (see References), the Analog Devices Literature Center via 1-800-ANALOGD (1-800-262-5643), or on the ADI support CD.

IBIS Models

IBIS (I/O Buffer Information Specification) models are used with various IBIS based simulators. IBIS models are used for transmission line simulation of digital systems. These models accurately simulate I/O buffers, termination, and circuit board traces. It is a behavioral model that relies on tabulated current versus voltage characteristics.

The IBIS specification is a fast and accurate behavioral method of modeling input/output buffers based on V/I curve data derived from measurements or full circuit simulation. It uses a standardized software-parsable format in the form of an ASCII file to store the behavioral information needed to model device characteristics of integrated circuits. IBIS is compatible with virtually every simulator and EDA tool existent.

Saber Models

Saber models are used to simulate analog, digital, and mixed-signal systems. Saber models are used to simulate and analyze systems, sub-systems, and components before building prototypes. Saber simulation uses a mathematical engine to solve a network of equations represented by interconnected models in a circuit or system.

ADIsimADC

Prior to the release of ADIsimADC™ data converter modeling was often overlooked, omitted or simply done using an ideal data converter. With more and more systems being implemented using mixed signal technology, the importance of system modeling is ever increasing. This coupled with shortened design cycles as well as pressures for first pass success drives the continuing importance of complete system modeling.

When modeling is used, ideal converter models are often used. While this is useful for functional modeling, it fails to give the details of performance required to determine if a particular device selected will actually meet the desired goals of the system. For this reason ADIsimADC™ was developed. For the first time, this model provides a means for customers to validate performance of the converter in their system, using their data in their conditions to determine the applicability of a selected device. While this version of the model doesn't model every characteristic of an ADC, it goes a very long way towards achieving the goal of allowing the customer the ability to model real data converters in their system simulations.

Behavioral vs. Bit Exact

The ADIsimADC modeling software is not a bit exact model. A bit exact model is a model that given a known stimulus provides a known and predictable output. These types of models are often found in digital systems. In dealing with analog functions, there is never a known response for a given input because of noise, distortion, and other nonlinearities. While some portion of the response may be predictable, much of the remainder is subject to distortion, noise, and even part-to-part variation. Additionally, to provide a bit exact model would require providing circuit simulation files such as Spice models that process transient response and requires complex initial conditions be set. However, these models are large, complex, very slow, and in the end provide very limited accuracy. A reduced or equivalent Spice model would not be able to provide adequate modeling of fine details of static and dynamic performance.

A behavioral model eliminates the complexity of a large Spice file, while at the same time allows modeling of fine performance detail not possible to attain with a circuit file. As provided, ADIsimADC can be included in many other 3rd party simulation tools including Matlab, C++, as well as stand alone converter evaluation using ADC Analyzer™.

Model vs. Hardware

Modeling a system, or even just an ADC, should never be a substitute for building and characterizing a real system. As any RF engineer will tell you, it is one thing to model a circuit, but it is completely another to actually build it up and test it. As with any analog or mixed signal device, proper layout and configuration is required to achieve the performance shown in simulation. Therefore it is important that all layout rules and

guidelines be followed as shown in the product data sheets. It is also important to provide adequate power supply bypass capacitors. Because mixed signal devices include some amount of digital circuitry, digital switching noise is often a problem and failure to provide capacitors to moderate these switching currents can significantly reduce performance of even the best devices. Often, other support devices are required around the converter. This includes additional capacitors, inductors, and resistors. The only way to know what is required is to consult the product data sheet and even the evaluation board schematic often supplied in the product data sheet. ADIsimADC is targeted at providing realistic performance of real devices based on recommend layouts as shown in the data sheet.

What Is Important to Model?

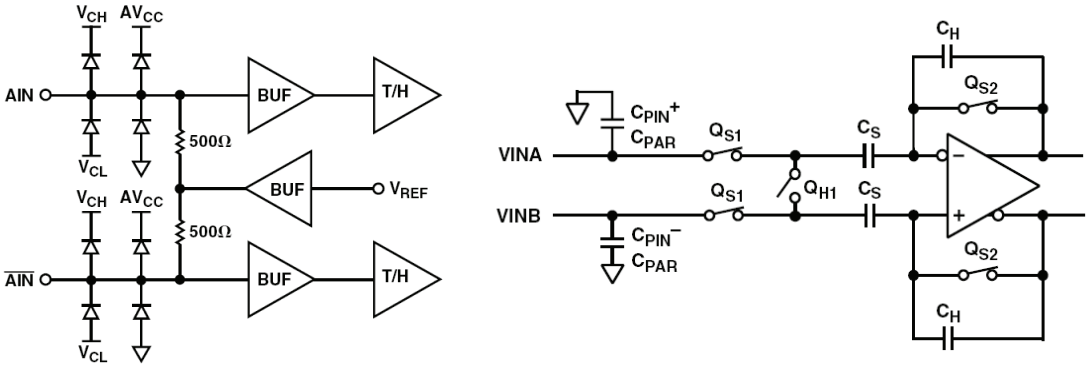
What is important to model depends on what kind of analysis you are trying to perform. For example, control loops would need accurate transfer function and delay information while radio systems may require an accurate representation of noise and distortion. ADIsimADC models many of the critical specification of data converters including: offset, gain, sample rate, bandwidth, jitter, latency, and both ac and dc linearity.

Gain, Offset and DC Linearity

The full-scale range of the converter is defined by the design of the converter. In some cases, the full-scale range of the converter is fixed while others are selectable or variable. Gain error of a converter is the deviation from the nominal value which is often called the input span. Since an ADC is a voltage input device, this value is specified in volts at dc or low frequency. As the input frequency is increased, attenuation in the amplitude response effectively increases the apparent full-scale range of the converter causing a roll off in the response of the converter. The frequency where the response has diminished to 3 dB is called the full power 3 dB bandwidth of the converter.

Offset represents the digital output if the input(s) are shorted to the reference. Many devices have internal connections that bias the input pins to the internal reference to set up the input common mode voltage. On such devices, it is not necessary to make this connection externally, and the input may be floated in the case of a single ended input, or shorted together in the case of a differential input. Devices that do not have connections internally to the common-mode voltage must be externally connected. As with input span, the common-mode voltage may either be fixed or may be adjustable. The data sheet should be consulted to determine how your device is configured.

ADIsimADC does not allow either the input span or the common-mode to be changed. Different models are provided for devices with different input spans. Common-mode is fixed for all devices and may not be changed. If modeling in a system that uses a different common-mode range, the difference may be subtracted by an external offset if necessary.



***Note**: Different input data structures showing those that are both connected to the internal common-mode voltage (on the left) and those that are not (on the right).*

***Figure 13.12:** Typical ADC Input Structures*

DC linearity is determined by the data converter transfer function. This is determined by a number of factors including the static transfer function (or dc linearity of the device). The dc linearity for an ADC is determined by the quantization method of the converter. There are many types of converters and a good summary is found in references. Each type of converter will have a unique transfer function, and will produce different results both at dc and at high frequency.

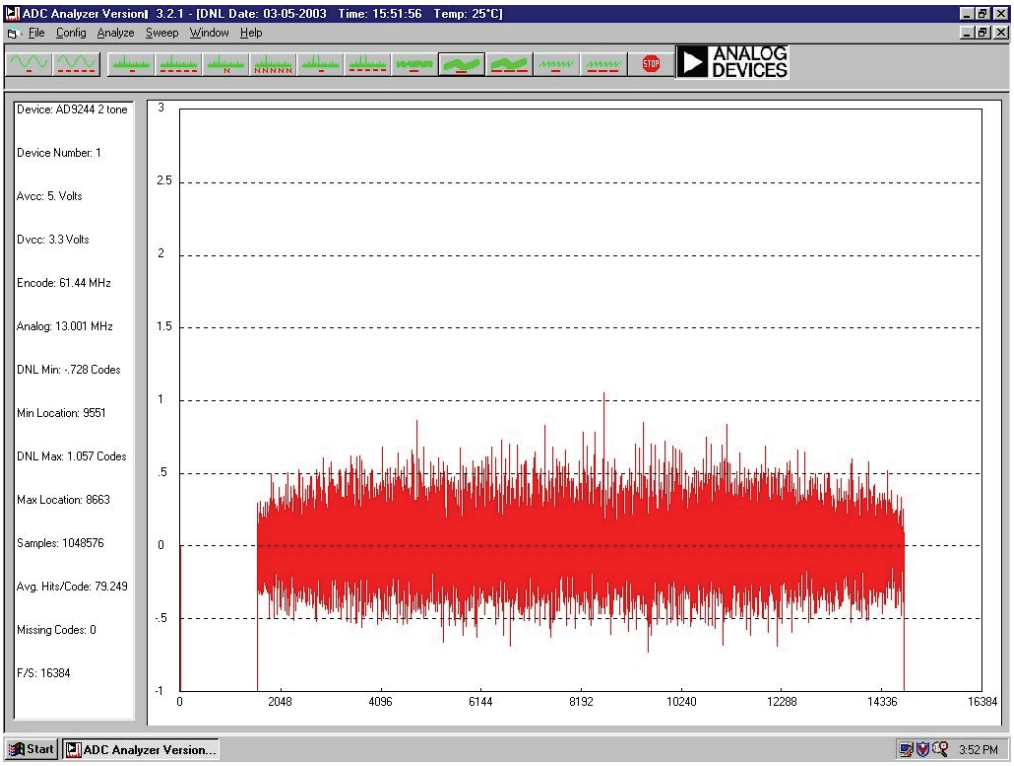


***Figure 13.13:** Typical Converter DNL, an Important Contributor to the Converter Transfer Function*

Sample Rate and Bandwidth

The performance of most converters changes with both the sample rate and analog input frequency change. From a sample rate point of few, most good converters provide consistent performance from the lowest sample rate to the highest specified sample rate. At very low sample rates, some converters will fail to properly operate because charges stored on on-chip capacitors will discharge or droop, causing incorrect data conversion. Therefore the data sheet should be consulted to determine what the lowest usable sample rate will be. Depending on the class of converter, this may either be 0 Hz or some other frequency. At the highest of the sample rates, one of two problems occurs. First, the device may simply not be able to pass on-chip digital signals from one stage to the next. This is the result of running out of either setup or hold time on-chip. The other problem is failure of a critical analog signal to stabilize during the time allocated. One such example is acquisition time for a hold capacitor. As before, the data sheet should be consulted to determine what the highest usable sample rate should be. ADIsimADC uses the specified sample rate to determine how the converter should perform. However outside the specified range of the device, the model will produce all zeros results.

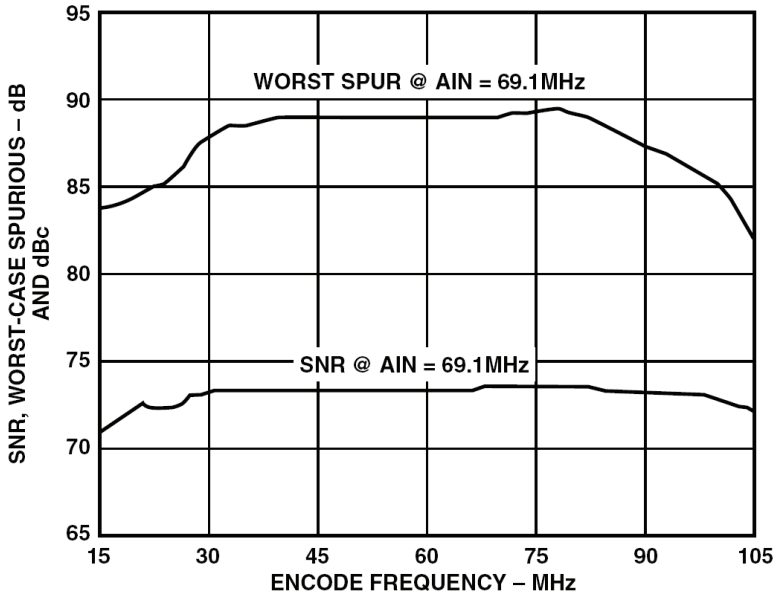


Figure 13.14: *Converter Performance vs. Sample Rate*

As the analog input frequency increases, the natural tendency of a converter like any other analog device will roll off in its frequency response. This is modeled in ADIsimADC and results in a reduced response within the model. This is noticed as the signal level of an FFT will show decreased signal level. To counter this loss, the input signal level must be increase above the span specified as the default for the model resulting in an input that appears to be above the full-scale range of the converter. In reality, this signal is attenuated by package parasitics, device parasitics as well as the filter formed by the hold capacitor of the internal sample and hold amplifier (SHA).

Distortion, Both Dynamic and Static

Because ADCs have a finite bandwidth, they also exhibit a fundamental slew rate limitation. This slew rate limitation is one source of distortion within an ADC. If the input frequency of the data converter is swept from dc to some upper frequency, the SFDR performance of the converter will consistently decline as the input frequency increases. This is caused by the dynamic limitations of the converter as outlined here. As the input frequency continues to increase, so do the harmonics.

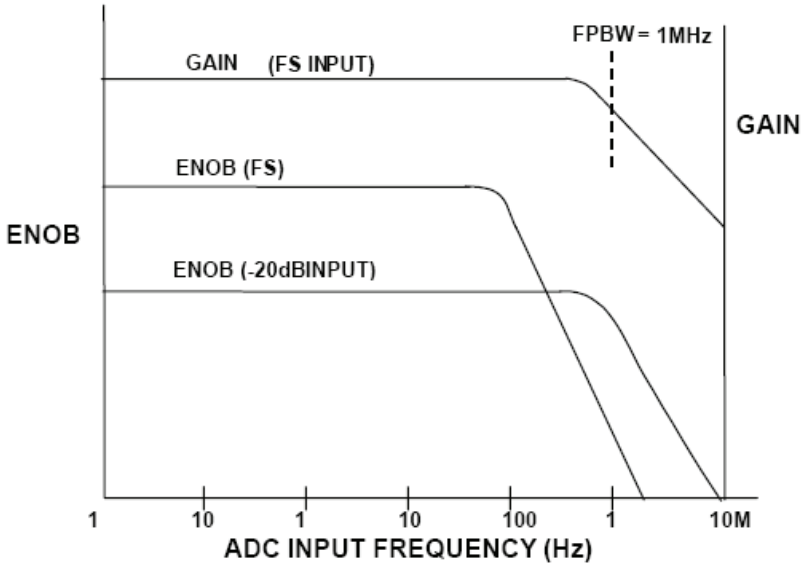


Figure 13.15: *Converter Analog Bandwidth*

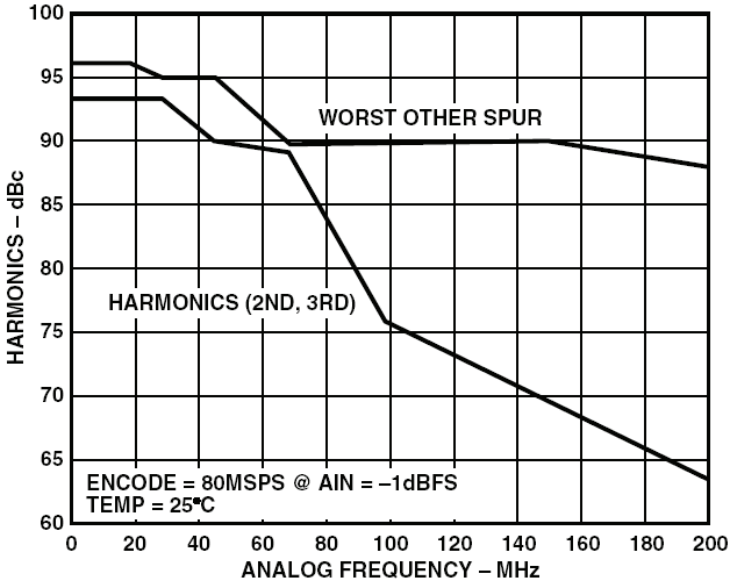


Figure 13.16: *Example Converter Performance vs. Analog Input Frequency*

Since these limitations are due at least in part to slew rate issues, the amplitude of these signals can be reduced (while keeping the analog frequency constant), resulting in a reduced slew rate and improved harmonics relative to the full-scale of the converter. While these spurious components do not always follow the classic trend of m-order products, this trend may often be casually observed. As the signal levels are reduced, slew rate effects diminish, but errors due to static distortion rapidly replace them as the dominant contributor to distortion.

Static distortion is the distortion due to the transfer function of the converter. This distortion often will have some very unpredictable results. This may include spurious components that change rapidly as a function of input level and can exhibit both positive and negative slope characteristics. Largely these spurs are due to the characteristics of the design architecture of the converter. That said, different converters will have very different static transfer functions, resulting in very different distortion responses. Additionally, since these are analog components, each part within the same design will also exhibit different responses to an input signal. The results are that some part to part variation will always exist.

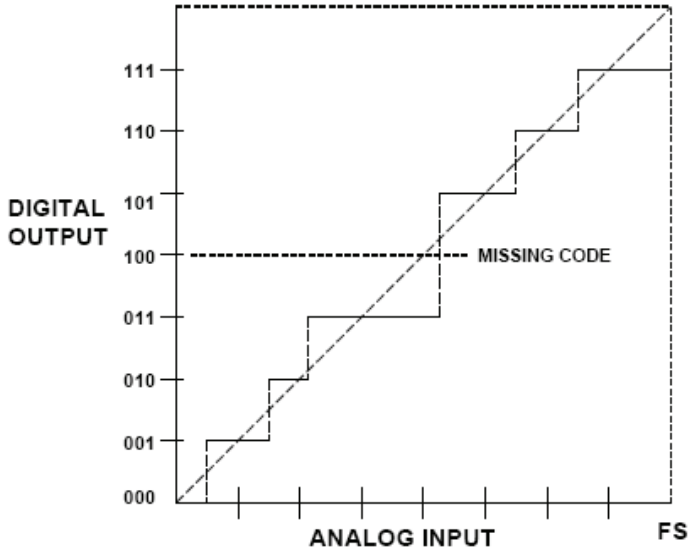


Figure 13.17: *Data Converter Transfer Function*

ADIsimADC attempts to model the nominal performance of the data converter. While it does an effective job at this, some part-to-part variation is normal. As stated earlier, the data sheet should be consulted to determine what performance variations are expected.

Jitter

In addition to the analog input slew rate limitations of the converter, one of the most difficult aspects of sampling high frequency analog signals is that of jitter. Jitter is the sample-to-sample variations in the sampling process at the front end of every data converter. At low analog input frequencies, this poses no problems at all. However at high analog frequencies, errors made in the analog sampling process due to jitter can cause significant errors. While the sampling time errors may be on the order of femtoseconds, the resulting limitations in SNR can be significant.

Although there are multiple contributors to overall noise, at high frequencies, jitter is clearly the dominant factor, especially for high resolution converters as shown in the equation below.

$$SNR = -20\log\left[\sqrt{\left(2\pi f_{ana\log} t_{jitter_{rms}}\right)^2 + \left(\frac{2}{3}\right)\left(\frac{1+\varepsilon}{2^N}\right)^2 + \left(\frac{2V_{Noise_{rms}}\sqrt{2}}{2^N}\right)^2}\right] \qquad \text{Eq. 13-1}$$

There are two sources for jitter. The first source is the native or internal jitter to the device. This is just the jitter of the ADC under test. Since most contemporary converter designers seek to minimize the internal jitter by various techniques, this number will usually be the smaller of the two (but not negligible). The second and major source of jitter is the external clock jitter. When the model is computing the noise due to jitter these two jitter sources are combined root summed squared (rss) before the noise is computed.

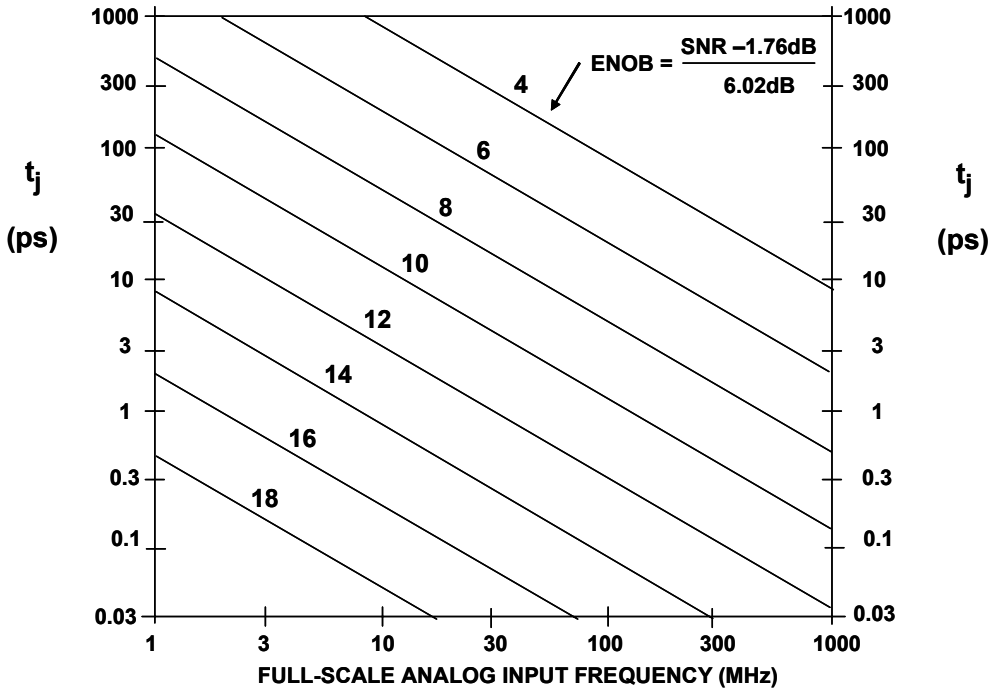


Figure 13.18: *SNR vs. Input Frequency vs. Jitter*

ADIsimADC estimates the instantaneous slew rate of the input signal and multiplies this by a Gaussian modeled jitter with a sigma equal to the combined rss values of the internal and external jitter. The result is a jitter contribution to the noise that accurately models the effects of jitter as a function of both the analog input frequency and amplitude level. The default for external jitter is that of the setup used during characterization of the device. This, however, can be set by the user to any value.

Latency

Many types of converters include a pipeline delay between the sample time and when the data appears on the digital outputs. SAR and FLASH converters generally provide output data immediately after the sample period. However multistage converters such as pipelined and Sigma-Delta (also known as Delta-Sigma) converters do not offer an output for tens and hundreds of clock cycles later. While many times this is not relevant, it is important for control and other systems where latency is important. ADIsimADC models latency in terms of whole values of the clock period. This has the effect of producing garbage at the beginning of a conversion period while the pipeline fills until it produces valid data after the end of the conversion period while the pipeline flushes. Care must be taken when using the model to properly account for the pipeline delay of the model either by “flushing” the buffer or by other means.

ADIsimPLL™

Traditionally, PLL Synthesizer design relied on books and published application notes to assist in the design of the PLL loop filter. It was necessary to build prototype circuits to determine key performance parameters such as lock time, phase noise, and reference spurious levels. Optimization was limited to "tweaking" component values on the bench and repeating lengthy measurements.

Using ADIsimPLL both streamlines and improves upon the traditional design process. Starting with the "new PLL wizard" a designer constructs a PLL by specifying the frequency requirements of the PLL, selecting an integer-N or fractional-N implementation and then choosing from a library of PLL chips, library of custom VCOs, and a loop filter from a range of topologies. The wizard designs a loop filter and sets the simulation program to display key parameters including phase noise, reference spurs, lock time, lock detect performance, and others.

ADIsimPLL operates with spreadsheet-like simplicity and interactivity. The full range of design parameters such as loop bandwidth, phase margin, VCO sensitivity, and component values can be altered with real-time update of the simulation results. This allows the user to easily tailor and optimize the design for their specific requirements. Varying the bandwidth, for example, enables the user to observe the trade-off between lock time and phase noise in real-time and with bench-measurement accuracy.

ADIsimPLL includes accurate models for phase noise, enabling reliable prediction of the synthesizer closed-loop phase noise. Users report excellent correlation between simulation and measurement.

ADIsimPLL also accurately simulates locking behavior in the PLL, including the most significant nonlinear effects. Unlike simple linear simulators based on Laplace transform solutions, ADIsimPLL includes the effects of phase detector cycle slipping, charge pump saturation, curvature in the VCO tuning law and the sampling nature of the phase-frequency detector. As well as providing accurate simulation of frequency transients, giving detailed lock-time predictions for frequency and phase lock, ADIsimPLL also simulates the lock detect circuit. For the first time designers can easily predict how the lock detect circuit will perform without having to resort to measurements.

The simulation engine in ADIsimPLL is fast, with all results typically updating "instantaneously," even transient simulations. As well as providing an interactive environment that enables the design to be easily optimized, it also encourages the designer to explore the wide range of design options and parameters available. Contrary to the traditional methods where to design, build, and then measure parameters takes days, ADIsimPLL enables the user to change the PLL circuit design and observe instantly the performance changes. ADIsimPLL allows the designer to work at a higher level and directly modify derived parameters such as the loop bandwidth; phase margin, pole locations, and the effects of the changes on performance are shown instantly (and without burning fingers with a soldering iron!).

If necessary the designer can work directly at the component level and observe the effects of varying individual component values.

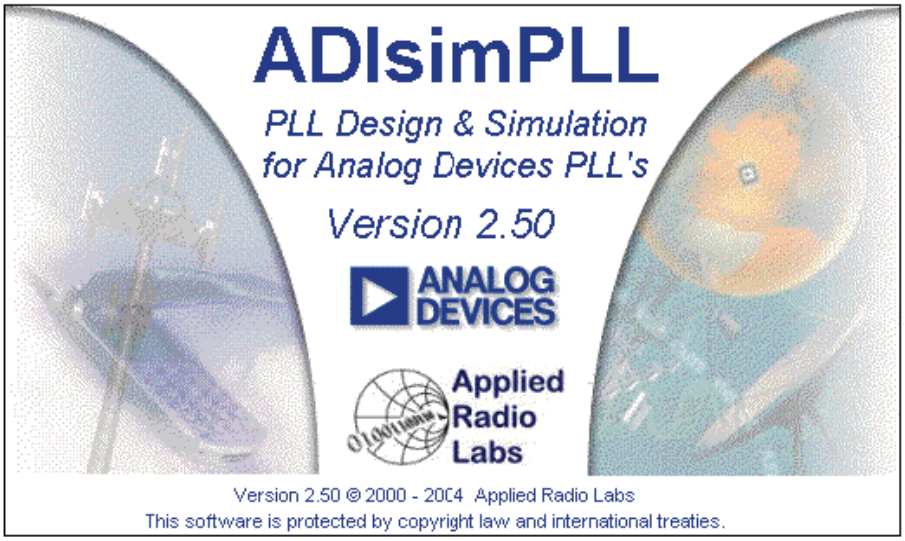


Figure 13.19: *ADIsimPLL Front page*

ADIsimPLL Version 2.5 includes many enhancements:

- the new PLL wizard now includes a short-form selector guide for choosing the PLL chip, displaying short-form data for all chips, with links to the product pages on the Analog Devices website.
- Similar short-form selector guides are available for choosing the VCO device, and these contain links to detailed device data on vendor's websites. The data in the selector guides can be sorted by any parameter.
- The chip-programming assistant enables rapid calculation of programming register values to set the chip any specified frequency. This is also great for checking channels that cannot be reached due to prescaler restrictions
- The range of loop filters has been expanded to include a 4-pole passive filter and a noninverting active filter. As with all loop filter designs in ADIsimPLL, these models accurately include the thermal noise from resistors, the op amp voltage and current noise, as well as predicting reference spurs resulting from the op amp bias current.
- Phase jitter results can now be displayed in degrees, seconds, or Error Vector Magnitude (EVM).
- It is now possible to simulate the power-up frequency transient.
- Support has been included for the new Analog Devices PLL chips with integrated VCO's.

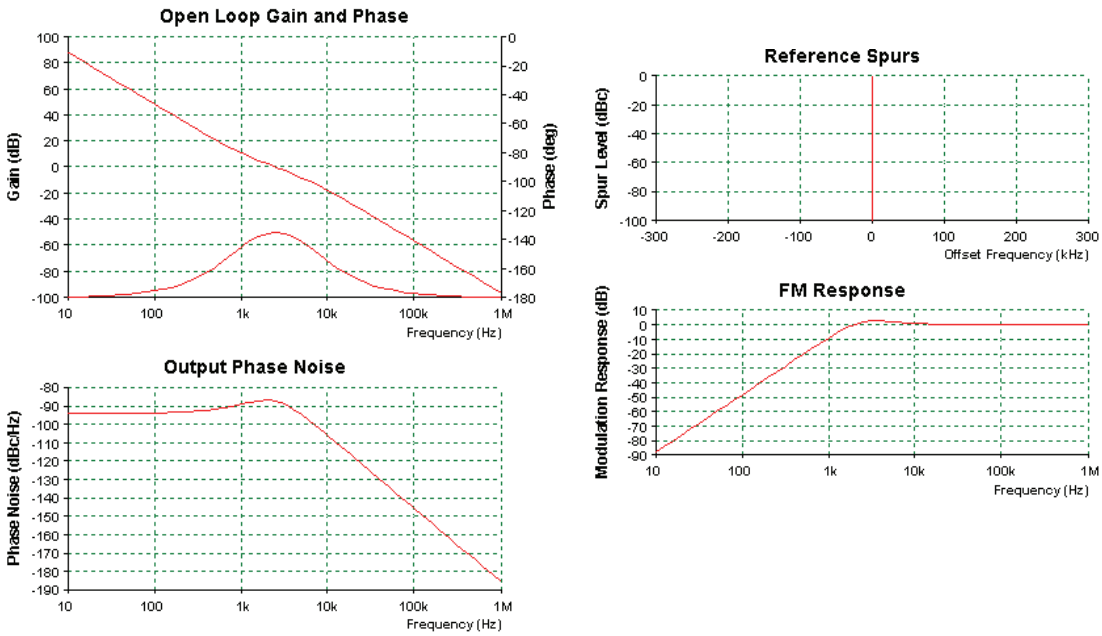


Figure 13.20: *ADIsimPLL Frequency Domain Results*

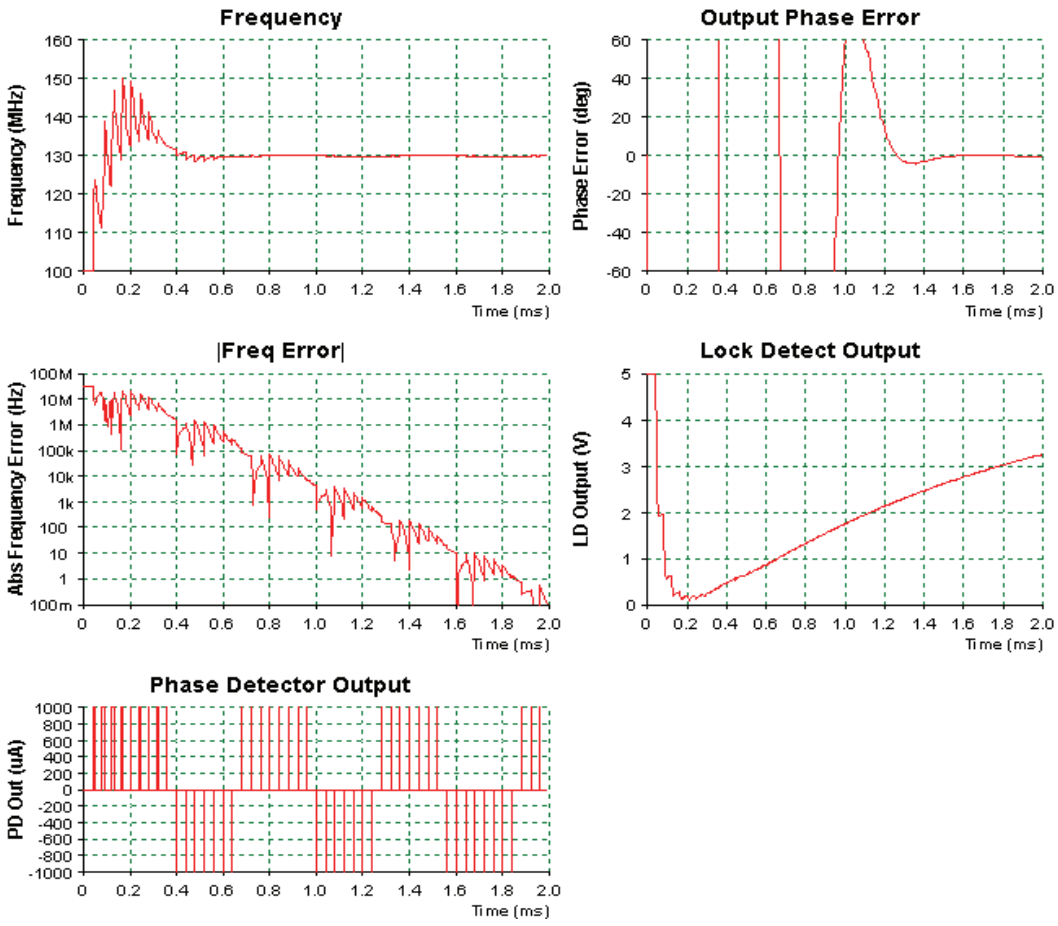


Figure 13.21: *ADIsimPLL Time Domain Results*

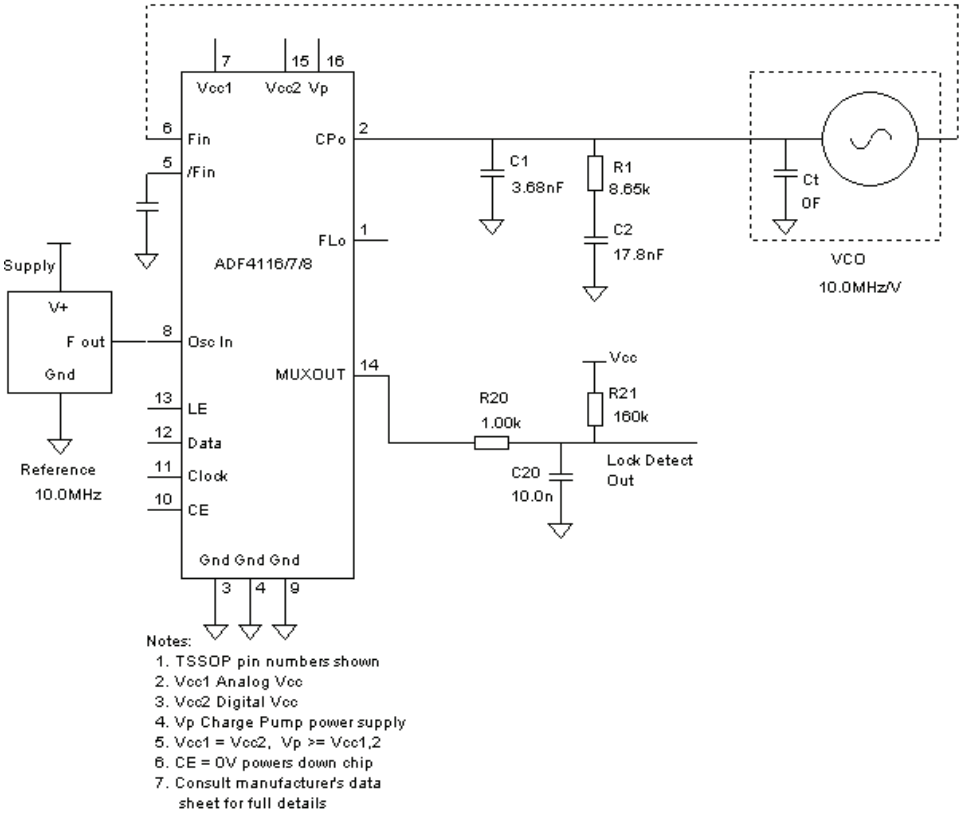


Figure 13.22: *ADIsimPLL Schematic Output*

Transient Analysis of PLL
Frequency change from 100MHz to 130MHz
Simulation run for 2.00ms

Frequency Locking
Time to lock to 1.00kHz is 1.21ms
Time to lock to 10.0 Hz is 1.60ms

Phase Locking (VCO Output Phase)
Time to lock to 10.0 deg is 1.21ms
Time to lock to 1.00 deg is 1.48ms

Lock Detect Threshold
Time to lock detect exceeds 2.50 V is 1.42ms

---- End of Time Domain Results ----

Figure 13.23: *ADIsimPLL Time Domain Results*

Design1 analysed at 07/23/02 07:02:53

PLL Chip is ADF4116
VCO is custom
Reference is custom

Frequency Domain Analysis of PLL
Analysis at PLL output frequency of 114MHz

Phase Noise Table

Freq	Total	VCO	Ref	Chip	Filter
100	-93.73	--	--	-93.81	-111.5
1.00k	-88.97	--	--	-91.73	-92.25
10.0k	-106.0	--	--	-110.5	-107.9
100k	-145.7	--	--	-150.3	-147.6
1.00M	-185.7	--	--	-190.3	-187.6

Phase jitter using brick wall filter
from 10.0kHz to 100kHz
Phase Jitter **0.02 degrees rms**

Carrier Recovery phase jitter
Carrier recovery bandwidth 6.40kHz damping factor 0.7071
Symbol Filter cutoff 32.0kHz Butterworth with 3 poles
Phase Jitter **0.09 degrees rms**

Residual FM
from 300 Hz to 5.00kHz is **8.52 Hz**

FM SNR
sinusoidal modulation with 10.0kHz peak deviation
Signal to Noise Ratio = **58.4 dB**

ACP - Channel 1
Channel 1 is centred 25.0kHz from carrier with bandwidth 15.0kHz
Power in channel = **-78.6dBc**

---- End of Frequency Domain Results ----

Figure 13.24: *ADIsimPLL Frequency Domain Results*

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15. W. Hobbs, A. Muranyi,, R. Rosenbaum, D. Telian. "IBIS:I/O Buffer Information Specification Overview," Intel Corp.,

16. vhdl.org:(198.31.14.3) has been a central location to find various IBIS related information. This includes: Models, Golden Parser, BIRD (Buffer Issue Resolution Documents), Summit information, and a participating company roster listing. This is an anonymous ftp site and anyone can log on as *anonymous* and user their E-mail ID as a password. Dial up modem access also is available at (415)335-0110

17. ANSI/EIA-656: This IBIS web site serves as a central location that will continually provide various tools and resources in helping create IBIS models. IBIS related articles, FAQ (Frequently Asked Questions), Hypertext links to information on vhdl.org, Virtual Poster pages with hot links to member companies are some of the items available through this web site.

18. North Carolina State University. The University provides SPICE-to-IBIS translator tools from their site.

SECTION 13.2: ON-LINE TOOLS AND WIZARDS

Analog Devices is developing a large number of design tools designed to run on the worldwide Web. The purpose of these tools is to assist in the design process. Many of the tools are simply dressed up spreadsheets. Many of the processes are simple in a mathematical sense, so the lend themselves well to this approach.

Simple Calculators

For example consider the V rms/dBm/dBu/dBV Calculator. This simple utility converts between any of the several ways of expressing the ac voltage level. The impedance, which is nessasary to the dBm (the "m" standing for milliwatt) measurement, is included in the calculation. An example of the V rms/dBm/dBu/dBV Calculator screen is shown in Figure 13.25.

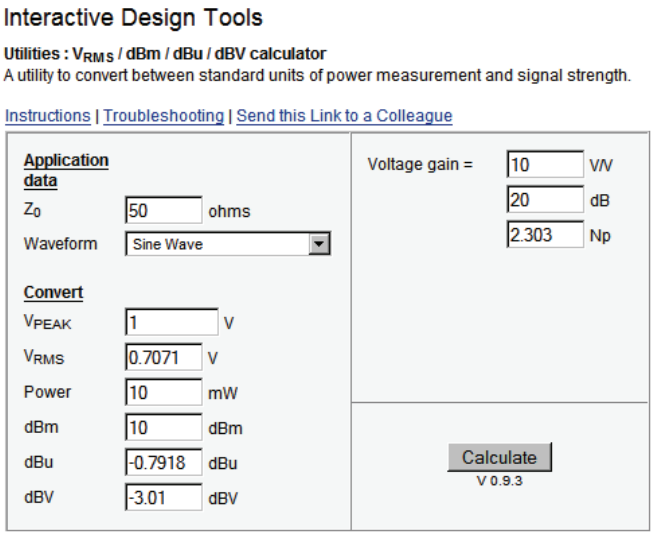


Figure 13.25: *V rms/dBm/dBu/dBV Calculator screen*

The Power Dissipation Calculator computes die power dissipation and temperature for a linearly regulated output from quantities specified under "Parameters." It also computes power dissipated in an external load.

The model is of a linear push-pull output driving an external resistive load. Two common examples would be a digital bipolar output or a Class A amplifier. The voltage across the resistor, V_{OUT}-V_{GND} determines the current, I_L, supplied by the output, which requires the internal driver dissipate I_L * (V_+-V_{OUT}) or I_L * (V_{OUT}-V_-) to supply the current linearly. Which rail supplies the current depends on whether the load current is positive or negative.

Total on-chip power, P_{TOTAL}, is the sum of the power dissipated driving the load, plus the quiescent power, I_Q * (V_+ - V_-). The on-chip rise is equal to $T_A + \theta_{JA}*P_{TOTAL}$. $\theta_{JA} = \theta_{JP}$ (junction-to-package thermal resistance) + θ_{PA} (package-to-ambient thermal resistance).

To use this calculator, simply enter the appropriate quantities in the parameter fields and then click "Calculate" or tab from field to field.

An example screen of the power dissipation calculator is shown in Figure 13.26.

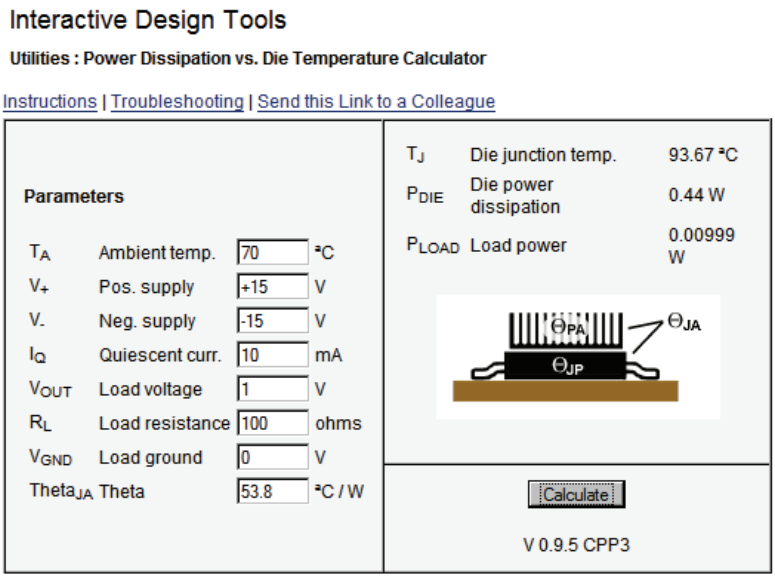


Figure 13.26: *Power Dissipation Calculator Screen*

Another simple example is the SNR/THD/SINAD Calculator. This calculator computes one of SNR, THD, or SINAD from the other two as specified by radio buttons located to the left of the quantity name. SINAD equals the rms sum of THD + SNR. For the computed / entered SINAD, the corresponding rms noise and the equivalent number of bits are shown in an output field at right. Figure 13.28 shows the SNR/THD/SINAD Calculator.

As we mentioned in an earlier section, driving capacitive loads is one of the biggest problems confronting an analog circuit designer. Also, large is a relative term. Loads that would not affect a low speed precision amp may give a high speed amp fits. Usually, driving large capacitive loads is not a matter of choice, most often it's an unwanted parasitic. An example would be the capacitance of a length of coaxial cable. However, situations do arise where it's desirable to decouple a dc voltage at the output of an op amp, for example, when an op amp is used to invert a reference voltage and drive a dynamic load. In this case, you might want to place bypass capacitors directly on the output of an op amp. Either way, a capacitive load affects the op amp's performance.

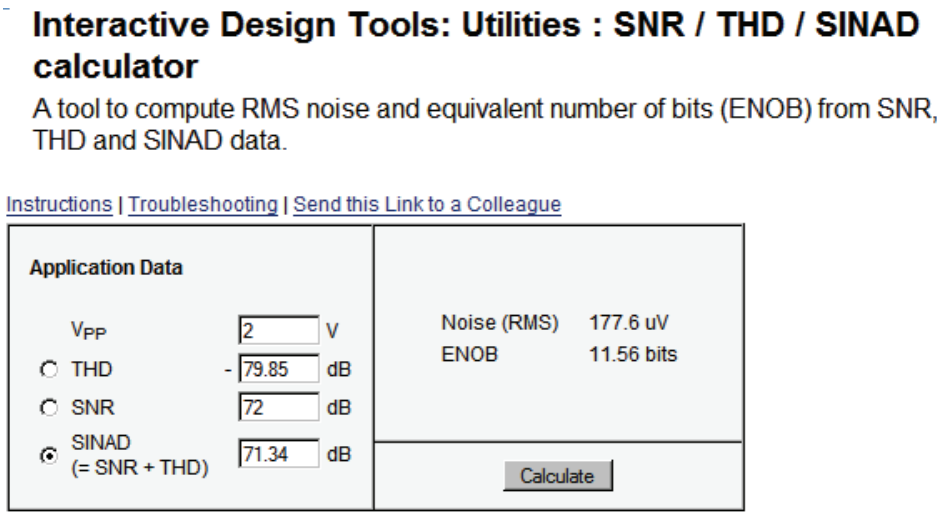


Figure 13.27: *SNR/THD/SINAD Calculator Screen*

In fact, load capacitance can turn your amplifier into an oscillator. Op amps have an inherent output resistance, R_o, which, in conjunction with a capacitive load, forms an additional pole in the amplifier's transfer function. As a Bode plot shows, at each pole the amplitude slope becomes more negative by 20 dB/decade. Also each pole adds −90° of phase shift. We can view instability from either of two perspectives. Looking at amplitude response on the log plot, circuit instability occurs when the sum of open-loop gain and feedback attenuation is greater than unity. Similarly, looking at phase response, an op amp will oscillate at a frequency where loop phase shift exceeds −180°, if this frequency is less than the closed-loop bandwidth.

Phase margin of an op amp circuit can be thought of as the amount of additional phase shift at the closed-loop bandwidth required to make the circuit unstable (i.e., phase shift + phase margin = −180°). As phase margin approaches zero, the loop phase shift approaches −180° and the op amp circuit approaches instability. Typically, values of phase margin much less than 45° can cause problems such as "peaking" in frequency response, and overshoot or "ringing" in step response. In order to maintain conservative phase margin, the pole generated by capacitive loading should be at least a decade above the circuit's closed-loop bandwidth. When it is not, consider the possibility of instability.

A few op amp data sheets specify the open-loop output resistance (R_o), from which you can calculate the frequency of the added pole described above. The circuit will be stable if the frequency of the added pole (f_P) is more than a decade above the circuit's bandwidth.

If the op amp's data sheet doesn't specify capacitive load drive or open-loop output resistance, and has no graph of overshoot versus capacitive load, then to assure stability you must assume that any load capacitance will require some sort of compensation technique. There are many approaches to stabilizing standard op amp circuits to drive capacitive loads. Here are a few:

Noise-gain manipulation: A powerful way to maintain stability in low frequency applications—often overlooked by designers involves increasing the circuit's closed-loop gain (a/k/a "noise gain") without changing signal gain, thus reducing the frequency at which the product of open-loop gain and feedback attenuation goes to unity. Some circuits to achieve this, by connecting R_D between the op amp inputs, are shown below. The "noise gain" of these circuits can be arrived at by the given equation.

Since stability is governed by noise gain rather than by signal gain, the circuits in Figure 13.29 allow increased stability without affecting signal gain. Simply keep the "noise bandwidth" (GBP/A_{NOISE}) at least a decade below the load generated pole to guarantee stability.

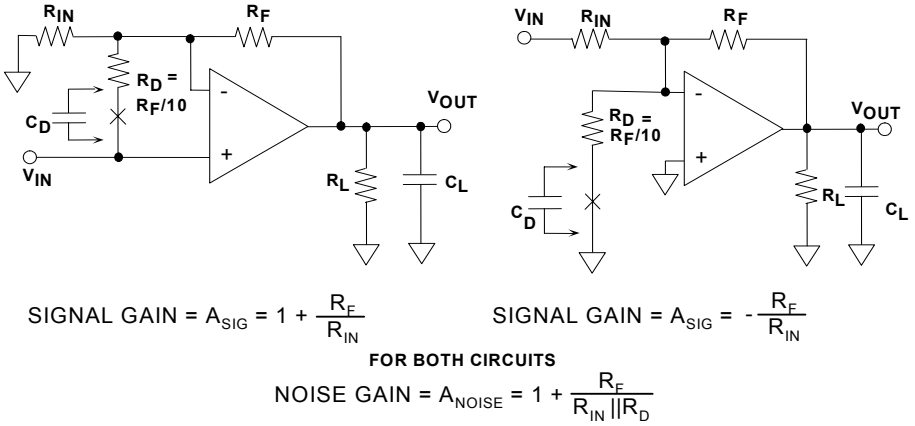


Figure 13.28: *Noise Gain Manipulation*

One disadvantage of this method of stabilization is the additional output noise and offset voltage caused by increased amplification of input-referred voltage noise and input offset voltage. The added dc offset can be eliminated by including C_D in series with R_D, but the added noise is inherent with this technique. The effective noise gain of these circuits with and without C_D are shown in the figure. C_D, when used, should be as large as feasible; its minimum value should be $10*A_{NOISE}/(2*\pi*R_D*GBP)$ to keep the "noise pole" at least a decade below the "noise bandwidth".

Out-of-loop compensation: Another way to stabilize an op amp for capacitive load drive is by adding a resistor, R_X, between the op amp's output terminal and the load capacitance, as shown in Figure 13.29. Though apparently outside the feedback loop, it acts with the load capacitor to introduce a zero into the transfer function of the feedback network, thereby reducing the loop phase shift at high frequencies.

To ensure stability, the value of R_X should be such that the added zero (f_Z) is at least a decade below the closed loop bandwidth of the op amp circuit. With the addition of R_X, circuit performance will not suffer the increased output noise of the first method, but the

output impedance as seen by the load will increase. This can decrease signal gain, due to the resistor divider formed by R_X and R_L. In addition, if there is capacitance (C_L) the voltage divider is frequency dependant. If R_L is known and reasonably constant, the results of gain loss can be offset by increasing the gain of the op amp circuit.

This method is very effective in driving transmission lines. The values of R_L and R_X must equal the characteristic impedance of the cable (often 50 Ω or 75 Ω) in order to avoid standing waves. So R_X is pre-determined, and all that remains is to double the gain of the amplifier in order to offset the signal loss from the resistor divider. Problem solved.

It is also important to note that C_L must be of a known (and constant) value in order for this technique to be applicable. In many applications, the amplifier is driving a load "outside the box," and C_L can vary significantly from one load to the next. It is best to use the abo*ve circuit only when C_L is part of a closed system.*

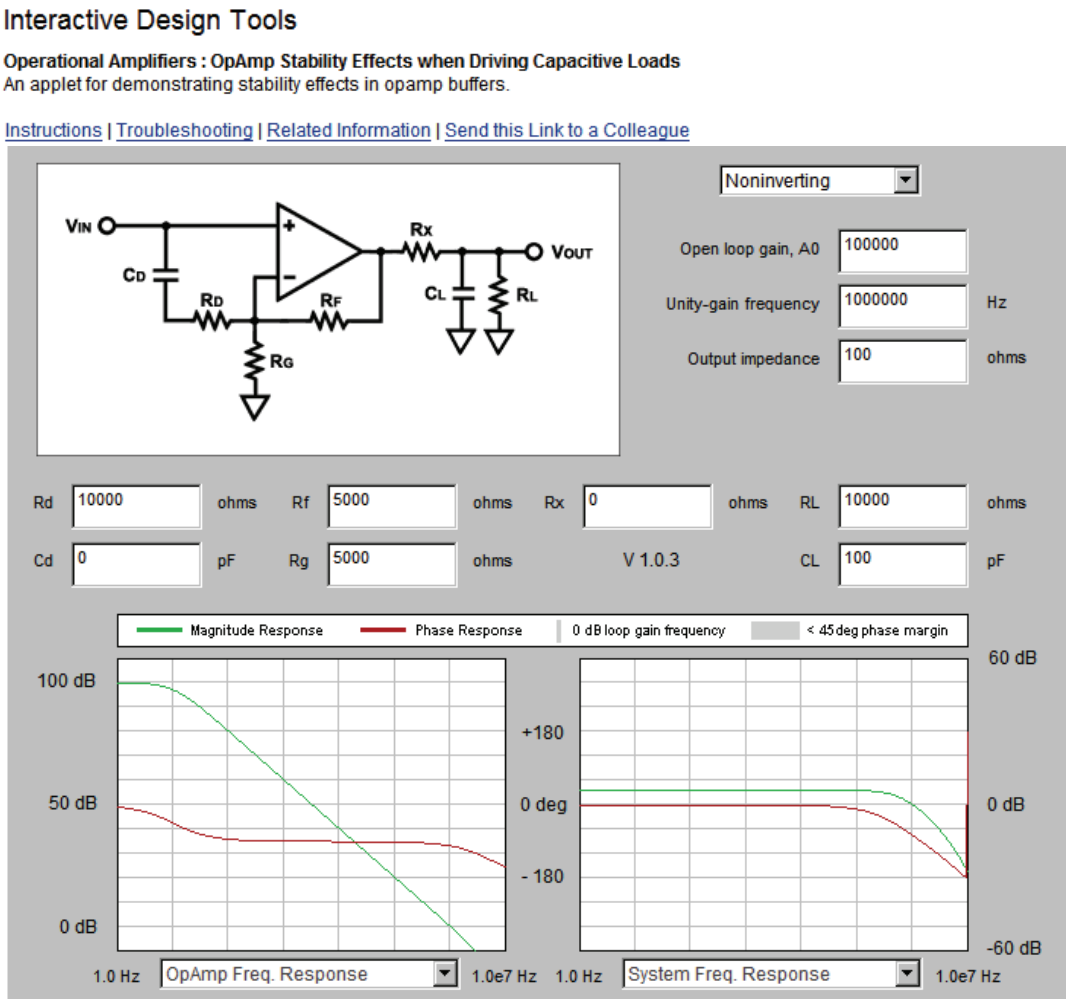


Figure 13.29: *Op Amp Stability Tool Screen*

An example of a tool to help in the stability analysis is shown in Figure 13.30. Values for the open-loop gain, Gain Bandwidth Product (unity gain frequency) and R_O, along with the closed-loop gain (with R_F and R_G) and the load (R_L and C_L). The gain and phase will then be plotted. If it needs to be modified, both in line resistance and noise gain manipulation are available.

The settling time calculator, shown in Figure 13.31, estimates settling time for a multiplexer by calculating the slower of the two time constants for a cascaded RC network, then computing how many time constants must pass before the system will settle to within 1%, 0.1%, 0.01%, and 0.001% of its final value.

The calculator also estimates the maximum sampling rate possible for a classic A/D converter with S/H input. The sampling rate is estimated as 1/sqrt($(t_{settle}+t_{transition})^2$ + t_{PGA}^2). This number should be less than the sum of $t_{ACQ}+t_{CONV}$, otherwise the maximum sampling frequency will be limited. The maximum sampling frequency estimate is shown in megasamples/second to the right of the settling time number.

To use the calculator, enter the multiplexer parameters in R_{ON}, $C_{S,}$ and C_D and the application parameters in R_{SOURCE}, $R_{LOAD,}$ and C_{LOAD}. Tabbing from one field to the other updates the tabular display at the right, or click "Calculate."

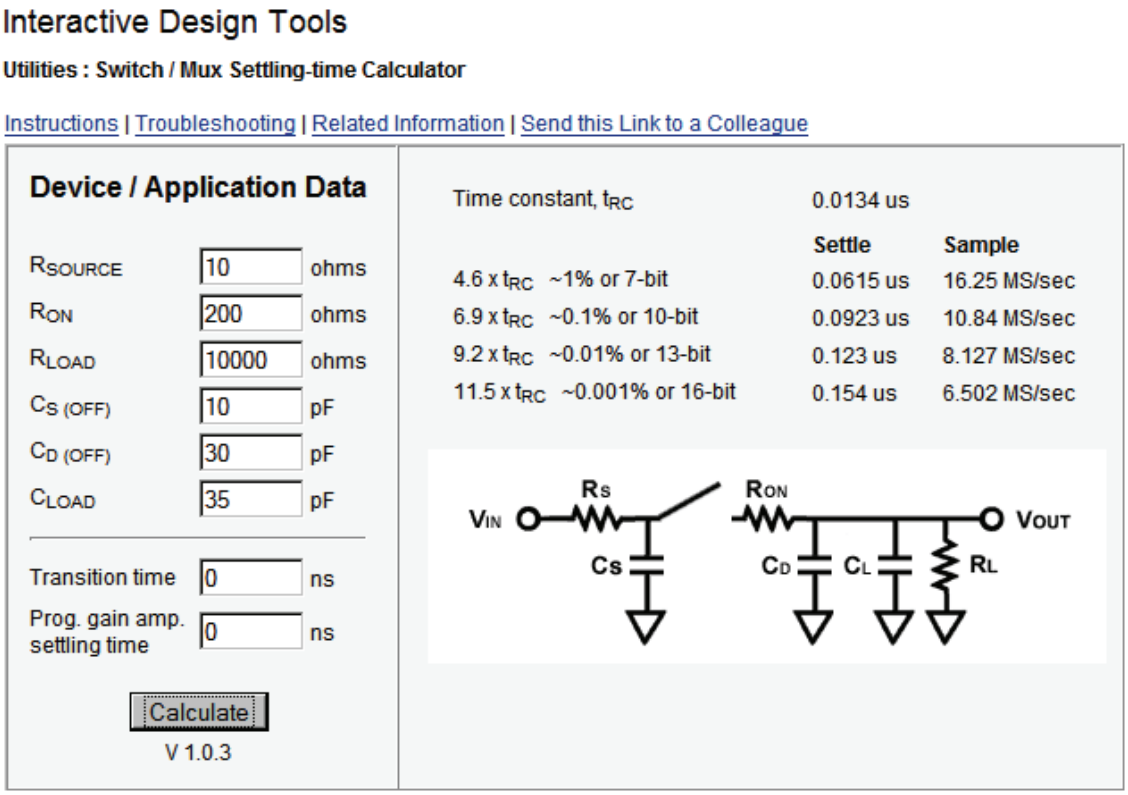


Figure 13.30: *Settling Time Calculator*

As we saw in the section on op amp error sources, there are a number of sources of potential error in an op amp design. The Error Budget Calculator has two parts: an annotated schematic at top and a table of contributing error sources at bottom. Op amp parametric data is automatically entered in the appropriate fields of the bottom table, and default values for the application parameters have been assigned to the application-specific fields at the top. All input data can be manually overridden, however output fields (surrounded by light gray) cannot be changed. This is a great time savings from having to enter all the data by hand.

After entering data in a field, hit tab, or click "Update" to compute derived values and see node voltages updated on the schematic. If the inputs are out of range an alert will appear. If the combination of inputs causes internal or external output limits to be exceeded, the problem node value will be highlighted in red and an "Out of Range!" message will appear. When this message is present, **all** node values should be considered invalid. Do not leave fields blank: if you see "NaN" (Not a Number), this means that insufficient data was entered to compute a value.

"Gain" and "R_F" are computed automatically from one another, based on the value of "R_G." The calculation is ideal and doesn't reflect R_S, R_X, and R_L, for example.

Equations listed in the "Calculation" column are approximate and reflect the worst case between the three amplifier configuration choices. Modifications to the equation for particular configuration types are indicated in ( ). For example (1/2 : noninv) means an additional factor of 1/2 should be used to compute this quantity for the noninverting configuration.

Specs shown are *worst-case* for the selected part, if available, otherwise typical values are used. If no spec is available, "N/S" will appear in that field and an ideal spec (usually zero) will be used for the calculation. Please note that it is highly unlikely that all worst-case specs would ever be present at the same time in the same part. The designer should always refer to the appropriate datasheet and substitute numbers most appropriate to the application. All calculations are approximations, with errors displayed and summed in absolute PPM, even though in some scenarios the actual values would be negative.

The error calculated is separated into two parts, as discussed in the error source section on op amps. It is separated into "resolution error," which are errors which cannot be adjusted out of the system, and drift/gain errors, which can be adjusted out with the proper circuitry. Please refer to the op amp section on error sources for more information.

Figures 13.31(a) and 13.31(b) show the op amp error calculator tool screen.

Interactive Design Tools

Operational Amplifiers :

AD8021 **Simple OpAmp Buffer Error Budget Calculator**

An online tool to illustrate range, gain
and accuracy issues in simple opamp buffers.

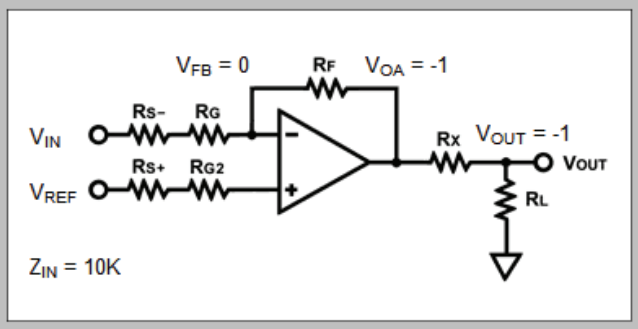
Instructions | Troubleshooting | Related Information | Send this Link to a Colleague

Topology: Inverting

Positive Supply: 12

Ideal Gain: -1

Ideal Node Voltages: ☑



$V_{IN(+)}$	1 V	V_{REF} / V_{IN-}	0
R_{S+}	0 K ohms	R_{S-}	0 K ohms
R_G	10 K ohms	R_{G2}	5 K ohms
R_F	10 K ohms	R_{F2}	K ohms
R_X	0 K ohms	R_L	10 K ohms

Negative Supply: -12

Reset

Application Parameters

Operating Temp., T_A: 85 °C

Supply Variability (ripple+load reg.): 1 %

Update

Error Source	Specification	Approx. Calculation	Absolute Error	Drift/Gain Error	Resolution Error
Resistor Tolerance	0.1 %		2000 ppm		
Resistor Drift, TC_R	25 ppm / °C	~ (1/2 : noninv) $TC_R \times T_{DIFF}$		125 ppm	
Temp. difference, T_{DIFF}	5 °C				
Nom. Open Loop Gain, A_{OL}	25 V/mV		80 ppm		
Min. Open Loop Gain	16 V/mV				45 ppm
Input Offset Voltage, V_{OSI}	1 mV	V_{OSI} / (V_{IN}-V_{REF})	2000 ppm		
Input Offset Voltage Drift, V_{OSI_TC}	0.2 µV / °C	(2 : inv.) $V_{OSI\_TC} \times (T_A\text{-}25)$ / (V_{IN}-V_{REF})		24 ppm	

Figure 13.31(a): *Op Amp Error Budget Calculator Screen (1 of 2)*

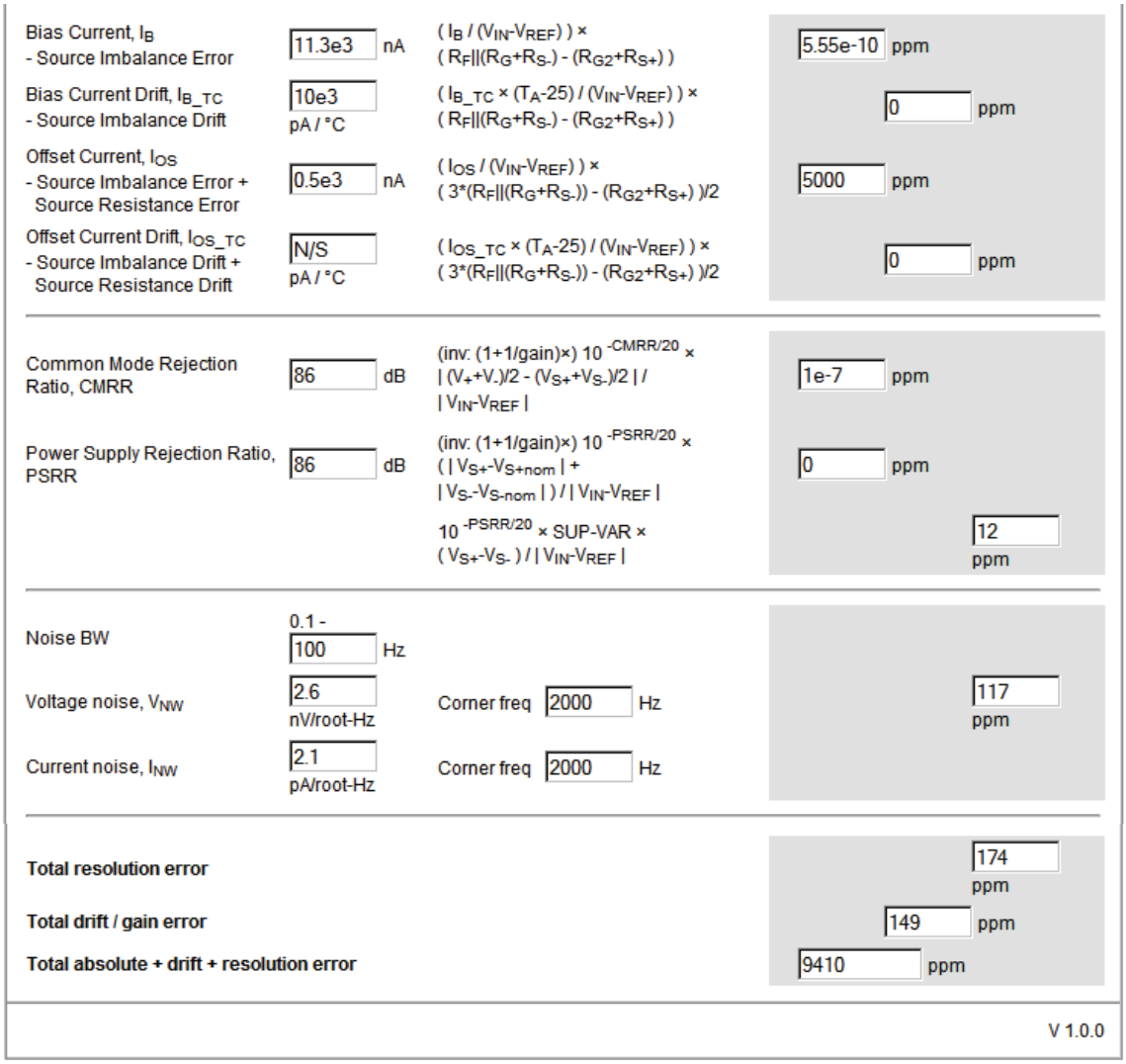
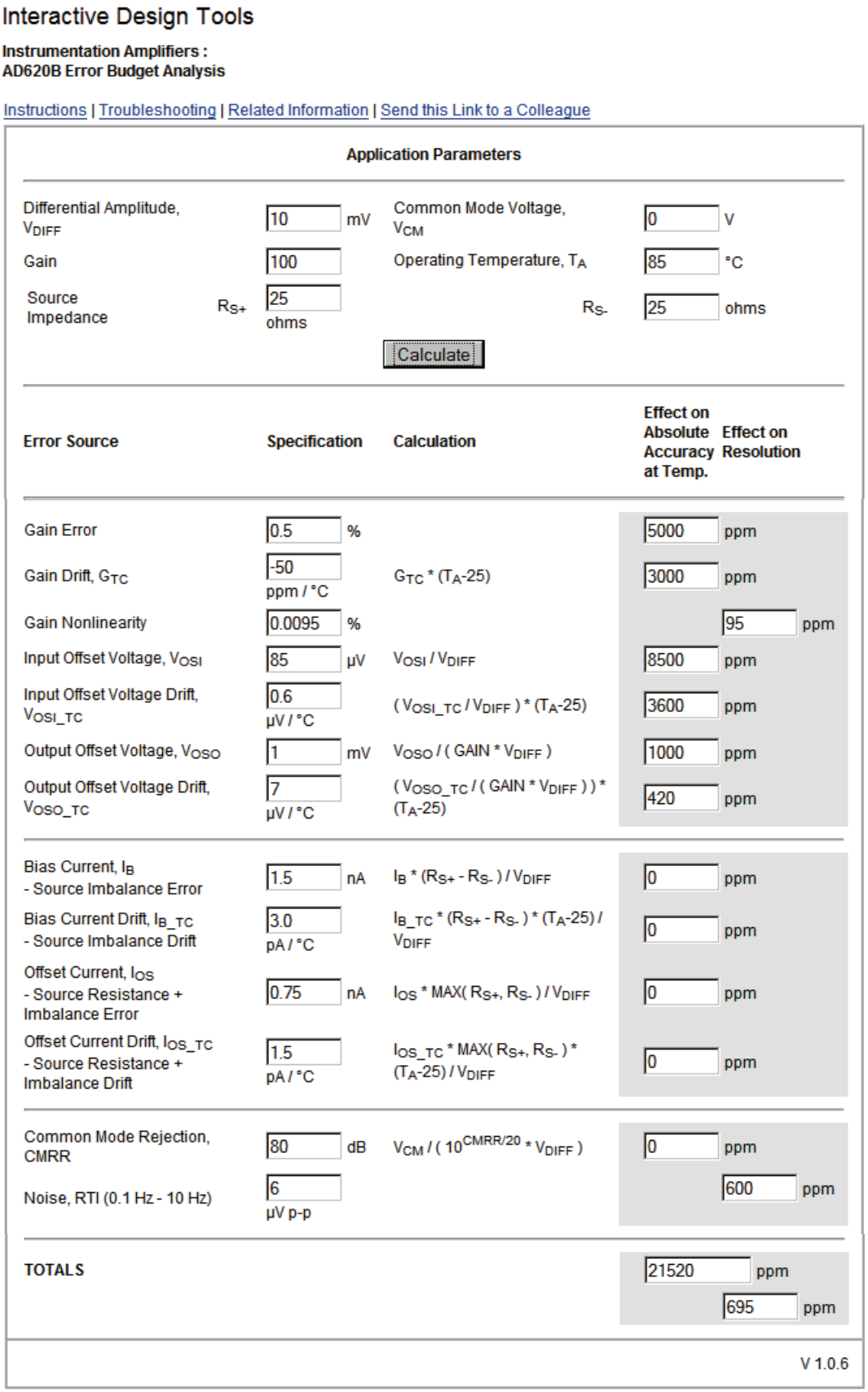


Figure 13.31(b): *Op Amp Error Budget Calculator Screen (2 of 2)*

A similar error budget calculator also exists for instrumentation amplifiers. For this tool the pertinent data is entered into the top field of the calculator. The tool automatically enters the specification data for the particular instrumentation amplifier selected and then calculates the error. Again, the error is separated into "resolution error," which is the non-reducible part and the drift/gain error. Figure 13.32 shows the Instrument Amplifier Calculator screen.



Interactive Design Tools

Instrumentation Amplifiers :
AD620B Error Budget Analysis

Instructions | Troubleshooting | Related Information | Send this Link to a Colleague

Application Parameters

Differential Amplitude, V_{DIFF}	10	mV	Common Mode Voltage, V_{CM}	0	V
Gain	100		Operating Temperature, T_A	85	°C
Source Impedance R_{S+}	25	ohms	R_{S-}	25	ohms

Calculate

Error Source	Specification		Calculation	Effect on Absolute Accuracy at Temp.	Effect on Resolution
Gain Error	0.5	%		5000 ppm	
Gain Drift, G_{TC}	-50	ppm / °C	$G_{TC} * (T_A-25)$	3000 ppm	
Gain Nonlinearity	0.0095	%			95 ppm
Input Offset Voltage, V_{OSI}	85	µV	V_{OSI} / V_{DIFF}	8500 ppm	
Input Offset Voltage Drift, V_{OSI_TC}	0.6	µV / °C	$(V_{OSI\_TC} / V_{DIFF}) * (T_A-25)$	3600 ppm	
Output Offset Voltage, V_{OSO}	1	mV	$V_{OSO} / (GAIN * V_{DIFF})$	1000 ppm	
Output Offset Voltage Drift, V_{OSO_TC}	7	µV / °C	$(V_{OSO\_TC} / (GAIN * V_{DIFF})) * (T_A-25)$	420 ppm	
Bias Current, I_B - Source Imbalance Error	1.5	nA	$I_B * (R_{S+} - R_{S-}) / V_{DIFF}$	0 ppm	
Bias Current Drift, I_{B_TC} - Source Imbalance Drift	3.0	pA / °C	$I_{B\_TC} * (R_{S+} - R_{S-}) * (T_A-25) / V_{DIFF}$	0 ppm	
Offset Current, I_{OS} - Source Resistance + Imbalance Error	0.75	nA	$I_{OS} * MAX(R_{S+}, R_{S-}) / V_{DIFF}$	0 ppm	
Offset Current Drift, I_{OS_TC} - Source Resistance + Imbalance Drift	1.5	pA / °C	$I_{OS\_TC} * MAX(R_{S+}, R_{S-}) * (T_A-25) / V_{DIFF}$	0 ppm	
Common Mode Rejection, CMRR	80	dB	$V_{CM} / (10^{CMRR/20} * V_{DIFF})$	0 ppm	
Noise, RTI (0.1 Hz - 10 Hz)	6	µV p-p			600 ppm
TOTALS				21520 ppm	695 ppm

V 1.0.6

Figure 13.32: *Instrumentation Amplifier Error Budget Calculator Screen*

The Instrumentation Amplifier Gain Calculator calculates the gain of an in-amp circuit given the gain-setting resistor or conversely gives the value of the resistor need for a particular gain. It also checks to insure all nodes, even those internal, are kept in their operational range.

To use the tool, simply enter data in the fields provided. If an input is out of range an alert will appear (in red, along with an “error” message).

Click "Update" or tab to another field to see node voltages annotate the schematic on the right. Internal node voltages are for the equivalent 3-op amp (or 2-op amp) circuit, assuming a 0.5 V level shift. This may not reflect the exact internal implementation, but is instead a simplified schematic.

If the combination of inputs causes internal or external limits to be exceeded, the problem node value will be highlighted in red and an "Out of Range!" message will appear. When this message is present, all node values should be considered invalid. These input conditions could include such things as overranging the output or, especially in single supply applications, putting an internal node out of range. The fact that the tool will show the conditions of internal nodes is useful, since you cannot probe those nodes directly and maybe mislead into believing the circuit is working when, in fact, it is not.

Only one of "Gain" or "R_G" can be specified - the other is computed automatically.

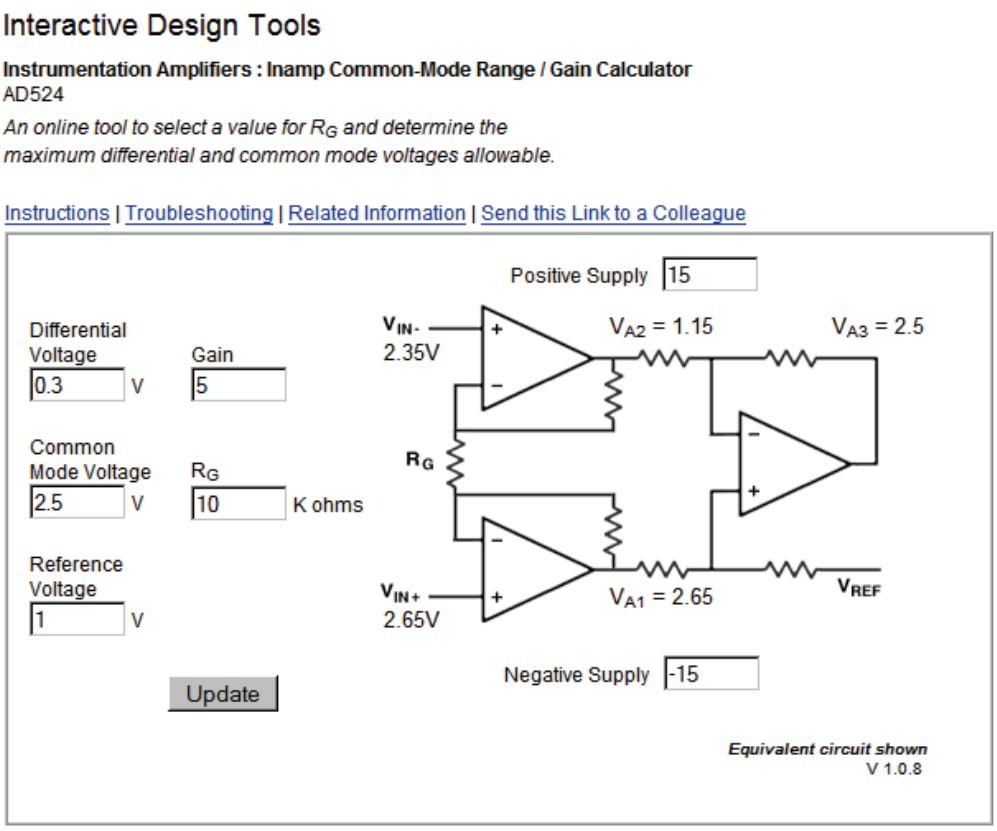


Figure 13.33: *Instrumentation Amplifier Common-Mode Range/Gain/Noise Calculator Screen*

The same basic tool also exists for differential amplifiers and active feedback amplifiers. Figure 13.34 shows the Differential Amplifier Common-Mode Range/Gain/Noise calculator screen.

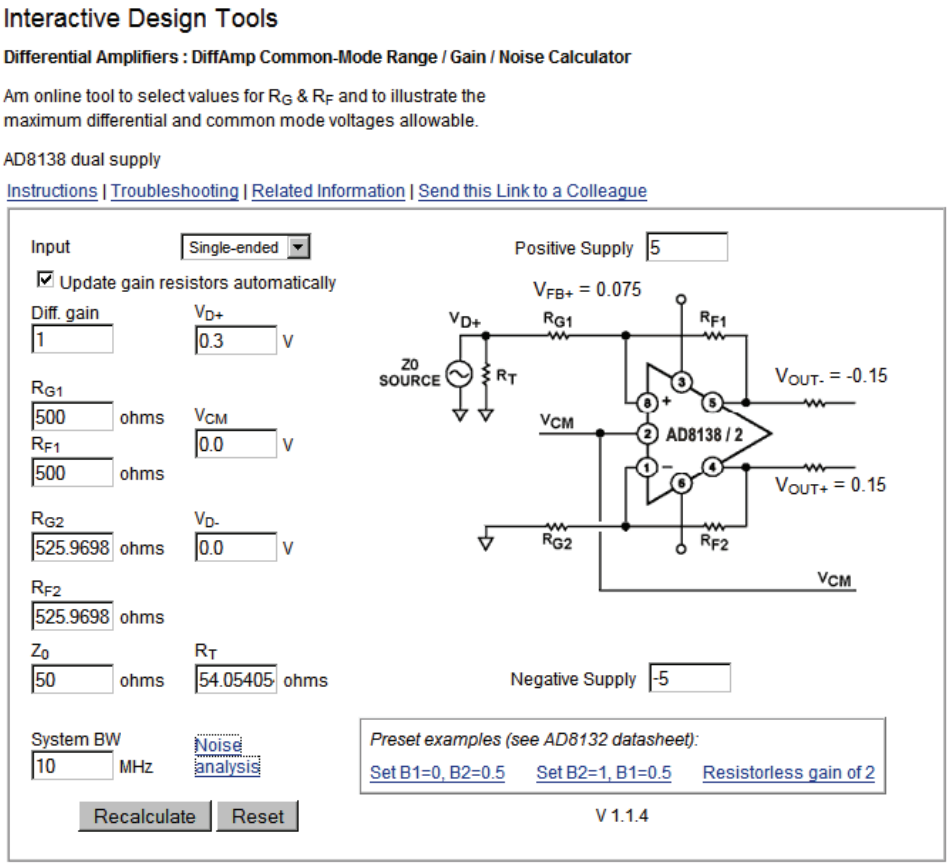


Figure 13.34: *Differential Amplifier Common-Mode Range/Gain/Noise Calculator Screen*

The Differential Amplifier Calculator has two basic modes: manual and automatic. The default is automatic in which it is assumed you want to calculate resistor values (incl. termination) to match a source impedance. In the automatic mode, R_F is computed from R_G and Gain**:** changing either of the latter will affect the former. Changing Z_0 affects all the gain resistors (which should always be a minimum of 10 × Z_0), as well as R_T**.** R_T is the value for the termination resistor taking into account the impedance of the differential amplifier's gain network and is recalculated when either of R_F or R_G are changed (changing R_T, however, affects nothing). Single-ended termination resistances are calculated assuming V_{CM} = 0. For other fixed voltages, the input impedance is nonlinear.

By unchecking "Update resistor values automatically," the calculator is placed in the manual mode where each resistor can be set independently. Gain and the node voltages are the only thing computed when "Recalculate" is clicked or a new field is entered. For

open circuits or "infinite" resistors use a large number instead, such as 1e99. Do not leave any fields blank.

The schematic shows a matched Thevenin source driving a terminated line, however input voltages are actually set independently for each value of R_G**.** Consequently Z_0 and R_T don't affect the calculation of node voltages. For unterminated calculations set Z_0 to zero.

Note: For clarity, this calculator shows ideal behavior and does not show the effects of input offset currents and voltages.

Figure 13.35 shows the Active Feedback Calculator

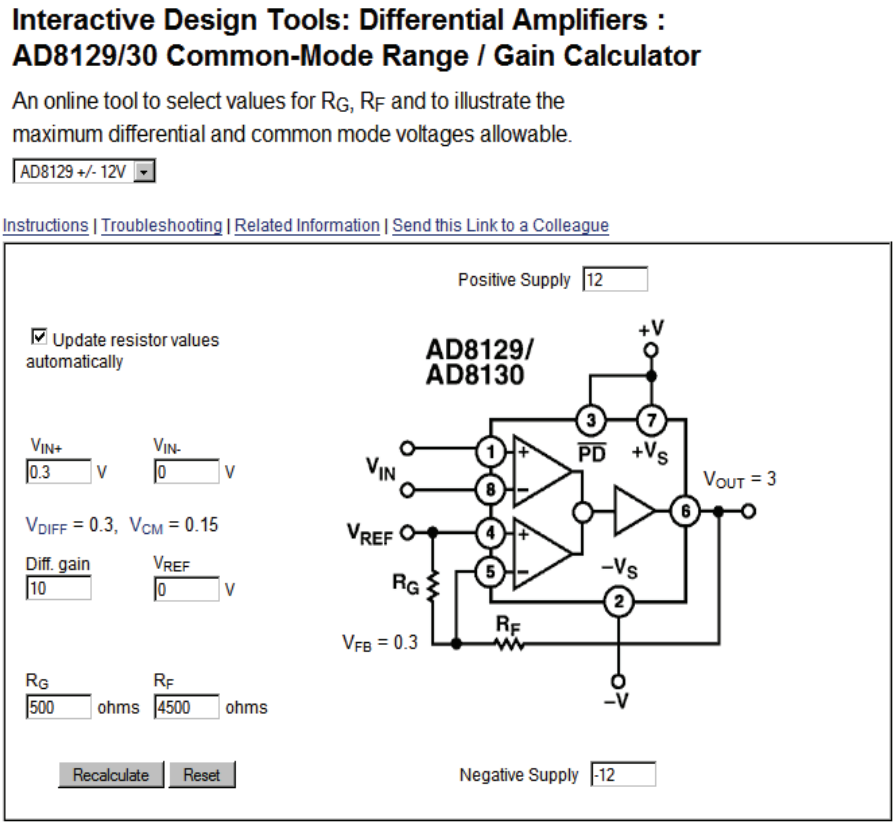


Figure 13.35: *Active Feedback Common-Mode Range/Gain Calculator Screen*

Configuration Assistants

Another type of “on line” design assistant are the configuration assistants. Many modern converters are actually small systems, usually with significant digital content. This digital content is used to set operating conditions (which channel of a multichannel input ADC, for instance). While it is possible to take the register descriptions in the data sheets and use them to set the correct bits in the correct registers, it is much easier to use a configuration assistant.

An example is the configuration assistant for the AD7730 Σ-Δ ADC (see Figure 13.36). Each dark gray rectangle shows a single register's content in two different ways. Most of the space is taken up with pull-down menus and a few hex input fields that display bit fields within the register, MSB to LSB. Eight bits are displayed per row, with the bits aligned in numbered columns. At the right is the combined hex code corresponding to values selected for the individual bit fields.

Changing either the hex code or the bit fields updates the other. Registers that can't be broken into separate fields are shown for completeness, even though not much can be done with them.

In the actual AD7730, registers are programmed by first setting the Register Select bits in the Communications Register (CR2:0). In this tool, however, each register can be changed directly without first selecting it in the CR.

Similarly, one of three pairs of calibration offset/gain registers is addressed by setting the Channel Select bits in the Mode Register (MR1:0—note there are only two channels, however). The active pair is highlighted in pink.

To set up the clock register, first choose an update rate and set the Filter Selection bits and MCLK frequency accordingly. The Filter Selection bits can be automatically configured by setting the desired Update Rate or -3 dB point, however, the frequencies are quantized, and you may need to adjust the MCLK frequency to get the exact update rate or cutoff frequency desired. See the AD7730 data sheet for further details.

By default, reading and writing register pseudocode is, like the real AD7730, a two-step process: the Comm register must first be set up to select a target for the next read or write. After a register has been configured to your liking, select it in the Comm register and click "W". The selected register is now highlighted in yellow (and the channel in pink). To complete the cycle, click on the enabled "W" or "R." This will also clear the Register Select bits which must be manually reset for each access. Please note that the multiple read settings are nonfunctional—an ordinary read will be performed instead.

Both operations append pseudo-code instructions to a ticker of instructions at the bottom right of the applet. "writeSerial (val, length)" is an abstract subroutine that takes the quantity "val" and sends "length" bits of it serially to the AD7730, MSB first. The code list can be copied and pasted into another application (on most platforms).

Checking "Auto" above the Code output window puts code generation into a second mode, enabling all registers and automatically prepending the appropriate Comm register write when "W" or "R" for any register is clicked. Please note that in this mode the register select bits in the Comm register are ignored.

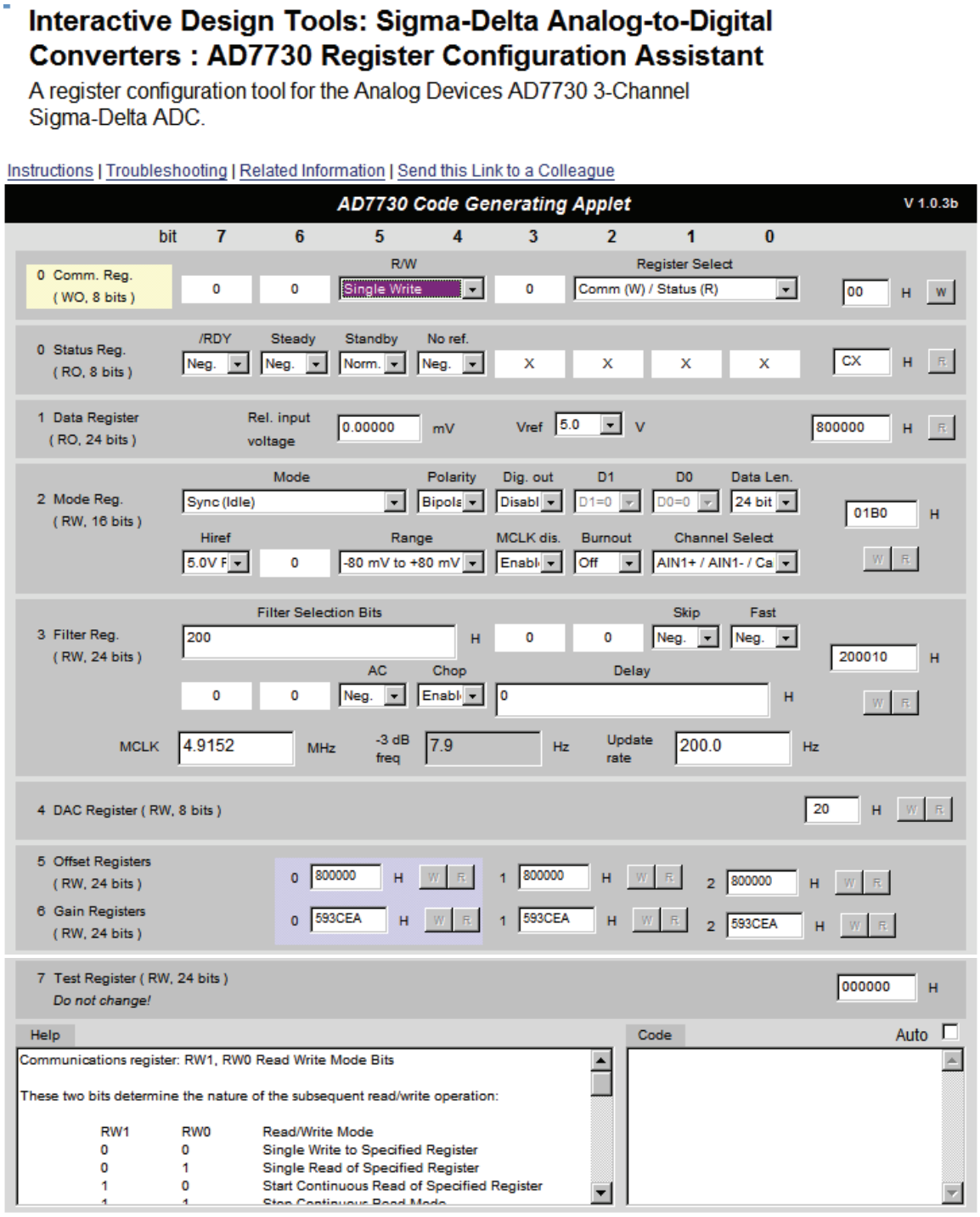


Figure 13.36: *AD7730 Register Configuration Assistant Screen*

The ideal (low frequency, low noise/distortion, perfectly calibrated) digitized value for a given input voltage can be obtained by entering a voltage in the field to the right of the data register "R" button. Either a 5.0 V or 2.5 V V_{REF} (= V(REF+) - V(REF-)) may be selected, but the input voltage is always *relative* to the reference. *Please note: this calculator is not a simulator and so, for example, changing the calibration registers will not change the calculated digital value.*

Documentation is available for each field simply by selecting it, and is shown in the Help text area at the bottom of the Applet. Use the scroll bar to scroll down through the text.

Another example of a register configuration assistant is the one for an AD9850 Direct Digital Synthesis (DDS) system.

This calculator has several distinct functions. First, it's a tool for selecting a value for $R_{SET,}$ which sets the output current, and checking that the output level remains within limits for a given load.

The AD9850 has complementary current output structures which limit the current and voltage that can be supplied and still meet other datasheet specifications. The output current level, I_{OUT}, is set by a single external resistor, R_{SET}, and the two are related by an equation. Changing one of these fields in the calculator updates the other automatically. If too high a current is selected, an error is noted. The I_{OUT} current develops a voltage into the selected R_{LOAD}, shown on the schematic, and is checked against the AD9850's compliance voltage.

Second, it's an assistant for selecting a 32-bit tuning word, given a reference clock and desired output frequency. Third, it shows the tuning word and other configuring bits encoded as a sequence of hex codes for use in programming the AD9850 via its parallel or serial interface.

A tuning word is selected by simply entering the desired REFCLK and output frequency. REFCLK has a maximum frequency that depends on supply voltage, selected at the top of the screen. Because the tuning word is limited to 32 bits there is typically a small deviation between the desired and actual output frequencies, which is shown in a field at right. The actual output frequency is what is encoded as the tuning word and this comprises the last four bytes of the parallel hex codes and the first four of the serial codes. Tuning words greater than 7FFFFFFF H exceed the Nyquist frequency and will cause error messages to appear.

The AD9850 has 5 bits of programmable phase which is selected in a manner similar to the desired output frequency. The closest available phase setting appears in the field at the right and in the corresponding hex code with the power down bit. The hex code fields are bidirectional, and a known set of hex codes can be entered to retrieve the programmed frequency and phase.

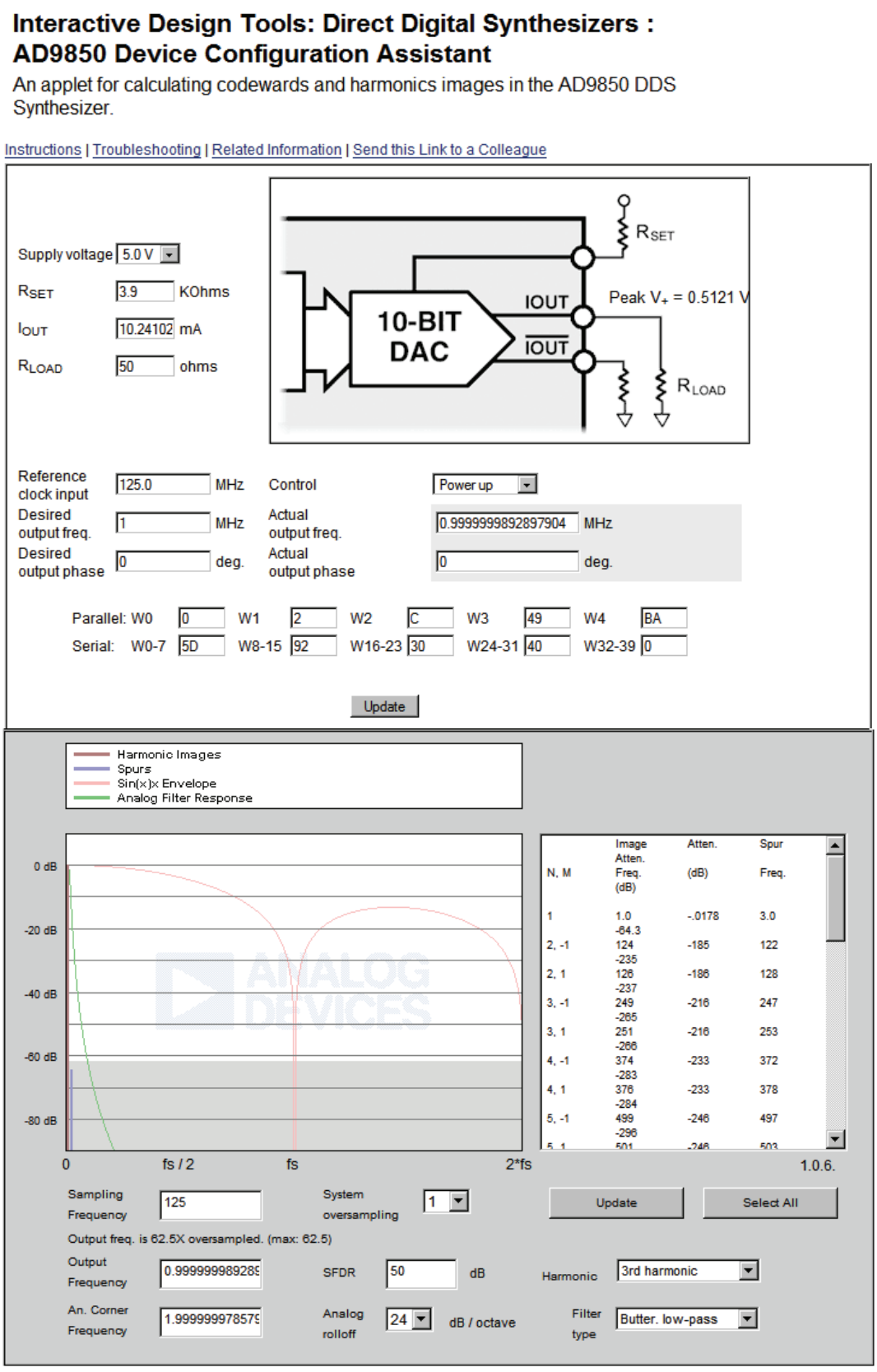


Figure 13.37: *AD9850 DDS Register Configuration Assistant Screen*

Lastly, output harmonics are shown for the selected reference clock and output frequency after an external reconstruction filter has been applied.

Suppression of images and spurs (waveform reconstruction) can be simulated by selecting corner frequency, filter order and type of a simple analog filter (last line of images calculator; magnitude rolloff). A region corresponding to 10 bits of quantization noise is shaded at the bottom of the graph for reference. This calculator is based on a highly simplified model of the AD9850: check data sheet for parameters appropriate to your application.

Calculating the location of harmonics for an amplifier is a fairly simple process. The 2nd harmonic is at 2× the fundamental, the 3rd harmonic is at 3× the fundamental and so on. For a DAC, however, the situation is a bit different. More often than not, it's the image of the harmonic aliased by the sampling rate. This means that the harmonics may actually be below the fundamental and the will change their relative positions as the DAC output frequency is varied. There is a design tool that addresses this issue.

The DAC image applet (see Figure 12.38) shows the harmonic images and spurs for single frequency output from a DAC, an AD9772 in this example. The model of the AD9772 is simplified and idealized—only SFDR is modeled and it is assumed frequency-independent. The response characteristics of the internal digital filter have been approximated. See the datasheet for actual performance data.

For an ordinary DAC, images are located at $N*F_{DAC} \pm F_{OUT}$. The AD9772 contains an integral interpolator which doubles the input data rate creating an image of the output frequency mirrored about $F_{DATA}/2$. An interpolation filter suppresses the upper image in low-pass mode (MOD0=0), or suppresses the fundamental when in high-pass mode (MOD0=1). Both the filtered and unfiltered images then create further images and spurs at the DAC data rate, according to the $N*F_{DAC}$ +/- F_{OUT} rule.

The AD9772 also has a "zero-stuffing" mode (MOD1=1) which allows the data stream to be doubled a second time by inserting zeroes between each sample. Zero-stuffing doubles again the number of images per F_{DAC} harmonic, but F_{DAC} is twice what it would be without zero-stuffing and the mathematics work so that the location of the images is the same as without zero-stuffing—only the amplitudes change. These new images are <u>not</u> filtered internally, so the upper image can be used for direct IF synthesis. MOD0 and MOD1 are often used together for this purpose.

Spurious 2nd or 3rd harmonics of each image are assumed to result from D/ nonlinearities and so are folded within the first Nyquist Zone (NZ) of F_{DAC}. These spurs then have their own harmonic images that roll off as sin(x)/x (where $x = \pi*F_{SPUR} / F_{DAC}$). The magnitude response of the AD9772, combining its internal interpolation with the sin(x)/x envelope, is shown.

To show external selection/suppression of desired/undesired images and spurs, the applet can apply a simulated post-DAC analog filter.

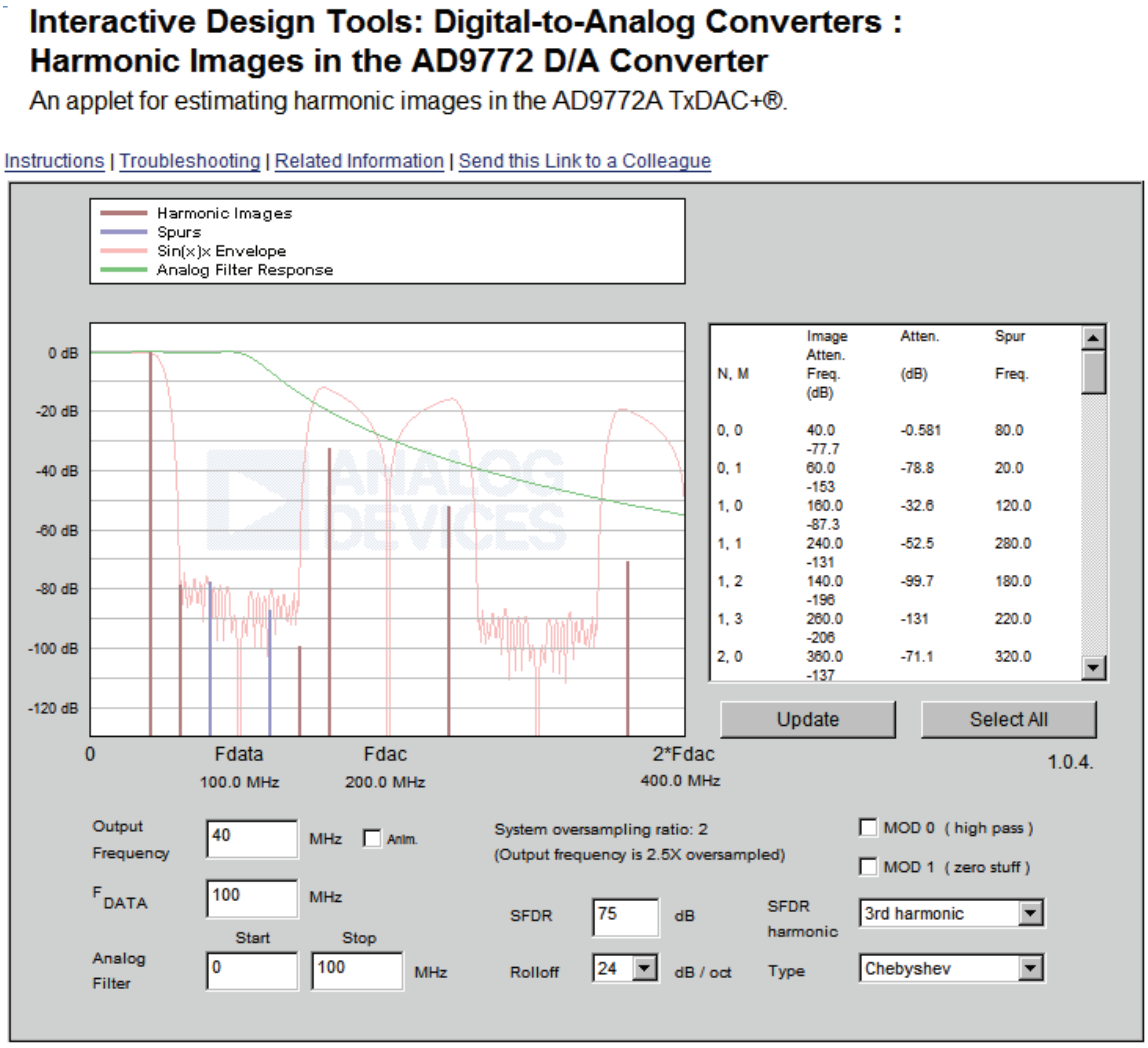


Figure 13.38: *DAC Harmonic Images Calculator Screen*

How to use this applet:

Enter $\mathbf{F_{DATA}}$ and the Output Frequency in the provided text fields. Hit "Enter" or click "Update" to recompute the display.

Select the Start and Stop Frequencies of the Analog Filter. A zero turns off that portion of the filter, i.e. entering a zero for the start frequency makes the filter low-pass only.

Select filter roll-off and type. The analog filter magnitude is shown.

Image frequencies and amplitudes are shown in a table at top right. The first column gives the DAC multiple, N, and then a sequence number for the image around that multiple. For nonzero-stuffing images, the order of these images for N>0 is $N*F_{DAC}$ + 1) $-F_{OUT}$ 2) $+F_{OUT}$ 3) $-(F_{DATA} - F_{OUT})$ and 4) + $(F_{DATA} - F_{OUT})$. The table data is selectable and can be copied and pasted into a spreadsheet. Use "Select all" to conveniently select the entire contents before copying.

FDR is used to set the relative level of spurs, which are assumed here to be the result of D/A nonlinearity. SFDR Harmonic selects whether these distortion spurs are most prominent at 2× or 3× (default) an interpolation/zero-stuffing image. In reality, SFDR depends on both the sample rate and output frequency, among other variables. However, a single compromise number is used here.

A similar design assistant is available to help in designing the anti-aliasing filter of an ADC system. This applet (see Figure 13.40) illustrates aliasing and its suppression through filtering and oversampling in a classic (nonsigma-delta) A/D converter. An ideal ADC is assumed—distortion free, unlimited bandwidth, etc.—in order to focus solely on aliasing effects. The input signal is also assumed to be noise free, but the most practical use of this applet is to find a combination of filtering and oversampling that pushes the aliased terms below the noise floor of the input, or the overall system .

The finite rolloff of practical analog filters means there are always some undersampled high frequency components that fold into the pass band, or "Nyquist Zone" (NZ), and appear in the sampled signal as noise. For the simple case of an input composed of band limited white noise, this applet gives an estimate of how much out-of-band signal will be folded into the base band (1st NZ). In many real-world situations, the out-of-band signal is of lesser amplitude and so this estimate is too conservative; in other cases it might not be conservative enough—it depends on the out-of-band signal level. *The bandwidth limit for the input white noise signal is a multiple of the sampling frequency. By default, that multiple is 32×; the maximum is 256×.*

Aliasing suppression in oversampled systems is achieved through a combination of analog and digital filtering, but digital filtering cannot replace a high-quality analog filter because it cannot remove aliasing noise after it's been folded into the pass band by the sampling process. Instead, oversampling must be used to put enough octaves and attenuation between the Nyquist frequency and the highest pass band frequency of interest. Digital filtering can then be used on the sampled signal to eliminate frequencies between pass band and Nyquist. For simplicity, the additional aliasing noise that results from downsampling the sampled signal is not shown.

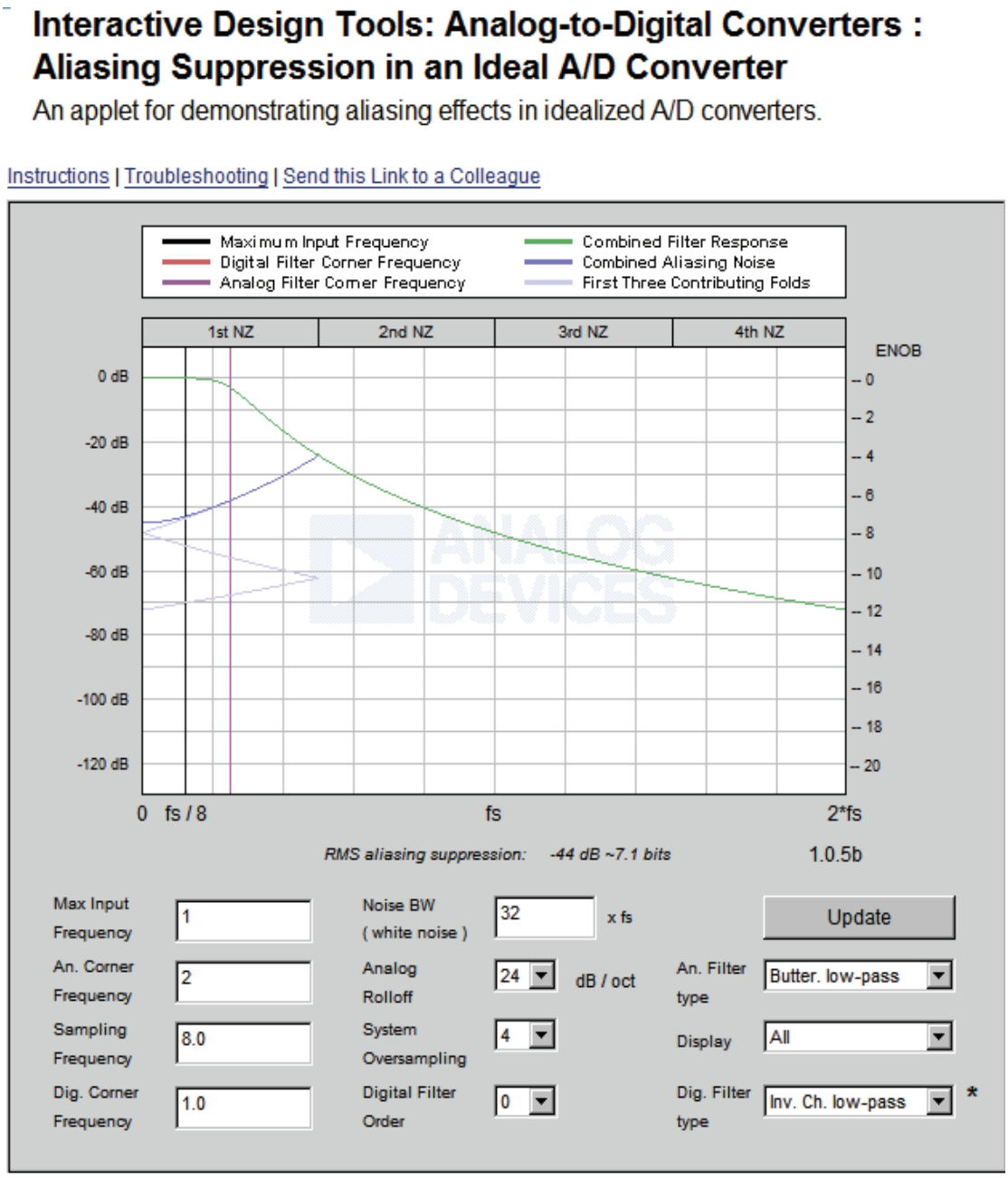


Figure 13.39: *ADC Antialiasing Suppression Assistant Screen*

How to use this applet:

Enter the Maximum Input Frequency**,** Sampling Frequency, and Oversampling Ratio in the fields provided. Hit "Enter" or click "Update" to recompute the display. (The maximum input frequency is marked with a black line.)

Select Digital and Analog Corner Frequencies. Behavior of this hypothetical ADC is assumed frequency-independent, so only frequency ratios matter—the units must be uniform, but are otherwise irrelevant. A cursor marks the digital filter corner frequency and another analog filter corner. The default example places the analog corner at 2× the maximum frequency of interest to minimize potential phase distortion in the passband. *Please note that for speed of computation, digital filter characteristics are those of a BT-transformed IIR filter.*

Select filter rolloffs and types. The combined filter response of the analog and digital filters is shown.

Combined aliasing noise is shown with the first three contributing folds in a different color. Combined noise is summed from dc to the frequency specified by Noise BW. (Note: 32× the sampling frequency is usually plenty and the applet will slow down if too much noise BW is specified.)

Suppression in dB is shown on the left vertical axis with the corresponding Equivalent Number of Bits (ENOB) shown at right. A summary of the rms average suppression over the passband is immediately below the chart.

Experiment by changing the analog filter parameters and comparing the results to changing the oversampling ratio. Changing the oversampling ratio multiplies the max input frequency to get a sampling frequency but the reverse direction doesn't work—it's sampling frequency that's important and the oversampling ratio menu is just a convenience.

Once the filter requirements are know, the Filter Design Wizard, to be discussed shortly, can aid in the actual implementation of the filter.

Another branch of design assistants take into account a complete application rather than just a block. An example of this is the Photodiode Error Budget Analysis Tool. This calculator has two parts: an annotated schematic at top and a table of contributing error sources at bottom. Op amp parametric data is automatically entered in the appropriate fields by choosing an op amp from the menu at the top. Default application parameters have been entered in the fields at the top with default photodiode parameters placed in the section below this and above the opamp parametrics (a few application parameters are mixed in with the op amp data). All input data can be manually overridden, however, output fields cannot be changed.

After entering data in a field, hit tab or click "Update" to compute derived values and see node voltages updated on the schematic. If the inputs are out of range an alert will appear. If the combination of inputs causes internal or external output limits to be exceeded, the problem node value will be highlighted in red and an "Out of Range!" message will appear. When this message is present, all node values should be considered invalid. Do not leave fields blank: if you see NaN (Not a Number), this means that insufficient data were entered to compute a value.

This tool uses a highly simplified model of an op amp, and any results must be used with care. In particular please note that calculated errors are highly dependent on which op amp parametric data is used, which is application-specific. For many of the op amps, two sets of numbers are available in the pull-down: “typical” and "conservative." It is highly unlikely that all worst-case specs would ever be present at the same time in the same part. The designer should always refer to the appropriate data sheet and substitute numbers most appropriate to the application. All calculations are approximations, with errors displayed and summed in absolute PPM, even though in some scenarios the actual values would be negative (and could offset other errors).

Equations listed in the "Calculation" column are approximate and reflect the worst case between the three buffer choices. Modifications to the equation for particular buffer types are indicated in ( ). For example (1/2 : noninv) means an additional factor of 1/2 should be used to compute this quantity for noninverting buffers.

Noise is calculated as an integrated quantity, assuming uniform spectral density over the noise bandwidth given (white noise). By default, the noise bandwidth is initialized to the closed-loop bandwidth X $\pi/2$ ($\pi/2$ adjusts for the equivalent noise bandwidth for single-pole rolloff of white noise). If a smaller signal bandwidth is entered, the assumption is that the output will be filtered to this bandwidth so as to remove out-of-band noise. Please also note that it is assumed the noninverting input resistor is perfectly bypassed and so is not included in the noise calculations.

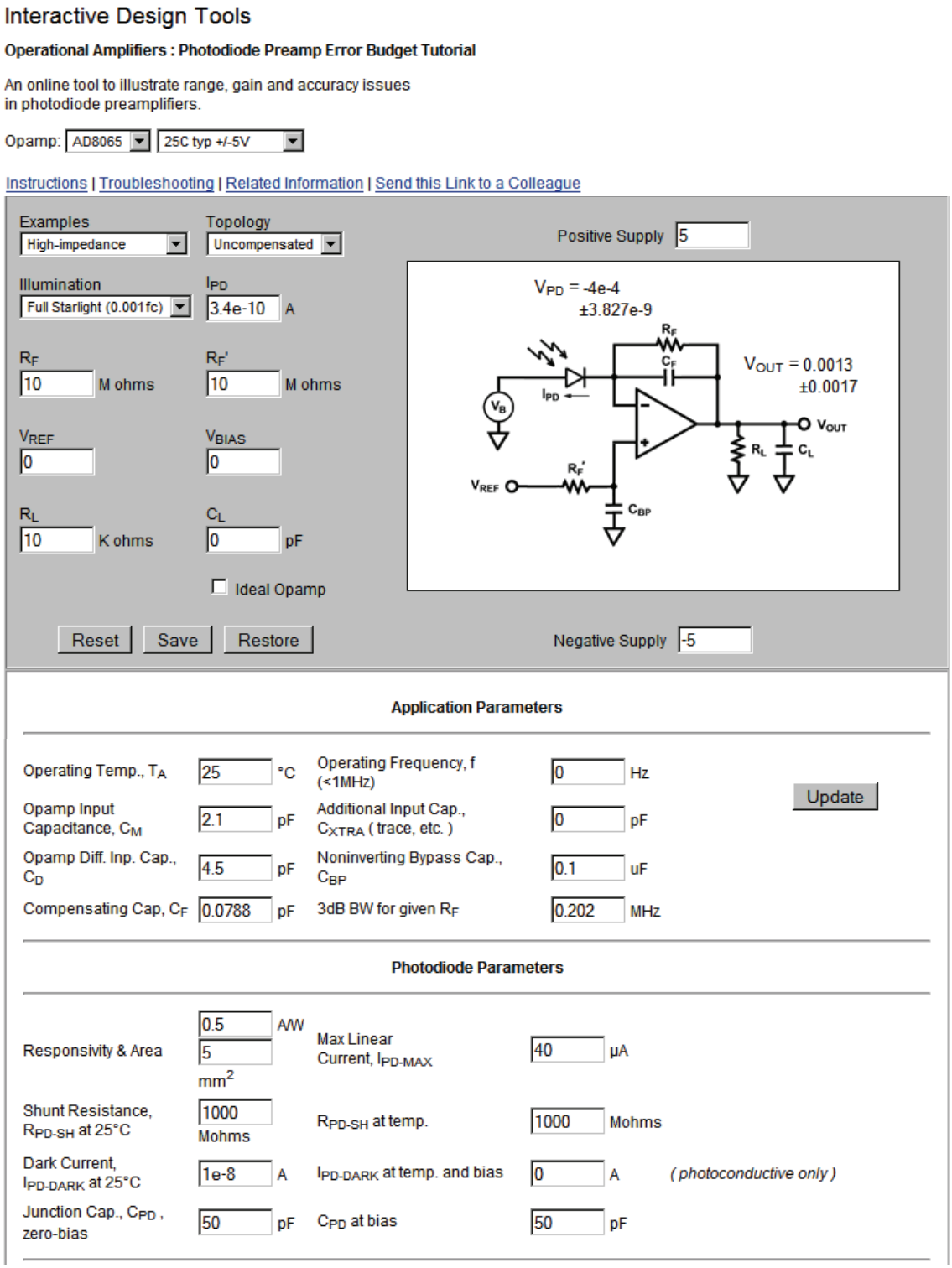
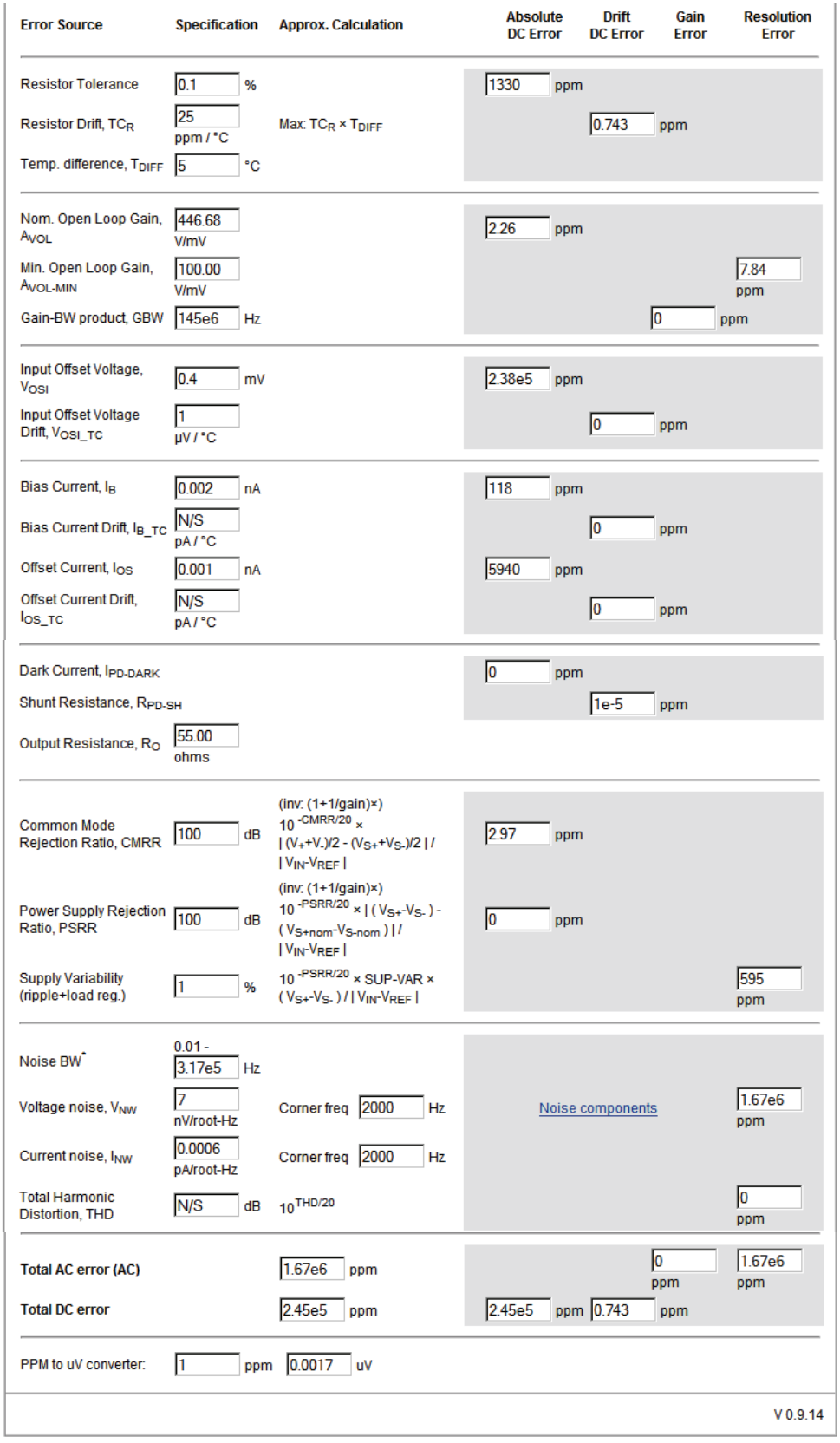


Figure 13.40: *Photodiode Error Budget Analysis Screen (1 of 2)*



Error Source	Specification	Approx. Calculation	Absolute DC Error	Drift DC Error	Gain Error	Resolution Error
Resistor Tolerance	0.1 %		1330 ppm			
Resistor Drift, TC_R	25 ppm / °C	Max: $TC_R \times T_{DIFF}$		0.743 ppm		
Temp. difference, T_{DIFF}	5 °C					
Nom. Open Loop Gain, A_{VOL}	446.68 V/mV		2.26 ppm			
Min. Open Loop Gain, $A_{VOL-MIN}$	100.00 V/mV					7.84 ppm
Gain-BW product, GBW	145e6 Hz				0 ppm	
Input Offset Voltage, V_{OSI}	0.4 mV		2.38e5 ppm			
Input Offset Voltage Drift, V_{OSI_TC}	1 µV / °C			0 ppm		
Bias Current, I_B	0.002 nA		118 ppm			
Bias Current Drift, I_{B_TC}	N/S pA / °C			0 ppm		
Offset Current, I_{OS}	0.001 nA		5940 ppm			
Offset Current Drift, I_{OS_TC}	N/S pA / °C			0 ppm		
Dark Current, $I_{PD-DARK}$			0 ppm			
Shunt Resistance, R_{PD-SH}				1e-5 ppm		
Output Resistance, R_O	55.00 ohms					
Common Mode Rejection Ratio, CMRR	100 dB	(inv: (1+1/gain)×) $10^{-CMRR/20}$ × | $(V_+ + V_-)/2 - (V_{S+} + V_{S-})/2$ | / | $V_{IN} - V_{REF}$ |	2.97 ppm			
Power Supply Rejection Ratio, PSRR	100 dB	(inv: (1+1/gain)×) $10^{-PSRR/20}$ × | ($V_{S+} - V_{S-}$) - ($V_{S+nom} - V_{S-nom}$) | / | $V_{IN} - V_{REF}$ |	0 ppm			
Supply Variability (ripple+load reg.)	1 %	$10^{-PSRR/20}$ × SUP-VAR × ($V_{S+} - V_{S-}$) / | $V_{IN} - V_{REF}$ |				595 ppm
Noise BW*	0.01 - 3.17e5 Hz					
Voltage noise, V_{NW}	7 nV/root-Hz	Corner freq 2000 Hz	Noise components			1.67e6 ppm
Current noise, I_{NW}	0.0006 pA/root-Hz	Corner freq 2000 Hz				
Total Harmonic Distortion, THD	N/S dB	$10^{THD/20}$				0 ppm
Total AC error (AC)		1.67e6 ppm			0 ppm	1.67e6 ppm
Total DC error		2.45e5 ppm	2.45e5 ppm	0.743 ppm		
PPM to uV converter:	1 ppm	0.0017 uV				

V 0.9.14

Figure 13.41: *Photodiode Error Budget Analysis Screen (2 of 2)*

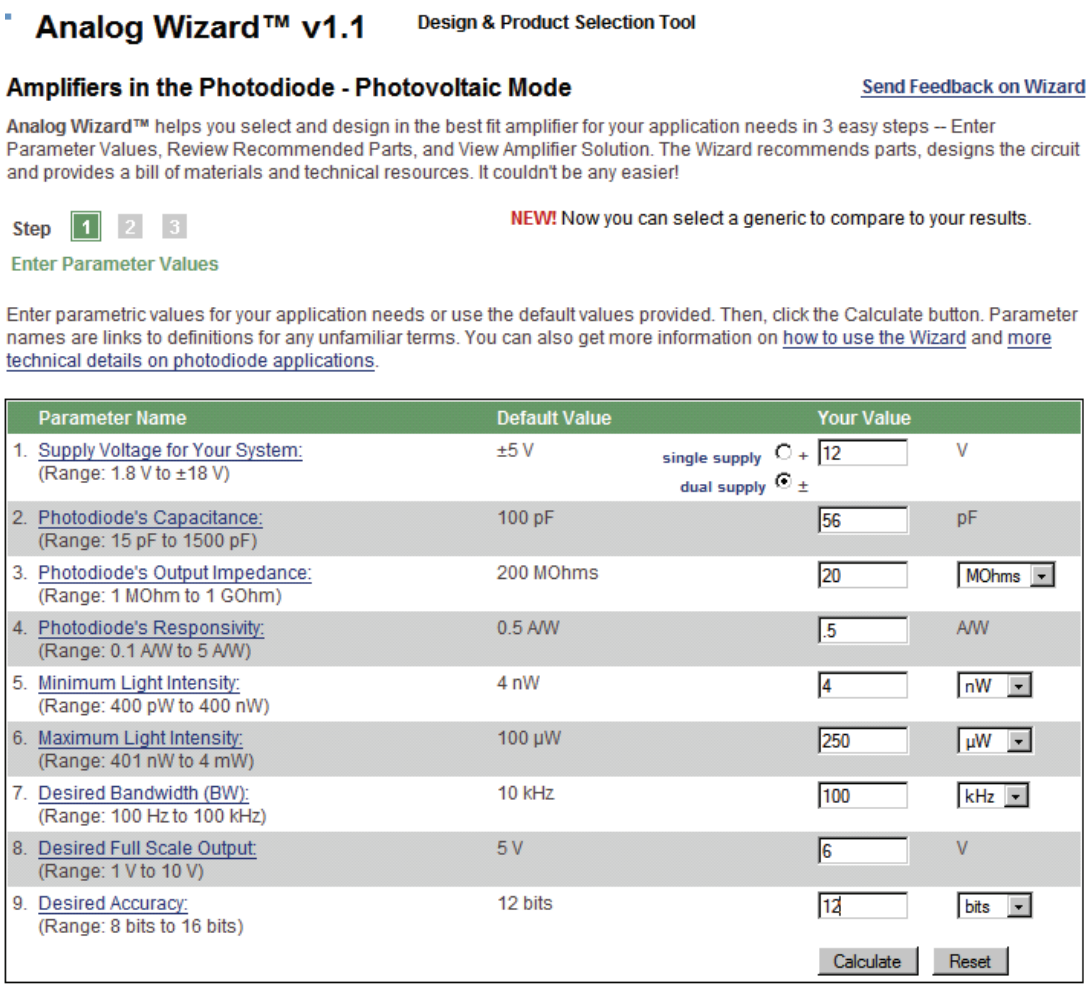
Design Wizards

Photodiode wizard

An extension of the error budget tool is the design wizard. The Analog Wizard™ uses a 3-step process to help you find parts for your photodiode application quickly and easily. The Wizard recommends parts, designs the circuit and provides a bill of materials and technical resources.

Step 1: Enter parametric values.

Enter the parametric values for your application or use the default values provided. A range for each parameter is displayed to help you enter values within the appropriate boundaries. NOTE: Analysis will only be accurate if all actual values for the photodiode are entered.



.

Figure 13.42: *Photodiode Wizard First Page*

When you click Search, the Wizard uses your entered values to calculate the amplifier requirements and pull matching parts from Analog Devices' product database. These are the recommended parts. See Figure 13.43

Step 2: Choose the Op Amp

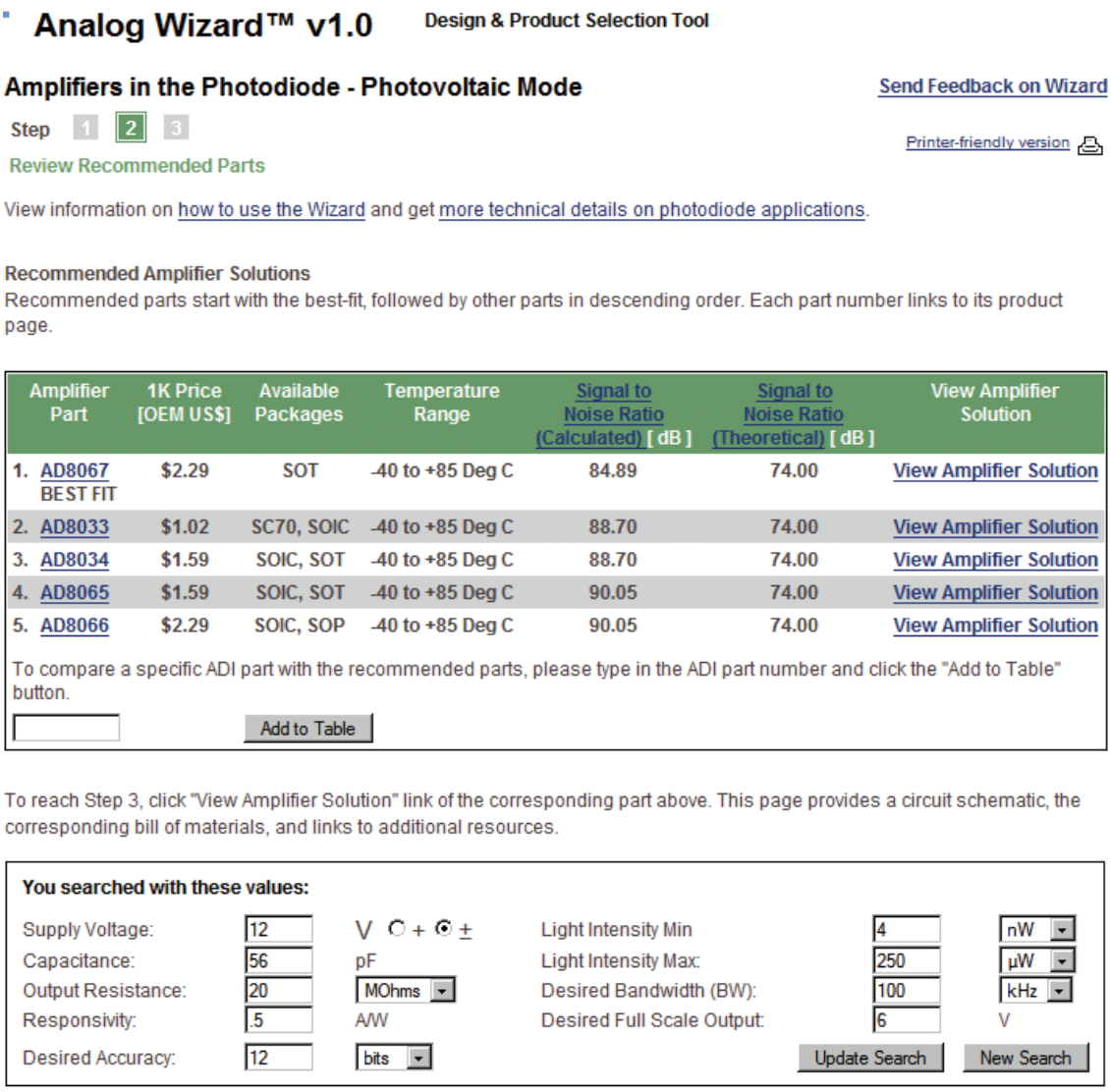


Figure 13.43: *Photodiode Wizard Second Page*

Step 3: View amplifier solution.

A suggested circuit schematic and its corresponding bill of materials is provided, based on your application requirements and the specifications of the selected amplifier. You can print this page for further reference or inclusion into a design notebook.

Analog Wizard™ v1.0 Design & Product Selection Tool

Amplifiers in the Photodiode - Photovoltaic Mode Send Feedback on Wizard

Step 1 2 3

View Amplifier Solution

Printer-friendly version

View information on how to use the Wizard and get more technical details on photodiode applications.

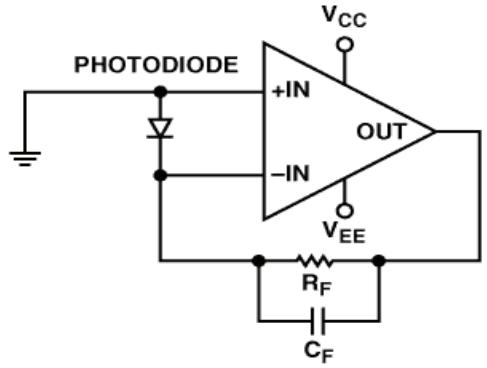
You searched with these values:

Supply Voltage:	+-12 V	Light Intensity Min & Max:	4 nW & 250 µW
Capacitance:	56 pF	Desired Bandwidth (BW):	100 k Hz
Output Resistance:	20 MOhms	Desired Full Scale Output:	6 V
Responsivity:	.5 A/W	Desired Accuracy:	12 bits

Back to Results | Edit Search | New Search

Amplifier Solution using the AD8067

Circuit schematic using the AD8067: Perform Error Analysis Noise Analysis Graph



SPICE Netlist(s)
There are no spice models for AD8067.

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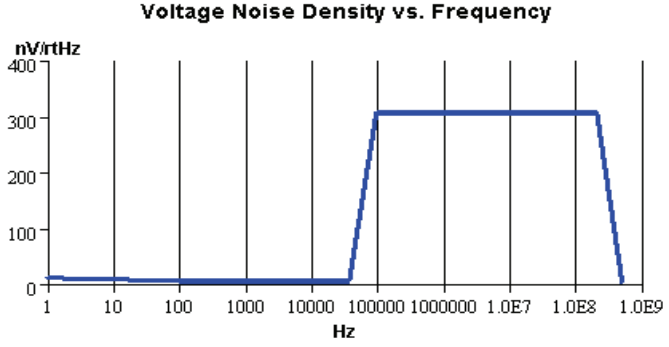
Bill of Materials - AD8067

1K Price [OEM$US]:	$2.29	Signal to Noise Ratio (Calculated):	84.89 dB
Available Packages:	SOT	Signal to Noise Ratio (Theoretical):	74 dB
Temperature Range:	-40 to 85 Deg C	Supply Voltage (Vcc):	12 V
Feedback Resistance (Rf):	0.0432 MOhms	Supply Voltage (Vee):	-12 V
Feedback Capacitance (Cf):	36.8414 pF		

Noise Analysis Graph



Additional Photodiode Resources

Application Notes:
High Impedance Sensors (pdf, 993 kb)

Figure 13.44: *Photodiode Wizard Third Page*

The Analog Filter Wizard

The last application we will look at is the Filter Design Wizard. It is designed to assist in the design, and part selection for, active filters. For a better understanding of filter applications please refer to Chapter 8, which covers active filters in detail.

Step 1: Enter the filter parameters

There are two modes of operation for the Filter Wizard. The first is the "expert" mode. In this mode the designer knows the type of filter to be designed. That is he knows that he needs, for instance, a 5^{th} order 0.5 dB Chebyshev. Otherwise, you describe the response of the filter (see Figure 13.46).

The wizard will then come back with several possible filters that will satisfy the requirements in a pull down menu. Beside the filter response pull down is a discussion that gives a brief description of the trade-offs of each of the possible choices. There is also a link to the filter section which will give a much more detailed description of each filter type.

Designing a filter is a two step process. The first is to decide what it is you want to build. This means to determine the response characteristics and order of the filter, which is what we have just done. The next step is to determine how to build it. What this means is to determine the circuit topology. Again, several choices are available in a pull down box. Next to the pull down, again, is a brief description of the circuit, with a link to a more detailed description. A schematic is also included.

Step 2: Review recommended parts.

The Wizard then suggests op amps that best fit the application performance values you entered. See Figure 13.48.

"Best-fit" is determined by the results of a parametric search of Analog Devices' product database. The order of parametric preference is: input bias current, voltage noise density, current noise density, input offset voltage, open-loop gain, and power supply voltage.

Each product number is a link to the product page. The product page provides links to the product description, data sheet, package/price, samples, and purchasing information.

Each recommendation also contains a link to the circuit schematic and bill of materials. Click "Amplifier Solution" for step 3 in the process.

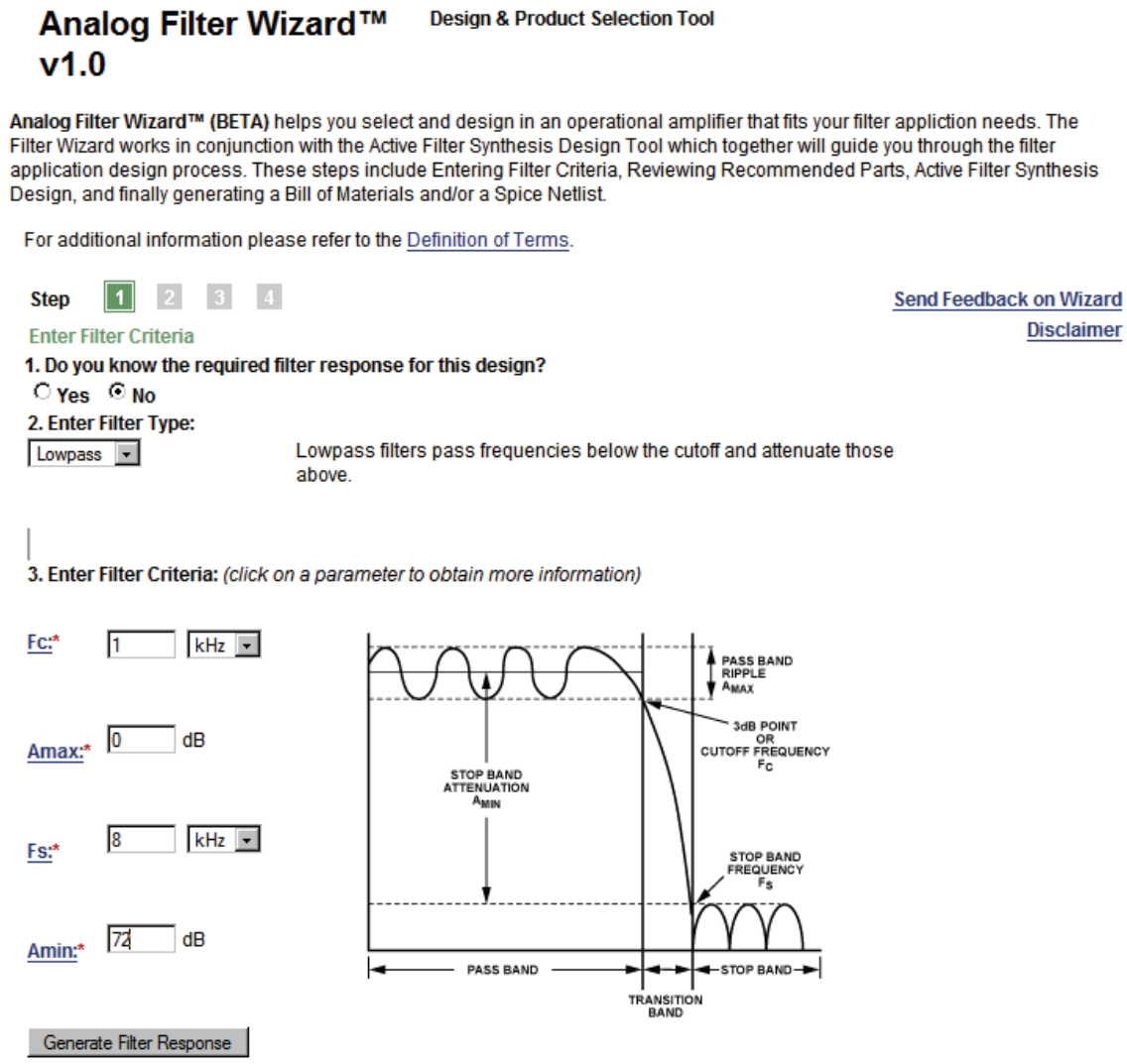


Figure 13.45: *Filter Design Wizard First Page*

4. Filter Response - Order:

< choose response/order >

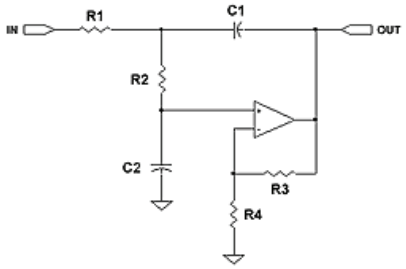
This describes the transfer function of the filter as it relates to amplitude and phase response. Standard responces that we support are Bessel, Butterworth, Chebyshev (0.01 dB to 1 dB), Equiripple (0.05° & 0.5°), Gaussian (6 dB & 12 dB). More Info (pdf, 5,434,001 bytes)

5. Enter Filter Topology:

Sallen-Key

The Sallen-Key configuration, is one of the most widely used filter topologies. This configuration shows the least dependence of filter performance on the performance of the op amp. More Info (pdf, 5,434,001 bytes)

Sallen Key Lowpass:



6. Enter Independent Variable Info:

	Parameter Name	Default Value	Your Value	
a.	Power Supply: *(Warning)* (Range: +1.8 V to ±18 V)	±15 V	single supply ○ + dual supply ◉ ± 12	V
b.	Common Mode Voltage: *(Warning)* (Range: +/- V Supply)	0	0	V
c.	Input Signal Level: (Range: 1uV to 18V)	1 V P-P	5	V P-P
d.	Gain: (Range: 1 to 100)	1	1	

Find OpAmps Reset

Figure 13.46: *Filter Design Wizard First Page (Part II)*

Once the selection of circuit topology has been made, the designer enters information on a few more variables, such as supply voltages and signal levels and the wizard then returns a selection of op amps that will work in the circuit.

Since the open loop response of an op amp is, in itself, a low-pass filter, the op amps are chosen so that the open-loop gain is large enough that the op amp response will not materially affect the response of the filter.

Once the op amp is chosen from the list provided, the designer enters the third page (see Figure 13.49). Here, the component values for the filter are determined.

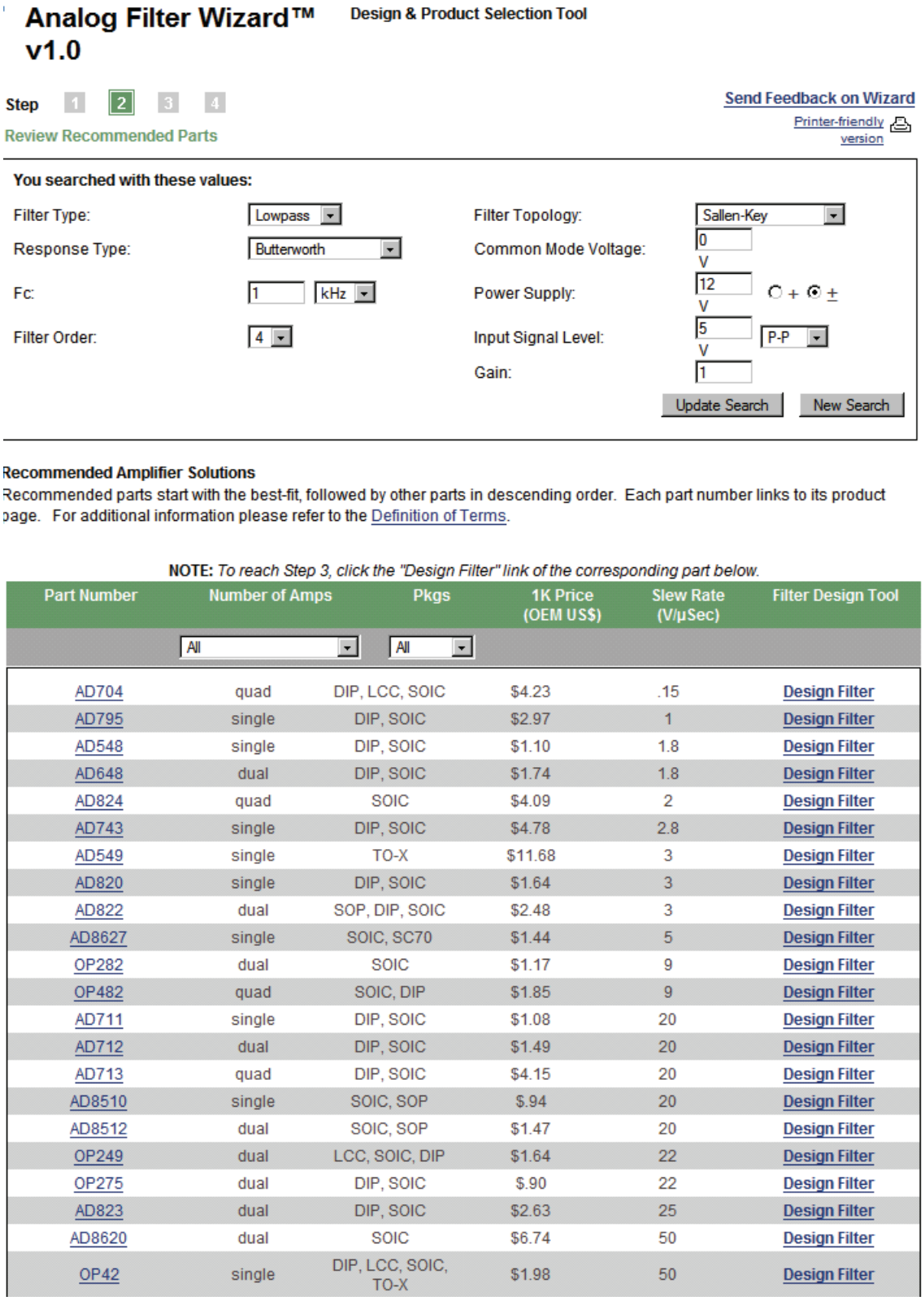
Multipole filters are made up of cascaded first order and second order sections. While it is possible to design a 3^{rd} order section with only 1 active element, the circuit value sensitivities increase, so we have limited the choices here to 1^{st} and 2^{nd} order sections.

The pertinent parameters (Fo and Q) for each of the filter section are loaded into the wizard. Since all of the component values are ratiometric, one value has to be chosen to set the rest of the variables. We typically choose a capacitor, since there are fewer choices of values than there is with resistors.

The values returned are exact values. There is the option to choose standard values (0.5% to 2% for resistors and 2% to 5% for capacitors). The designer has the ability to overwrite these values as well. Since changing the resistor and capacitor values will cause a small change in the Fo and Q of the filter. The wizard will recalculate these values and return the error introduced by going to standard values.

Once this process is completed for each section of the filter, the design is done.

The possible outputs of the wizard include magnitude and phase plots, a schematic page (see Figure 13.50), and a spice deck. With the spice deck further characterization of the filter is possible. This includes Monte-Carlo analysis of the component values and possibly including the op amp response with the filter response.



Analog Filter Wizard™ v1.0 Design & Product Selection Tool

Step 1 2 3 4

Review Recommended Parts

Send Feedback on Wizard

Printer-friendly version

You searched with these values:

Filter Type:	Lowpass	Filter Topology:	Sallen-Key
Response Type:	Butterworth	Common Mode Voltage:	0 V
Fc:	1 kHz	Power Supply:	12 V + ±
Filter Order:	4	Input Signal Level:	5 V P-P
		Gain:	1

Update Search New Search

Recommended Amplifier Solutions

Recommended parts start with the best-fit, followed by other parts in descending order. Each part number links to its product page. For additional information please refer to the Definition of Terms.

NOTE: *To reach Step 3, click the "Design Filter" link of the corresponding part below.*

Part Number	Number of Amps	Pkgs	1K Price (OEM US$)	Slew Rate (V/µSec)	Filter Design Tool
	All	All			
AD704	quad	DIP, LCC, SOIC	$4.23	.15	Design Filter
AD795	single	DIP, SOIC	$2.97	1	Design Filter
AD548	single	DIP, SOIC	$1.10	1.8	Design Filter
AD648	dual	DIP, SOIC	$1.74	1.8	Design Filter
AD824	quad	SOIC	$4.09	2	Design Filter
AD743	single	DIP, SOIC	$4.78	2.8	Design Filter
AD549	single	TO-X	$11.68	3	Design Filter
AD820	single	DIP, SOIC	$1.64	3	Design Filter
AD822	dual	SOP, DIP, SOIC	$2.48	3	Design Filter
AD8627	single	SOIC, SC70	$1.44	5	Design Filter
OP282	dual	SOIC	$1.17	9	Design Filter
OP482	quad	SOIC, DIP	$1.85	9	Design Filter
AD711	single	DIP, SOIC	$1.08	20	Design Filter
AD712	dual	DIP, SOIC	$1.49	20	Design Filter
AD713	quad	DIP, SOIC	$4.15	20	Design Filter
AD8510	single	SOIC, SOP	$.94	20	Design Filter
AD8512	dual	SOIC, SOP	$1.47	20	Design Filter
OP249	dual	LCC, SOIC, DIP	$1.64	22	Design Filter
OP275	dual	DIP, SOIC	$.90	22	Design Filter
AD823	dual	DIP, SOIC	$2.63	25	Design Filter
AD8620	dual	SOIC	$6.74	50	Design Filter
OP42	single	DIP, LCC, SOIC, TO-X	$1.98	50	Design Filter

Figure 13.47: *Filter Design Wizard Second Page*

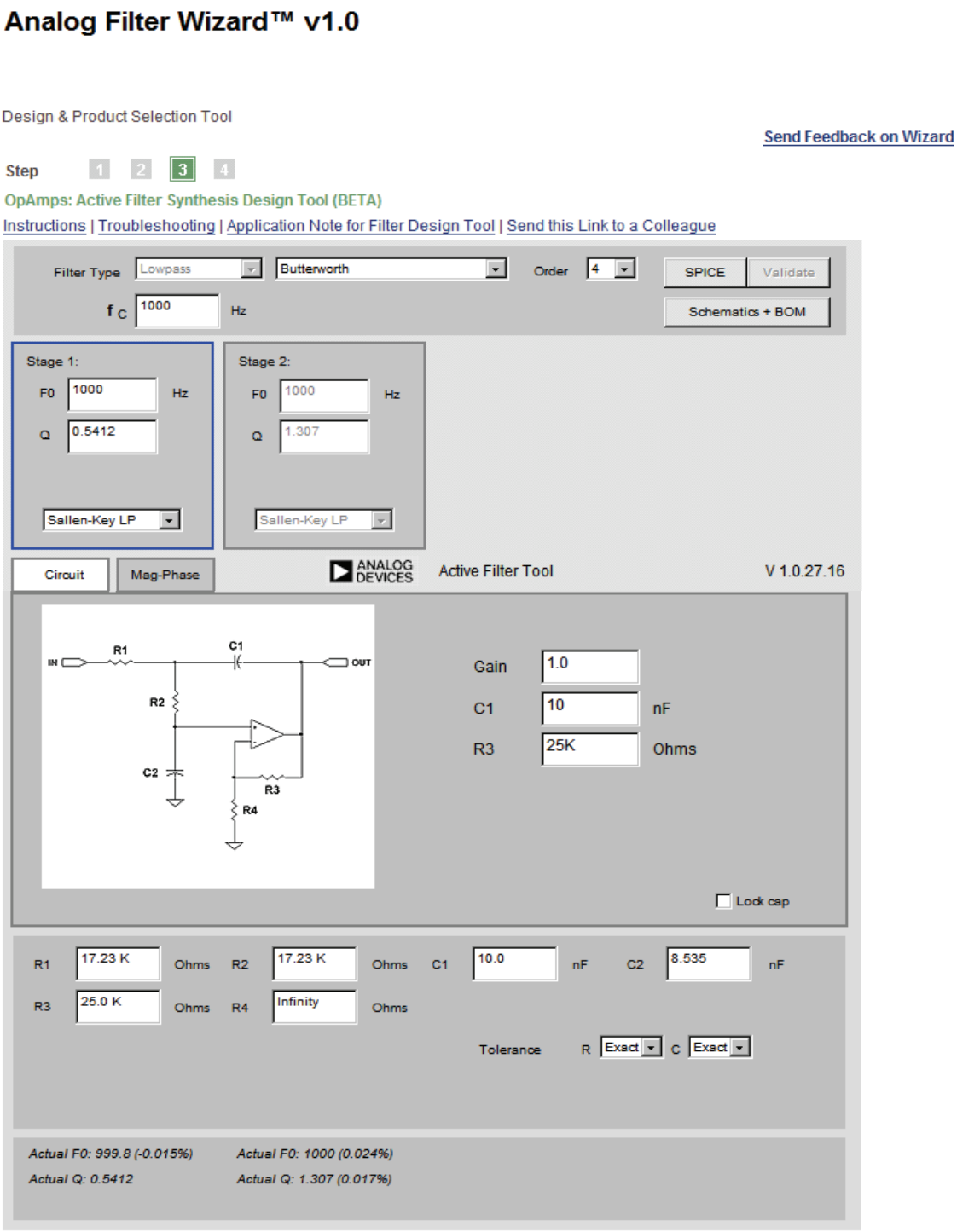


Figure 13.48: *Filter Design Wizard Third Page*

Analog Filter Wizard™ v1.0

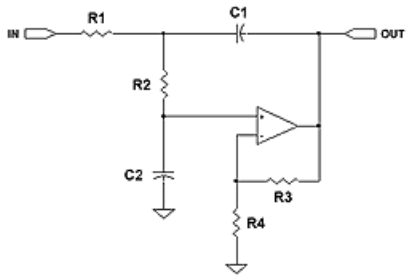
Step 1 2 3 4

Send Feedback on Wizard

Printer-friendly version

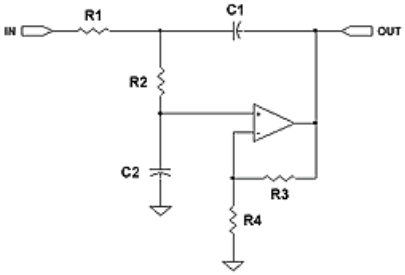
Bill of Materials

Stage 1: AD712 Sallen-Key LP



AD712
R1 1.723e4
C1 1.000e-8
R2 1.723e4
C2 8.535e-9
R3 2.500e4
R4 Inf.

Stage 2: AD712 Sallen-Key LP



AD712
R1 4.160e4
C1 1.000e-8
R2 4.160e4
C2 1.463e-9
R3 2.500e4
R4 Inf.

Figure 13.49: *Filter Design Wizard Schematic Page*

Summary

In this section we have looked at some of the online design tools provided by Analog Devices. It is, by no means an all-inclusive list, but has been designed to give an idea of the current capabilities as of 2006. Also, this is an ongoing effort, so new tools are being added all the time.

SECTION 13.3: EVALUATION BOARDS AND PROTOTYPING

Evaluation Boards

No matter how much simulation is performed, there is no substitution for actually building the circuit. The main reason for this is that it is impossible to simulate all the parasitics and other effects, such as RF interference, power, and ground issues that will exist in real world applications.

Most manufacturers of analog ICs provide *evaluation boards* usually at a nominal cost. These boards allow customers to evaluate ICs without constructing their own prototypes. Regardless of the product, the manufacturer has taken proper precautions regarding grounding, layout, and decoupling to ensure optimum device performance. Where applicable, the evaluation PCB artwork is usually made available free of charge, should a customer wish to copy the layout directly or make modifications to suit an application. A word of warning here, though, is order. An evaluation board is a small system. While some clues as to layout issues may be gleaned, blind inclusion of an evaluation board layout into a larger design may not be the answer.

General Purpose Op Amp Evaluation Boards

Evaluation boards can be either dedicated to a particular IC, or they can also be general purpose. With op amps the most universal linear IC, it is logical that evaluation boards be developed for them, to aid easy applications. However, it is also important that a good quality evaluation board avoid the parasitic effects discussed in the PC Issues chapter. An example is the general-purpose dual amplifier evaluation board of in Figure 13.50.

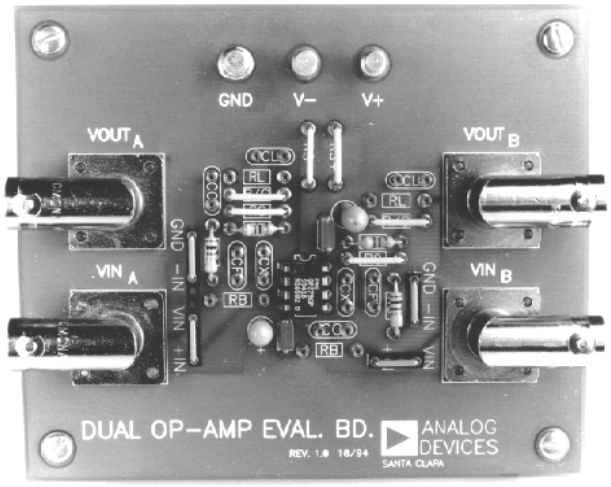


Figure 13.50: *A General-Purpose Op Amp Evaluation Board Allows Fast, Easy Configuration of Low Frequency Op Amp Circuits*

This board uses pin sockets for any standard dual op amp pinout device, and a flexible set of component jumper locations allows it to be setup for inverting or noninverting amplifiers. Various gains can be configured by choice of the component values, in either ac- or dc-coupled configurations.

The card design provides signal coupling via BNC connectors at input and output. It also uses external lab power supplies, which are wired to the lug terminals at the top. The card does, however, contain local supply voltage decoupling and bypassing components.

These general-purpose boards are intended for medium to high precision uses at frequencies below 10 MHz, with moderate op amp input currents. For higher operating speeds, a dedicated, device-specific evaluation board is likely to be a better choice. This is because the stray capacitance of the added component locations added to these boards for flexibility will be a severe limitation at higher frequencies.

Dedicated Op Amp Evaluation Boards

In high speed/high precision ICs, special attention must be given to power supply decoupling. For example, fast slewing signals driven into relatively low impedance loads produce high speed transient currents at the power supply pins of an op amp. The transient currents produce corresponding voltages across any parasitic impedance that may exist in the power supply traces. These voltages, in turn, may couple to the amplifier output, because of the op amp's finite power supply rejection at high frequencies.

The AD8001 high speed current-feedback amplifier is a case in point, and a dedicated evaluation board is available for it. A bottom side view of this SOIC board is shown in Figure 13.52. A triple decoupling scheme was chosen, to ensure a low impedance ground path at all transient frequencies. Highest frequency transients are shunted to ground by dual 1000 pF/0.01 μF ceramic chip capacitors, located as close to the power supply pins as possible to minimize series inductance and resistance. With these surface mount components, there is minimum stray inductance and resistance in the ground plane path. Lower frequency transient currents are shunted by the larger 10 μF tantalum capacitors.

The input and output signal traces of this board are 50 Ω microstrip transmission lines, as can be noted towards the right and left. Gain-set resistors are chip-style film resistors, which have low parasitic inductance. These can be seen in the center of the photo, mounted at a slight diagonal.

Note also that there is considerable continuous ground plane area on both sides of the PCB. Plated-through holes connect the top and bottom side ground planes at several points, in order to maintain lowest possible impedance and best high frequency ground continuity.

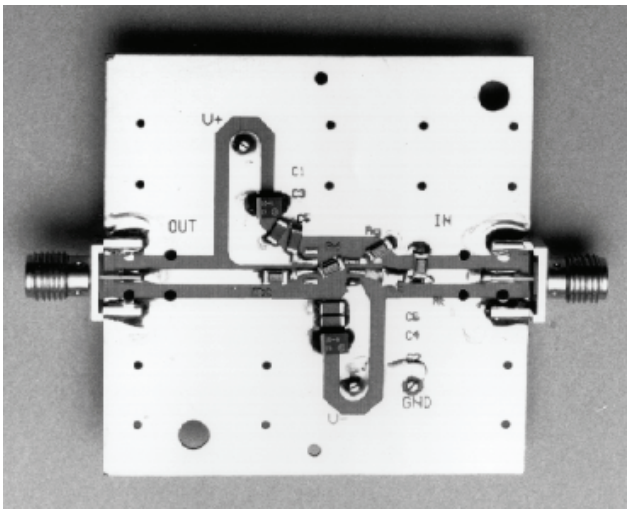


Figure 13.51: *The AD8001 Requires a Dedicated Evaluation Board*

Input and output connections to the card are provided via the SMA connectors as shown, which terminate the input/output signal transmission lines. The board's power connection from external lab supplies is made via solder terminals, which are seen at the ends of the broad supply line traces.

Some of these points are more easily seen in a topside view of the same card, which is shown in Figure 13.51. This AD8001 evaluation board is a noninverting signal gain stage, optimized for lowest parasitic capacitance. The cutaway area around the SOIC outline of the AD8001 provides lowest stray capacitance, as can be noted in this view.

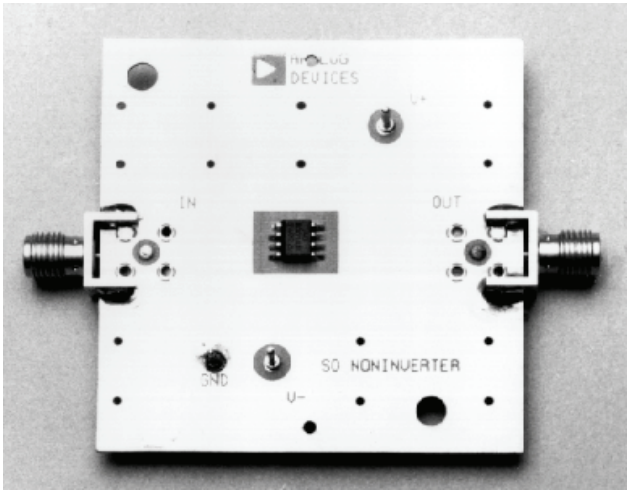


Figure 13.52: *The AD8001 Evaluation Board Top View*

In this view is also seen the virtually continuous ground plane and the multiple vias, connecting the top/bottom planes.

Data Converter Evaluation Boards

A well designed manufacturers' evaluation board can also be a powerful tool that can greatly simplify the integration of an ADC or DAC into a system. Probably the best feature of an evaluation board is that its layout is designed to optimize the performance of the data converter, so that the performance of the converter, not the performance of the PC board it is attached to sets the performance limits of the system. Analog Devices provides a complete electrical schematic and parts list as well a PC board layout of its evaluation boards on the data sheet for most ADCs and DACs. Each layer of the multilayer board is also shown, and Analog Devices will supply the CAD layout files (Gerber format) for the board if needed. Many system level problems related to layout can be avoided simply by studying the evaluation board layout and using it as a guide in the system board layout—perhaps even copying critical parts of the layout directly if needed. Again a warning is in order that blindly incorporating the design of an evaluation board into a larger system may not give satisfactory performance. A system must be viewed as a complete system, not a collection of individual subcircuits.

ADC and DAC evaluation boards typically have input/output connectors for the analog, digital, and power interfaces to facilitate interfacing with external test equipment. Any required support circuitry such as voltage references, crystal oscillators for clock generation, etc., are generally included as part of the board.

Many modern data converters have a considerable amount of on-chip digital logic for controlling various modes of operation, including gain, offset, calibration, data transfer, etc. These options are set by loading the appropriate words into internal control registers, usually via a serial port. In some converters, especially sigma-delta ADCs, just setting the basic options requires considerable knowledge of the internal control registers and the interface. For this reason, most ADC/DAC evaluation boards have interfaces (parallel, serial, or USB) and software to allow easy menu-driven control of the various internal options from an external PC. In many cases, configuration files created in the evaluation software can be downloaded into the final system design.

Figure 13.53 shows the evaluation board for the AD7730 24-bit bridge transducer sigma-delta ADC. This ADC has an on-chip PGA and is designed to interface directly to a variety of bridge transducers. A load cell with a 10-mV full-scale output can be connected directly to the ADC input, and the output is read by the PC via the parallel port interface. The evaluation board software allows the system designer to see the effects of sample rate, gain, filter bandwidth, and output data averaging on the overall effective resolution. The software also provides histogram displays for direct evaluation of system noise.

In reality, the evaluation board is actually an evaluation system, composed of the actual board, interconnection cables, required power supply, and the software to operate from a host PC.

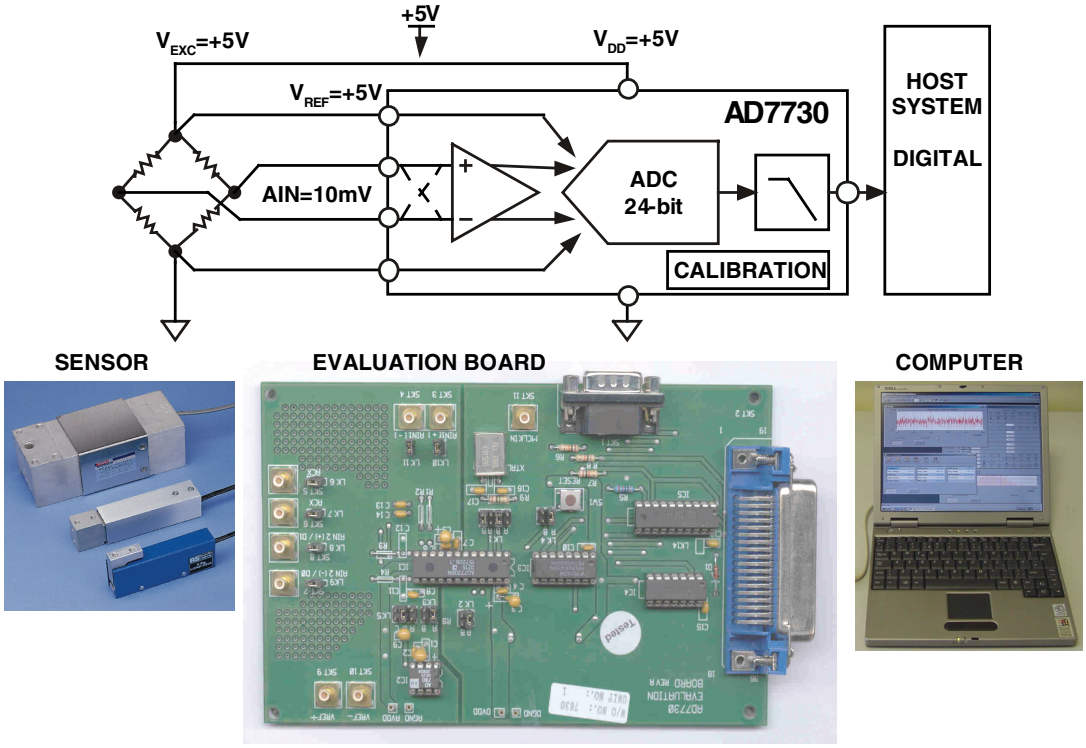


Figure 13.53: *AD7730 Measurement ADC Evaluation System*

Figure 13.54 shows the evaluation board for the AD5535 32-channel 14-bit high voltage DAC. The evaluation board interfaces with an external PC via a parallel port connector. The software provided with the board allows data to be easily loaded into the individual DAC registers via the 3-wire serial interface.

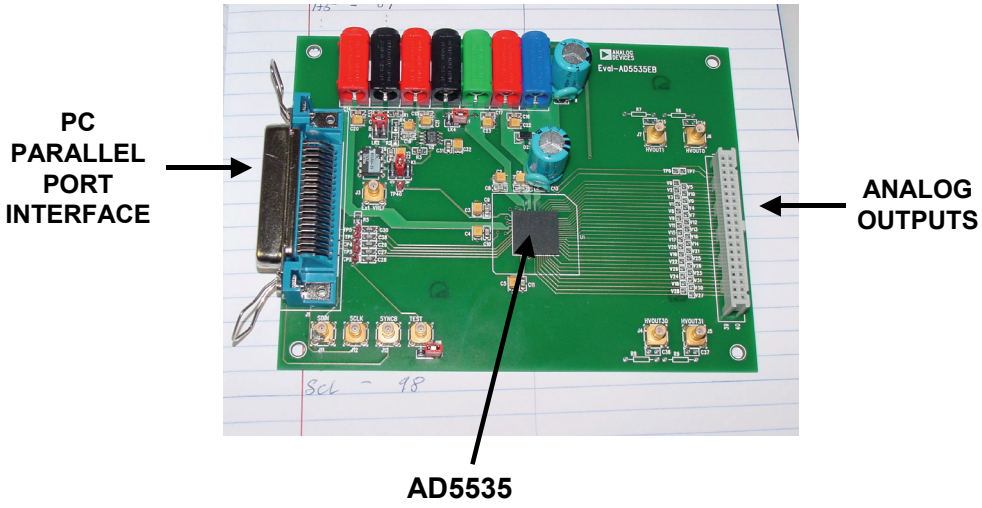


Figure 13.54: *AD5535 32-Channel, 14-Bit, 200 V Output DAC Evaluation Board*

High Speed FIFO Evaluation Board System

Figure 13.55 shows an ADC evaluation board for the AD7450 12 bit, 1 MSPS ADC connected to an Evaluation/Control board. The ADC evaluation board (right side of diagram) is product-specific, but the evaluation/control board interfaces to a variety of ADC evaluation boards has an on-board 16-bit buffer memory and control logic which interfaces to a PC via the parallel port. The software provided includes an FFT routine which allows evaluating the ADC under dynamic conditions. The evaluation/control board can handle ADCs with sampling rates up to several MHz.

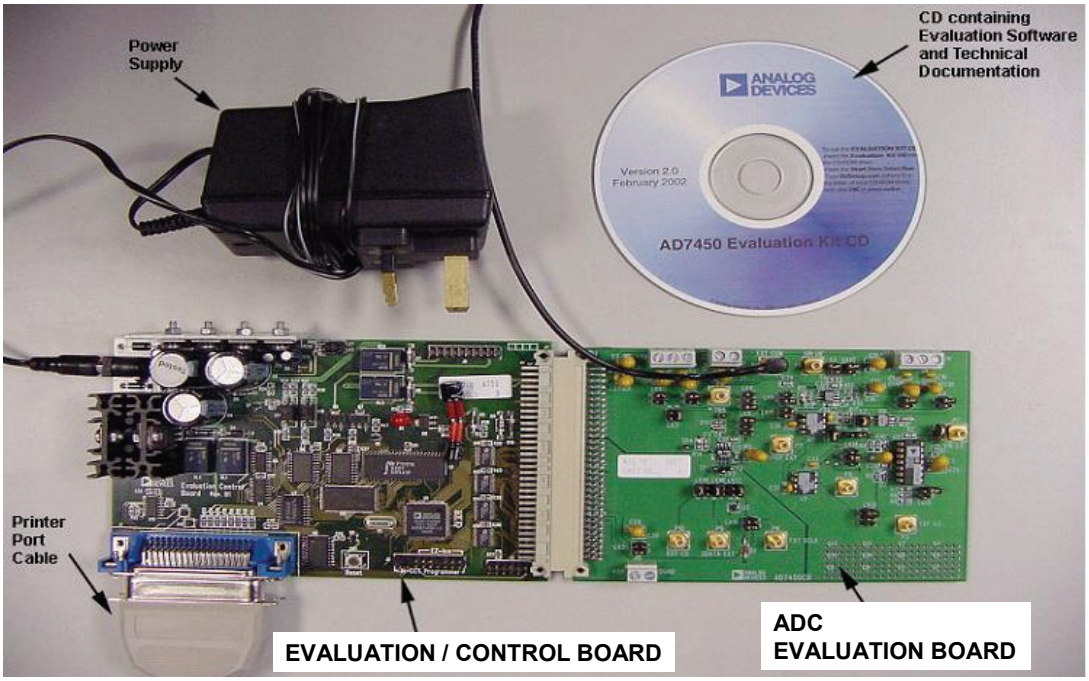


Figure 13.55: *Evaluation/Control Board and ADC Evaluation Board for ADCs*

Figure 13.56 shows Analog Devices' high speed ADC FIFO evaluation kit which interfaces to a variety of high speed ADC evaluation boards. The high speed ADC FIFO evaluation kit includes the latest version of ADC Analyzer and a memory board to capture blocks of digital data from Analog Devices' high speed analog-to-digital converter (ADC) evaluation boards. This FIFO board can be connected to a PC through a USB port (older version used a parallel port connection) and used with ADC Analyzer to evaluate the performance of high speed ADCs quickly. Users can view an FFT for a specific analog input and encode rate and analyze SNR, SINAD, SFDR, and harmonic information.

The evaluation kit is easy to set up. Additional equipment needed includes an Analog Devices' high speed ADC evaluation board (specific to the part type to be evaluated), a

power supply, a signal source, and a clock source. Once the kit is connected and powered, the evaluation is enabled instantly on the PC.

Two versions of the FIFO are available. The HSC-ADC-EVALA-DC is used with dual ADCs and converters with demultiplexed digital outputs. The HSC-ADC-EVALA-SC evaluation board is used with single-channel ADCs. Dual ADCs are typically used in systems where, for instance, in-phase, and quadrature modulation schemes are to be received and demodulated

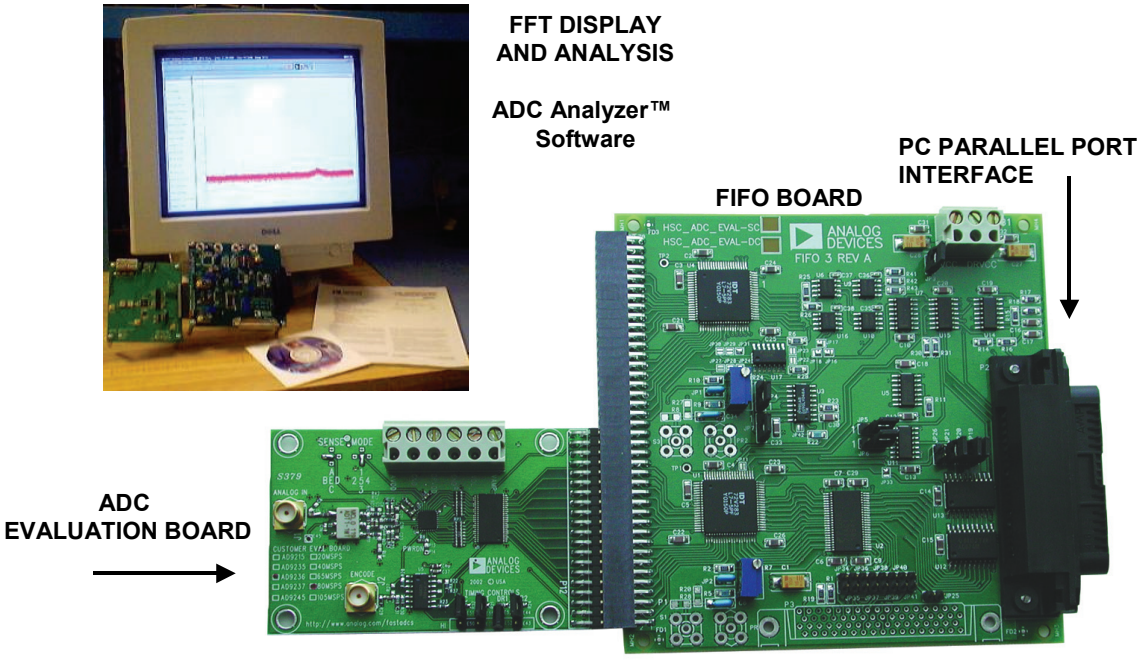


Figure 13.56: *Analog Devices' High Speed ADC FIFO Evaluation Kit*

FIFO Board Theory of Operation

The FIFO evaluation board can be divided into several circuits, each of which plays an important part in acquiring digital data from the ADC and allows the PC to upload and process that data. The evaluation kit is based around a chip. The system can acquire digital data at speeds up to 133 MSPS and data record lengths up to 32 kB using the HSC-ADC-EVALA-SC FIFO evaluation kit. The HSC-ADC-EVALA-DC, which has two FIFO chips, is available to evaluate dual ADCs or demultiplexed data from ADCs sampling faster than 133 MSPS. A USB 2.0 microcontroller communicating with ADC Analyzer allows for easy interfacing to newer computers using the USB 2.0 (USB 1.1 compatible) interface.

The process of filling the FIFO chip(s) and reading the data back requires several steps. First, ADC Analyzer initiates the FIFO chip(s) fill process. The FIFO chip(s) are reset

using a master reset signal (MRS). The USB Microcontroller then is suspended, which turns off the USB oscillator, ensuring that it does not add noise to the ADC input. After the FIFO chip(s) completely fill, the full flags from the FIFO chip(s) send a signal to the USB microcontroller to wake up the microcontroller from suspend. ADC Analyzer waits for approximately 30 ms and begins the readback process.

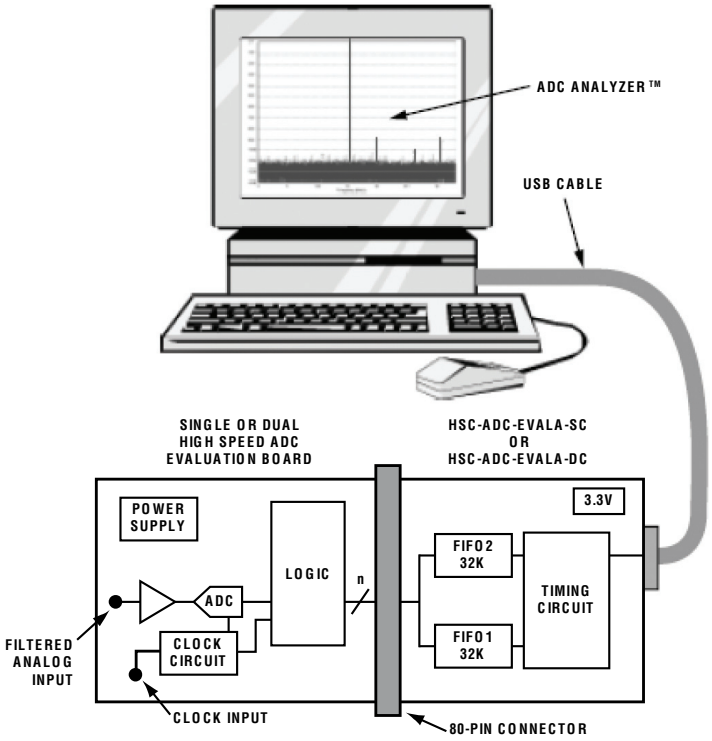


Figure 13.57: ADC FIFO Evaluation Board Evaluation Kit Simplified Functional Block Diagram

During the readback process, the acquisition of data from FIFO 1 (U201) or FIFO 2 (U101) is controlled via the signals OEA and OEB. Because the data outputs of both FIFO chips drive the same 16-bit data bus, the USB microcontroller controls the OEA and OEB signals to read data from the correct FIFO chip. From an application standpoint, ADC Analyzer sends commands to the USB microcontroller to initiate a read from the correct FIFO chip, or both FIFO chips in dual or interleaved mode.

Clocking Description

Each channel of the buffer memory requires a clock signal to capture data. These clock signals are normally provided by the ADC evaluation board and are passed along with the data through Connector J104/204 (Pin 37 for both Channel 1 and Channel 2). If only a single clock is passed for both channels, they can be connected together by a jumper.

Jumpers at the output of the LVDS receiver allow the output clock to be inverted by the LVDS receiver. By default, the clock outputs are inverted by the LVDS receiver.
The single-ended clock signal from each data channel is buffered and converted to a differential CMOS signal by two gates of a low voltage differential signal (LVDS) receiver. This allows the clock source for each channel to be CMOS, TTL, or ECL. The clock signals are ac-coupled by 0.1 µF capacitors. Potentiometers allow for fine tuning the threshold of the LVDS gates. In applications where fine-tuning the threshold is critical, these potentiometers may be replaced with a higher resistance value to increase the adjustment range. Resistors set the static input to each of the differential gates to a dc voltage of approximately 1.5 V.

At assembly, solder Jumpers J310–J313 are set to bypass the potentiometer. For fine adjustment using the pot, the solder jumpers must be removed.

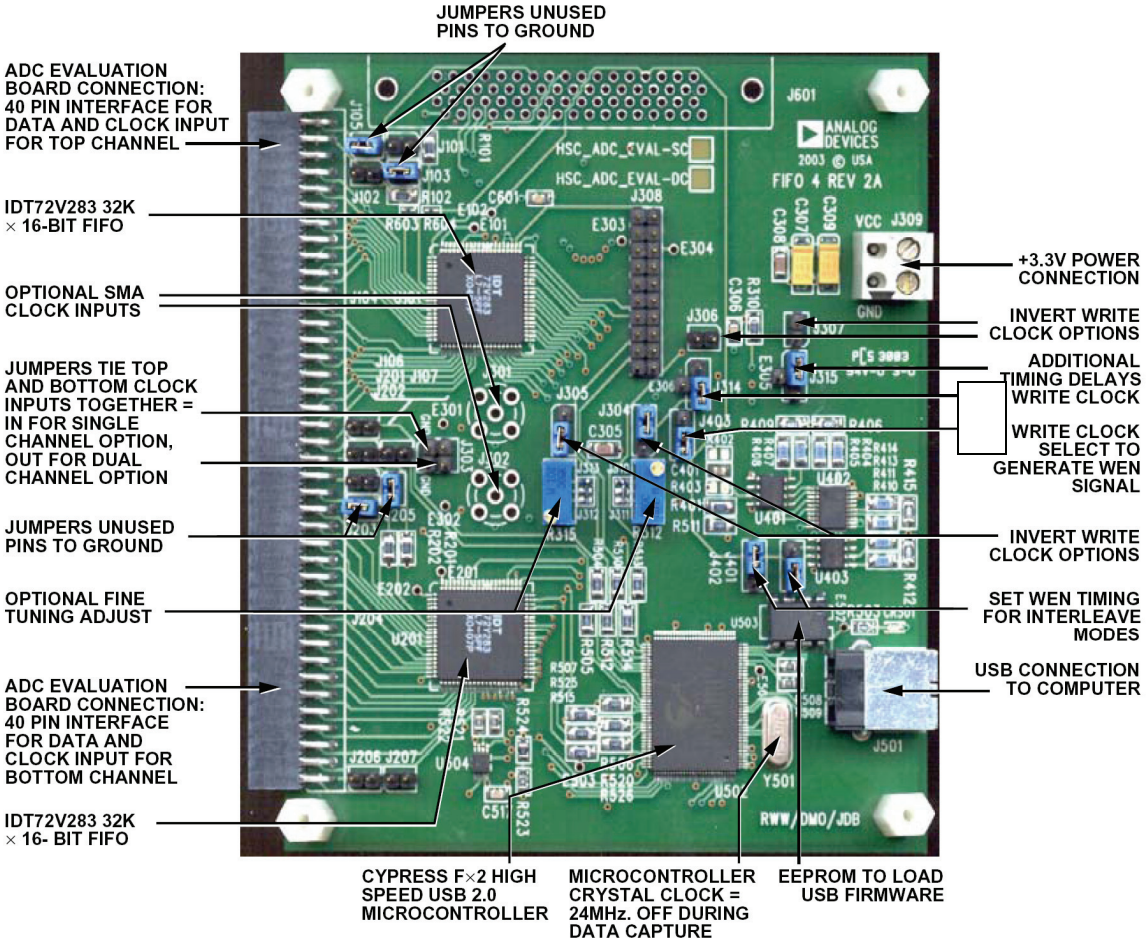


Figure 13.58: *ADC FIFO Evaluation Kit*

An XOR gate array, is included in the design to let users add gate delays to the FIFO memory chips clock paths. They are not required under normal conditions and are bypassed at assembly by jumpers. Jumpers also allow the clock signals to be inverted through an XOR gate. In the default setting, the clocks are not inverted by the XOR gate.

The clock paths described above determine the WRT_CLK1 and WRT_CLK2 signals at each FIFO memory chip. The timing options above should let you choose a clock signal that meets the setup and hold time requirements to capture valid data.

A clock generator can be applied directly to S1 and/or S3. This clock generator should be the same unit that provides the clock for the ADC. These clock paths are ac-coupled, so that a sine wave generator can be used. DC bias can be adjusted by. Note that J301 and J302 (SMA connectors) and R301, R302, R305, and R306 (the Bias setting resistors) are not installed at the factory and must be installed by the user.

The differential line receiver is used to square the clock signal levels applied externally to the FIFO evaluation board. The output of this clock receiver can either directly drive the write clock of the FIFO(s), or first pass through the XOR gate timing circuitry described above.

Clocking With Interleaved Data

ADCs with very high data rates may exceed the capability of a single buffer memory channel (~133 MSPS). These converters often demultiplex the data into two channels to reduce the rate required to capture the data. In these applications, ADC Analyzer must interleave the data from both channels to process it as a single channel. The user can configure the software to process the first sample from Channel 1, the second from Channel 2, and so on, or vice versa. The synchronization circuit included in the buffer memory forces a small delay between the write enable signals (WENA and WENB) to the FIFO memory chips (Pin 1, U101, and U201), ensuring that the data is captured in one FIFO before the other. Jumpers J401 and J402 determine which FIFO receives WENA and which FIFO receives WENB.

Controller for Precision ADCs

The Evaluation Board Controller is the main component in a complete self-contained evaluation and demonstration system for Analog Devices Precision Converters. The block diagram shown below indicates the major blocks of the Evaluation Board Controller. It is a complete unit allowing the PC to communicate with a range of evaluation boards supplied by Analog Devices via a high speed parallel data link. Software is provided to allow the user to send commands to the evaluation board and read data samples or on-board registers for the device being evaluated.

The Evaluation Board Controller connects to the evaluation board via a 96-pin edge connector. The pinout of the connector is a standard format which is consistent between evaluation boards.

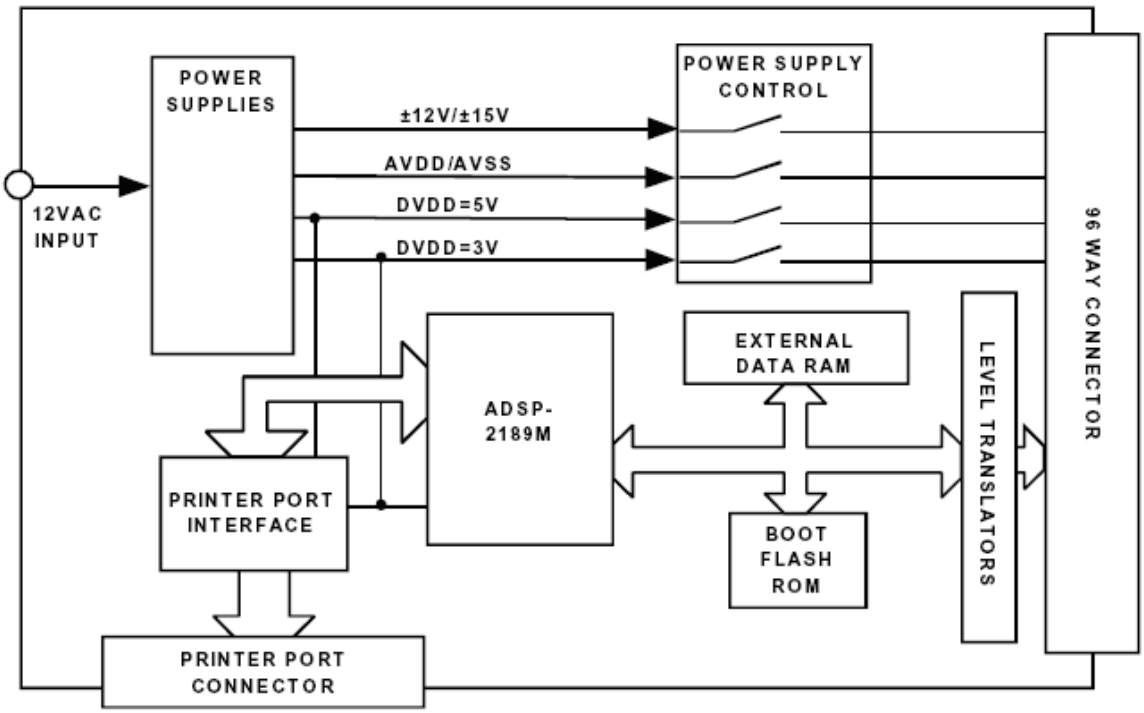


Figure 13.59: *Precision ADC Controller/Evaluation Board Functional Block Diagram*

The system allows speedy demonstration and evaluation of Analog Devices Precision Converter Products, allowing the user to directly test the device in question and to shorten the time required to develop their own software and hence speed up their design process.

Hardware Description

The Evaluation Board Controller is based around an ADSP-2189M Digital Signal Processor (DSP). The DSP runs from a 20 MHz crystal and an on-chip clock doubler gives an instruction speed of 40 MIPS. The DSP features 32K words of Internal Program Ram and 48K words of internal Data RAM. The Data RAM is supplemented with 64K words of external data RAM. The DSP also provides two Serial Ports (SPORTs) which have a maximum output serial clock rate of 20 MHz. Both SPORTs are available on the 96 way edge connector as is a section of the parallel Data and Address bus.

To facilitate operation of both 3 V and 5 V evaluation boards all logic signal are equipped with level translators. For 3 V devices no level translation is required (since the DSP operates from 3 V) so the level translators act as closed switches. For 5 V devices all logic 1 signals coming from the DSP are level translated to 5 V. 5 V logic signals coming from the device under test are translated to 3 V by the translators before reaching the DSP.

Communications

The Evaluation Board Controller allows a user to gather a large number of samples from an evaluation board and upload them to the PC for analysis. The Evaluation Board Controller uses a high speed interface based around the PCs Printer Port. As the port is used both for sending and receiving data it must have bidirectional capability. Most PCs (particularly the Pentium class) have this facility as standard but it is possible to check in the PCs BIOS. How the BIOS is viewed depends on the make of PC being used but typical methods are pressing CTRL, ALT, and ENTER during power up. The user should consult the operating manual of their PC for further details. Suitable printer port types may be described as bidirectional, PS/2, EPP, or ECP.

Power Supplies

The Evaluation Board Controller has its own on-board power supplies which are derived from a 12 VAC power supply with a 1 A current capability. These supplies are used to supply the current for the Evaluation Board Controller itself as well as that required for the evaluation board and are available from Analog Devices. The power supplies which go to the evaluation board via the edge connector are fully controllable by the software supplied. The Evaluation Board Controller can provide ±3 V or ±5 V analog supplies as well as a +3 V or +5 V digital supply. There is also a ±12 V / ±15 V supply for powering op amps, etc. The value of the supplies is selected by jumpers LK1 and LK2.

Output Connector

The 96-pin edge connector provides connection to all the available power supplies, serial ports and data/address buses required to operate the range of Analog Devices evaluation boards which are compatible with this system.

Software

The Evaluation Board Controller comes supplied with a CD which contains software for previously released evaluation boards. Therefore if the user has an evaluation board which was compatible with the previous version of the Controller (Eval Control Board), they will be able to use the Evaluation Board Controller as well.

When the user purchases a new evaluation board kit, it will contain all the software necessary to operate that particular evaluation board. The most up-to-date evaluation software is always available on the Analog Devices web site (www.analog.com). The documentation which is supplied with the evaluation board also contains information about installing the software, as well as a detailed description of the evaluation board and a data sheet for the device in question.

All software supplied for the Evaluation Board Controller and evaluation boards comes on a CD ROM. When the CD is inserted into the PC, an installation program will automatically begin. This program will install the evaluation software onto the user's machine and will also install the Technical Note for the evaluation board as well as the Data Sheet for the device in questions. All literature on the CD is in Adobe's Portable Document Format (PDF) and will require Acrobat Reader to be viewed or printed.

Prototyping

There are times when an evaluation board is not available for parts of a circuit design. In that case a breadboard may be required.

A basic principle of a breadboard or a prototype structure is that it is a *temporary* one, designed to test the performance of an electronic circuit or system. By definition it must therefore be easy to modify.

There are many commercial prototyping systems, but unfortunately for the analog designer, almost all of them are designed for prototyping *digital* systems. In such environments, noise immunities are hundreds of millivolts or more. Prototyping methods commonly used include non-copper-clad Matrix board, Vectorboard, wire-wrap, and plug-in breadboard systems. Quite simply, these all are unsuitable for high performance or high frequency analog prototyping, because of their excessively high parasitic resistance, inductance, and capacitance levels. Even the use of standard IC sockets is inadvisable in many prototyping applications (more on this, below).

One of the more important considerations in selecting a prototyping method is the requirement for a large-area ground plane. This is required for high frequency circuits as well as low speed precision circuits, especially when prototyping circuits involving ADCs or DACs. The differentiation between *high speed* and *high precision* mixed-signal circuits is difficult to make. For example, 16+ bit ADCs (and DACs) may operate on high speed clocks (>10 MHz) with rise and fall times of less than a few nanoseconds, while the effective throughput rate of the converters may be less than 100 kSPS. Successful prototyping of these circuits requires that equal (and thorough) attention be given to good high speed and high precision circuit techniques.

Deadbug Prototyping

A simple technique for analog prototyping uses a solid copper-clad board as a ground plane. In this method, the ground pins of the ICs are soldered directly to the plane, and the other components are wired together above it. This allows HF decoupling paths to be very short indeed. All lead lengths should be as short as possible, and signal routing should separate high level and low level signals. Connection wires should be located close to the surface of the board to minimize the possibility of stray inductive coupling. In most cases, Parallel runs should not be "bundled" because of possible coupling. Ideally the layout (at least the relative placement of the components on the board) should be similar to the layout intending to be used on the final PCB. This approach is often referred to as *deadbug* prototyping, because the ICs are often mounted upside down with their leads up in the air (with the exception of the ground pins, which are bent over, and soldered directly to the ground plane). The upside-down ICs look like deceased insects, hence the name.

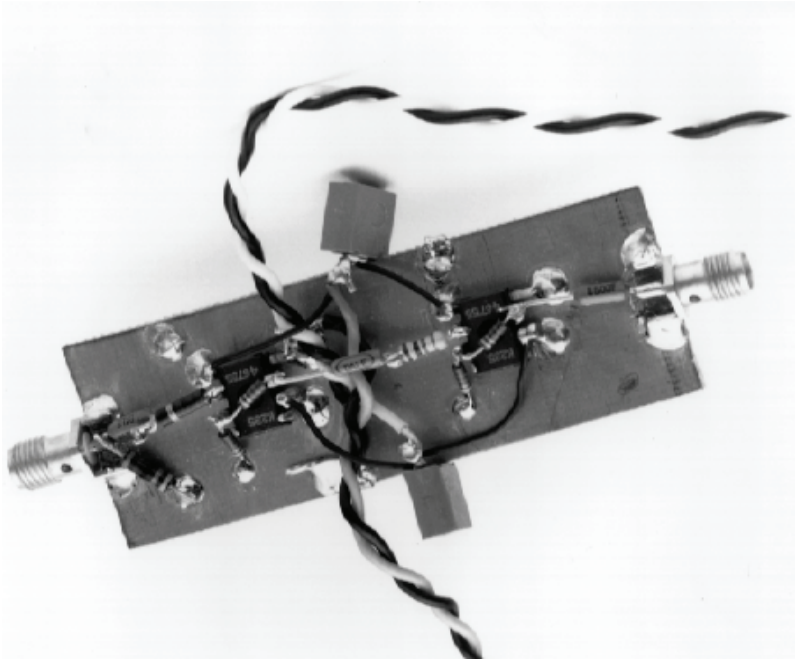


Figure 13.60: *A "Deadbug" Analog Breadboard*

Figure 13.60 shows a hand-wired "deadbug" analog breadboard. This circuit uses two high speed op amps, and in fact gives excellent performance in spite of its lack of esthetic appeal. The IC op amps are mounted upside down on the copper board with the leads bent over. The signals are connected with short point-to-point wiring. The characteristic impedance of a wire over a ground plane is about 120 Ω, although this may vary as much as ±40% depending on the distance from the plane. The decoupling capacitors are connected directly from the op amp power pins to the copper-clad ground plane. When working at frequencies of several hundred MHz, it is a good idea to use only one side of the board for ground. Many people drill holes in the board and connect the sides together by soldering short pieces of wire. If care isn't taken, this may result in unexpected ground loops between the two sides of the board, especially at RF frequencies.

Pieces of copper-clad board may be soldered at right angles to the main ground plane to provide screening, or circuitry may be constructed on both sides of the board (with through-hole connections) with the board itself providing screening. For this, the board will need corner standoffs to protect underside components from being crushed.

When the components of a breadboard of this type are wired point-to-point in the air (a type of construction strongly advocated by Bob Pease and sometimes known as "bird's nest" construction) there is always the risk of the circuitry being crushed and resulting short-circuits. Also, if the circuitry rises high above the ground plane, the screening effect of the ground plane is diminished, and interaction between different parts of the circuit is more likely. Nevertheless, the technique is very practical and widely used because the

circuit may easily be modified (this of course assumes the person doing the modifications is adept with soldering techniques).

Another prototype breadboard variation is shown in Figure 13.61. Here the single sided, copper-clad board has pre-drilled holes on 0.1" centers. Power busses are used at the top and bottom of the board. The decoupling capacitors are used on the power pins of each IC. Because of the loss of copper area due to the predrilled holes, this technique does not provide as low a ground impedance as a completely covered copper-clad board of Figure 13.60, so be forewarned.

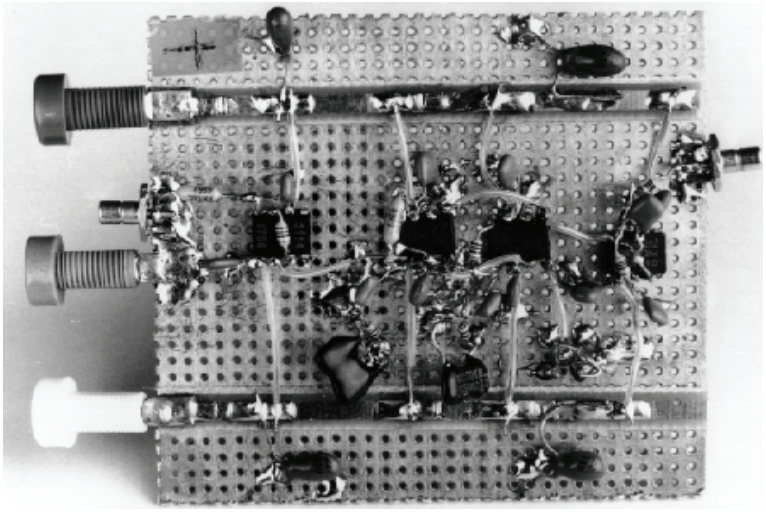


Figure 13.61: *"A Deadbug" Prototype Using 0.1" Pre-Drilled Single-Sided, Copper-Clad Printed Board Material*

In a variation of this technique, the ICs and other components are mounted on the noncopper-clad side of the board. The holes are used as vias, and the point-to-point wiring is done on the copper-clad side of the board. Note that the copper surrounding each hole used for a via must be drilled out, to prevent shorting. This approach requires that all IC pins be on 0.1" centers. For low frequency circuits, low profile sockets can be used, and the socket pins then will allow easy point-to-point wiring.

The obvious problem with this method of prototyping is that it is much more difficult to perform with surface mount components.

Solder-Mount Prototyping

There is a commercial breadboarding system which has most of the advantages of the above techniques (robust ground, screening, ease of circuit alteration, low capacitance and low inductance) and several additional advantages: it is rigid, components are close to the ground plane, and where necessary, node capacitances and line impedances can be calculated easily. This system is made by Wainwright Instruments and is available in

Europe as "Mini-Mount" and in the USA (where the trademark "Mini-Mount" is the property of another company) as "Solder-Mount."

Solder-Mount consists of small pieces of PCB with etched patterns on one side and contact adhesive on the other. These pieces are stuck to the ground plane, and components are soldered to them. They are available in a wide variety of patterns, including ready-made pads for IC packages of all sizes from 8-pin SOICs to 64-pin DILs, strips with solder pads at intervals (which intervals range from 0.040" to 0.25", the range includes strips with 0.1" pad spacing which may be used to mount DIL devices), strips with conductors of the correct width to form microstrip transmission lines (50 Ω, 60 Ω, 75 Ω, or 100 Ω) when mounted on the ground plane, and a variety of pads for mounting various other components. Self-adhesive tinned copper strips and rectangles (LO-PADS) are also available as tie-points for connections. They have a relatively high capacitance to ground and therefore serve as low inductance decoupling capacitors. They come in sheet form and may be cut with a knife or scissors.

The main advantage of Solder-Mount construction over "bird's nest" or "deadbug" is that the resulting circuit is far more rigid, and, if desired, may be made far smaller (the latest Solder-Mounts are for surface-mount devices and allow the construction of breadboards scarcely larger than the final PCB, although it is generally more convenient if the prototype is somewhat larger). Solder-Mount is sufficiently durable that it may be used for small quantity production as well as prototyping.

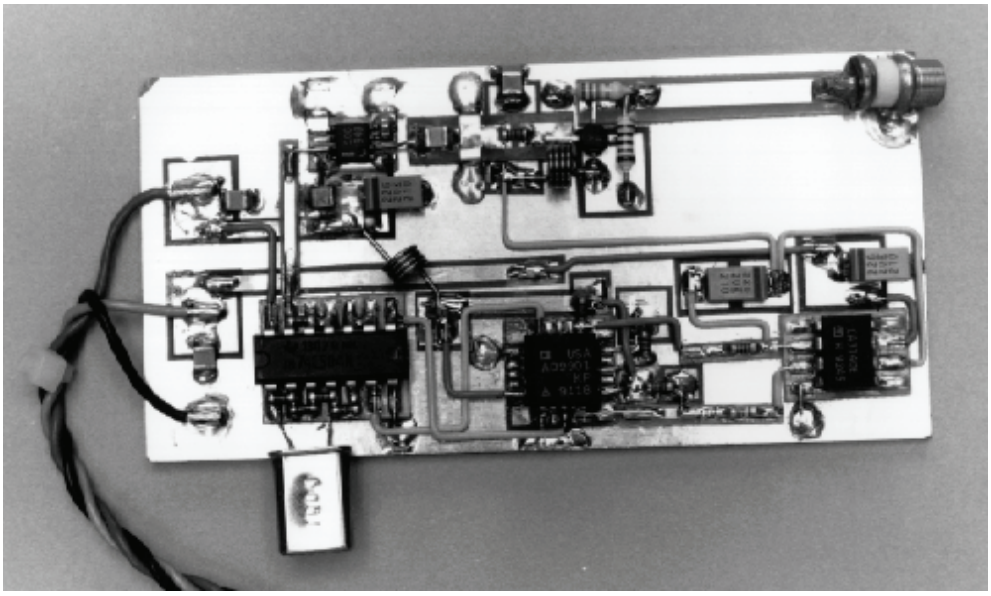


Figure 13.62: *A "Solder-Mount" Constructed Prototype Board*

Figure 13.62 shows an example of a 2.5 GHz phase-locked loop prototype, built with Solder-Mount techniques. While this is a high speed circuit, the method is equally suitable for the construction of high resolution low frequency analog circuitry.

A particularly convenient feature of Solder-Mount at VHF is the relative ease with which transmission lines can be formed. As noted earlier, if a conductor runs over a ground plane, it forms a microstrip transmission line. The Solder-Mount components include strips which form microstrip lines when mounted on a ground plane (they are available with impedances of 50 Ω, 60 Ω, 75 Ω, and 100 Ω). These strips may be used as transmission lines for impedance matching, or alternately, more simply as power buses. Note that glass fiber/epoxy PCB is somewhat lossy at VHF/UHF, but losses will probably be tolerable if microstrip runs are short.

Milled PCB Prototyping

Both "deadbug" and "Solder-Mount" prototypes become tedious for complex analog circuits, and larger circuits are better prototyped using more formal layout techniques.

There is a prototyping approach that is but one step removed from conventional PCB construction, described as follows. This is to actually lay out a double-sided board, using conventional CAD techniques. PC-based software layout packages offer ease of layout as well as schematic capture to verify connections. Although most layout software has some degree of auto-routing capability, this feature is best left to digital designs. The analog traces and component placements should be done by hand, following the rules discussed elsewhere in this chapter. After the board layout is complete, the software verifies the connections per the schematic diagram net list.

Many designers find that they can make use of CAD techniques to lay out simple boards. The result is a pattern generation tape (or Gerber file) which would normally be sent to a PCB manufacturing facility where the final board is made.

Rather than use a PCB manufacturer, however, automatic drilling and milling machines are available which accept the PG tape directly. An example of such a prototype circuit board is shown in Figure 13.63 (top view).

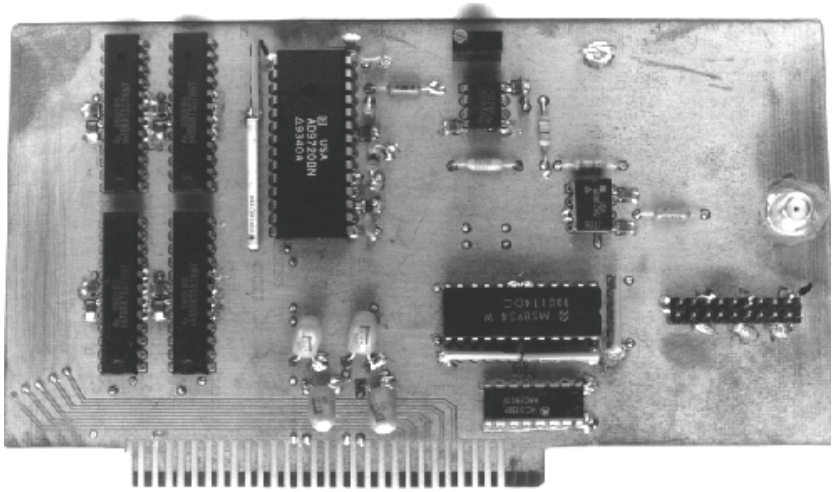


Figure 13.63: *A Milled Circuit Construction Prototype Board (top view)*

These systems produce either single or double-sided circuit boards directly, by drilling all holes, and using a milling technique to remove conductive copper, thus creating the required insulation paths, and finally, the finished prototype circuit board. The result can be a board functionally quite similar to a final manufactured double-sided PCB.

However, it should be noted that a chief caveat of this method is that there is no "plated-through" hole capability. Because of this, any conductive "vias" required between the two layers of the board must be manually wired and soldered on both sides.

Minimum trace widths of 25 mils (1 mil = 0.001"), and 12 mil spacing between traces are standard, although smaller trace widths can be achieved with care. The minimum spacing between lines is dictated by the size of the milling bit used, typically 10 mils to 12 mils.

A bottom-side view of this same milled prototype circuit board is shown in Figure 13.64. The accessible nature of the copper pattern allows access to the traces for modifications.

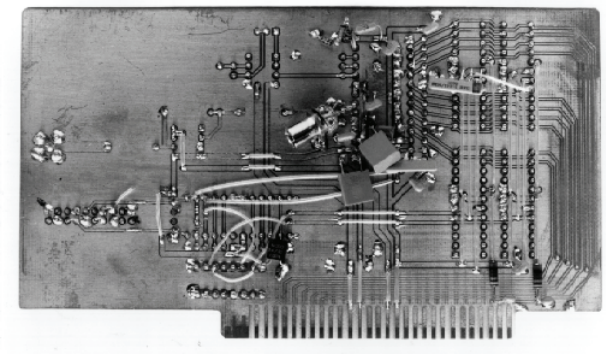


Figure 13.64: *A Milled Circuit Construction Prototype Board (bottom view)*

Perhaps the greatest single advantage of the milled circuit type of prototype circuit board is that it approaches the format of the final PCB design most closely. By its very nature however, it is basically limited to only single or double-sided boards.

Beware of Sockets!

IC sockets can degrade the performance of high speed or high precision analog ICs. Although they make prototyping easier, even *low profile* sockets often introduce enough parasitic capacitance and inductance to degrade the performance of a high speed circuit. If sockets must be used, a socket made of individual *pin sockets* (sometimes called *cage jacks*) mounted in the ground plane board may be acceptable, as in Figure 13.65.

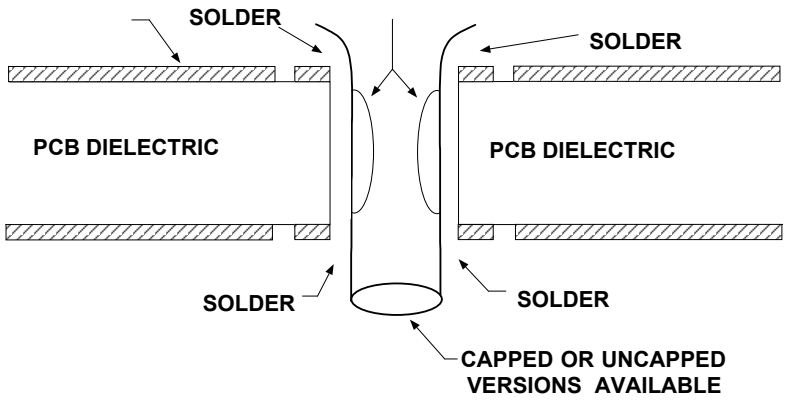


Figure 13.65: *When Necessary, Use Pin Sockets for Minimal Parasitic Effects*

To use this technique, clear the copper (on both sides of the board) for about 0.5 mm around each ungrounded pin socket, then solder the grounded socket pins to ground, on both sides of the board.

Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6, respectively). The pin sockets protrude through the board far enough to allow point-to-point wiring interconnections.

Because of the spring loaded, gold-plated contacts within the pin socket, there is good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade the performance of the pin socket, so this factor should be kept in mind.

Note also that the uncapped versions allow the IC pins to extend out the bottom of the socket. This feature leads to an additional useful function. Once a prototype using the pin sockets is working and no further changes are to be made the IC pins can be soldered directly to the bottom of the socket. This establishes a rugged, permanent connection.

Some Additional Prototyping Points

The prototyping techniques discussed so far have been limited to single or double-sided PCBs. Multilayer PCBs do not easily lend themselves to standard prototyping techniques. If multilayer board prototyping is required, one side of a double-sided board can be used for ground and the other side for power and signals. Point-to-point wiring can be used for additional runs which would normally be placed on the additional layers provided by a multilayer board. However, it is difficult to control the impedance of the point-to-point wiring runs, and the high frequency performance of a circuit prototyped in this manner may differ significantly from the final multilayer board.

Other difficulties in prototyping may occur with op amps or other linear devices having bandwidths greater than a few hundred megahertz. Small variations in parasitic

capacitance (<1 pF) between the prototype and the final board can cause subtle differences in bandwidth and settling time.

Sometimes, prototyping is done with DIP packages, when the final production package is an SOIC. *This is not recommended!* At high frequencies, small package-related parasitic differences can account for different performance, between prototype and final PCB. To minimize this effect, always prototype with the final packages. As an example, using the AD8001 op amp, Figure 13.66 shows the differences in recommended components and bandwidth for the different packages.

	AD8001AN (PDIP) Gain					AD8001AR (SOIC) Gain					AD8001ART (SOT-23-5) Gain				
Component	–1	+1	+2	+10	+100	–1	+1	+2	+10	+100	–1	+1	+2	+10	+100
R_F (Ω)	649	1050	750	470	1000	604	953	681	470	1000	845	1000	768	470	1000
R_G (Ω)	649		750	51	10	604		681	51	10	845		768	51	10
R_O (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_S (Ω)	0					0					0				
R_T (Nominal) (Ω)	54.9	49.9	49.9	49.9	49.9	54.9	49.9	49.9	49.9	49.9	54.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	340	880	460	260	20	370	710	440	260	20	240	795	380	260	20
0.1 db Flatness (MHz)	105	70	105			130	100	120			110	300	145		

Figure 13.66: *Recommend Components for AD8001 Op Amp Showing Different Values for Different Packages*

Full Prototype Board

In many instances after the various subcircuits have been checked out, a prototype board of the full design is the next step. While there is some support in the digital arena to go directly from simulation to a PC board, it is emphatically not the proper approach for high frequency or high precision analog circuits.

Things like grounding philosophy and parasitic coupling can really only be verified with a prototype board. And many times, more than one pass is required to get the maximum performance out of a design.

Another point should be kept in mind. You should resist the temptation to apply "small fixes" to a board as long as you are going to build another run anyway for the first production run. The simple point is that when you change something, you change something. In the scenario above, what you have done is gone from your prototype to your next prototype. Depending on the nature of the change, your exposure may be small, but it is still a question.

Summary

The prototyping techniques described earlier in this section are quite useful for ICs which are in DIP packages, and it is well worth the effort to prototype at least some of the critical analog circuitry before going to a final board layout. However, modern high performance ADCs and DACs are often provided in small surface mount packages which do not lend themselves to simple prototyping techniques. In the system, multilayer PC boards are required which further complicates the prototyping process.

In many cases, the only effective prototype for high performance analog systems is an actual PC board layout, especially if a multilayer is required in the final design. Evaluation boards are not only useful in the initial evaluation phases, but their layouts can be used as guides for the actual system board layout.

Successful integration of a high performance data converter into a system therefore requires excellent support from the manufacturer as well as care and attention to detail by the user.

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