Electrostatic Discharge

Fight ESD and keep your components healthy.

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CONSIDER THIS SCENARIO: YOU'VE REceived a MOS IC, removed it from its black foam or pink foam packing, and soldered it in place. Your project might work initially, but its performance falls far below expectations. Your IC is probably a victim of electrostatic discharge (ESD), and was likely damaged by improper handling. ESD is one of the most common causes of component failure, and as the actual transistor- device geometries on board a silicon chip shrink, an IC becomes more sensitive to it.

ESD can cause component failure or performance degradation that's difficult or impossible to detect, and is a major concern in modern electronics. The problems of ESD can occur as erroneous data, incorrect instructions, or system shutdown on operating hardware. This article will attempt to explain the mechanisms behind IC failure due to ESD, how to handle sensitive IC's properly, and how to set up a safe work area.

How ESD is generated

ESD is also called triboelectric charging. When two insulators are rubbed together, charge is transferred by friction, like what occurs if you run your feet across a carpet. The charge is a function of separation, extent of contact, rate of separation, humidity, and, of course, the triboelectric material itself (see Fig. 1).

ESD current is pretty low, while potential can exceed 300 kV. When charge is built up in a human body and discharges as a perceptible arc (felt as a slight tingle), no damage is done if the potential is under 2.5 kV (the "discomfort threshold"). Levels below that are barely noticeable, but can disrupt equipment. Table 1 shows the relative susceptibility of various semiconductor devices to ESD.

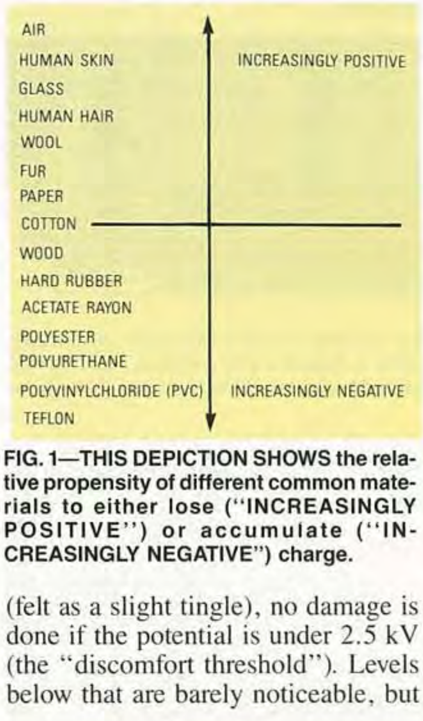

FIG. 1—THIS DEPICTION SHOWS the relative propensity of different common materials to either lose ("INCREASINGLY POSITIVE") or accumulate ("INCREASINGLY NEGATIVE") charge.

TABLE 1—SUSCEPTIBILITY TO ESD

DEVICE TYPE	RANGE OF ESD SUSCEPTIBILITY, kV
Power MOSFET	0.1-0.2
JFET	0.14-10
CMOS	0.25-2
Schottky Diodes, TTL	0.3-2.5
Bipolar Transistors	0.38-7
ECL	0.5
SCR	0.68-1

You might notice that you get electrostatic shocks more often in the winter than in the summer. That's because, in the summer, the relative humidity levels are much higher, and the buildup of moisture on a surface provides a discharge path. By comparison, materials that reject moisture exhibit the highest propensity toward ESD. Above 65% relative humidity, there's no real ESD problem, while below 20%, over 300 times more static charge is generated.

How much charge a human body will accumulate is dependent upon on the individual's size and skin conductivity. Another example of reduced humidity giving rise to electrostatic charging and ESD occurs when you put nylon and polyester clothing together in a dryer. You've no doubt seen how you can often generate as much as 650 volts by doing so, since the primary object in a dryer is the removal of moisture, and the combination of nylon and polyester are prime triboelectric materials. Typical ESD voltages are given in Table 2, for a number of common configurations.

ESD and MOS IC's

All MOS devices have an insulated gate that's subject to voltage breakdown. The gates on Motorola's devices are about 800 angstroms thick, and they break down at a gate-source potential (V_{GS}) of about 100 volts.

The high-impedance gates are protected by onboard resistor-diode networks, but they don't make an IC immune to ESD. Laboratory tests indicate that devices can fail after one very high voltage discharge, or after the cumulative effect of several lower potential discharges.

ESD-damaged devices behave in various ways. The most severely damaged devices are easiest to detect because their inputs or outputs have been completely destroyed; they're either shorted to V_{DD} or V_{SS}, or are open, and the device no longer functions. In other cases, detection can be more difficult because the device is intermittent or degraded. From the data in Fig. 1 and Table 2, you can easily see why MOS IC's can be damaged by improper handling.

ESD and Power MOSFET's

Being MOS devices, TMOS™ transistors (Motorola's trade name for its power MOSFET's) can also be damaged by ESD. However, they're not as susceptible as CMOS, due to large input capacitances that let them absorb more energy before breaking down. However, at breakdown potential, there's enough energy in the C_{GS} to totally perforate the gate-oxide. With a typical V_{GS} maximum rating of ±20 volts DC, and ESD potentials typically reaching 100 volts–25 kV, you can see why special handling is needed.

TABLE 2—TYPICAL ELECTROSTATIC VOLTAGES

MEANS OF STATIC GENERATION	ELECTROSTATIC VOLTAGES, kV	
	RELATIVE HUMIDITY	
	10-20%	65-90%
Walking across carpet	35	1.5
Walking across vinyl floor	12	0.25
Worker at bench	6	0.1
Vinyl envelope	7	0.6
Common polyethylene bag picked up from bench	20	1.2
Work chair padded with polyurethane foam	18	1.5

Curve-tracer plots of a MOS device before and after ESD degradation are shown in Figs. 2-*a* and *b*. Where most power MOSFET's have the ±20-volt DC rating, Motorola power MOSFET's use the Bullet-Proof4TM process, resulting in more reliable devices with higher V_{GS} breakdown levels. They're guaranteed to withstand ±40 volts DC for a single, non-repetitive pulse of 50-μs duration or less, achieved by control of gate-oxide thickness. With improved dielectric strength comes better resistance to ESD damage.

Classification of devices

Military specifications are used to classify ESD sensitivity of semiconductor devices. Through measurements, the model of Fig. 3 closely approximates the human body. Discharge of that network directly into a device indicates that the model assumes that a "hard ground" is in contact with the part. Although all pin combinations should be evaluated (six different versions for a power MOSFET), preliminary tests usually show that gate-oxide breakdown is most likely, and that reverse-bias makes a junction about an order of magnitude more sensitive than forward-bias. The damage mechanism is usually gate-oxide punch-through or junction melt-through. In other words, when a semiconductor device is subjected to unusually high voltages, the charges (holes and electrons) move apart in directions that they were never intended to go.

Static protection

The basic method for ESD protection combines prevention of static build-up and removal of existing charge. Charge-dissipation procedures differ for insulators and conductors. Since charge can't flow through an insulator, it has to be removed by contact with a conductor. If the item is an insulator (plastic box, clothing, etc.), ionized air is required. If it's a conductor (metal tray, conductive bag, person's body, etc.), complete discharge can be accomplished by grounding.

Many methods are used to inhibit ESD; carpets are made with antistatic materials and coatings. Equipment can be sprayed with antistatic solutions, materials with low triboelectric propensity can be used, and clothing can be made of triboelectrically insensitive fabric. Static-safe work stations are also used. Components are packaged in conductive or antistatic packaging. In addition, relative humidity within the environment is maintained above 65%.

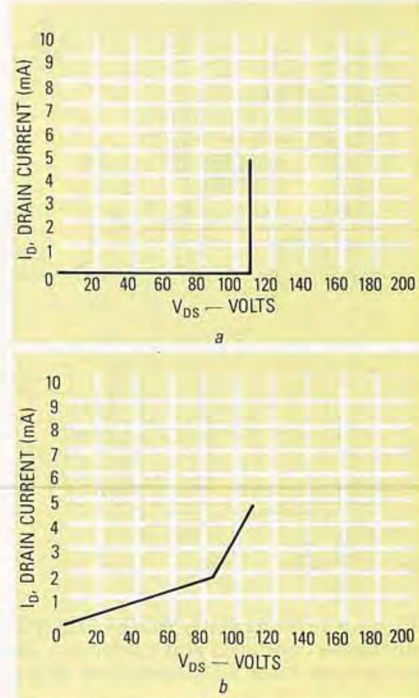

FIG.2—CURVE TRACER PLOTS OF A MOS device before (*a*) and after (*b*) being subjected to ESD degradation.

How to prevent ESD?

You might find industrial-grade precautions impractical, but if you're educated in ESD and its effects, you'll have better control of your

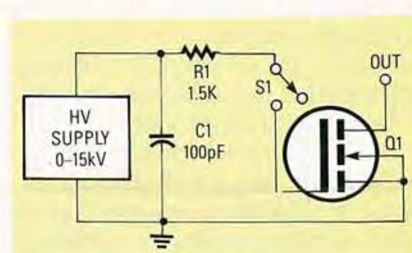

FIG. 3—THIS MODEL CLOSELY approximates the human body. Discharge of this network directly into a device indicates that the model assumes a "hard ground" is in contact with the part.

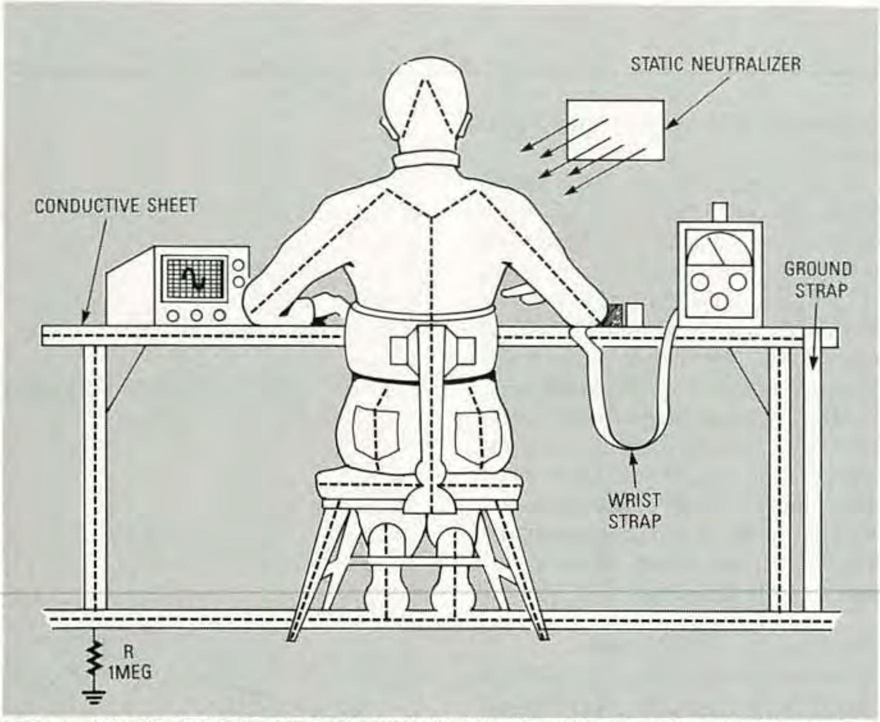

FIG. 4—A TYPICAL ESD-PROTECTED WORK STATION, with a $\frac{1}{16}$-inch metallic bench top, conductive floor mats and containers, ionized air blowers, wrist straps, and soldering-iron ground. Place all MOS devices on a grounded bench prior to handling.

working environment. A typical work station is shown in Fig. 4. The steps to be taken are listed below:

FIG. 5—ALWAYS USE PACKAGING labels like this one to indicate ESD-sensitive parts, and that proper handling of the parts is required.

- Never exceed maximum specified data-sheet ratings.
- Work benches should have grounded metallic tops, conductive floor mats and containers, and ionized air blowers.
- Use wrist straps in contact with the skin.
- Use a ground strap on the tip of all soldering irons.
- Place all MOS devices on a grounded bench prior to handling, since they can be statically charged with regard to the surface of a bench.
- Never use brush or spray cleaning to remove solder flux from a MOS-populated PC board with the IC's installed. If you want to clean such a PC board in this way prior to installing the IC's, fine.
- Place completed PC-board assemblies in antistatic bags if they're transported to another location.
- Keep work benches free of coffee cups and stirrers, paper, styrofoam, tobacco ash, cellophane wrappers, and plastic.
- *Never* insert or remove an IC from its socket with power applied.
- Check all power supplies for voltage transients like ripple or spikes.
- All low-impedance equipment like pulse generators should be connected to MOS devices *only* after power up, and disconnected before being shut off.

MOS-device packaging is critical; components purchased for home projects should come with antistatic or conductive packaging. Static-sensitive IC's are normally packaged in either black conductive foam, specially treated pink plastic bags, or an oily antistatic styrofoam. There should also be packaging labels indicating ESD-sensitive parts, and that proper handling is required, as in Fig. 5. Never insert a MOS device into a conventional plastic tray or piece of styrofoam. Keep it in its original packaging until ready to use.

All equipment should have a good earth ground, but particularly if it's ESD-sensitive. In a dry climate, attach a small metal plate with a good ground to your desk/workbench. By touching it to discharge any static potential built up while walking across carpeting, your equipment might live longer. **R-E**