International Rectifier

APPLICATION NOTE

Application Note AN-1035

DirectFET® Technology Board Mounting Application Note

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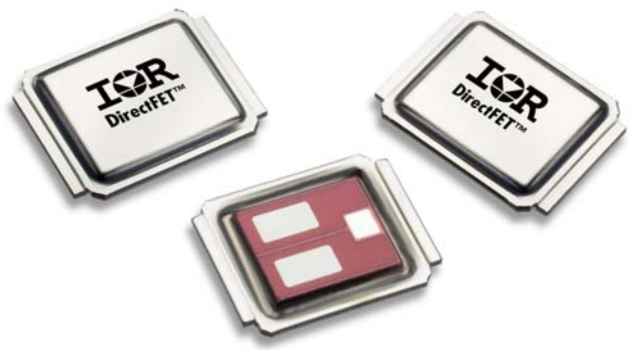
Introduction

DirectFET® is a surface mount semiconductor technology designed primarily for board-mounted power applications. It eliminates unnecessary elements of packaging that contribute to higher inductance and resistance, both thermal and electrical, so that its power capabilities exceed those of comparably sized packages.

The growing DirectFET range includes various can sizes and device outlines. There are now lead-free variants, pre-soldered with a tin-silver-copper alloy (Sn96.5 Ag3.0 Cu0.5) to improve performance with lead-free pastes and identified by a PbF suffix after the part number (for example, IRF6618PbF).



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Device construction

DirectFET devices use an innovative construction technique to make source and gate connections directly to the die surface (Figure 1). The remainder of the surface is coated with passivation to protect it and to control the position, shape and size of the solder contacts between device and substrate.

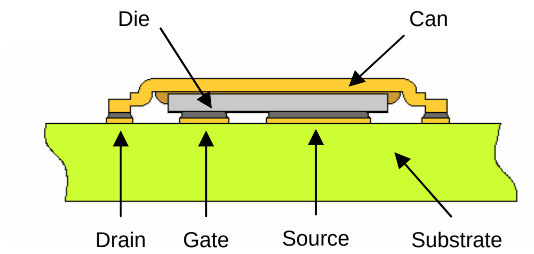
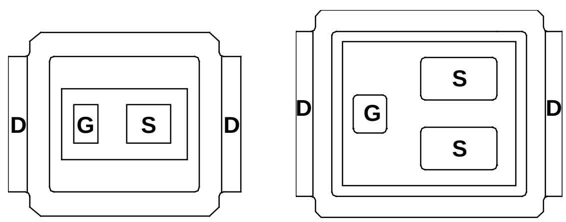


Figure 1 Sectional view

The drain connection is formed by a plated copper can, which is bonded to the drain side of the silicon die. The can has two contact areas, both of which must be soldered to the substrate although one can be used solely as a mechanical anchor. Using tracks of similar size under both drain contacts will help to ensure that the device does not tilt during reflowing.

Figure 2 shows typical contact configurations of DirectFET devices, covering most devices in the range. Specific pad assignments are shown in the data sheet for each product.



G – Gate, S – Source, D – Drain
(viewed from underside of device)

Figure 2 DirectFET contact configuration

Figure 3 shows how DirectFET devices are labeled. The part number, batch number and date code are provided to support product traceability. The last digit of the batch number on PbF variants is underlined.

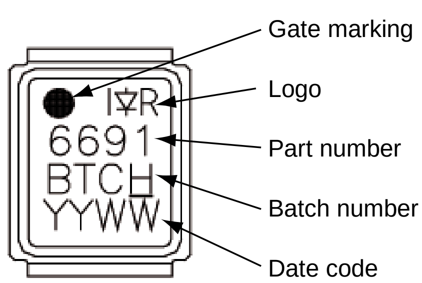


Figure 3 Device markings

Note: The dot shows at which end of the device the gate pad is located. **It is not Pin 1.** Figure 4 shows recommended pad numbering schemes.

Design considerations

Substrates

DirectFET technology was originally developed and evaluated for use with epoxy and polyimide glass-woven substrates. The test substrates were finished in electroless nickel immersion gold but any of the numerous surface finishes available are suitable. Subsequent evaluations have confirmed that DirectFET devices can be used with insulated metal substrates made from aluminum silicon carbide (AlSiC) and copper (Cu). For more information, refer to the DirectFET Technology Materials and Practices Application Note (AN-1050), available at:

www.irf.com/technical-info/appnotes/an-1050.pdf

The substrate finish can affect the amount of energy required to make solder joints; this can in turn be a factor in solder quality issues such as solder balling, tombstoning (or tilt) and the formation of voids. It is important to ensure that the appropriate reflow profile is used for the selected substrate finish.

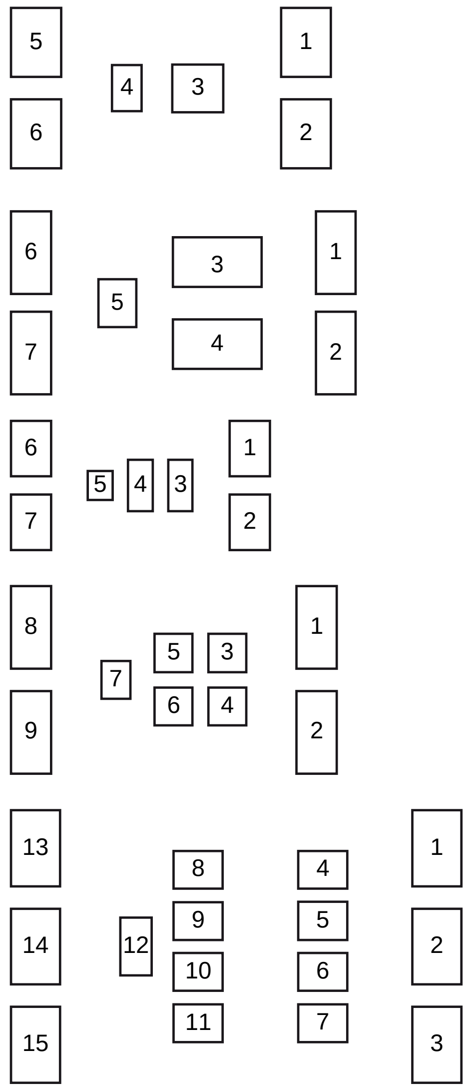
Substrate designs

To achieve low-loss track layouts, DirectFET devices were designed for use with solder-mask-defined layouts. Although the devices can be used with pad-defined (non-solder-mask-defined) layouts, these have not been evaluated. The outline of DirectFET devices and the use of solder-mask-defined pads contribute to efficient substrate design. Large-area tracks optimize electrical and thermal performance.

If pad numbering is required to produce a component outline within the library of a CAD system, International Rectifier recommends that the conventions shown in Figure 4 are adopted. This makes it easier to discuss any issues that may arise during design and assembly.

DirectFET devices can be placed in parallel using simple layouts (Figure 5). International Rectifier recommends a minimum separation of 0.500mm (0.020"). The separation can be adjusted to reflect local process capabilities but should allow for rework. Micro-screen design and desoldering tool type may affect how closely devices are placed to each other and to other components.

Refer to Appendix A for device outlines, substrate layouts and stencil designs for each can size and device outline in the DirectFET range. These are common to both standard and lead-free devices.



1,2	Drain
3	Source
4	Gate
5, 6	Drain

1,2	Drain
3,4	Source
5	Gate
6,7	Drain

1,2	Drain
3,4	Source
5	Gate
6,7	Drain

1,2	Drain
3-6	Source
7	Gate
8,9	Source

1-3	Drain
4-11	Source
12	Gate
13-15	Drain

(viewed from top of substrate)

Figure 4 Recommended pad numbering

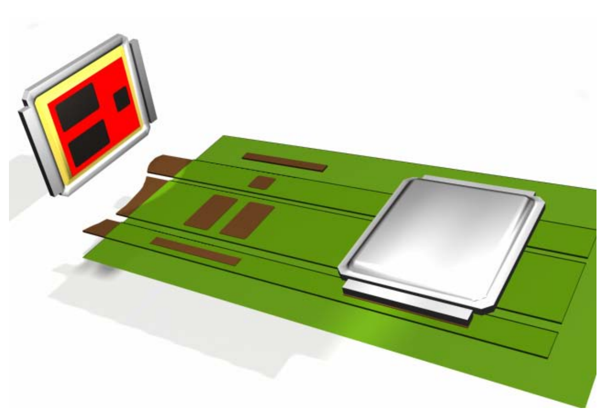


Figure 5 Placing DirectFET devices in parallel

Standardised pad layouts

Later devices in the DirectFET range use standardised pad outlines (Figure 6). This means that devices of the same can size can easily be interchanged and upgraded. For example, a substrate layout for a small can device with one source pad can be designed to accept a small can device with two source pads; the gate pads are in the same positions on the two devices and the first of two source pads is in the same position as the single source pad.

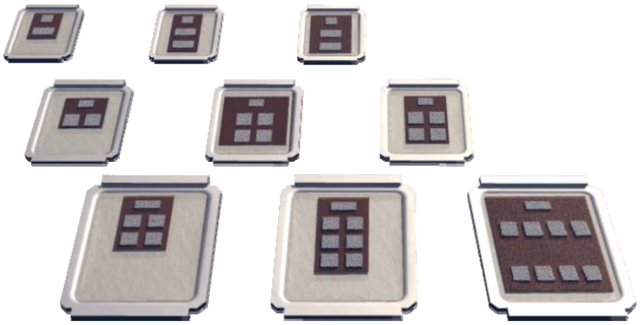


Figure 6 Standardised pad layouts

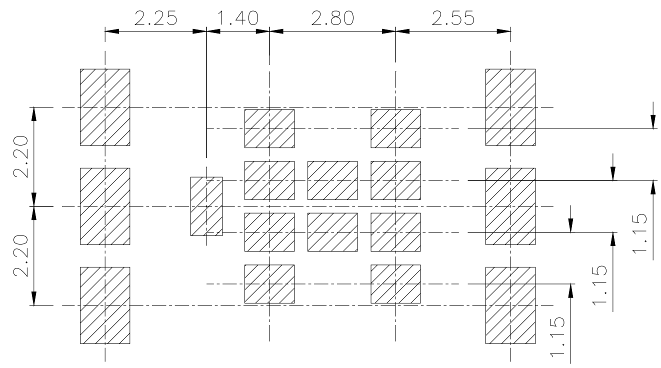
For many devices (see table below), it is possible to use either a device-specific or a universal pad outline on the substrate. The stencil design determines where solder paste is applied to a universal outline. To avoid wastage and flux residues, International Rectified recommends using a device-specific stencil design.

Device outline	Stencil design	Dedicated pad outline	Universal pad outline
S1	S1	S1	S2
S2	S2	S2	S2
SB	SB	SB	SB
M2	M2	M2	M4
M4	M4	M4	M4
L4	L4	L4	L10
L6	L6	L6	L10
L8	L8	L8	L10

Note: L10 is the universal pad layout for large-can devices (Figure 7). All other pad layouts are shown in Appendix A.

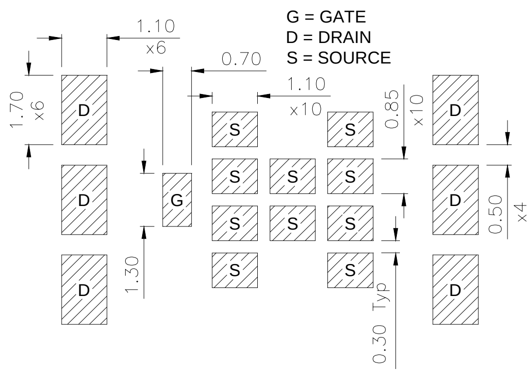
The device outline code indicates the can size and number of source pads (see table below).

Can size		Number of source pads
S	small	n – 1, 2, 4, 6, 8 or 10
M	medium	
L	large	



(dimensions in mm)

Figure 7(a) L10-outline substrate/PCB layout



(dimensions in mm)

Figure 7(b) L10-outline substrate/PCB layout

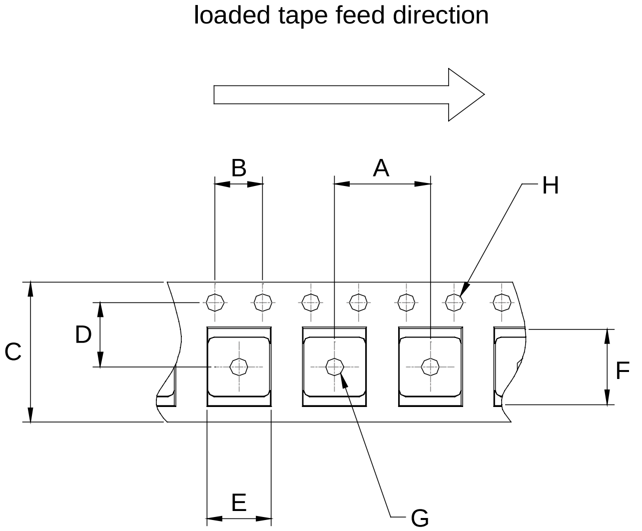
Assembly considerations

International Rectifier designed DirectFET devices to be as easy as possible to assemble using standard surface mounting techniques. Recessing the die within the package (Figure 8) forces a standoff between die and substrate, which helps to reduce solder balling problems and improves device reliability. However, procedures and conditions can have a profound influence on assembly quality. It is therefore necessary to develop an effective process based on the individual requirements for the application.

Figure 8 Contact planarity

Packaging

DirectFET devices are supplied in tape and reel format (Figure 9). The gate contact is furthest from the tape index holes.



Dimensions (mm)						
	Small can		Medium can		Large can	
Code	Min	Max	Min	Max	Min	Max
A	7.90	8.10	7.90	8.10	11.90	12.10
B	3.90	4.10	3.90	4.10	3.90	4.10
C	11.90	12.30	11.90	12.30	15.90	16.30
D	5.45	5.55	5.45	5.55	7.40	7.60
E	4.00	4.20	5.10	5.30	7.20	7.40
F	5.00	5.20	6.50	6.70	9.90	10.10
G	1.50	NC	1.50	NC	1.50	NC
H	1.50	1.60	1.50	1.60	1.50	1.60

Figure 9 Tape and reel packaging

Storage requirements

DirectFET devices are packed in sealed, nitrogen-purged, antistatic bags. The plating configuration of certain areas of the device is photosensitive and can be tarnished by the high levels of atmospheric pollution that occur in some heavily industrialized areas. The sealed bags provide adequate protection against normal light levels but it is prudent to avoid prolonged exposure to bright light sources. The bags also provide protection from the ambient atmosphere. Devices in sealed, unopened bags have a shelf life of two years. Once a bag has been opened, its contents should be treated as Moisture Sensitivity Level (MSL) 3 to guarantee good solderability (unless identified as MSL 1 on the package label).

To reduce the risk of tarnishing, International Rectifier recommends that, when not in use, reels of devices (both MSL 1 and MSL 3) should be resealed into the protective bags in which they are supplied.

Solder pastes

International Rectifier evaluated different types of solder paste from various manufacturers. The properties of pastes vary from manufacturer to manufacturer, meaning that some perform better than others. In general, high slumping pastes tend to suffer more from solder balling than slump-resistant pastes; solder balling is discussed in the next section on stencil design. In addition, some pastes appear to be more prone to voiding than others.

Solder alloys, metal contents and flux constituents all influence the rheology of the solder paste. This in turn influences how the paste reacts during processing. DirectFET products with a PbF suffix have been evaluated using both lead-containing pastes (Sn63 Pb37) and lead-free pastes (Sn96.5 Ag3.0 Cu0.5). Products without the PbF suffix are not recommended for use with lead-free pastes.

Evaluations of both standard and lead-free devices used a reflow profile that conforms to IPC/JEDEC standard J-STD-020C (July 2004 revision). As devices may be subjected to multiple reflows when PCBs are double-sided or reworked, the evaluations used up to three reflows. International Rectifier recommends that customers should conform to J-STD-020C in setting reflow profiles and should not exceed three reflows.

Stencil design

Stencil design is instrumental in controlling the quality of solder joints. Appendix A shows stencil designs that have given good results with recommended substrate outlines, both at International Rectifier and at customers' locations. They are based on reductions of 25% (equivalent to printing 75% of the PCB pad area).

The designs assume a stencil thickness of 0.150mm (0.006"); they should be revised for other thicknesses. DirectFET can be used with thicknesses of 0.100-0.250mm (0.004-0.010"). Stencils thinner than 0.100mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the die; high reductions sometimes create similar problems. Stencils in the range of 0.125mm-0.200mm (0.005-0.008"), with suitable reductions, give the best results.

Post-reflow evaluations can help to assess how a stencil is performing within a given process. Two main problem areas can be addressed by improving stencil design:

- **Solder balling around the perimeter of the die.** This can be caused by too much solder paste, in which case the stencil might need to be reduced by more than 25%. The reduction can be symmetrical but biasing it unevenly may help to prevent solder balling; the stencil designs in Appendix A have apertures moved further from the die edge for this reason. Solder balling can result from other external factors, such as the moisture content of the board and incorrect ramp rates or insufficient soak times in the reflow profile. Leadless devices like DirectFET can sometime accentuate existing deficiencies within a process.
- **Misshapen joints.** If the joints are smaller or seem to be only partially made, this might suggest that there is insufficient solder to make the joint. If, however, the joints have what appear to be additional areas extending from their edges, they are usually the result of too much solder; this almost certainly the case if solder balls are also present. Insufficient solder can also cause voiding but this is more likely to arise from other factors, including surface finish, solder paste and substrate condition.

Device placement

Due to the recessed position of the die, DirectFET devices should ideally be depressed into the solder paste by at least 0.050mm (0.002") to ensure that the contact areas are in full contact with the paste. Placement machines operate on various principles, some based on over-travel and others on placement pressure. Good results have been achieved using over-travel of 0.050mm-0.100mm (0.002-0.004") and placement pressure of 150-250g.

Insufficient placement pressure may result in poor solder joints or in devices being tilted and/or misaligned. Although it is better to avoid perceptible tilt, poor placement does not always cause reflow problems. Ideally, devices should be placed to an accuracy of 0.050mm on both X and Y axes but, during evaluations, devices centered themselves from placement inaccuracies of more than 0.200mm.

Heatsinks

DirectFET devices are designed to deliver superior thermal performance compared with other packages. In many applications, heatsinks are not required but they may sometimes be applied to achieve even greater cooling in use.

For optimum ruggedness, International Rectifier recommends attaching heatsinks to the substrate using clips, screws or other fasteners (Figure 10). However, if limited board space prevents this, they may be attached to the top of devices (Figure 11). When heatsinks are attached to the top of devices without mechanical fastenings to the substrate, potential mechanical stresses on the heatsink must be considered. Such stresses will be transferred to the device and may cause mechanical damage and, in extreme cases, device failure.

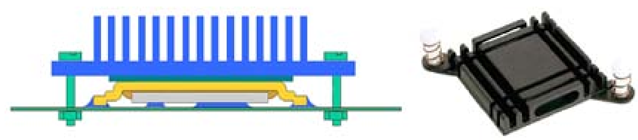


Figure 10 Heatsinks attached to substrates

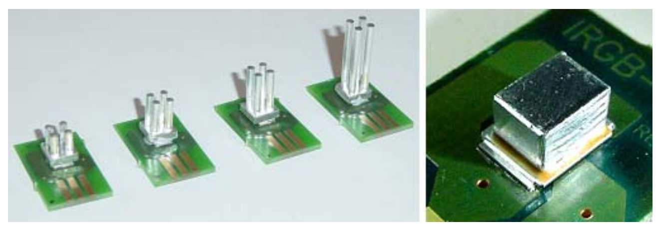


Figure 11 Heatsinks attached to devices

Whichever heatsink design and application method is used, heatsinks can be applied to single or multiple devices. Figure 12 shows multiple device heatsinking.

Figure 12 Heatsinks attached to multiple devices

When one heatsink covers multiple devices, problems can arise from variances in the thermal expansion of substrate, solder, device, thermal interface material (TIM) and heatsink. This is especially true when the heatsink is attached to the top of the devices without mechanical fastenings to the substrate. As well as normal operating conditions, calculations of thermal expansion must include other heat excursions applied to the assembly (for example, during reflow soldering).

TIMs should be used to improve thermal contact by filling air gaps (voids) between the mating faces of the device and the heatsink. Without a TIM (Figure 13), there is a significant proportion of voids over the area. With a TIM (Figure 14), there is full contact.

Many TIMs are available in various forms. The table below summarises the advantages and disadvantages of each form, although individual examples may differ. The suitability of each form depends on the design and use of the assembly. Evaluations will be needed to establish the most suitable material for an application.

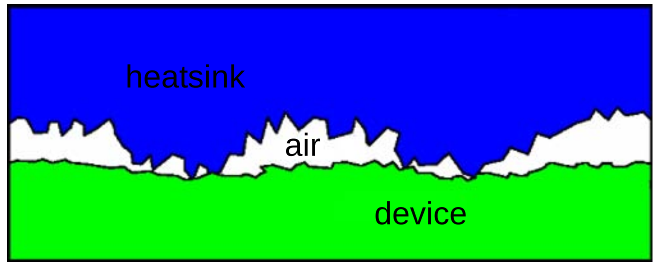


Figure 13 Thermal contact (no TIM) K≈0.024 W/(m•K)

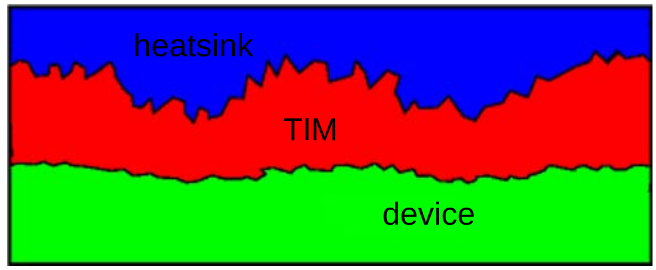


Figure 14 Thermal contact (TIM) K≈0.5–10.0 W/(m•K)

Type	Description	Advantages	Disadvantages
Grease	Traditional form, filled with conductive particles of Al_2O_3, BeO, Al or Ag Thermal conductivity: 0.3–2.0 W/(m·K) (up to 6 W/(m·K) for Al) Vendors: Shinetsu, Bergquist	Good surface conformance Good surface wetting Thin bonds (<0.005")	Difficult to pre-apply Messy processing Can leak out over time Needs controlled dispensation No electrical isolation
Gel	Grease replacement, cross-links in curing to form a gel-like substance Thermal conductivity: 0.3–2.0 W/(m·K) Vendors: Thermoset (Lord MG series)	Good surface conformance Good surface wetting Thin bonds (<0.005") Does not leak out over time	Cannot be pre-applied Needs curing (can be from burn-in) Messy processing Needs controlled dispensation No electrical isolation
Adhesive	Heat-cured and filled with conductive particles similar to grease Thermal conductivity: 0.3–1.3 W/(m·K) Vendors: Dow Corning, 3M	Good surface conformance Good surface wetting Thin bonds (<0.005") Mechanical attachment	Cannot be pre-applied Needs curing (can be from burn-in) Messy processing Needs controlled dispensation No electrical isolation
Tape	Pressure-sensitive and adhesive-filled, with conductive particles on a fibreglass or plastic carrier Thermal conductivity: 0.7–1.5 W/(m·K) Vendors: Bergquist, Dow Corning, 3M	Moderate surface wetting Mechanical attachment Can be die-cut and pre-applied Clean and simple processing Electrical isolation	Poor surface conformance Thick bonds
Phase change	Waxy material, changes to a gel at about 50°C Thermal conductivity: 0.8–1.5 W/(m·K) Vendors: Bergquist, Dow Corning, 3M	Good surface conformance for irregularities < 0.002" Good surface wetting Clean processing Can be pre-applied or on a carrier Thin bonds (<0.005") (if pre-applied) Electrical isolation (if on carrier)	Poor surface conformance for large irregularities and bowing
Pads	Thickness: 0.010–0.250" Thermal conductivity: 0.8–4.0 W/(m·K) Vendors: Bergquist, Dow Corning, 3M	Good surface conformance for large irregularities Simple to use Can be reused Can be die-cut and pre-applied Clean processing	Poor surface conformance for small irregularities Poor wetting Thick bonds Pressure required to fit pads can make them difficult to use effectively

When applying a TIM to the device-heatsink joint, it is important to consider the material and the way it is applied. If a fluid or flowable material is used, it must not be allowed to seal the sides of the device that are not in contact with the substrate. Such seals can trap air under the device, both around the die and between the device and substrate. If the assembly is then subjected to heating for any reason (whether in normal operation, further processing or burn-in testing), the trapped air will expand and may break either the device-die bond or the device-substrate joints. Although tests have shown that this generally happens only when a large heat excursion is applied to a large DirectFET body containing a small silicon die, it is still worthy of consideration.

If excess TIM is applied, this can flow under the DirectFET device. Thermal expansion can then break the device-substrate joints. In Figure 15, a heatsink has been removed with floss to show that excess heatsink adhesive has spread across the substrate. It has covered the devices and sealed their sides.

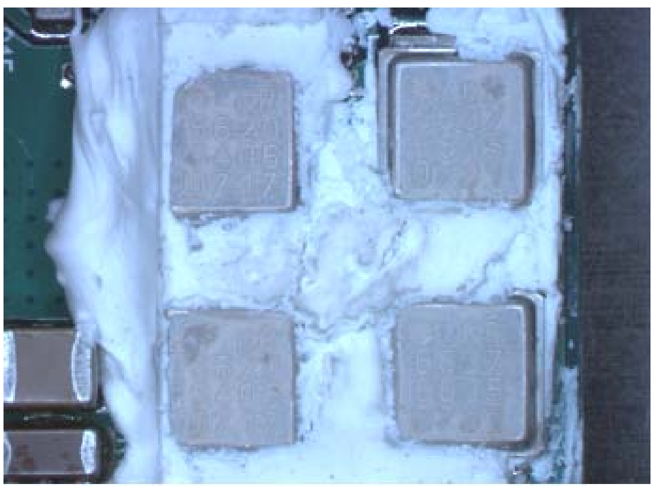


Figure 15 Excess heatsink adhesive covering devices

In Figure 16, a cross-section reveals that the adhesive has flowed under the DirectFET devices. It has filled the gap between substrate, die and device body.

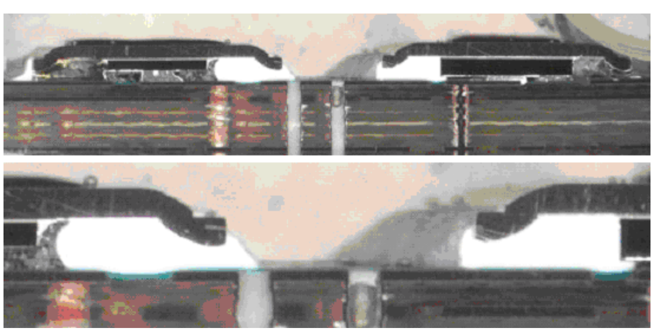


Figure 16 Heatsink adhesive under devices

In Figure 17, the TIM has expanded and separated the silicon die from the device body.

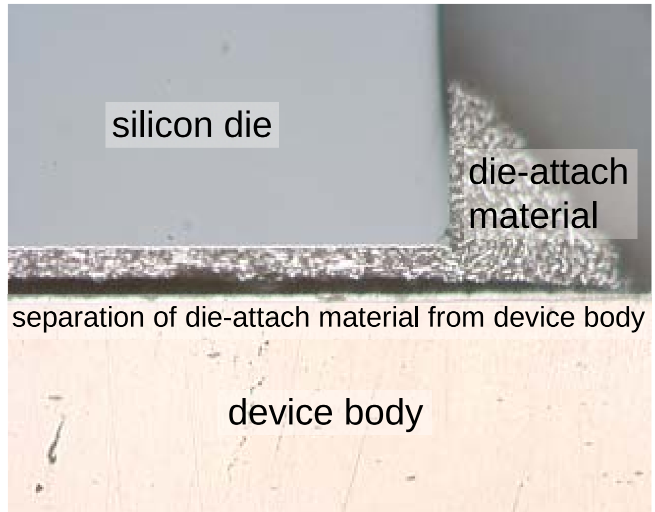


Figure 17 Die separated from device body

With so many heatsink designs and materials, proposed combinations must be fully evaluated to establish their suitability for a planned application.

Reflow equipment

DirectFET devices are suitable for assembly using surface mount technology reflowing equipment and are recommended for use with convection, vapor phase and infrared equipment. PbF qualified devices have a good resistance to short-term exposure to high temperatures, making them suitable for reflow profiles of up to 260°C (measured by attaching a thermocouple to a DirectFET device).

There are no special requirements for successful assembly but all reflow processes used in evaluation and qualification complied with the recommendations of solder paste suppliers. Using incorrect reflow profiles can cause solder quality issues such as solder balling, tombstoning (or tilt) and the formation of voids; if such problems arise, the reflow profile should be checked.

The DirectFET package is designed to have superior thermal resistance properties. For this reason, it is essential that the core of the substrate reaches thermal equilibrium during the pre-heating stage of the reflow profile to ensure that adequate thermal energy reaches the solder joint. For more information, visit www.irf.com/product-info/directfet/dfmanuengineer.html.

Inspection

For comprehensive information on inspecting board-mounted DirectFET devices, refer to the DirectFET Inspection Application Note (AN-1080), available at:

www.irf.com/technical-info/appnotes/an-1080.pdf

As with all chip scale packaging (including land grid arrays and ball grid arrays), the best way to inspect devices after reflow is by taking X-ray images. The images for DirectFET and DirectFET PbF devices will differ slightly, as shown in Figure 18.

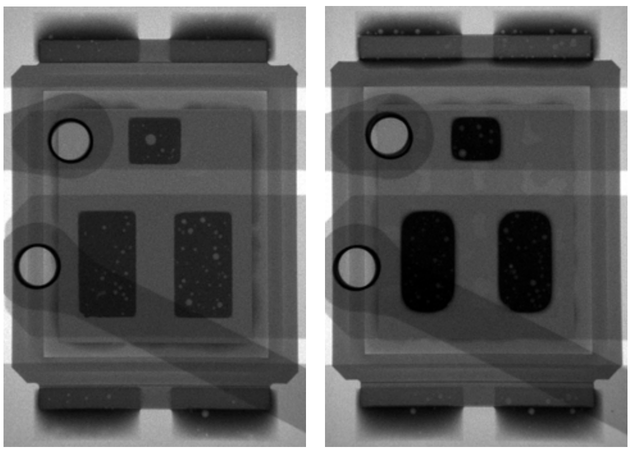


Figure 18 X-rays of DirectFET (left) and DirectFET PbF

An X-ray image of a board-mounted DirectFET PbF device shows denser solder joints, with fewer voids and solder balls, but also with poorer edge definition than seen in DirectFET devices processed under the same conditions. The reason for this is that the solder joints are significantly thicker for the DirectFET PbF devices, which are pre-soldered. As solder tends to adhere more readily to pre-soldered surfaces, the solder joints on the lead-free devices have a more pronounced hour-glass shape. In an X-ray image, this results in blurring of the joint edges and rounding of the joint corners.

Rework guidelines

Modern rework stations for ball grid array and leadless packages often use two heating stages. The first heats the substrate, either with a conventional hot-plate or a hot-air system. The second stage uses a hot-air system for localized heating, often with the option of unheated air for faster cooling of the solder interconnections on the replaced device; this improves the solder grain structure.

The device placement mechanism or arm usually has a hot-air de-soldering gun as part of the pick head, equipped with a vacuum cup and thermocouple. Once the solder reflow temperature has been reached, the vacuum is automatically engaged to allow the device to be removed from the substrate. This reduces the risk of causing damage by premature removal.

International Rectifier does not recommend reusing devices removed from a substrate. Dispose of the old device and use a new replacement.

To replace a DirectFET device:

Note: If you usually bake to remove residual moisture before rework, insert your normal procedure here.

1. Heat the site to approximately 100^{o}C using the substrate heating stage. This reduces the amount of heating required from the hot-air de-soldering tool, which in turn reduces the risk of damaging either the substrate or surrounding components.
2. Lower the placement arm to bring the de-soldering tool into contact with the device. When the device and the solder interconnects reach reflow temperature, lift the placement arm to remove the device from the substrate.
3. Clear residual solder and flux from the site with a blade-type de-soldering tool and de-soldering braid. Take care in cleaning the site: damage to the solder-resist may produce undesirable results. When the site is ready, apply new solder paste with a micro-screen and squeegee.
4. Heat the site to approximately 100^{o}C using the substrate heating stage. Position the new device with the placement arm and then use the de-soldering tool to heat both device and solder interconnects to reflow temperature. Retract the arm, leaving the device in place. Cool as quickly as possible to achieve good grain structure in the new joint.

Mechanical test results

International Rectifier has subjected board-mounted DirectFET devices to extensive mechanical tests, conducted in accordance with industry standards and practices. The devices tested were of medium can size, one MQ-outline and one MT-outline. Given that all DirectFET devices are made in the same way, other can sizes should perform to the same high standard.

This section contains summarized results for bend tests, compression tests, drop tests and vibration tests. Full reports are available on request.

Bend tests

Method

These tests were carried out in accordance with BS EN 60068-2-21:1999 Test U: Robustness of terminations and integral mounting devices.

- To gauge relative performance, DirectFET devices were tested against ceramic capacitors of a similar size.
- Substrates were initially tested over knife edges set at 90mm pitch but, as few devices failed, the pitch was changed to 70mm. This meant that the same deflection formed a more acute radius, increasing the strain and reducing the deflection needed to cause failure (13-14mm deflection over 70mm pitch causes approximately the same strain as 25mm deflection over 90mm pitch).
- The speed of deflection was 1mms^{-1} for all tests.
- The test board measured 100x40mm and was manufactured from FR4 2oz copper, finished in nickel gold. The solder used was Sn63 Pb37.
- Devices were mounted both longitudinally and transversely, and were tested with the devices mounted on both front and back of the board.

Results

Figures 19 and 20 show the deflection required to cause failure in MQ-outline and MT-outline medium can devices.

Note: The shaded areas indicate the point at which the substrates failed. No components survived beyond this.

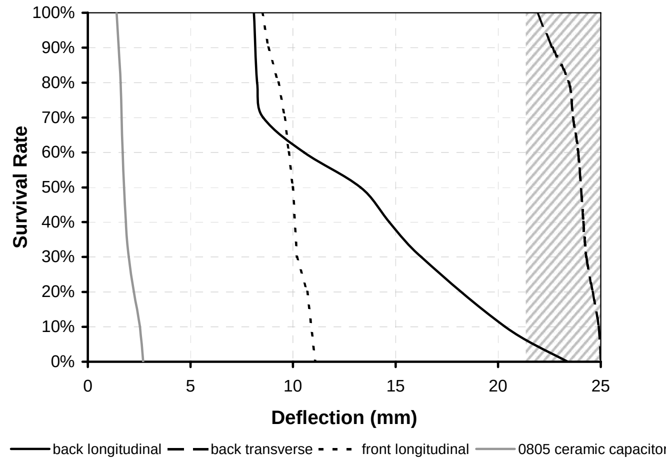


Figure 19 MQ-outline deflection test results

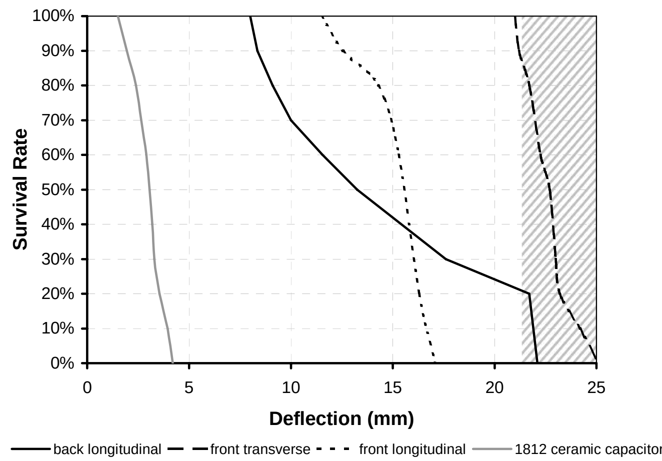


Figure 20 MT-outline deflection test results

Compression tests

Method

- Tests were carried out at ambient room temperature (22°C).
- Test speed was 0.5mmmin^{-1} (return speed of 20mmmin^{-1} where applicable).
- Test duration was measured from the point at which 0.05N of force registered on the tester.
- A maximum force of 1750N was used as a termination point for the test.

Continuous pressure:

Pressure was applied to the top of the device until the gate threshold voltage ($V_{g\text{-}th}$) shifted by ±20%.

Stepped pressure:

MQ-outline: Pressure was raised to 400N, relieved and the device allowed to return to neutral. The pressure was then raised to 700N and relieved; this process was repeated in steps of 50N until the device failed. The gate threshold was monitored throughout.

MT-outline: The MQ-outline test was replicated but with an initial pressure of 600N and increments of 100N.

Note: Initial pressures were set close to the expected failure point to minimize the number of cycles and, therefore, the fatigue induced by them.

Results

The table below shows the average compression required to cause failure in DirectFET devices.

	MQ-outline	MT-outline
Continuous	1204N	1407N
Stepped	663N	1106N

Note: Gravity (1g) was assumed to be 9.81ms^{-2}.

Figure 21 shows mortality curves for the survival rate of board-mounted DirectFET devices when increasing pressure is applied to the top surface.

Survival rates are calculated as follows:

$$\text{Survival rate} = \frac{n_{dt} - n_{df}}{n_{dt}} \times 100$$

n_{dt} Number of devices tested
n_{df} Number of devices failed

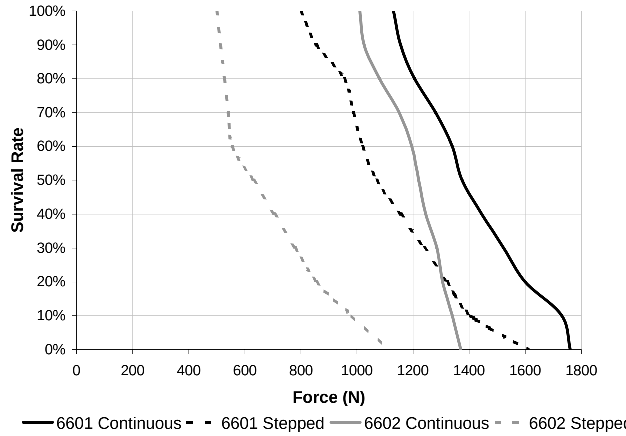


Figure 21 DirectFET survival rates

Drop tests

Method

These tests were carried out in accordance with BS 2011: Part 2.1 Ed:1992 Test Ed: free fall.

DirectFET devices were dropped onto a steel block from different heights and in five attitudes:

1. On the short edge of the device
2. On the long edge of the device
3. On the corner of the device
4. With device flat, on top of the substrate
5. With the device flat, underneath the substrate

BS 2011 specifies drop heights of 25mm, 50mm, 100mm, 250mm, 500mm and 1000mm. When no devices failed, International Rectifier increased the drop height to 1500mm.

Results

	MQ-outline		MT-outline	
Drop height (mm)	1000	1500	1000	1500
Attitude 1	0/10	0/10	0/10	0/10
Attitude 2	0/10	0/10	0/10	0/10
Attitude 3	0/10	0/10	0/10	0/10
Attitude 4	0/10	0/10	0/10	0/10
Attitude 5	0/10	0/10	0/10	0/10

Note: 10 devices were tested for each combination of height and attitude. Each device was dropped 20 times.

Vibration tests

Method

These tests were carried out in accordance with BS 2011: Part 2.1 Fd:1973 Test Fd: random vibration — wide band general requirements.

DirectFET devices were subjected for three hours to random vibrations from 20Hz to 2kHz, experiencing 3.2g_{rms} (31.4$ms^{-2}{}_{rms}$) with an acceleration spectral density value of 0.005g^2Hz^{-1} ([0.48ms^{-2}] $^2Hz^{-1}$). Figure 22 shows the bandpass filter frequency chart.

The devices were tested in three attitudes:

1. On the short edge of the device
2. On the long edge of the device
3. With device flat, on top of the substrate

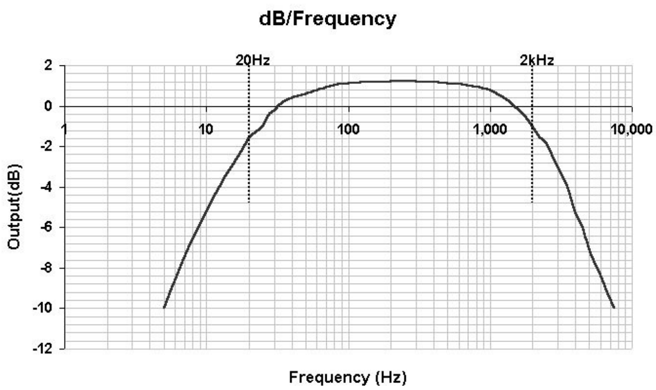


Figure 22 Bandpass filter frequency chart

Results

	6601
Attitude 1	0/16
Attitude 2	0/16
Attitude 3	0/16

Note: 16 devices were tested in each attitude.

Acknowledgements

International Rectifier would like to thank:
Indium Corporation of Europe, Multicore Solders Limited, Litton Kester Solders, Tamura Kaken (UK), Agmet Ltd (ESL Europe) and Alpha Metals for supplying solder paste samples and information.
Mike Fenner of Indium, for support during the applications work, and James Taylor of Litton, for providing information on surface mount technologies.
The Bergquist Company for supplying insulated metal substrate samples and information.

Further reading

Frear, D R; Vianco, P T (1994) 'Intermetallic Growth and Mechanical Behavior of Low and High Melting Temperature Solder Alloys', *Metallurgical and Materials Transactions A*. Vol 25A pp1509-1523 July 1994.
Frear, Darrel R (1990) 'Microstructural Evolution during Thermomechanical Fatigue of 62Sn-36Pb-2Ag and 60Sn-40Pb Solder Joints', *IEEE Transactions on Component, Hybrids, and Manufacturing Technology*, Vol 13 No 4 December 1990.
Frear, Darrel; Morgan, Harold; Burchett, Steven; Lau, John. *The Mechanics Of Solder Alloy Interconnects*. Chapman & Hall. ISBN 0-442-01505-4.
Manko, Howard H (4th edn) *Solders and Soldering*. McGraw-Hill. ISBN 0-07-134417-9.
Prasad, Ray P (2nd edn) *Surface Mount Technology*. Kluwer Academic Publishers. ISBN 0-412-12-12921-3.

Standards

BS EN 60068-2-21:1999 / IEC 60068-2-21:1999
Environmental testing — Part 2-21 Test U:
Robustness of terminations and integral mounting devices.
ICS 19.040
BS 2011: Part 2.1 Fd:1973
Basic environmental testing procedures — Part 2.1 Test Fd: random vibration — wide band general requirements.
BS 2011: Part 2.1 Ed:1992 / IEC 68-2-32:1975
Environmental testing — Part 2.1 Test Ed: free fall.

Appendix A

Model-specific data

DirectFET devices are available in a growing range of can sizes and device outlines. At present, there are 19 variants in three can sizes. Devices shown here with the die outlined in red use standardised pad layouts (see page 4).

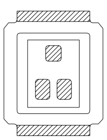
This appendix contains the following information about each combination of can size and device outline currently available:

- Device outline drawing
- Recommended substrate/PCB layout
- Suggested designs for stencils of 0.150mm (0.006") thickness

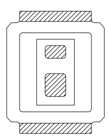
For more details about individual devices, and to find out their size and outline, refer to the relevant product data sheet and package outline drawing.

Small can outlines

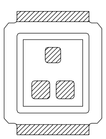
ST-outline



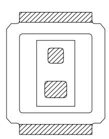
SQ-outline



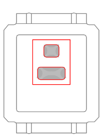
SJ-outline



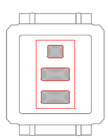
SH-outline



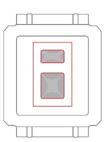
S1-outline



S2-outline

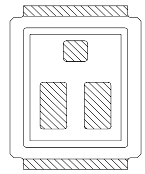


SB-outline

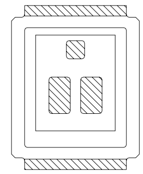


Medium can outlines

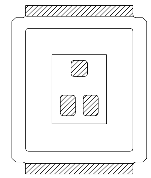
MT-outline



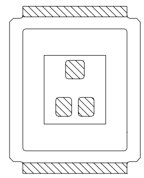
MX-outline



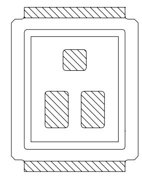
MP-outline



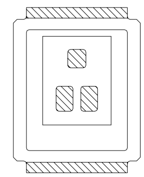
MQ-outline



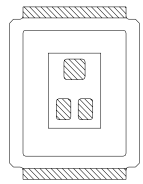
MN-outline



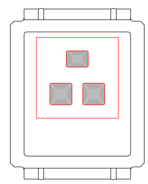
MZ-outline



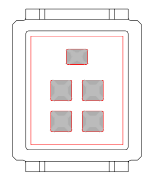
MU-outline



M2-outline

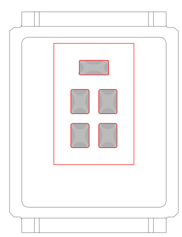


M4-outline

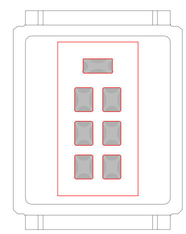


Large can outlines

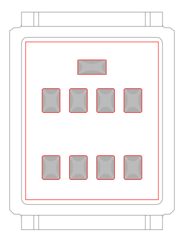
L4-outline



L6-outline



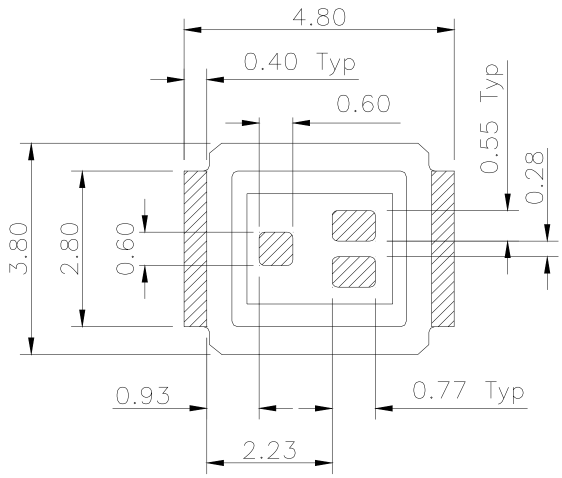
L8-outline



Appendix A.1 ST-outline

Device outline

Figure A.1.1 shows the outline for ST-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

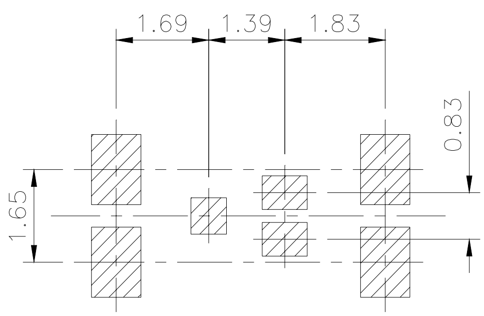


(dimensions in mm)

Figure A.1.1 ST-outline device outline

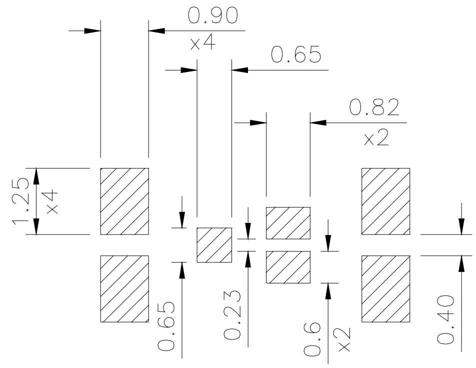
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.1.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.1.2(a) ST-outline substrate/PCB layout



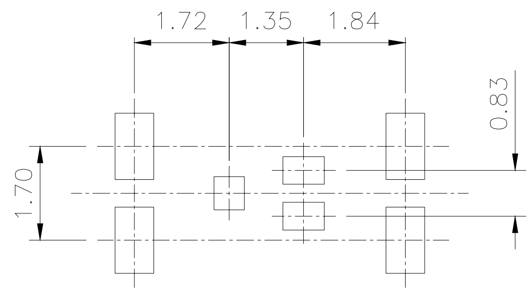
(dimensions in mm)

Figure A.1.2(b) ST-outline substrate/PCB layout

Stencil design

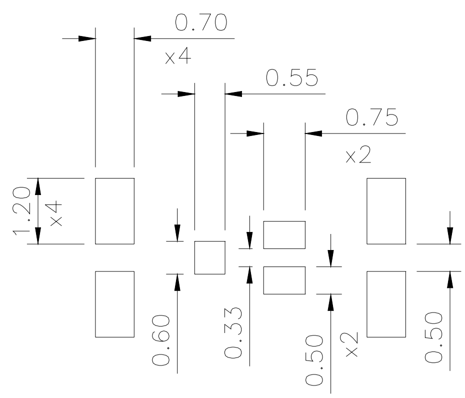
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.1.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.1.3(a) ST-outline stencil design



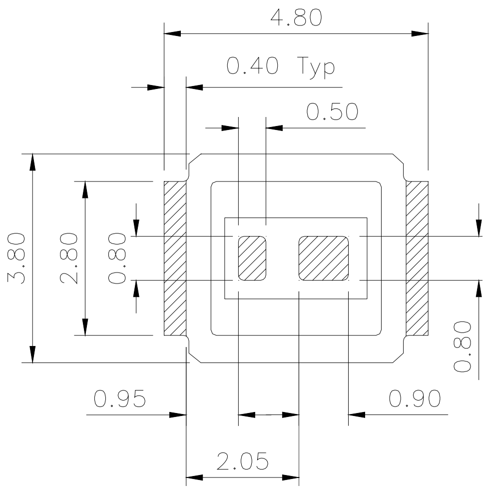
(dimensions in mm)

Figure A.1.3(b) ST-outline stencil design

Appendix A.2 SQ-outline

Device outline

Figure A.2.1 shows the outline for SQ-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

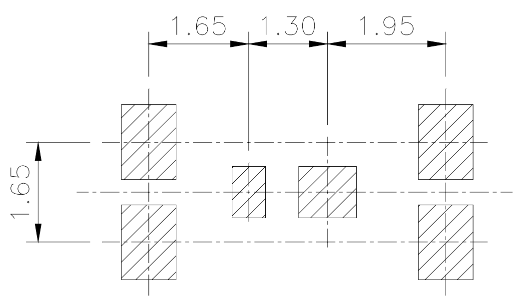


(dimensions in mm)

Figure A.2.1 SQ-outline device outline

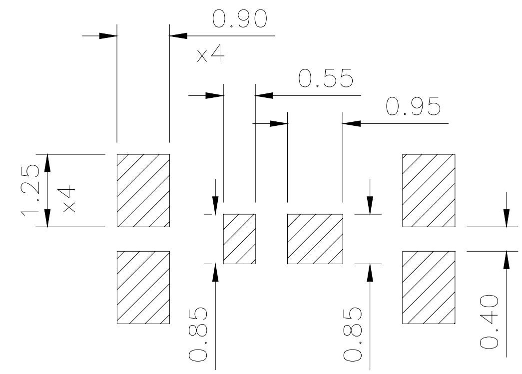
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.2.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.2.2(a) SQ-outline substrate/PCB layout



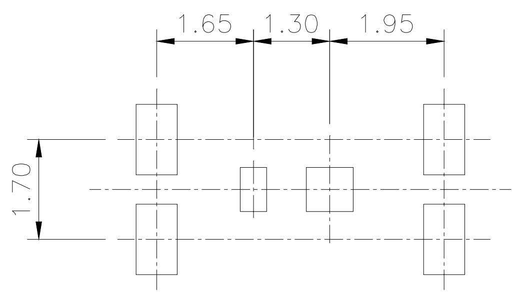
(dimensions in mm)

Figure A.2.2(b) SQ-outline substrate/PCB layout

Stencil design

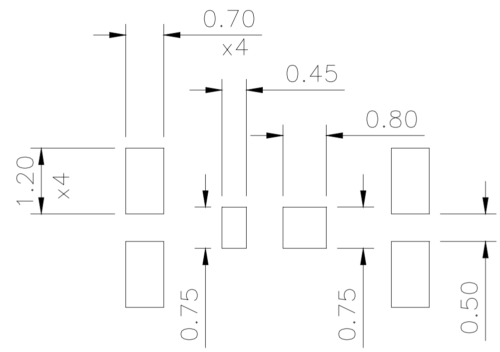
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.2.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.2.3(a) SQ-outline stencil design



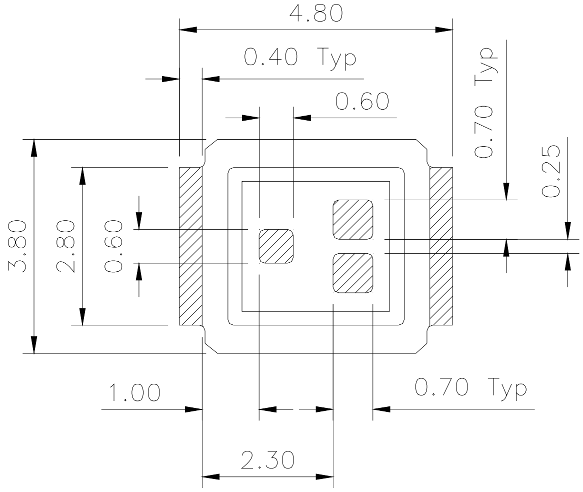
(dimensions in mm)

Figure A.2.3(b) SQ-outline stencil design

Appendix A.3 SJ-outline

Device outline

Figure A.3.1 shows the outline for SJ-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

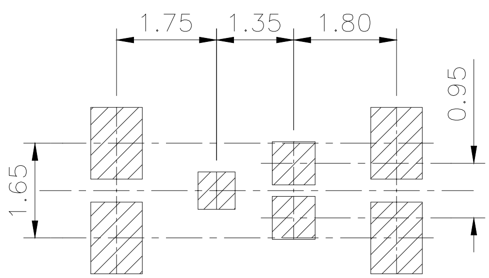


(dimensions in mm)

Figure A.3.1 SJ-outline device outline

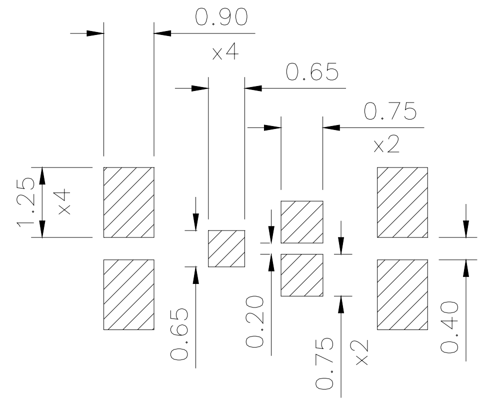
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.3.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.3.2(a) SJ-outline substrate/PCB layout



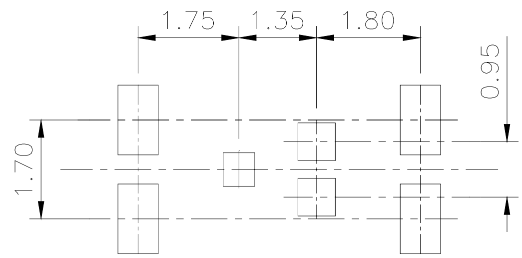
(dimensions in mm)

Figure A.3.2(b) SJ-outline substrate/PCB layout

Stencil design

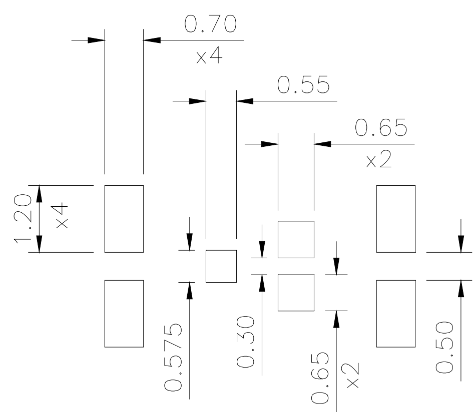
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.3.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.3.3(a) SJ-outline stencil design



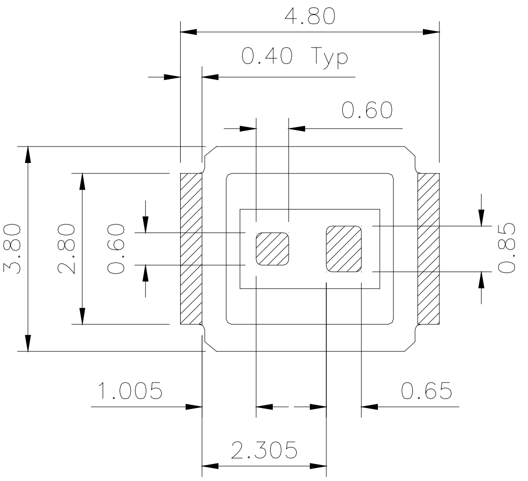
(dimensions in mm)

Figure A.3.3(b) SJ-outline stencil design

Appendix A.4 SH-outline

Device outline

Figure A.4.1 shows the outline for SH-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

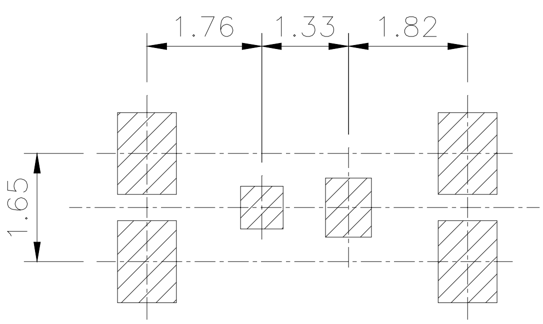


(dimensions in mm)

Figure A.4.1 SH-outline device outline

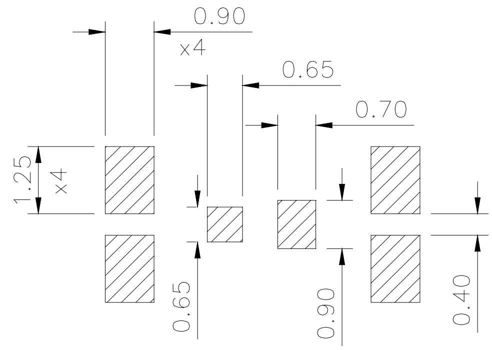
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.4.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.4.2(a) SH-outline substrate/PCB layout



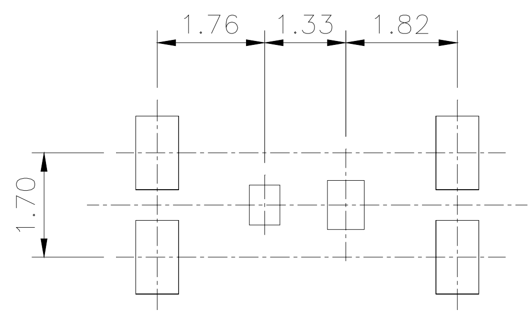
(dimensions in mm)

Figure A.4.2(b) SH-outline substrate/PCB layout

Stencil design

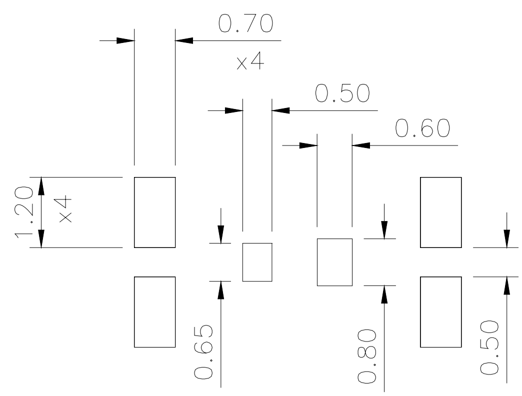
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.4.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.4.3(a) SH-outline stencil design



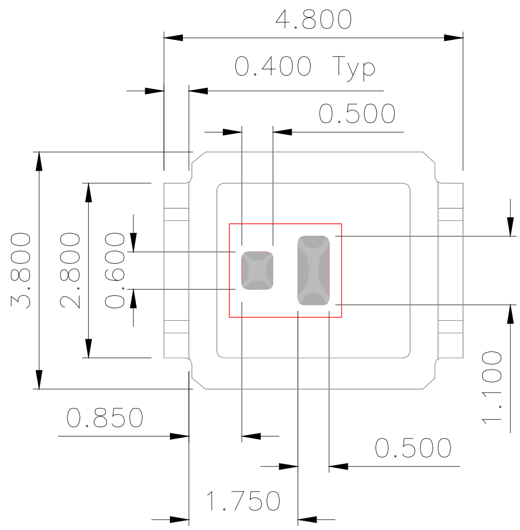
(dimensions in mm)

Figure A.4.3(b) SH-outline stencil design

Appendix A.5 S1-outline

Device outline

Figure A.5.1 shows the outline for S1-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

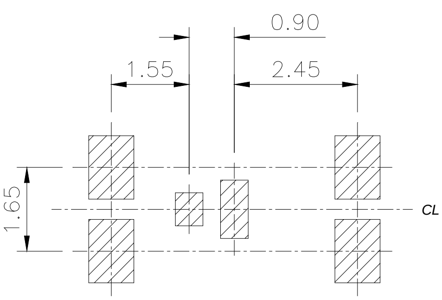


(dimensions in mm)

Figure A.5.1 S1-outline device outline

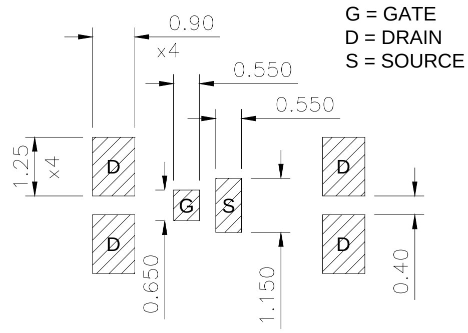
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.5.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.5.2(a) S1-outline substrate/PCB layout



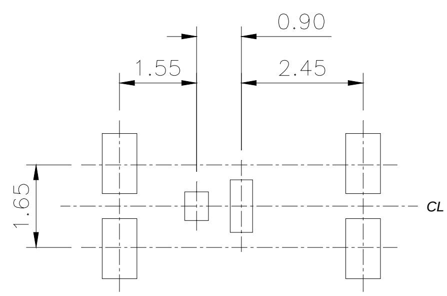
(dimensions in mm)

Figure A.5.2(b) S1-outline substrate/PCB layout

Stencil design

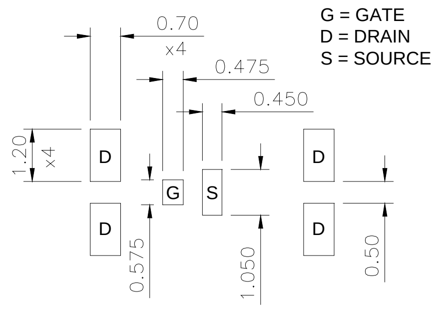
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.5.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.5.3(a) S1-outline stencil design



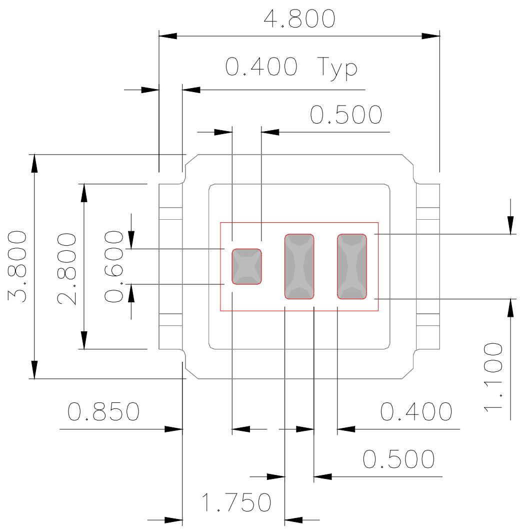
(dimensions in mm)

Figure A.5.3(b) S1-outline stencil design

Appendix A.6 S2-outline

Device outline

Figure A.6.1 shows the outline for S2-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

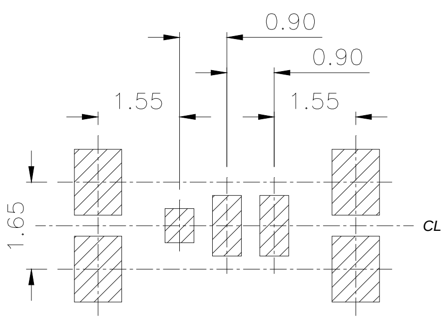


(dimensions in mm)

Figure A.6.1 S2-outline device outline

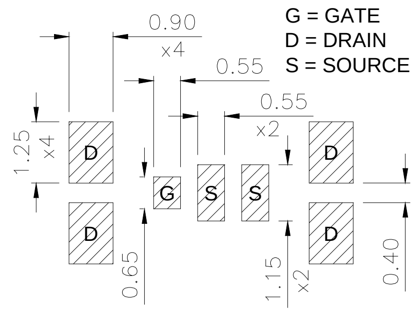
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.6.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.6.2(a) S2-outline substrate/PCB layout



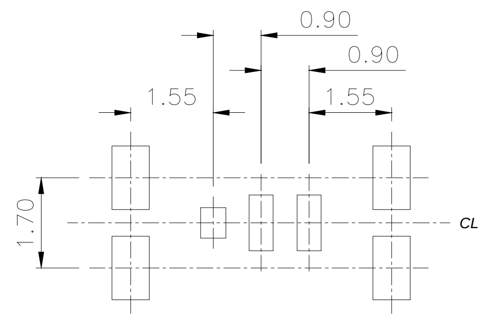
(dimensions in mm)

Figure A.6.2(b) S2-outline substrate/PCB layout

Stencil design

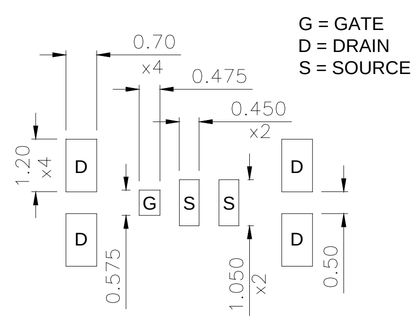
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.6.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.6.3(a) S2-outline stencil design



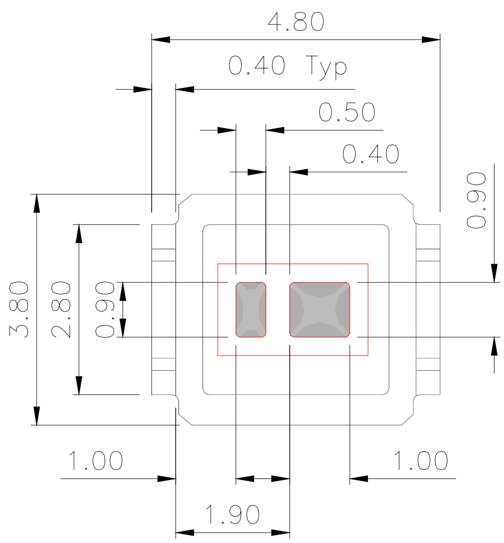
(dimensions in mm)

Figure A.6.3(b) S2-outline stencil design

Appendix A.7 SB-outline

Device outline

Figure A.7.1 shows the outline for SB-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

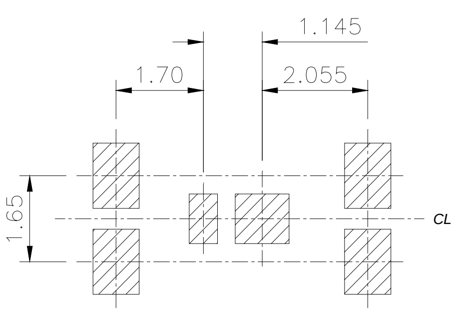


(dimensions in mm)

Figure A.7.1 SB-outline device outline

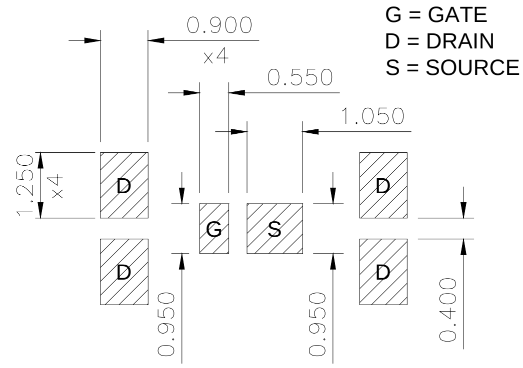
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.7.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.7.2(a) SB-outline substrate/PCB layout



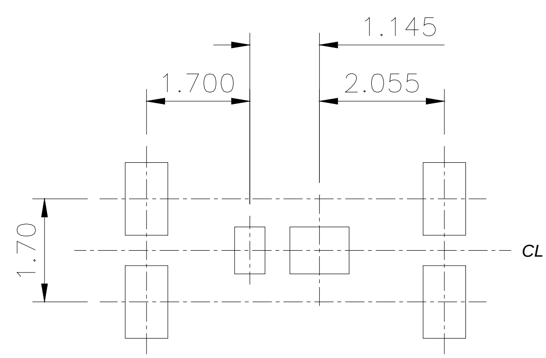
(dimensions in mm)

Figure A.7.2(b) SB-outline substrate/PCB layout

Stencil design

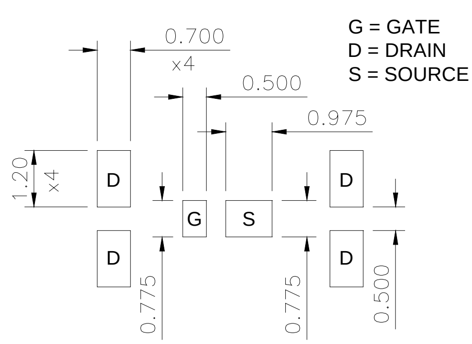
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.7.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.7.3(a) SB-outline stencil design



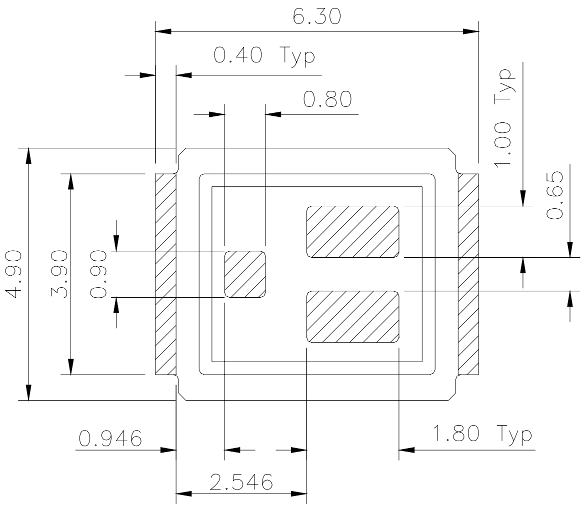
(dimensions in mm)

Figure A.7.3(b) SB-outline stencil design

Appendix A.8 MT-outline

Device outline

Figure A.8.1 shows the outline for MT-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

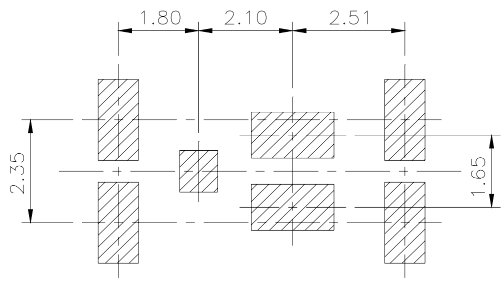


(dimensions in mm)

Figure A.8.1 MT-outline device outline

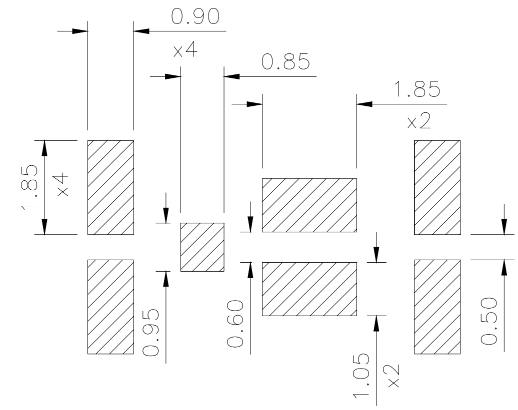
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.8.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.8.2(a) MT-outline substrate/PCB layout



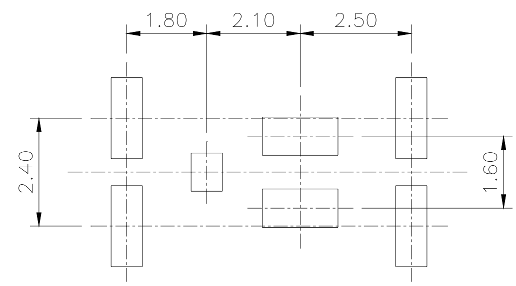
(dimensions in mm)

Figure A.8.2(b) MT-outline substrate/PCB layout

Stencil design

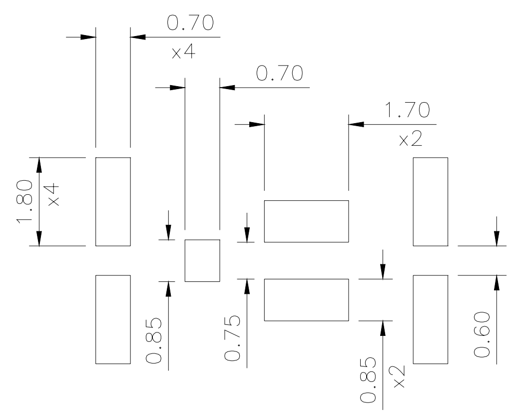
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.8.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.8.3(a) MT-outline stencil design



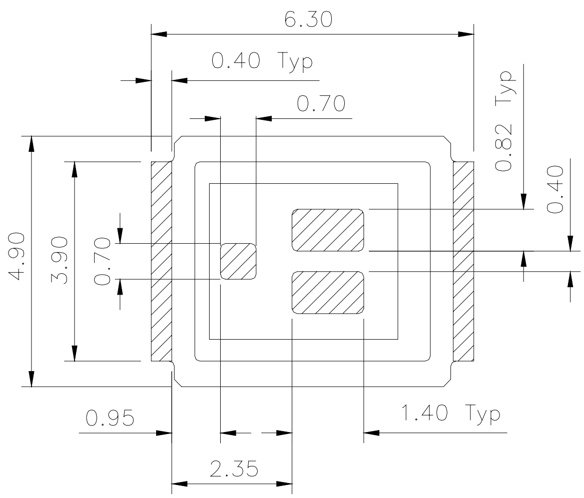
(dimensions in mm)

Figure A.8.3(b) MT-outline stencil design

Appendix A.9 MX-outline

Device outline

Figure A.9.1 shows the outline for MX-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

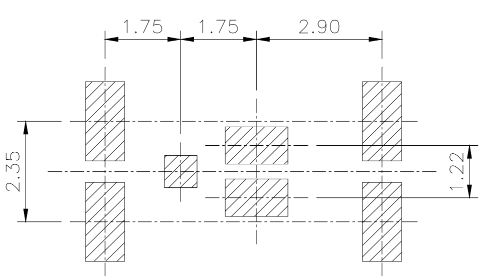


(dimensions in mm)

Figure A.9.1 MX-outline device outline

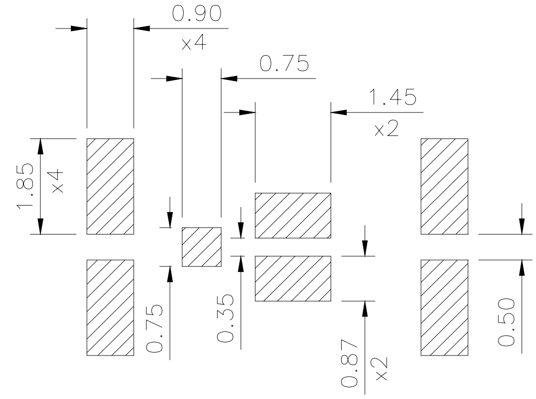
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.9.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.9.2(a) MX-outline substrate/PCB layout



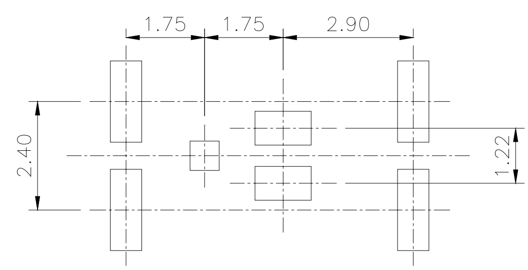
(dimensions in mm)

Figure A.9.2(b) MX-outline substrate/PCB layout

Stencil design

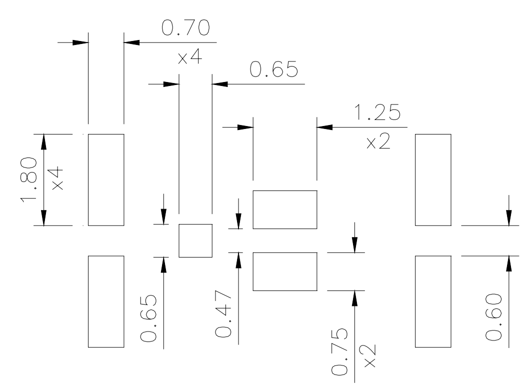
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.9.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.9.3(a) MX-outline stencil design



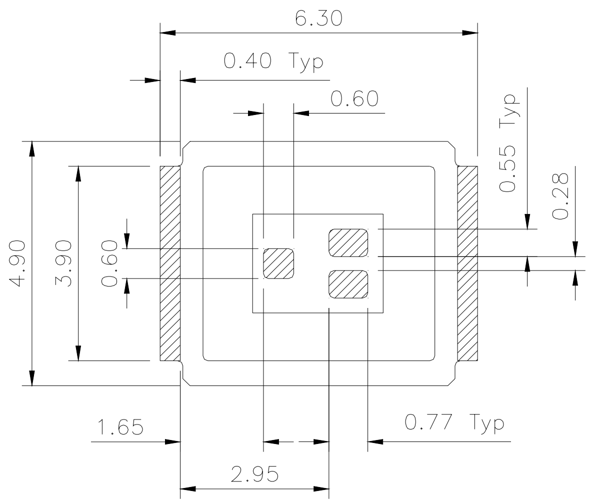
(dimensions in mm)

Figure A.9.3(b) MX-outline stencil design

Appendix A.10 MP-outline

Device outline

Figure A.10.1 shows the outline for MP-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

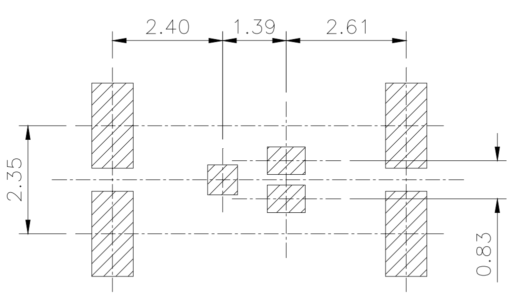


(dimensions in mm)

Figure A.10.1 MP-outline device outline

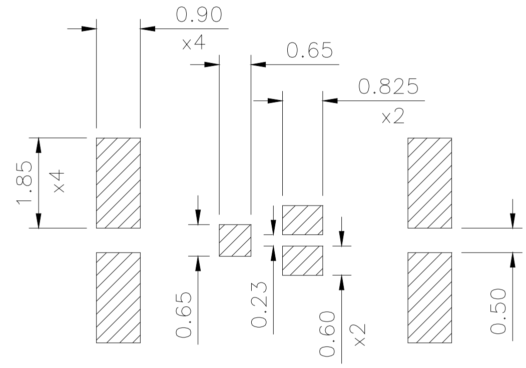
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.10.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.10.2(a) MP-outline substrate/PCB layout



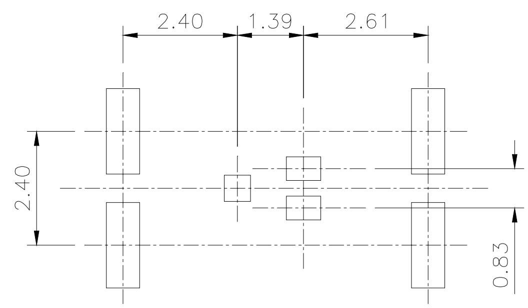
(dimensions in mm)

Figure A.10.2(b) MP-outline substrate/PCB layout

Stencil design

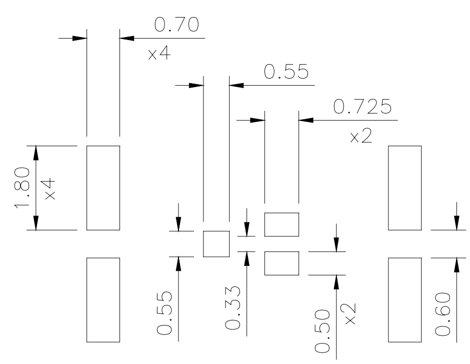
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.10.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.10.3(a) MP-outline stencil design



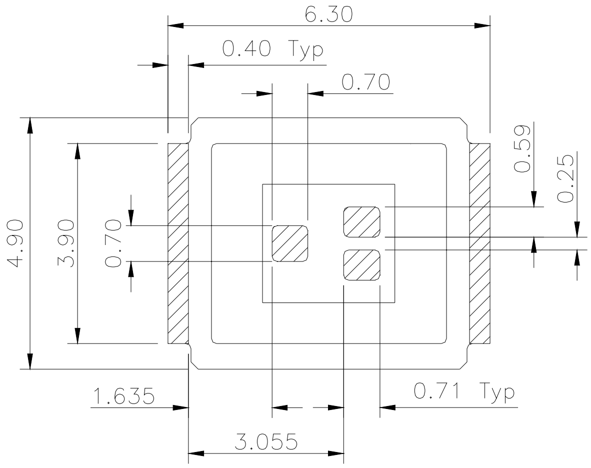
(dimensions in mm)

Figure A.10.3(b) MP-outline stencil design

Appendix A.11 MQ-outline

Device outline

Figure A.11.1 shows the outline for MQ-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

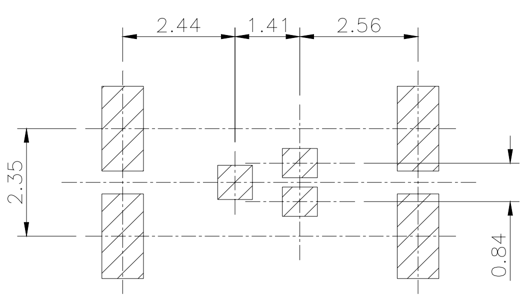


(dimensions in mm)

Figure A.11.1 MQ-outline device outline

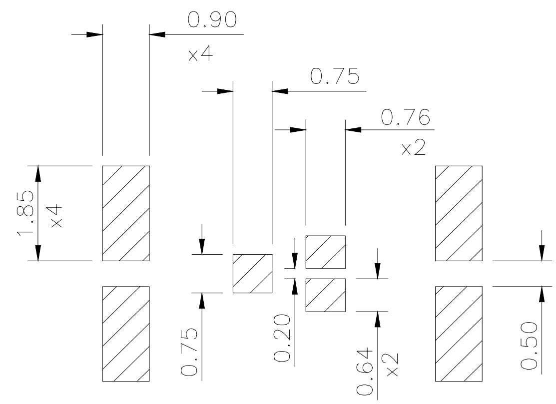
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.11.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.11.2(a) MQ-outline substrate/PCB layout



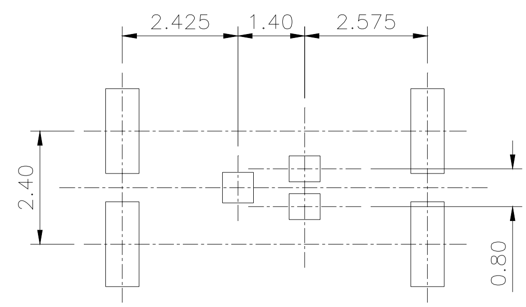
(dimensions in mm)

Figure A.11.2(b) MQ-outline substrate/PCB layout

Stencil design

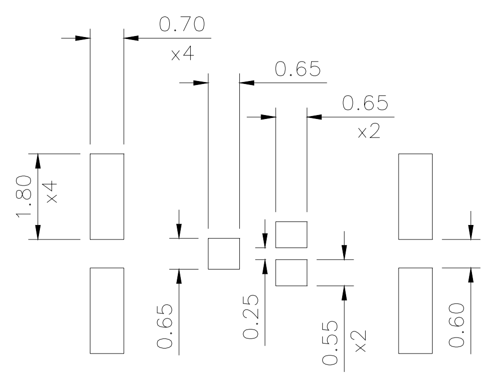
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.11.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.11.3(a) MQ-outline stencil design



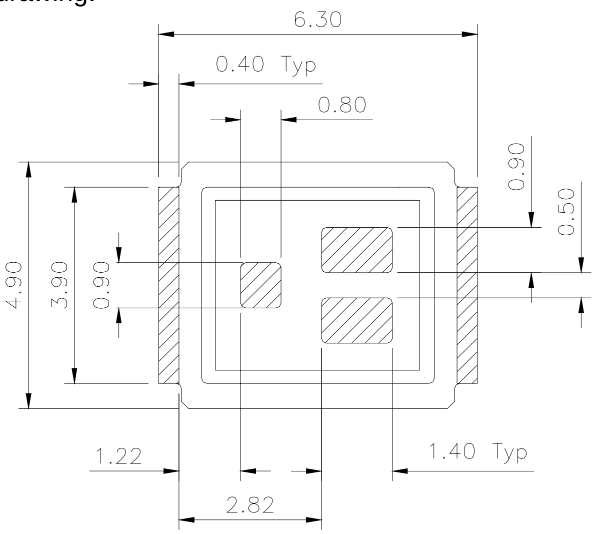
(dimensions in mm)

Figure A.11.3(b) MQ-outline stencil design

Appendix A.12 MN-outline

Device outline

Figure A.12.1 shows the outline for MN-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

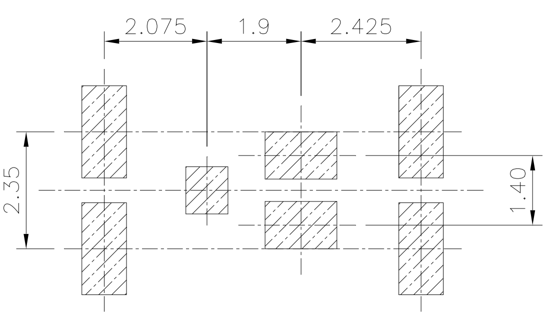


(dimensions in mm)

Figure A.12.1 MN-outline device outline

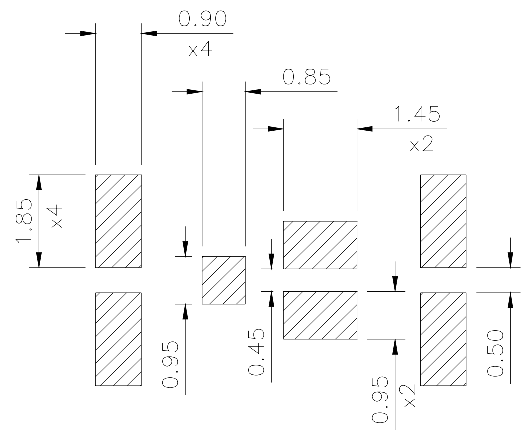
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.12.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.12.2(a) MN-outline substrate/PCB layout



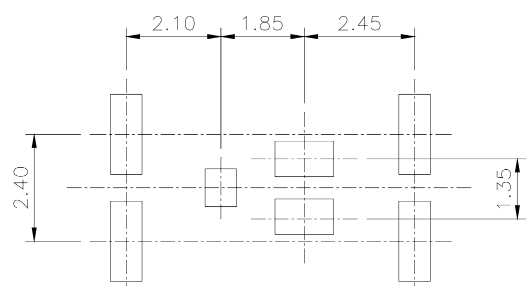
(dimensions in mm)

Figure A.12.2(b) MN-outline substrate/PCB layout

Stencil design

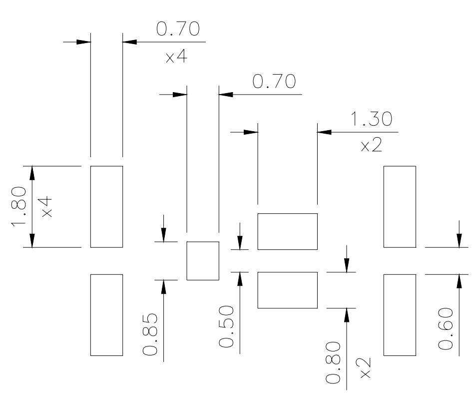
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.12.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.12.3(a) MN-outline stencil design



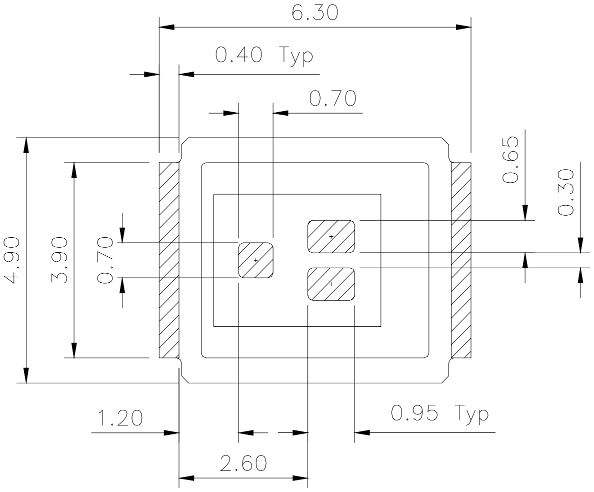
(dimensions in mm)

Figure A.12.3(b) MN-outline stencil design

Appendix A.13 MZ-outline

Device outline

Figure A.13.1 shows the outline for MZ-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

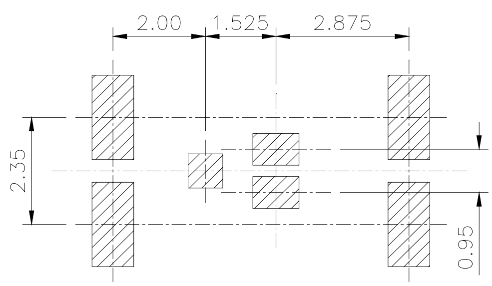


(dimensions in mm)

Figure A.13.1 MZ-outline device outline

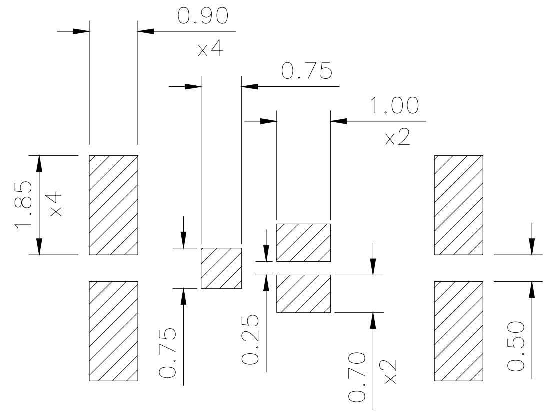
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.13.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.13.2(a) MZ-outline substrate/PCB layout



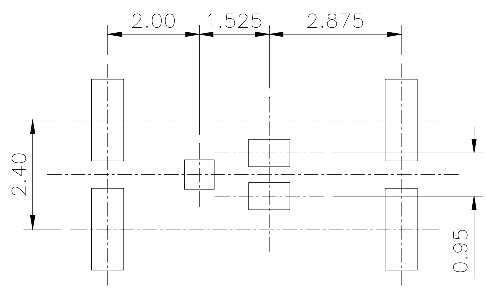
(dimensions in mm)

Figure A.13.2(b) MZ-outline substrate/PCB layout

Stencil design

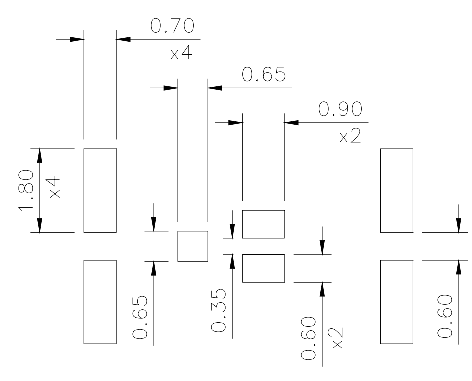
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.13.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.13.3(a) MZ-outline stencil design



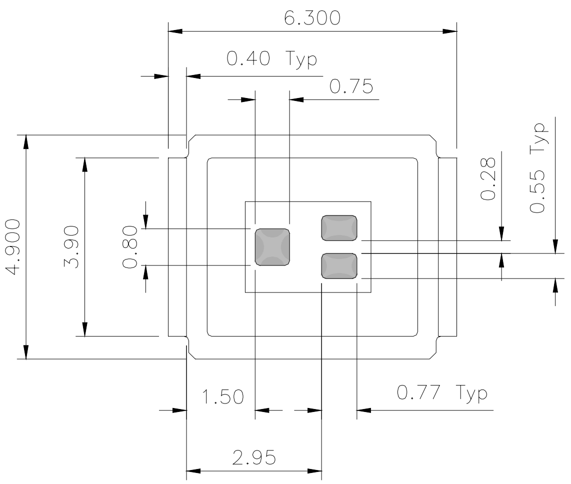
(dimensions in mm)

Figure A.13.3(b) MZ-outline stencil design

Appendix A.14 MU-outline

Device outline

Figure A.14.1 shows the outline for MU-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

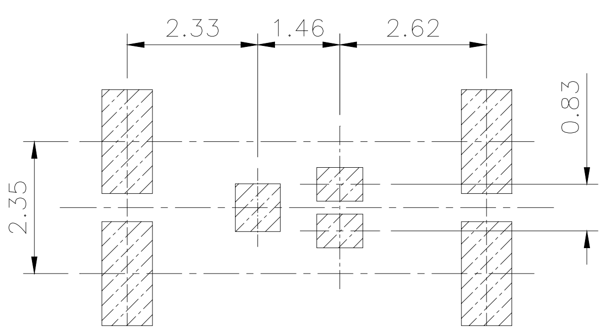


(dimensions in mm)

Figure A.14.1 MU-outline device outline

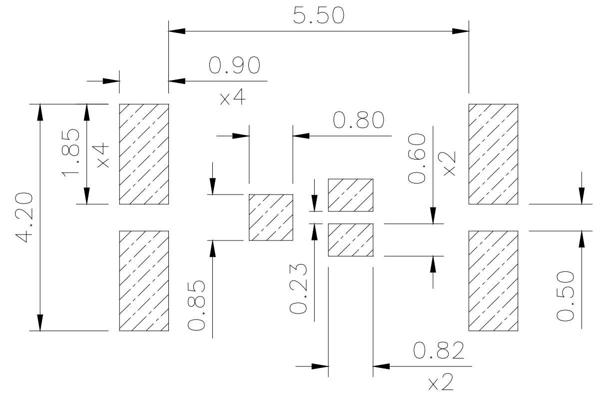
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.14.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.14.2(a) MU-outline substrate/PCB layout



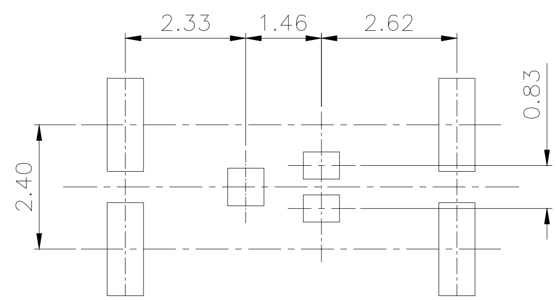
(dimensions in mm)

Figure A.14.2(b) MU-outline substrate/PCB layout

Stencil design

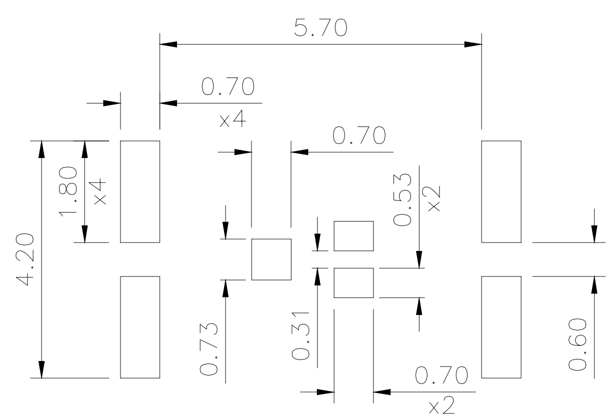
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.14.3 (a and b).

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.14.3(a) MU-outline stencil design



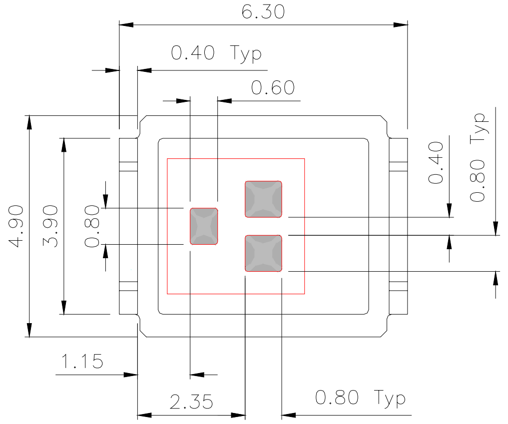
(dimensions in mm)

Figure A.14.3(b) MU-outline stencil design

Appendix A.15 M2-outline

Device outline

Figure A.15.1 shows the outline for M2-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

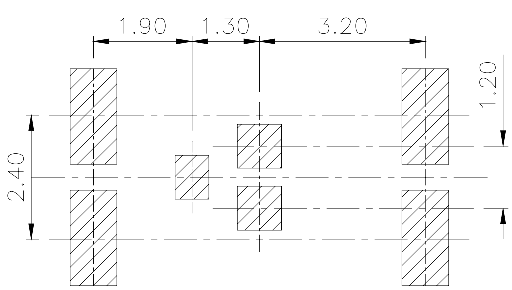


(dimensions in mm)

Figure A.15.1 M2-outline device outline

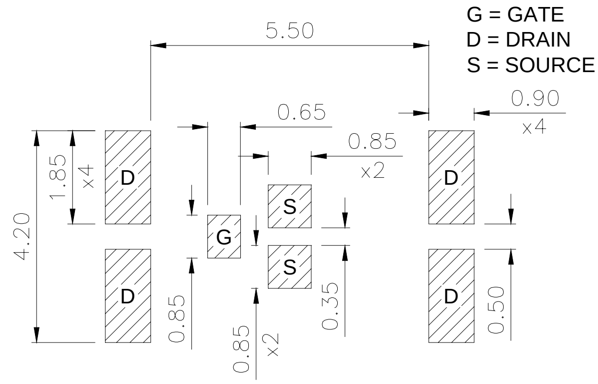
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.15.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.15.2(a) M2-outline substrate/PCB layout



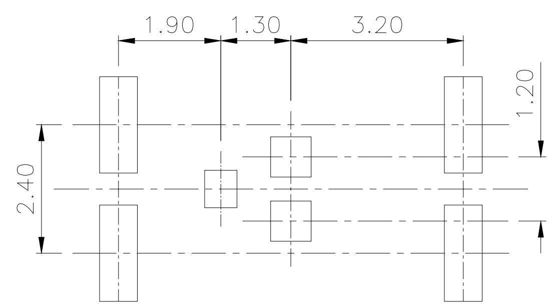
(dimensions in mm)

Figure A.15.2(b) M2-outline substrate/PCB layout

Stencil design

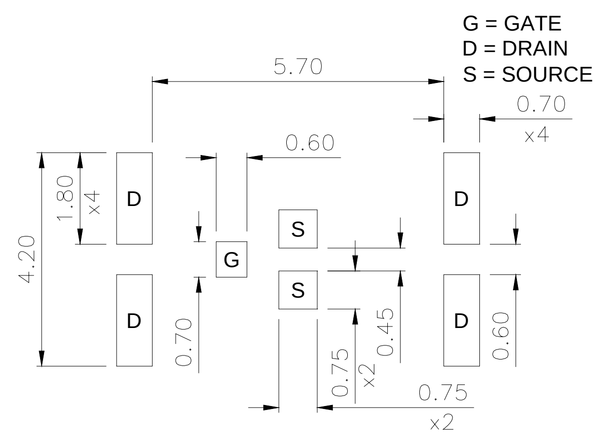
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.15.3 (a and b)

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.15.3(a) M2-outline stencil design



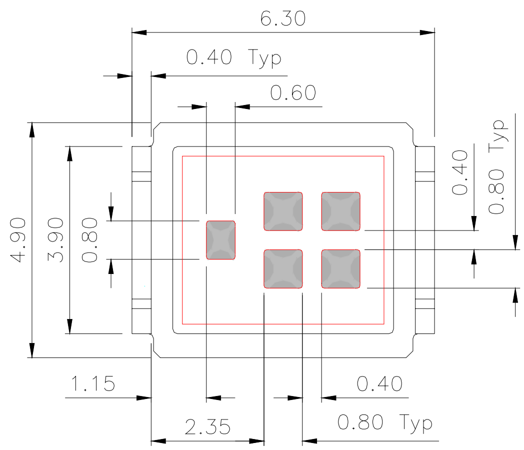
(dimensions in mm)

Figure A.15.3(b) M2-outline stencil design

Appendix A.16 M4-outline

Device outline

Figure A.16.1 shows the outline for M4-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

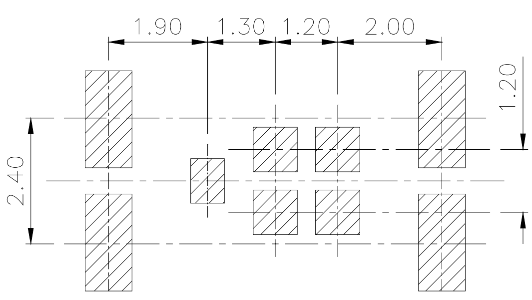


(dimensions in mm)

Figure A.16.1 M4-outline device outline

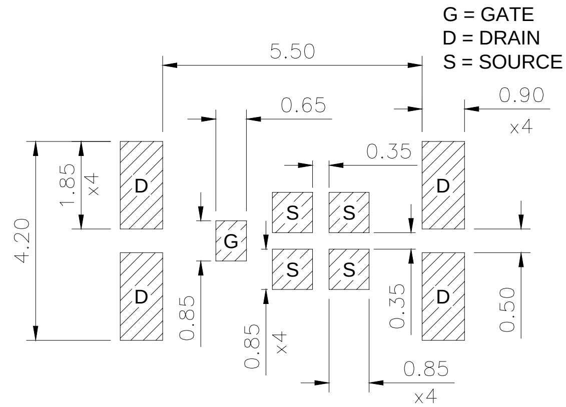
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.16.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.16.2(a) M4-outline substrate/PCB layout



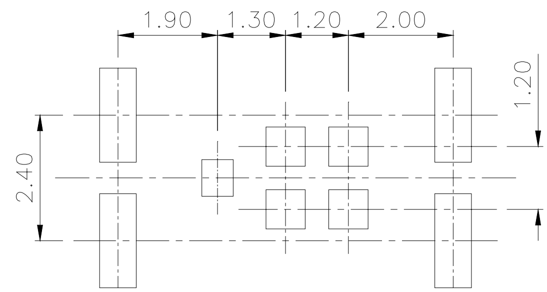
(dimensions in mm)

Figure A.16.2(b) M4-outline substrate/PCB layout

Stencil design

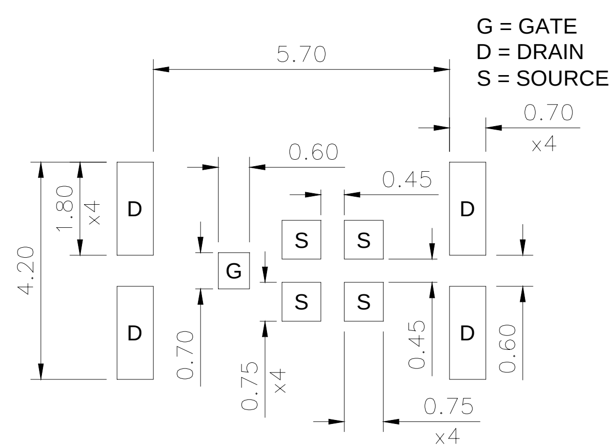
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.16.3 (a and b)

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.16.3(a) M4-outline stencil design



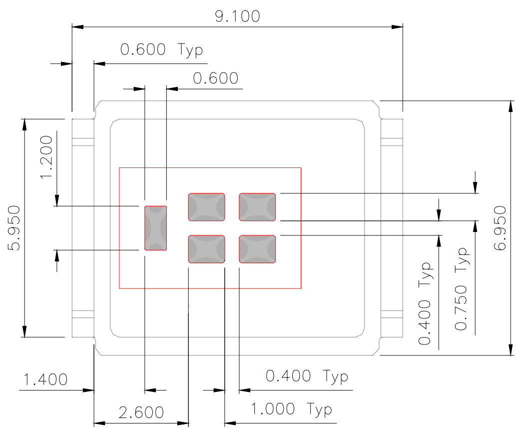
(dimensions in mm)

Figure A.16.3(b) M4-outline stencil design

Appendix A.17 L4-outline

Device outline

Figure A.17.1 shows the outline for L4-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

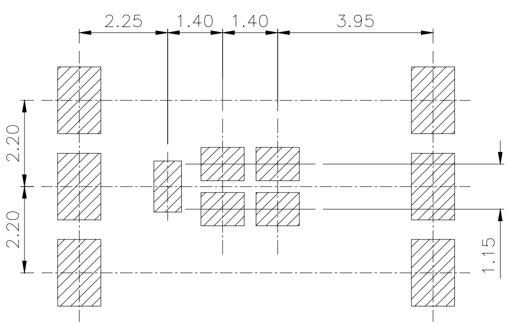


(dimensions in mm)

Figure A.17.1 L4-outline device outline

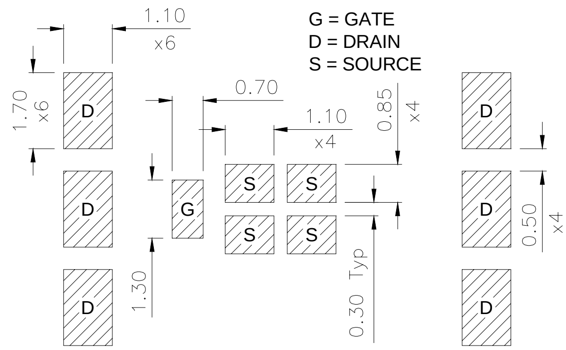
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.17.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.17.2(a) L4-outline substrate/PCB layout



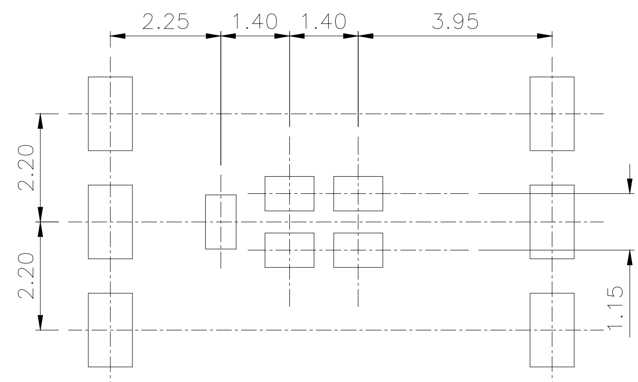
(dimensions in mm)

Figure A.17.2(b) L4-outline substrate/PCB layout

Stencil design

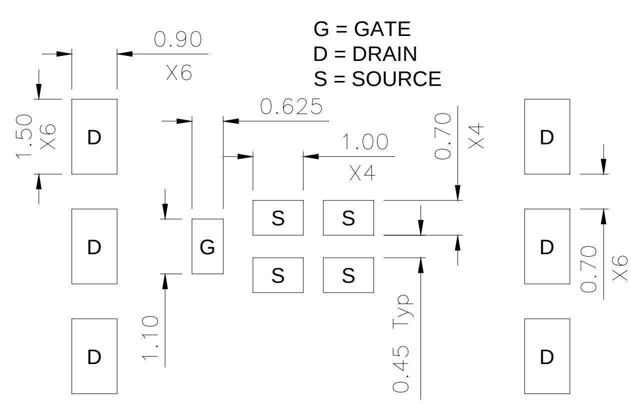
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.17.3 (a and b)

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.17.3(a) L4-outline stencil design



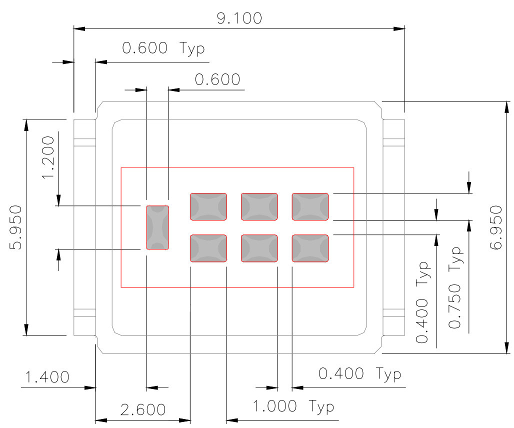
(dimensions in mm)

Figure A.17.3(b) L4-outline stencil design

Appendix A.18 L6-outline

Device outline

Figure A.18.1 shows the outline for L6-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

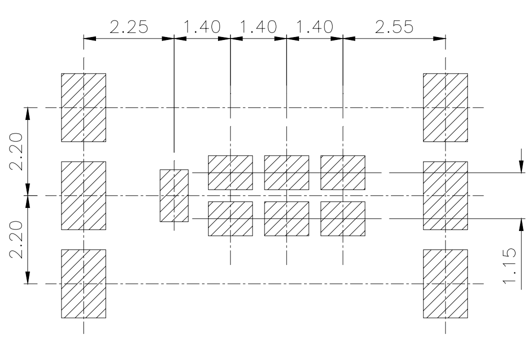


(dimensions in mm)

Figure A.18.1 L6-outline device outline

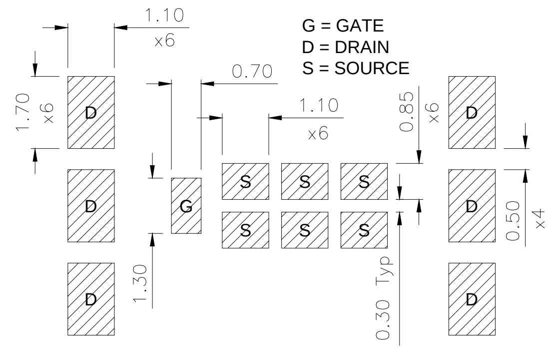
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.18.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.18.2(a) L6-outline substrate/PCB layout



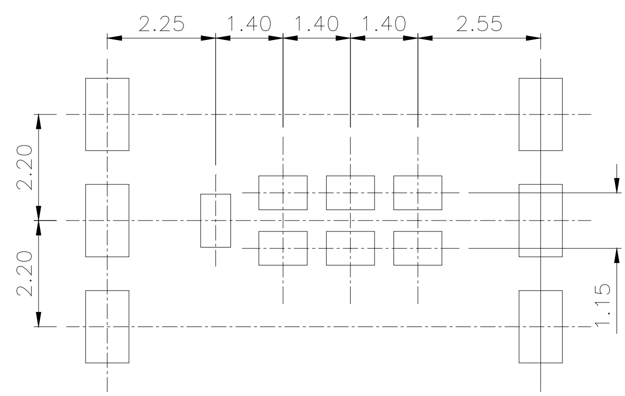
(dimensions in mm)

Figure A.18.2(b) L6-outline substrate/PCB layout

Stencil design

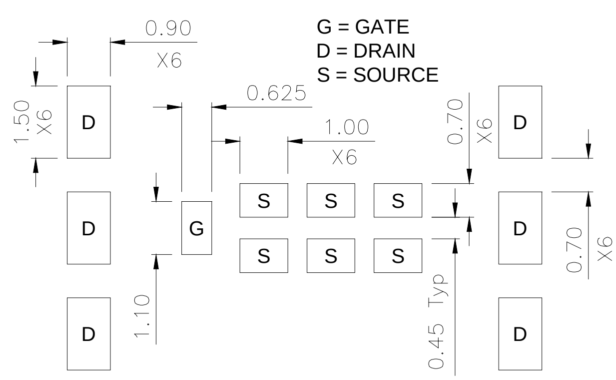
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.18.3 (a and b)

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.18.3(a) L6-outline stencil design



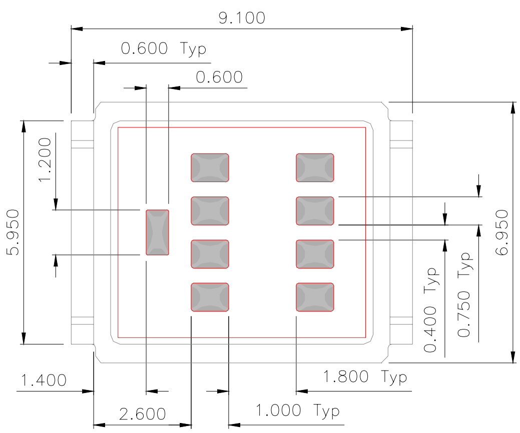
(dimensions in mm)

Figure A.18.3(b) L6-outline stencil design

Appendix A.19 L8-outline

Device outline

Figure A.19.1 shows the outline for L8-outline DirectFET devices. The relative pad positions are controlled to an accuracy of ±0.065mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing

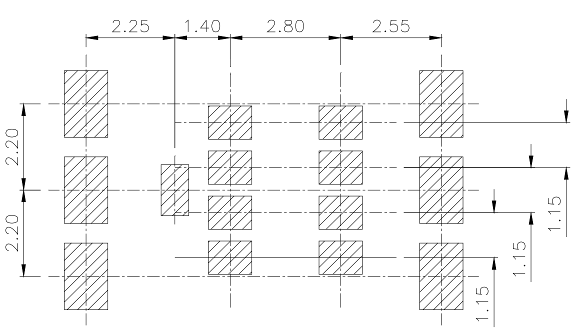


(dimensions in mm)

Figure A.19.1 L8-outline device outline

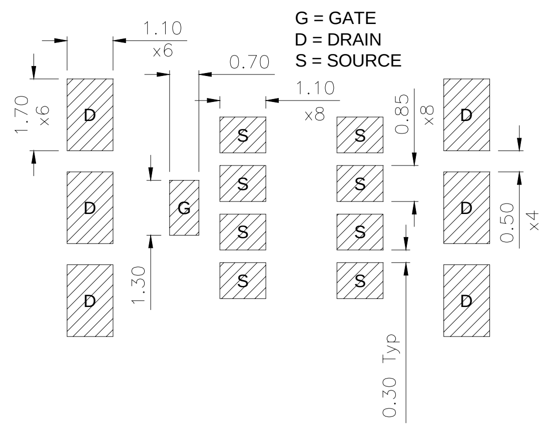
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.19.2 (a and b). Gate and source pads on the substrate are oversized by 0.025mm (0.001") on each side. Drain pads are thickened by 0.500mm (0.020"). Each drain contact pad is divided into two separate pads, as this has been shown to improve solder joint quality.



(dimensions in mm)

Figure A.19.2(a) L8-outline substrate/PCB layout



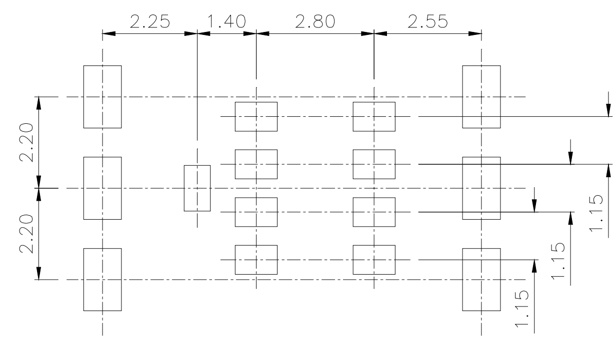
(dimensions in mm)

Figure A.19.2(b) L8-outline substrate/PCB layout

Stencil design

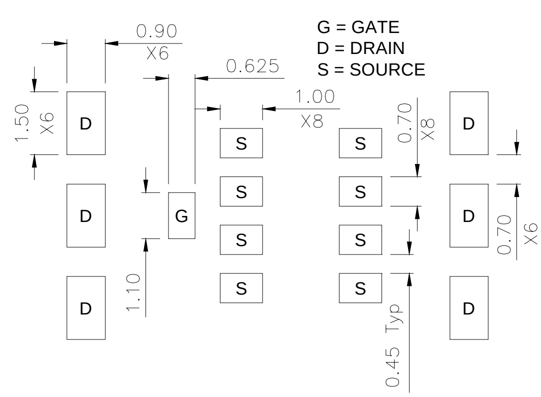
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.19.3 (a and b)

Note: This design is for a stencil thickness of 0.150mm (0.006"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.19.3(a) L8-outline stencil design



(dimensions in mm)

Figure A.19.3(b) L8-outline stencil design