A Practical Guide to High-Speed Printed-Circuit-Board Layout

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Despite its critical nature in high-speed circuitry, printed-circuit-board (PCB) layout is often one of the last steps in the design process. There are many aspects to high-speed PCB layout; volumes have been written on the subject. This article addresses high-speed layout from a practical perspective. A major aim is to help sensitize newcomers to the many and various considerations they need to address when designing board layouts for high-speed circuitry. But it is also intended as a refresher to benefit those who have been away from board layout for a while. Not every topic can be covered in detail in the space available here, but we address key areas that can have the greatest payoff in improving circuit performance, reducing design time, and minimizing time-consuming revisions.

Although the focus is on circuits involving high-speed op amps, the topics and techniques discussed here are generally applicable to layout of most other high-speed analog circuits. When op amps operate at high RF frequencies, circuit performance is heavily dependent on the board layout. A high-performance circuit design that looks good "on paper" can render mediocre performance when hampered by a careless or sloppy layout. Thinking ahead and paying attention to salient details throughout the layout process will help ensure that the circuit performs as expected.

The Schematic

Although there is no guarantee, a good layout starts with a good schematic. Be thoughtful and generous when drawing a schematic, and think about signal flow through the circuit. A schematic that has a natural and steady flow from left to right will tend to have a good flow on the board as well. Put as much useful information on the schematic as possible. The designers, technicians, and engineers who will work on this job will be most appreciative, including us; at times we are asked by customers to help with a circuit because the designer is no longer there.

What kind of information belongs on a schematic besides the usual reference designators, power dissipations, and tolerances? Here are a few suggestions that can turn an ordinary schematic into a *super*schematic! Add waveforms, mechanical information about the housing or enclosure, trace lengths, keep-out areas; designate which components need to be on top of the board; include tuning information, component value ranges, thermal information, controlled impedance lines, notes, brief circuit operating descriptions … (and the list goes on).

Trust No One

If you're not doing your own layout, be sure to set aside ample time to go through the design with the layout person. An ounce of prevention at this point is worth more than a pound of cure! Don't expect the layout person to be able to read your mind. Your inputs and guidance are most critical at the beginning of the layout process. The more information you can provide, and the more involved you are throughout the layout process, the better the board will turn out. Give the designer interim completion points—at which you want to be notified of the layout progress for a quick review. This "loop closure" prevents a layout from going too far astray and will minimize reworking the board layout.

Your instructions for the designer should include: a brief description of the circuit's functions; a sketch of the board that shows the input and output locations; the board *stack up* (i.e., how thick the board will be, how many layers, details of signal layers and planes—power, ground, analog, digital, and RF); which signals need to be on each layer; where the critical components need to be located; the exact location of bypassing components; which traces are critical; which lines need to be controlled-impedance lines; which lines need to have matched lengths; component sizes; which traces need to kept away from (or near) each other; which *circuits* need to be kept away from (or near) each other; which *components* need to be close to (or away from) each other; which components go on the top and the bottom of the board. You'll never get a complaint for giving someone too much information—too *little*, yes; too much, no.

> *A learning experience:* About 10 years ago I designed a multilayer surface-mounted board—with components on both sides of the board. The board was screwed into a gold-plated aluminum housing with many screws (because of a stringent vibration spec). Bias feedthrough pins poked up through the board. The pins were wire-bonded to the PCB. It was a complicated assembly. Some of the components on the board were to be *SAT* (set at test). But I hadn't specified where these components should be. Can you guess where some of them were placed? Right! On the bottom of the board. The production engineers and technicians were not very happy when they had to tear the assembly apart, set the values, and then reassemble everything. I didn't make that mistake again.

Location, Location, Location

As in real estate, location is everything. Where a circuit is placed on a board, where the individual circuit components are located, and what other circuits are in the neighborhood are all critical.

Typically, input-, output-, and power locations are defined, but what goes on between them is "up for grabs." This is where paying attention to the layout details will yield significant returns. Start with critical component placement, in terms of both individual circuits and the entire board. Specifying the critical component locations and signal routing paths from the beginning helps ensure that the design will work the way it's intended to. Getting it right the first time lowers cost and stress—and reduces cycle time.

Power-Supply Bypassing

Bypassing the power supply at the amplifier's supply terminals to minimize noise is a critical aspect of the PCB design process—both for high-speed op amps and any other high-speed circuitry. There are two commonly used configurations for bypassing high-speed op amps.

Rails to ground: This technique, which works best in most cases, uses multiple parallel capacitors connected from the op amp's power-supply pins directly to ground. Typically, two parallel capacitors are sufficient—but some circuits may benefit from additional capacitors in parallel.

Paralleling different capacitor values helps ensure that the power supply pins see a low ac impedance across a wide band of frequencies. This is especially important at frequencies where the op amp *power-supply rejection* (PSR) is rolling off. The capacitors help compensate for the amplifier's decreasing PSR. Maintaining a low impedance path to ground for many decades of frequency will help ensure that unwanted noise doesn't find its way into the op amp. Figure 1 shows the benefits of multiple parallel capacitors. At lower frequencies the larger capacitors offer a low impedance path to ground. Once those capacitors reach self resonance, the capacitive quality diminishes and the capacitors become inductive. That is why it is important to use multiple capacitors: when one capacitor's frequency response is rolling off, another is becoming significant, thereby maintaining a low ac impedance over many decades of frequency.

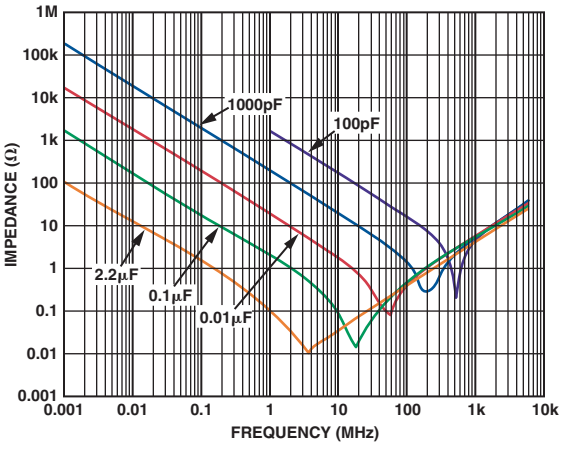

Figure 1. Capacitor impedance vs. frequency.

Starting directly at the op amp's power-supply pins; the capacitor with the lowest value and smallest physical size should be placed on the same side of the board as the op amp—and as close to the amplifier as possible. The ground side of the capacitor should be connected into the ground plane with minimal lead- or trace length. This ground connection should be as close as possible to the amplifier's load to minimize disturbances between the rails and ground. Figure 2 illustrates this technique.

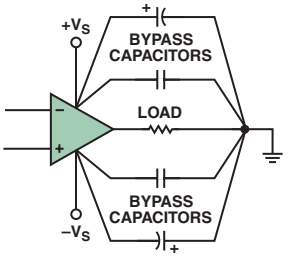

Figure 2. Parallel-capacitor rails-to-ground bypassing.

This process should be repeated for the next-higher-value capacitor. A good place to start is with 0.01 µF for the smallest value, and a 2.2-µF—or larger—electrolytic with low ESR for the next capacitor. The 0.01 µF in the 0508 case size offers low series inductance and excellent high-frequency performance.

Rail to rail: An alternate configuration uses one or more bypass capacitors tied between the positive- and negative supply rails of the op amp. This method is typically used when it is difficult to get all four capacitors in the circuit. A drawback to this approach is that the capacitor case size can become larger, because the voltage across the capacitor is double that of the single-supply bypassing method. The higher voltage requires a higher breakdown rating, which translates into a larger case size. This option can, however, offer improvements to both PSR and distortion performance.

Since each circuit and layout is different; the configuration, number, and values of the capacitors are determined by the actual circuit requirements.

Parasitics

Parasitics are those nasty little gremlins that creep into your PCB (quite literally) and wreak havoc within your circuit. They are the hidden stray capacitors and inductors that infiltrate high-speed circuits. They include inductors formed by package leads and excess trace lengths; pad-to-ground, pad-to-power-plane, and pad-to-trace capacitors; interactions with vias, and many more possibilities. Figure 3(a) is a typical schematic of a noninverting op amp. If parasitic elements were to be taken into account, however, the same circuit would look like Figure 3(b).

In high-speed circuits, it doesn't take much to influence circuit performance. Sometimes just a few tenths of a picofarad is enough. Case in point: if only 1 pF of additional stray parasitic capacitance is present at the inverting input, it can cause almost 2 dB of peaking in the frequency domain (Figure 4). If enough capacitance is present, it can cause instability and oscillations.

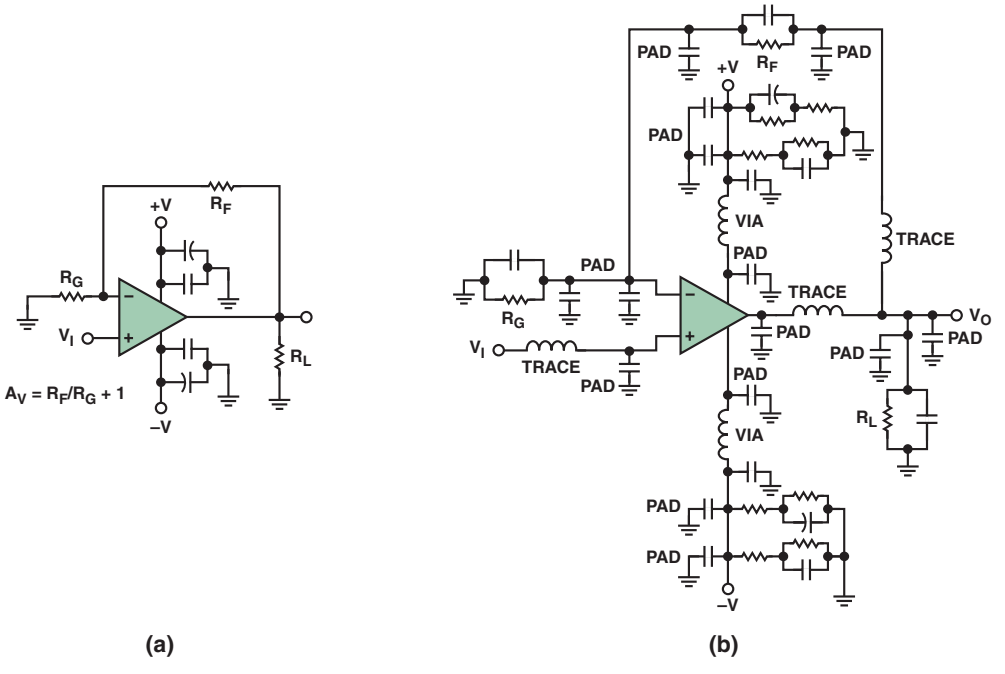

Figure 3. Typical op amp circuit, as designed (a) and with parasitics (b).

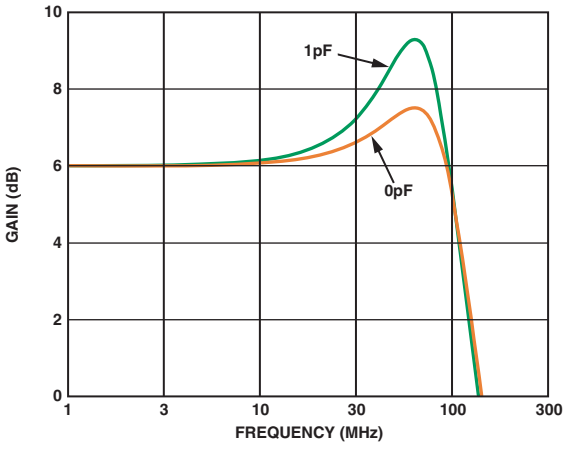

Figure 4. Additional peaking caused by parasitic capacitance.

A few basic formulas for calculating the size of those gremlins can come in handy when seeking the sources of the problematic parasitics. Equation 1 is the formula for a parallel-plate capacitor (see Figure 5).

$$C = \frac{kA}{11.3d}\,\text{pF} \tag{1}$$

C is the capacitance, A is the area of the plate in cm^2, k is the relative dielectric constant of board material, and d is the distance between the plates in centimeters.

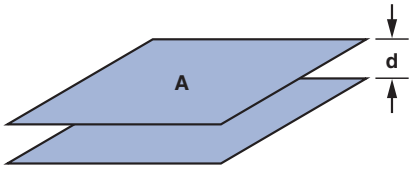

Figure 5. Capacitance between two plates.

Strip inductance is another parasitic to be considered, resulting from excessive trace length and lack of ground plane. Equation 2 shows the formula for trace inductance. See Figure 6.

$$\text{Inductance} = 0.0002L\left[\ln\frac{2L}{(W+H)} + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\mu\text{H} \tag{2}$$

W is the trace width, L is the trace length, and H is the thickness of the trace. All dimensions are in millimeters.

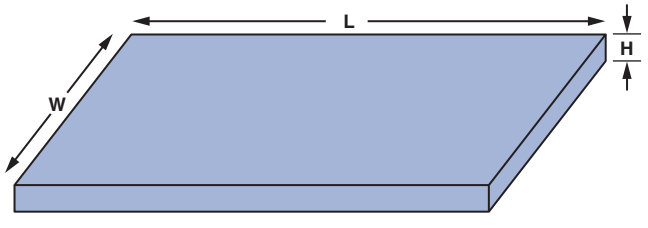

Figure 6. Inductance of a trace length.

The oscillation in Figure 7 shows the effect of a 2.54-cm trace length at the noninverting input of a high-speed op amp. The equivalent stray inductance is 29 nH (nanohenry), enough to cause a sustained low-level oscillation that persists throughout the period of the transient response. The picture also shows how using a ground plane mitigates the effects of stray inductance.

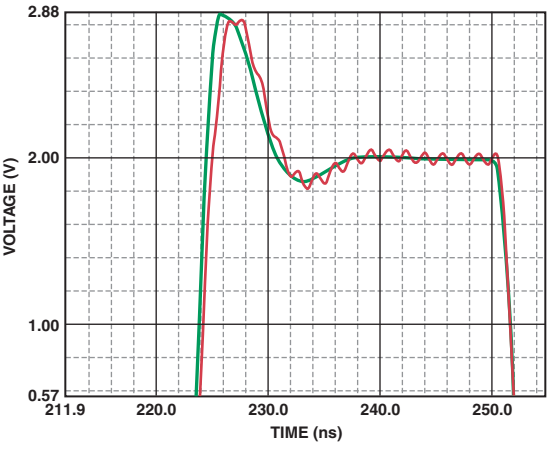

Figure 7. Pulse response with—and without—ground plane.

Vias are another source of parasitics; they can introduce both inductance and capacitance. Equation 3 is the formula for parasitic inductance (see Figure 8).

$$L = 2T\left[\ln\frac{4T}{d} + 1\right]\text{nH} \tag{3}$$

T is the thickness of the board and d is the diameter of the via in centimeters.

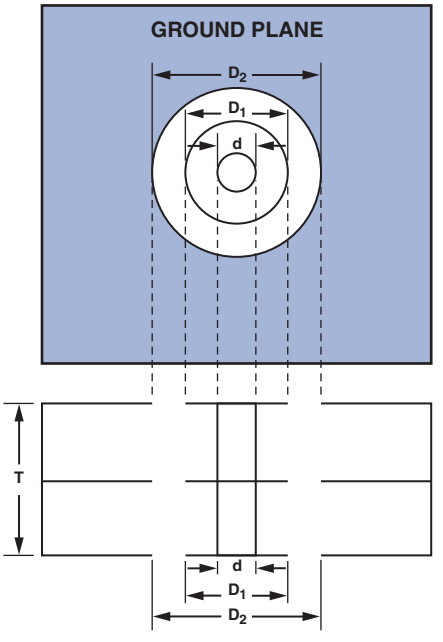

Figure 8. Via dimensions.

Equation 4 shows how to calculate the parasitic capacitance of a via (see Figure 8).

$$C = \frac{0.55\varepsilon_r TD_1}{D_2 - D_1}\,\text{pF} \tag{4}$$

ε_r is the relative permeability of the board material. T is the thickness of the board. D_1 is the diameter of the pad surrounding the via. D_2 is the diameter of the clearance hole in the ground plane. All dimensions are in centimeters. A single via in a 0.157-cm-thick board can add 1.2 nH of inductance and 0.5 pF of capacitance; this is why, when laying out boards, a constant vigil must be kept to minimize the infiltration of parasites!

Ground Plane

There is much more to discuss than can be covered here, but we'll highlight some of the key features and encourage the reader to pursue the subject in greater detail. A list of references appears at the end of this article.

A ground plane acts as a common reference voltage, provides shielding, enables heat dissipation, and reduces stray inductance (but it also increases parasitic capacitance). While there are many advantages to using a ground plane, care must be taken when implementing it, because there are limitations to what it can and cannot do.

Ideally, one layer of the PCB should be dedicated to serve as the ground plane. Best results will occur when the entire plane is unbroken. Resist the temptation to remove areas of the ground plane for routing other signals on this dedicated layer. The ground plane reduces trace inductance by magnetic-field cancellation between the conductor and the ground plane. When areas of the ground plane are removed, unexpected parasitic inductance can be introduced into the traces above or below the ground plane.

Because ground planes typically have large surface and cross-sectional areas, the resistance in the ground plane is kept to a minimum. At low frequencies, current will take the path of least resistance, but at high frequencies current follows the path of least *impedance*.

Nevertheless, there are exceptions, and sometimes less ground plane is better. High-speed *op amps* will perform better if the ground plane is removed from under the input and output pads. The stray capacitance introduced by the ground plane at the input, added to the op amp's input capacitance, lowers the phase margin and can cause instability. As seen in the parasitics discussion, 1 pF of capacitance at an op amp's input can cause significant peaking. Capacitive loading at the output—including strays—creates a pole in the feedback loop. This can reduce phase margin and could cause the circuit to become unstable.

Analog and digital circuitry, including grounds and ground planes, should be kept separate when possible. Fast-rising edges create current spikes flowing in the ground plane. These fast current spikes create noise that can corrupt analog performance. Analog and digital grounds (and supplies) should be tied at one common ground point to minimize circulating digital and analog ground currents and noise.

At high frequencies, a phenomenon called *skin effect* must be considered. Skin effect causes currents to flow in the outer surfaces of a conductor—in effect making the conductor narrower, thus increasing the resistance from its dc value. While skin effect is beyond the scope of this article, a good approximation for the skin depth in copper, in centimeters, is

$$\text{Skin Depth} = \frac{6.61}{\sqrt{f(\text{Hz})}} \qquad (5)$$

Less susceptible plating metals can be helpful in reducing skin effect.

Packaging

Op amps are typically offered in a variety of packages. The package chosen can affect an amplifier's high-frequency performance. The main influences are parasitics (mentioned earlier) and *signal routing*. Here we will focus on routing inputs, outputs, and power to the amplifier.

Figure 9 illustrates the layout differences between an op amp in an SOIC package (a) and one in an SOT-23 package (b). Each package type presents its own set of challenges. Focusing on (a), close examination of the feedback path suggests that there are multiple options for routing the feedback. Keeping trace lengths short is paramount. Parasitic inductance in the feedback can cause ringing and overshoot. In Figures 9(a) and 9(b), the feedback path is routed around the amplifier. Figure 9(c) shows an alternative approach—routing the feedback path under the SOIC package—which minimizes the feedback path length. Each option has subtle differences. The first option can lead to excess trace length, with increased series inductance. The second option uses vias, which can introduce parasitic capacitance and inductance. The influence and implications of these parasitics must be taken into consideration when laying out the board. The SOT-23 layout is almost ideal: minimal feedback trace length and use of vias; the load and bypass capacitors are returned with short paths to the same ground connection; and the positive rail capacitors, not shown in Figure 9(b), are located directly under the negative rail capacitors on the bottom of the board.

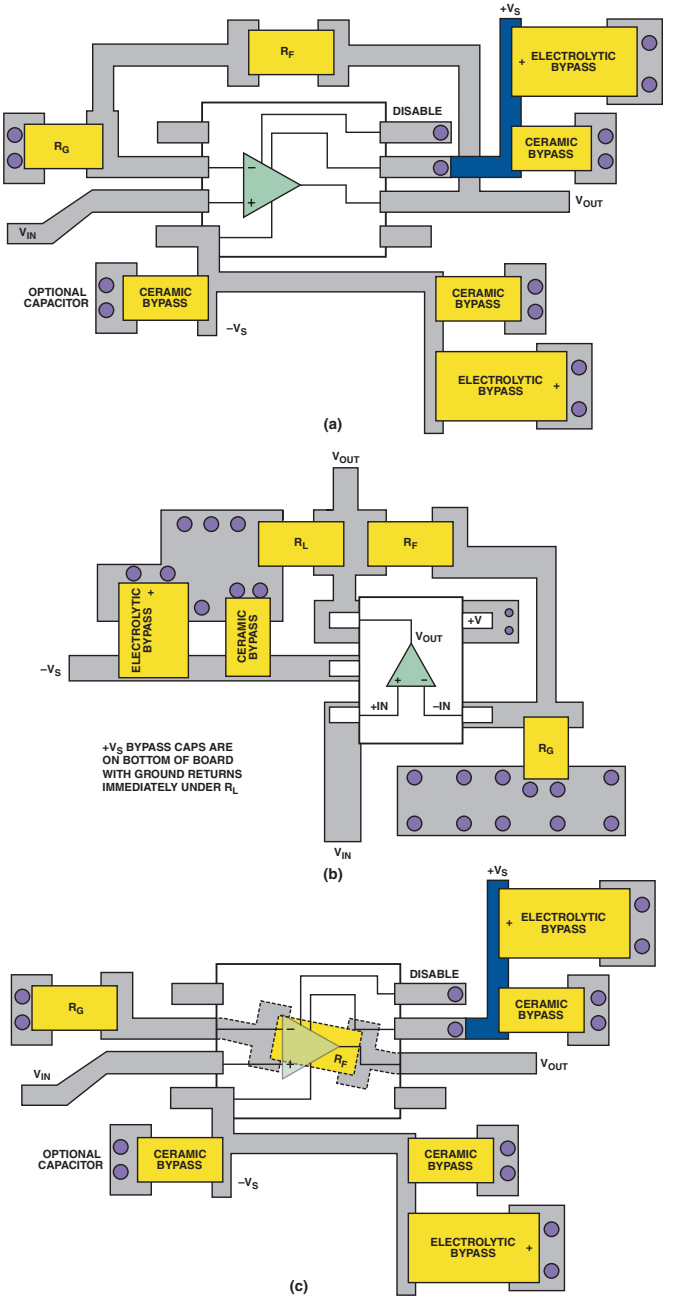

Figure 9. Layout differences for an op amp circuit. (a) SOIC package, (b) SOT-23, and (c) SOIC with R_F underneath board.

Low-distortion amplifier pinout: A new low-distortion pinout, available in some Analog Devices op amps (the AD8045,[1] for example), helps eliminate both of the previously mentioned problems; and it improves performance in two other important areas as well. The LFCSP's low-distortion pinout, as shown in Figure 10, takes the traditional op amp pinout, rotates it counterclockwise by one pin and adds a second output pin that serves as a dedicated feedback pin.

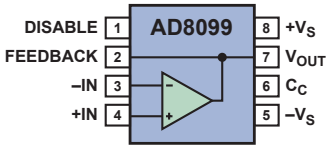

Figure 10. Op amp with low-distortion pinout.

The low-distortion pinout permits a close connection between the output (the dedicated feedback pin) and the inverting input, as shown in Figure 11. This greatly simplifies and streamlines the layout.

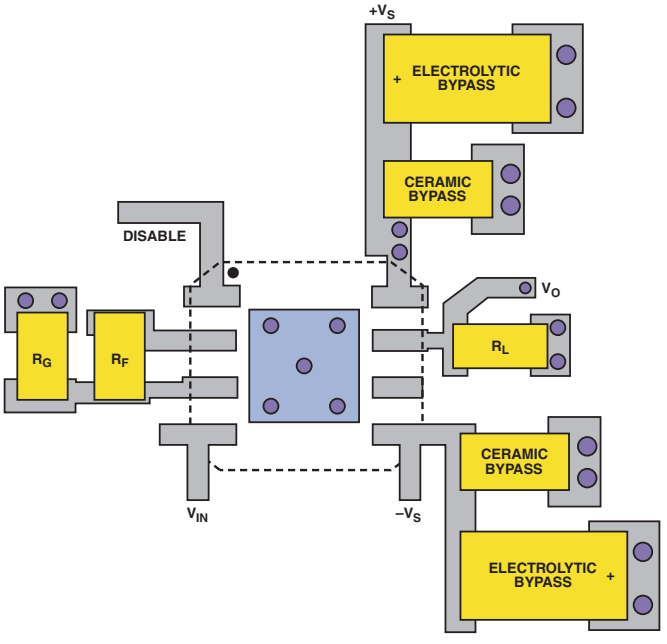

Figure 11. PCB layout for AD8045 low-distortion op amp.

Another benefit is decreased second-harmonic distortion. One cause of second-harmonic distortion in conventional op amp pin configurations is the coupling between the noninverting input and the negative supply pin. The low-distortion pinout for the LFCSP package eliminates this coupling and greatly reduces second-harmonic distortion; in some cases the reduction can be as much as 14 dB. Figure 12 shows the difference in distortion performance between the AD8099[2] SOIC and the LFCSP package.

This package has yet another advantage—in power dissipation. The LFCSP provides an exposed paddle, which lowers the thermal resistance of the package and can improve θ_{JA} by approximately 40%. With its lower thermal resistance, the device runs cooler, which translates into higher reliability.

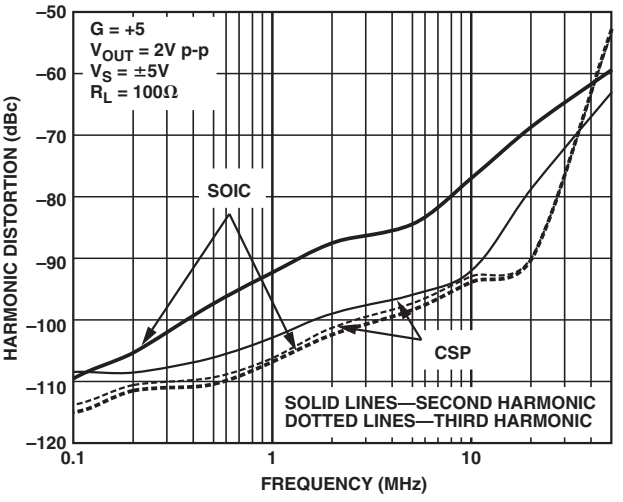

Figure 12. AD8099 distortion comparison—the same op amp in SOIC and LFCSP packages.

At present, three Analog Devices high-speed op amps are available with the new low-distortion pinout: AD8045, AD8099, and AD8000.[3]

Routing and Shielding

A wide variety of analog and digital signals, with high- and low voltages and currents, ranging from dc to GHz, exists on circuit boards. Keeping signals from interfering with one another can be difficult.

Recalling the advice to "trust no one," it is critical to think ahead and come up with a plan for how the signals will be processed on the board. It is important to note which signals are sensitive and to determine what steps must be taken to maintain their integrity. Ground planes provide a common reference point for electrical signals, and they can also be used for shielding. When signal isolation is required, the first step should be to provide physical distance between the signal traces. Here are some good practices to observe:

- Minimizing long parallel runs and close proximity of signal traces on the same board will reduce inductive coupling.
- Minimizing long traces on adjacent layers will prevent capacitive coupling.
- Signal traces requiring high isolation should be routed on separate layers and—if they cannot be totally distanced—should run orthogonally to one another with ground plane in between. Orthogonal routing will minimize capacitive coupling, and the ground will form an electrical shield. This technique is exploited in the formation of *controlled-impedance* lines.

High-frequency (RF) signals are typically run on controlled-impedance lines. That is, the trace maintains a characteristic impedance, such as 50 Ω (typical in RF applications). Two common types of controlled-impedance lines, *microstrip*[4] and *stripline*[5] can both yield similar results, but with different implementations.

A microstrip controlled-impedance line, shown in Figure 13, can be run on either side of a board; it uses the ground plane immediately beneath it as a reference plane.

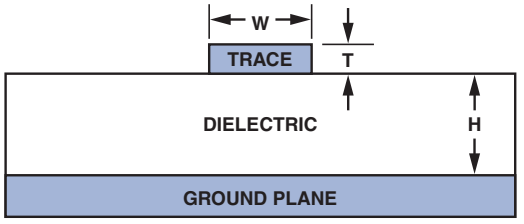

Figure 13. A *microstrip* transmission line.

Equation 6 can be used to calculate the characteristic impedance for an FR4 board.

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r} + 1.41} \ln\left[\frac{5.98H}{(0.8W + T)}\right] \quad (6)$$

H is the distance in from the ground plane to the signal trace, W is the trace width, T is the trace thickness; all dimensions are in mils (inches $\times 10^{-3}$). ε_r is the dielectric constant of the PCB material.

Stripline controlled-impedance lines (see Figure 14) use two layers of ground plane, with signal trace sandwiched between them. This approach uses more traces, requires more board layers, is sensitive to dielectric thickness variations, and costs more—so it is typically used only in demanding applications.

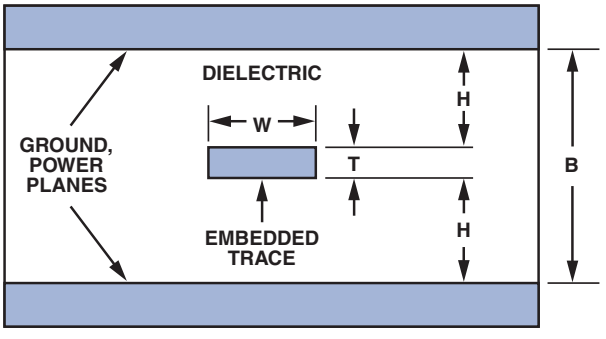

Figure 14. Stripline controlled-impedance line.

The characteristic-impedance design equation for stripline is shown in Equation 7.

$$Z_0(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(B)}{(0.8W + T)}\right] \quad (7)$$

Guard rings, or "guarding," is another common type of shielding used with op amps; it is used to prevent stray currents from entering sensitive nodes. The principle is straightforward—completely surround the sensitive node with a guard conductor that is kept at, or driven to (at low impedance) the same potential as the sensitive node, and thus sinks stray currents away from the sensitive node. Figure 15(a) shows the guard ring schematics for inverting and noninverting op amp configurations. Figure 15(b) shows a typical implementation of both guard rings for a SOT-23-5 package.

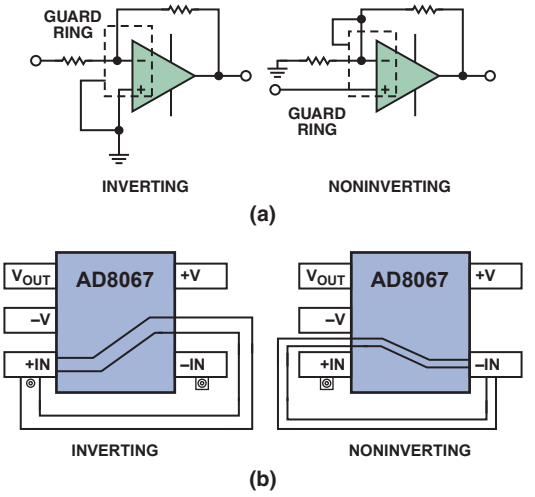

Figure 15. Guard rings. (a) Inverting and noninverting operation. (b) SOT-23-5 package.

There are many other options for shielding and routing. The reader is encouraged to review the references below for more information on this and other topics mentioned above.

CONCLUSION

Intelligent circuit-board layout is important to successful op amp circuit design, especially for high-speed circuits. A good schematic is the foundation for a good layout; and close coordination between the circuit designer and the layout designer is essential, especially in regard to the location of parts and wiring. Topics to consider include power-supply bypassing, minimizing parasitics, use of ground planes, the effects of op amp packaging, and methods of routing and shielding.

FOR FURTHER READING

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4 http://www.microwaves101.com/encyclopedia/microstrip.cfm
5 http://www.microwaves101.com/encyclopedia/stripline.cfm

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