

PHYSICAL DESIGN REUSE IN PADS®: HOW TO LEVERAGE CORPORATE IP TO INCREASE EFFICIENCY IN PCB DESIGN

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INTRODUCTION

If there is one constant in electronic product design it is that the development time for your next project is always less than that of your last project. To stay competitive, companies try to shorten product development time wherever possible. Reusing proven circuits can help. Physical design reuse (PDR) increases productivity, ensures product quality, and drives efficiency throughout the PCB design process.

Physical design reuse leverages your company's intellectual property (IP). You can reuse a design block, such as a multi-channel board or a memory array, multiple times in the same design. You can use a single circuit, such as a battery-charging circuit, in a series of related products. Or you can use circuits such as antenna designs in a host of different types of products where the circuit needs to be exactly the same in each.

The physical design reuse capabilities in PADS are useful in each of these use cases, helping you shorten design cycles and ensuring product quality by reusing proven circuits in each application. Coupled with PADS intuitive, easy-to-use GUI and handy automation, it's no wonder that PDR has been one of the most popular features in PADS since its introduction.

This paper illustrates how PADS can be used for physical design reuse, showing its positive effect on design time reduction and illustrating its superiority to competitive tools.

USING PHYSICAL DESIGN REUSE

You can think of PDR as simply using an entire, laid out PCB circuit as a single "component". But, now this component is on steroids. Instead of grabbing a single package design from the PCB design library, you can select an entire circuit, already laid out and already tested. This can be very valuable when designing multi-channel interfaces, incorporating common circuits into multiple products, or saving time when designing to meet EMI or regulatory compliance.

The PDR function in PADS allows you to do just that, but in a very powerful way. Unlike competitive products, the PADS PDR is not just a cut-and-paste tool. Rather, it is a very intelligent tool with a great deal of flexibility and automation built in.

With PADS, not just the "image" of the PCB layout segment is captured, but all characteristics, constraints, nets, and tolerances as well. That means you truly are inserting a "component" that has been extracted from a previous design along with intent. Everything that is selected for reuse — pads, vias, RF shapes, FPGAs, components, resistors, breakouts, escapes, and even test points — are saved in exact duplicate. Signal definitions are maintained from the schematic as well.

Automation can substantially speed up using PDR as well. When inserting reuse elements, reference designators and net names can be automatically updated with each insertion. Imagine the tedium that feature could reduce when laying out a 32-channel audio mixer! As with all automation in PDR, you can select which features you want automated and which features you want to manually control for maximum flexibility.

TWO MODES OF REUSE

There are two "modes" to employ reuse with the PDR: Reusing "golden circuits" from a reuse library and replicating circuits within the same PCB during design.

Duplication of existing, proven circuits ("Golden Circuits") allows designers to insert laid-out circuits into a PCB design. Using golden circuits reduces errors because these circuits have already been tested and proven in another design. Once a circuit has been proven, such as the battery charger circuit mentioned earlier, it can be stored in a reuse library for use on future projects.

When inserted into a new design, PDR scans the file and attempts to find components and connections that match the reuse block. When matched, all the entities from the golden circuit are selected and cloned to the reuse for placement. The task is little more difficult than placing any other component on the board design.

Cloning circuits on the PCB under design is the second mode. In this mode, you might not always want to save the circuit as “golden”, but rather use the circuit somewhat like a macro. The case of the 32-channel mixer is a perfect example of this mode. The output stage, while not necessarily useful enough to save as “golden”, can be designed once. Then, the circuit elements can be selected and then reused as many times as needed, with automation making the proper connections and updating net names and reference designators.

REUSE EXAMPLES

Let’s look at some reuse examples using PADS.

INSERTING A GOLDEN CIRCUIT

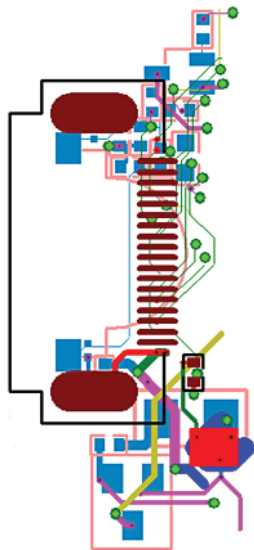


Figure 1: This “Golden” battery charging circuit will be used in many designs, so it has been saved in the reuse library for future designs.

A battery charging circuit is a good example of a golden circuit that could be reused on many products. The first time the battery charging circuit is laid out, the design is selected by drawing a box around the laid out portion of the PCB that you wish to save. Figure 1 shows the completed battery charger that has been saved to the reuse library. All components, pads, vias, test points, etc. are saved along with the circuit.

Reusing the circuit has very few limitations. The most important thing to remember is that the reuse circuit and the design into which it will be inserted must have the same number of layers. If the number of layers is different, PADS will present you with an error, (Figure 2) in this case, telling us that the reused battery charger is a two-layer design and the target design contains six layers. Simply adding four unused layers to the battery charger circuit will solve the problem.

Once the reuse element has the same number of layers, it is selected and in PADS it is designated “Make Reuse”. PADS matches the circuit to the schematic of the current design and then the circuit may be dropped into the design wherever needed. Then, you simply route the required signals to the reuse element as if it were any other component.

Another common circuit to save in a reuse library is an antenna design. With RF shapes, the exact dimensions are critical and inviolate if the same frequency and operating characteristics are to be maintained. This makes it an ideal element to store in the library and reuse on every product operating at the same frequency. As shown in Figure 3, this antenna design for an RFID product was pasted into the circuit next to the original design, showing the absolute duplication of all features.

```

Layout.err - Notepad
File Edit Format View Help
-----
Add Reuse Report -- Tue Aug 13 09:39:10 2013
-----
Design File: untitled
Reuse File: DxCorporateIOPort_2011.reu
Reuse Date: wed Aug 31 09:42:15 2011
-----
Checking reuse/design compatibility
ERROR: Electrical layer count mismatch.
        Electrical layer count in Design: 2
        Electrical layer count in Reuse: 6
WARNING: stack mismatch (Decal STANDARDVIA)
        Default pin stack for Decal STANDARDVIA in design
        Default pin stack for Decal STANDARDVIA in reuse
-----
Total ERRORS: 1
Total WARNINGS: 1

```

Figure 2: If the “golden circuit” and the design onto which it will be placed have different layer counts, an error will be generated.

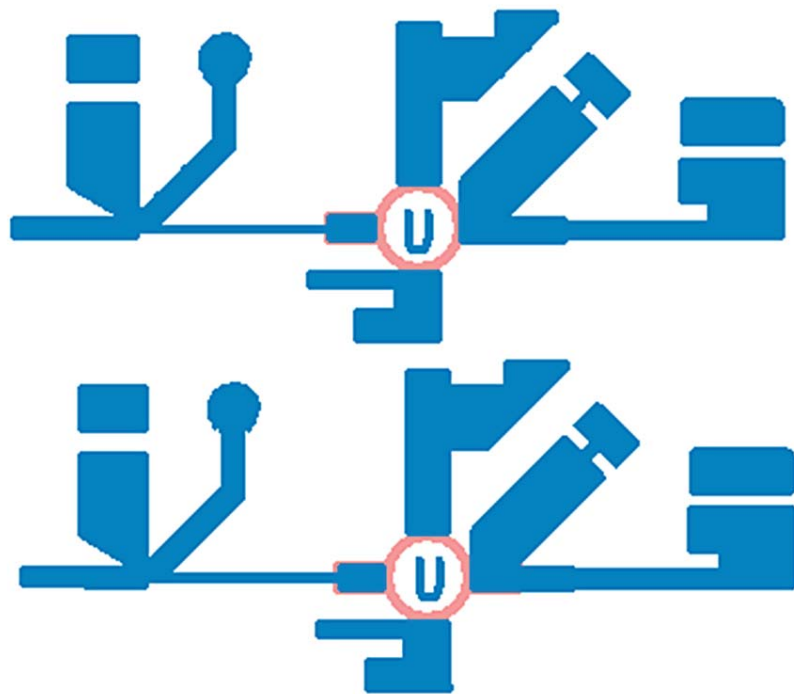


Figure 3: Two insertions of an RFID antenna design show they are indeed identical.

In addition to maintaining exact dimensions, traces, vias, and test points, keepouts can be assigned and copied along with the reuse as well. This is important in many circuits, and especially RF circuits. In Figure 4, you can see how easy it is to assign keepout areas that will be included with the resulting reuse circuit in the library.

CLONING A CIRCUIT FOR REUSE IN THE CURRENT DESIGN

The other mode, cloning within the current design, is even easier to use. With this mode, a single instance of the reuse circuit is designed, laid out, and routed the first time. Then, in the same way that the original golden circuit was selected for reuse, this circuit is selected and PADS is instructed to “Make Reuse”.

Now, the selection “Make Like Reuse” is executed. PADS looks at the schematic and automatically inserts the cloned circuit when a match is found. Reference designators and net definitions are updated automatically, as shown in Figure 4.

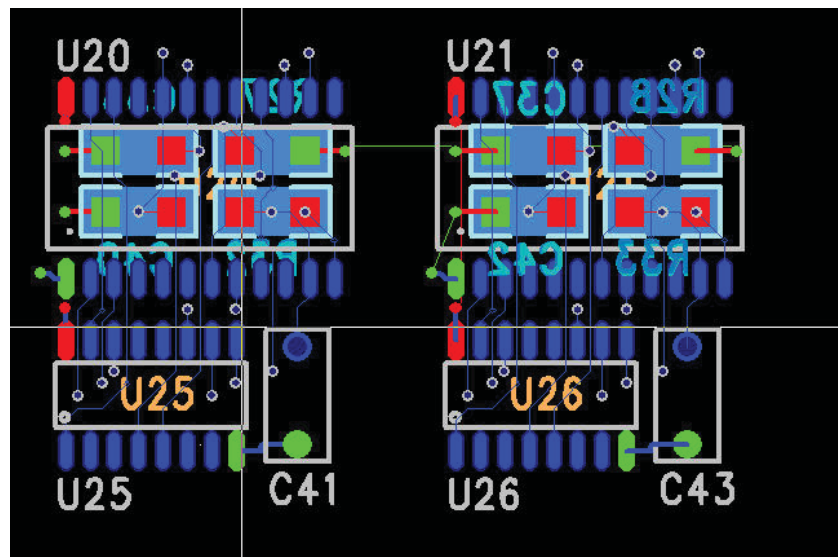


Figure 4: Shown here are two examples of reuse element insertion. Note how the reference designators have been automatically updated (from left to right).

Cloning circuits in this manner is extremely powerful and can save an enormous amount of PCB design time. The earlier reference to a 32-channel mixer was a design created by a PADS customer. In that design, the initial layout of a single audio stage required about two days...whether employing re-use or not. Then, when replicating manually, the remaining 31 circuits could be completed in about 3-5 days. By leveraging reuse, the remaining 31 channels were dropped onto the PCB in as little as 30 minutes. Not every product has multiple, identical circuits that can result in such a dramatic difference in layout time, but even a few replications of buffers, I/O ports, etc. can significantly shorten the product development time.

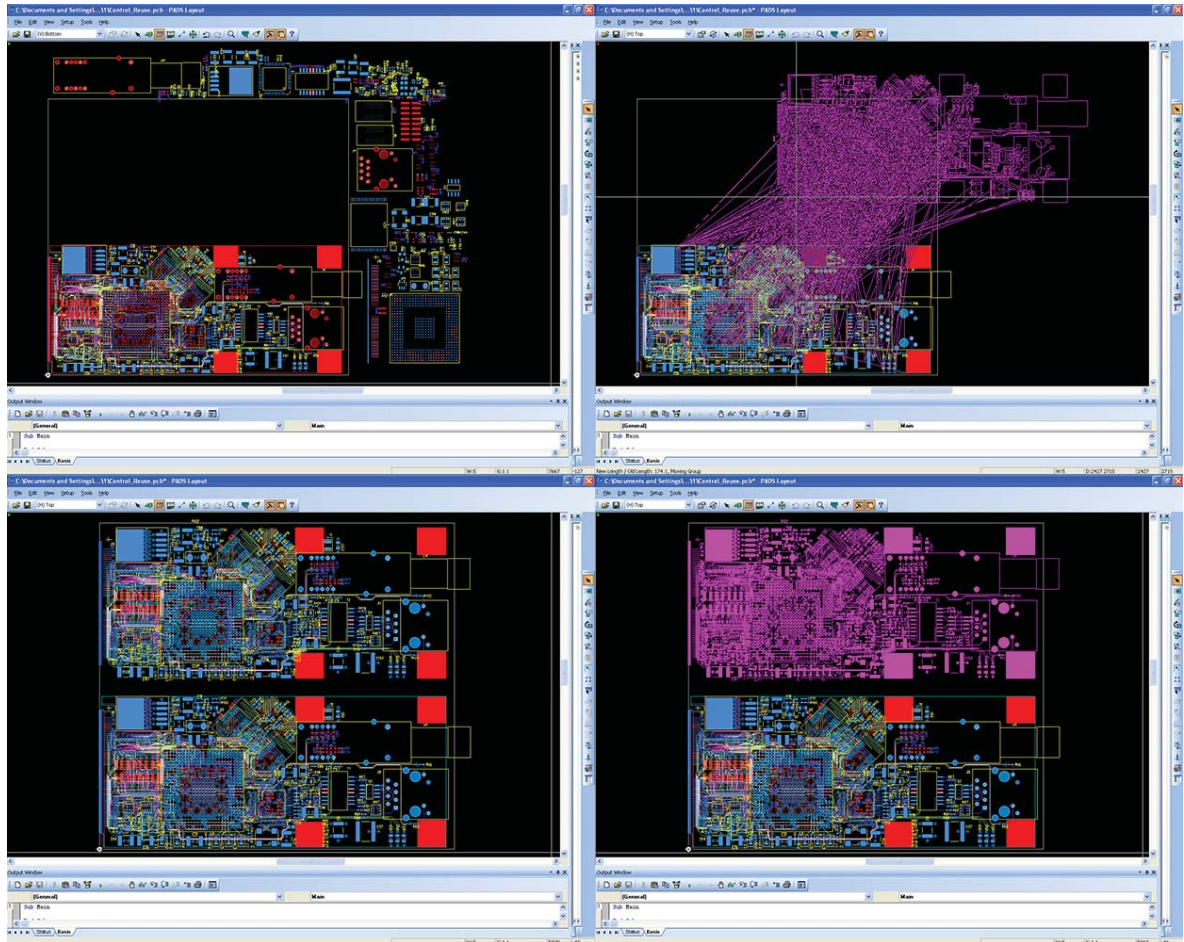


Figure 5: In this progressive image, we see a series of proven components chosen for the purpose of creating a reuse block. The reuse block is built with components that are outside the board with all routing in place. Once created, the block is moved and placed inside the board. Unlike simple cut-and-paste techniques that result in reference designator conflicts and other design issues, PADS physical design reuse captures the full intelligence of the reuse block.

DESIGN FOR MANUFACTURING

When using either mode, but especially cloning, editing the elements for DFM reasons is a snap. For example, suppose that the reuse circuit is discovered to not have enough clearance for a new capacitor vendor. By editing the reuse block once, the changes to make the circuit manufacturable will be propagated throughout the reused circuits.

CHOOSING YOUR PHYSICAL DESIGN SOLUTION

Many desktop PCB design tools rely on simple design reuse capabilities, literally using cut-and-paste techniques to snip the circuitry within the physical layout. Lacking intelligence, such reuse blocks are little more than flat graphics. They might look nice but they lack good implementation and give no control over how the design data are reused within the design. Users are forced into reusing identical copies of the copied segment, resulting in reference designator conflicts and other design issues during the design reuse. This lack of powerful implementation results in additional rework in order for a design segment to be reused within the physical layout.

PADS provides a simple and sophisticated solution that avoids these problems by capturing the full intelligence of the reuse blocks, including constraints, nets, and tolerances, thus speeding the design process and eliminating errors.

NOW IS THE TIME TO BEGIN EMPLOYING PHYSICAL DESIGN REUSE

The obvious advantage to design reuse is shortening PCB design time. Using the actual customer data for the mixer board example shows that reuse eliminated up to three days of design time: quite significant!

A second way that overall product development time is shortened is in test and regulatory compliance time. Once the charging circuit shown in Figure 3 has been developed and tested to be EMI compliant (or other standards such as UL/CSA etc.), reusing that circuit means that a great deal of testing time can be saved. This also can reduce headaches and finger-crossing when submitting products for standards and EMI testing for the first time!

If you have not taken advantage of the physical design reuse features in PADS PCB design software, now is a good time to try it. Use PDR in your next design project or look through recent projects and discover circuit layouts that could be copied and reused on future designs. PDR is included in the PADS ES suite and it can be added to any existing PADS seat. With PADS physical design reuse, you'll get significant rewards without investing a lot of time.

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