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Power and ground design

System-level power-supply design has always been challenging. The continual shrinking of IC-process geometries has generated a major increase in mixed-voltage and -mode SOCs (systems on chips). This development, in turn, has spawned a number of new software tools for assisting engineers in this design effort. These tools fall into two main categories: supply feed/drop and noise.

At the IC level, other approaches to the power-supply feed/drop problem are IR drop and electromigration analysis. The main challenges for IR and electromigration issues are simply accommodating the large lines in the space available, and the ability to deliver the necessary voltage and current to supply the active circuitry. In addition to addressing the size of the lines to minimize voltage drop, the size of the vias connecting the lines is critical to ensuring that the peak current can pass from layer to layer where necessary. Both these physical-manufacturing rules and their associated interlayer-design rules have systematic-analysis options that academia developed and then successfully implemented into commercial EDA tools. This design step has gone from being a manual task to being an automated-analysis task. Now, some SOC and board-level physical-design tools offer automated implementation with analysis.

The noise problem includes supply ripple and ground bounce. Supply ripple comprises injected signals that ride on the positive-power-supply rail, the negative-power-supply rails that are not at the system ground, or both. A variety of both automated and manual tools can analyze these signals. Automated tools generally do not quantify the noise. They give simple responses to simple questions, such as "Is the signal in an acceptable window?" In general, the industry does not use place-and-route or postlayout-verification tools but instead uses high-capacity SPICE tools for this task.

Ground bounce is one of the biggest challenges facing DSM (deep-submicron) design. Because ground bounce affects the system's global reference, none of the high-level simulation tools, such as analog/mixed-signal simulators, postlayout-validation tools, and place-and-route tools, can perform the analysis. This issue forces engineers to solve the problem with large input decks for SPICE simulation. SPICE simulation is necessary because of the requirement for analyzing both time- and frequency-domain simulation. This ground noise, which typically occurs through substrate injection and leakage, is especially critical for low-voltage applications with dramatically reduced PSRRs (power-supply-rejection ratios) and SNRs.

Standard mixed-signal designs operating at 3V or higher enjoy handcrafted power grids with wide lines, multiple vias, and interlayer shielding, in addition to guardbands and isolation techniques, all of which result in PSRR levels greater than 100 dB. Most mobile-battery applications require more than 60 dB of PSRR; otherwise, low-power-shutdown situations occur. Cable-interface circuitry, such as USB, HDMI, DVI, or Ethernet, uses differential-signal processing, and, as a result, ground ripple and its frequency composition are key, because the ground acts as a reference for extracting data embedded on a carrier signal.

Most automated power-grid options aim to minimize IR drop without taking into account the associated noise and harmonic performance; thus, they can produce PSRR levels lower than 60 dB. Solving this multivariable set of simultaneous IR-drop and noise conditions as separate and independent linear problems is unrealistic for designs of less than 130 nm or for systems operating at high frequencies or with accuracy of greater than 12 bits. No automated tools other than standard SPICE can perform this analysis. IC and systems designers in the automotive, audio, video, military, and industrial-electronic sectors point to hand layout, SPICE analysis, and a design guru in a dark cube as the main solutions for power-grid sign-off. An example is a system-level design by Creation Audio Labs (www.creationaudiolabs.com), which simultaneously supports both a PSRR and an SNR of greater than 110 dB. Further, the entire design has either a battery or a commercial-grade external power supply and less than 20 mV of IR drop.

For 65-nm and smaller processes, the reduced operating voltages and higher clock/switching frequencies dramatically increase the importance of power-supply sign-off and analysis in the design flow. This factor will drive multithreaded and multiprocessor SPICE tools that support both frequency- and time-domain analysis. EDN

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