Application Report
SPRA429B

TMS320C6000 BGA Manufacturing Considerations

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Abstract

When designing with a high-density BGA package, it is important to be aware of different techniques that aid in the quality of the manufacture. It is important to match the copper land diameter on the printed circuit board (PCB) to ensure reliability. Two processes are available for the copper lands: solder mask defined (SMD) and non-solder mask defined (NSMD). Each has advantages and disadvantages. Signal routing is a serious concern when designing with fine-pitch BGA packages. The standard method to connect the balls of a BGA to inner signal layers of the PCB is to place plated through hole (PTH) vias interstitial between the copper lands. Another method, which allows for less copper to be present on both the top and bottom layers of the PCB, is to use blind and buried vias, with large vias present only on the inner layers of the PCB. In addition to designing the PCB land area, it is necessary to properly attach the BGA to the board. BGAs inherently offer self-correction if slightly misplaced during reflow. This document contains the recommended reflow profile.

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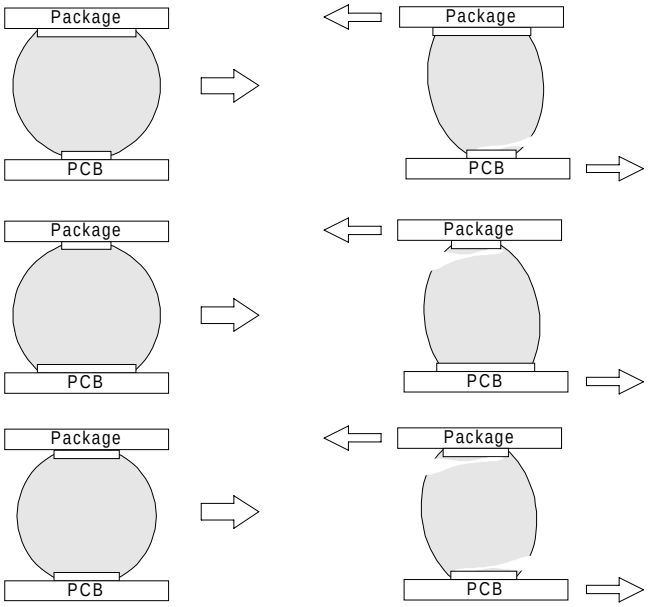
Solder Land Areas

Design of both the BGA itself and the printed circuit board (PCB) are important in achieving manufacturability and reliability. In particular, the diameter of the package vias and the board lands are critical. While the actual sizes of these dimensions are important, their ratio is more critical. Figure 1 illustrates why the package-to-PCB via configuration and ratio is critical.

Figure 1: Effect of Via/Land Ratios



In the top view, the package via is larger, and the solder ball is prone to crack prematurely at the PCB interface. In the middle view, the PCB via is larger, leading to cracks at the package surface. In the bottom view, where the ratio is almost 1:1, the stresses are more equally distributed across the height of the solder connection.

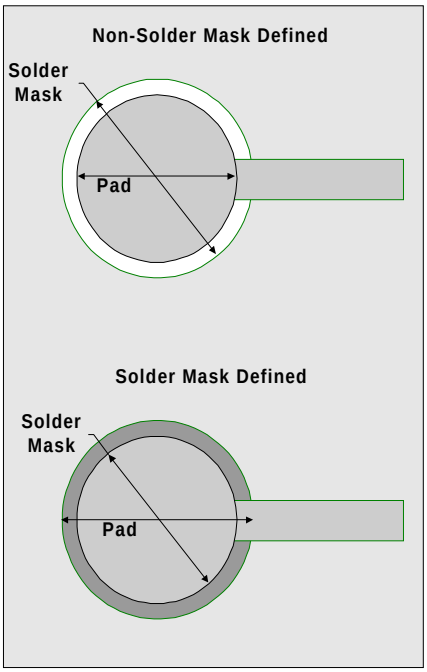
Solder lands on the PCB are generally simple round pads. There are two methods of defining the solder lands: solder mask defined (SMD), and non-solder mask defined (NSMD).

With the SMD method, the copper pad is made larger than the desired land area, and the opening size is defined by the opening in the solder mask material. The advantages normally associated with this technique include more closely controlled size and better copper adhesion to the laminate. Better size control is the result of photoimaging the stencils for masks. The chief disadvantage of this method is that the larger copper spot can make routing more difficult.

With the NSMD method, the land area is etched inside the solder mask area. While the size control is dependent on copper etching and is not as accurate as the SMD method, the overall pattern registration is dependent on the copper artwork, which is quite accurate. The tradeoff is between accurate dot placement and accurate dot size. NSMD lands are recommended for small-pitch BGA packages because more space is left between the copper lands for signal traces.

See Figure 2 for an example of optimum land diameters and configurations for a common BGA pitch.

Figure 2: Optimum Land Configuration



Non-Solder Mask Defined

Ball Pitch	Diameter	
	Copper	Mask
0.80mm	0.35mm	0.50mm
1.00mm	0.40mm	0.55mm
1.27mm	0.65mm	0.85mm

Solder Mask Defined

Ball Pitch	Diameter	
	Copper	Mask
0.80mm	0.48mm	0.38mm
1.00mm	0.55mm	0.45mm
1.27mm	0.90mm	0.70mm

Conductor Width/Spacing

Many of today's circuit board layouts are based on at most a 100-micron conductor line width and 200-micron spacing. To route between 0.8-mm pitch balls, given a clearance of roughly 380 microns between ball lands, only one signal can be routed between ball pads. The 380-micron ball spacing is worst case and calculated by assuming the diameter of the solder ball land is 410 microns. Conventionally, the pads are connected by wide copper traces to other devices or to plated through holes (PTH). As a rule, the mounting pads must be isolated from the PTH. Placing the PTH interstitial to (or in between, connected to the land with a trace) the land pads often achieves this.

High Density Routing Techniques

A challenge when designing with BGA packages is that as available space contracts, the space available for signal fanout also decreases. By using a few high-density routing techniques, the PCB designer can minimize many of these design and manufacturing challenges. This section focuses on TI designators GLS (384-pin) package, with a 0.8mm pitch. The GLS package has a solid six-row array configuration, with signals located on the outer three rows.

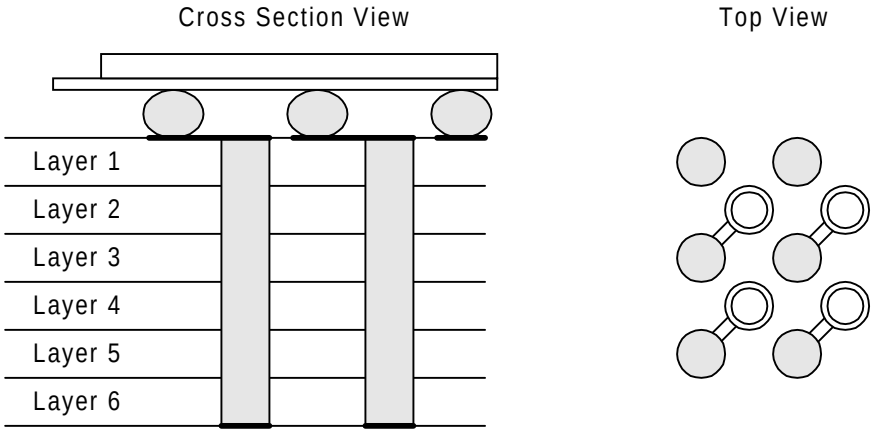
Via Density

Via density, as mentioned earlier, can be a limiting factor when designing high-density boards. Via density is defined as the number of vias in a particular board area. Using smaller vias increases the routability of the board by requiring less board space and increasing via density. The invention of the microvia has solved many of the problems associated with via density. Microvias are often created using a laser to penetrate the first few layers of dielectric. The laser can penetrate a 4-mil thick dielectric layer. The layout designer can now route to the first internal board layer. Two layers (each 4 mil thick) can be laser-drilled, creating a 200-micron microvia diameter. In this case, routing to the first two internal layers is possible. The number of board layers increases as board chip density and functional pin count increase. As an example, the Texas Instruments (TI™) TMS320C6202 digital signal processor (DSP) is available in a 384-pin GLS package and uses 198 balls for power and ground. Routing of the 186 signals can be accomplished on as little as two layers. The power and ground planes increase the board to four layers. By increasing the board layer stack-up to six or eight layers, high-density applications are possible with only 10 to 15 mils between the chips.

Conventional PCB Design

The relatively large via density on the package periphery, mentioned earlier, is caused by limited options when routing the signal from the ball. To reduce the via density problem on the periphery of the package, designers can build the PCB vertically from the BGA pad through the internal layers of the board, as shown in Figure 3. By working vertically and mechanical drilling 250-micron vias between the pads on the board and the internal layers, designers can create a “pick-and-choose” method. They can pick the layer and choose the route. A dog bone method is used to connect the through-hole via and the pad. This method requires a very small mechanical drill to create the 384 vias for one package.

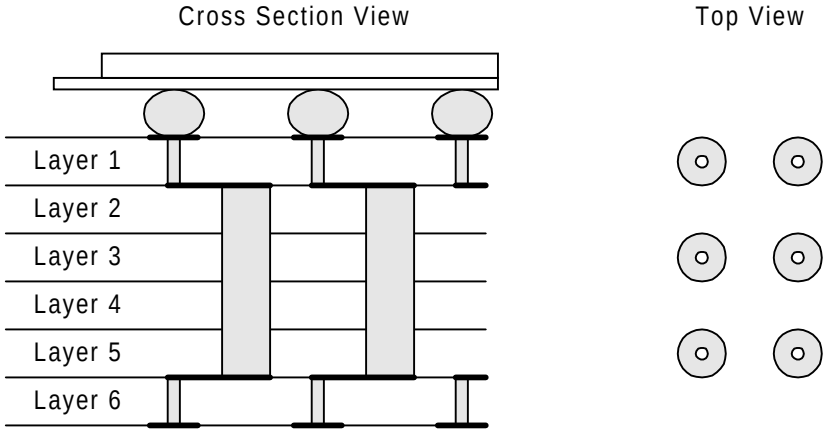
Figure 3: Conventional Via Structure



Advanced Design Methods

Another option is to use a combination of blind and buried vias. Blind vias connect either the top or bottom side of the board to inner layers as shown in Figure 4. Buried vias usually connect only the inner layers. This method uses 4-mil laser-drilled microvias in the center of the pads and burying the dog bone on layer 2. Since the buried via does not extend through the underside of the board, the designer can use another set of laser-drilled blind microvias, if needed, to connect the bypass capacitors and other discrete components to the bottom-side.

Figure 4: Buried Via Structure



Component placement

Component placement is the next operation followed by solder paste printing. BGA components exhibit the self-centering phenomena. The self-centering will correct for some amount of misplacement in the process. The surface tension of the molten solder and the wetting nature of the solder to the pad contribute to the self-centering of the component. As a general rule, placement offset of as much as 50% of the pad is normally allowed in the case of BGA placement.

Component placement is normally performed using equipment capable of placing the BGA with reference to the BGA balls. If ball vision is not available BGAs can be placed by aligning on component edges. In this type of placement, the offset could be much higher due to component to component variability. The preferred method is to use the BGA balls for placement. While placing the component, care should be exercised not to splatter the solder paste. A placement force of 200-300 grams is normally adequate for making contact wit the solder paste.

Reflow

The boards with all the components placed are then sent to the reflow oven. BGAs do not require any special process for reflowing. It is important to check the reflow profiles of all components on the board. It is important that all devices to be soldered experience an adequate reflow. Depending on the type of oven used there may be a temperature difference from the center of the board to the edges. Multiple thermocouples should be mounted on various parts of the board to get a broader spectrum of temperature profiles. If needed, the temperature should be re-adjusted to achieve good soldering of the parts.

While measuring the temperature profile of the BGA it is beneficial to have one of the thermocouples mounted on a joint in order to measure the actual temperature solder is experiencing. Table 1 illustrates a typical SMT profile that can be used for BGA reflow.

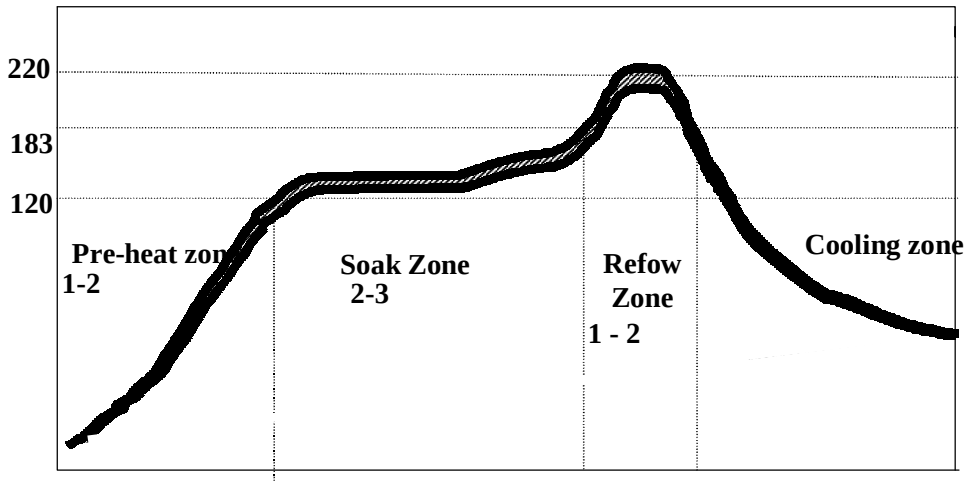
Table 1: Reflow Oven Zones

Reflow Oven Zones	Characteristics	Process window
Pre heat	Initial heating of the component/board	- 3 seconds /second 120-140 Degree C Peak Temp
Soak	Solder paste drying and flux activation zone	120-180 seconds soak 120-170 Degree C Peak temp
Reflow	Solder ring zone, Above 183 Degree	60-120 seconds above 183 C 220+/- 5 peak component temperature
Cool down	Assembly cooling zone	2- 3 Degree/Second to room temp

The preheat zone slowly heats the component and the rest of the assembly to around 120-140°C. The heating rate is maintained around 1.5°C to 2°C at this stage. The soak zone is where the excessive volatiles are driven off and the flux is activated. This zone is highly dependent on the type of solder paste used. The assembly should be maintained at this zone long enough to drive off all the volatiles, ensuring minimum voiding during assembly. The flux activation occurs around 150°C - 170°C or towards the end of the soak zone. This zone is normally 120- 180 seconds long. The third zone consists of the reflow zone. In this zone the temperature is ramped at a fast rate to above the liquidous temperature of solder. The maximum component temperature in this zone is normally maintained around 220°C. Time above 183°C can range from 60°C- 120°C depending on the board. Once the soldering is complete the board is passed on to the cooling zone. The assembly is rapidly cooled (2-3°/second) at this zone.

Figure 5 illustrates a typical reflow profile that can be used for BGA assembly.

Figure 5: Example Reflow Profile



Summary

By understanding the manufacturing processes available, as well as the impact different techniques have on a PCB design, reliable systems can be designed. For reliability, you should pay attention to the physical properties of the copper lands on the PCB. By matching the land diameter on the PCB to those on the BGA package, the solder connection will be robust. You must also keep signal routing in mind when designing with fine-pitch BGA devices. There are several methods available to connect the balls of the BGA to the inner layers of the PCB. Microvia and buried via technology allow more space to be left on each PCB layer for signal routing. In addition to properly designing the PCB, it is necessary to understand the reflow process to accurately attach the device to the PCB. A sample reflow process is provided, which should be followed for this. By understanding these design considerations, a PCB can be designed quickly and the BGA attached reliably.

References

Texas Instruments MicroStar BGA™ Packaging Reference Guide, Texas Instruments, (SSYZ015).

TI Contact Numbers

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www.ti.com/sc

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www.ti.com/sc/docs/distmenu.htm

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