THE CAD LIBRARY OF THE FUTURE August 2011

ABSTRACT

The electronics industry is constantly growing and introducing new technology sometimes faster than we can keep up with. This paper reviews one of the single most important, but sometimes overlooked or taken for granted, aspects of the electronics industry—The CAD Library Land Pattern.

Every electronic component requires a solder land pattern for PCB layout. The solder pattern can be placed into two categories.

1. Meet all the industry standard requirements for the sole purpose of electronic product creation automation.
2. Fail to meet the industry standard requirements and create electronic product creation chaos.

This paper will describe the industry standard requirements so EE Engineers, PCB Designers and PCB Assembly Lines can fully automate their processes, become more efficient and productive. Of course, this will lead to faster product development cycles, reduction in overall costs, and reduction in error rate. If correctly implemented, you can eventually achieve elimination of duplication.

However, if you do not follow standardization, there are companies that exist that will gladly take your money to verify whether the land patterns you created are correctly built. But, even if the component will fit the land pattern that you created, there are still other factors, like “Zero Component Rotation”, that must be considered to automate the manufacturing process.

The CAD Library of the Future will be a “One World Standard Library”, across all CAD tool platforms, that will be accepted by the electronics industry to eliminate duplication of effort and automate all of the engineering, design layout, manufacturing and assembly processes.

The following pages explain the criteria needed to create “The CAD Library of the Future”. But first, let’s meet the key players whose goal is to standardize the electronics product development industry.or:

Mentor Graphics Corp.

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2. Fail to meet the industry standard requirements and create electronic product creation chaos.

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The CAD Library of the Future will be a “One World Standard Library”, across all CAD tool platforms that will be accepted by the electronics industry to eliminate duplication of effort and automate all of the engineering, design layout, manufacturing and assembly processes.

The following pages explain the criteria needed to create “The CAD Library of the Future”. But first, let’s meet the key players whose goal is to standardize the electronics product development industry.

2 ELECTRONIC STANDARD ORGANIZATIONS

Standard component package outlines come from industry standard organizations that specialize in component packaging data and standardization of documents and publications.

These organizations include JEDEC, EIA, IEC, NIST, IPC, ANSI, EIAJ, NEMI and JEITA

2.1 Standard Organizations

3 LAND PATTERN NAMING CONVENTION

3.1 IPC-7351B SMT Standard Land Pattern Names

Component, Category	Land Pattern Name
Ball Grid Array's	**BGA** + Pin Qty + **C** or **N** + Pitch **P** + Ball Columns **X** Ball Rows _ Body Length **X** Body Width **X** Height
BGA w/Dual Pitch	**BGA** + Pin Qty + **C** or **N** + Col Pitch **X** Row Pitch **P** + Ball Columns **X** Ball Rows _ Body Length **X** Body Width **X** Height
BGA w/Staggered Pins	**BGAS** + Pin Qty + **C** or **N** + Pitch **P** + Ball Columns **X** Ball Rows _ Body Length **X** Body Width **X** Height
BGA Note: The **C** or **N** = Collapsing or Non-collapsing Balls	
Capacitors, Chip, Array, Concave	**CAPCAV** + Pitch **P** + Body Length **X** Body Width **X** Height **-** Pin Qty
Capacitors, Chip, Array, Flat	**CAPCAF** + Pitch **P** + Body Length **X** Body Width **X** Height **-** Pin Qty
Capacitors, Chip, Non-polarized	**CAPC** + Body Length + Body Width **X** Height
Capacitors, Chip, Polarized	**CAPCP** + Body Length + Body Width **X** Height
Capacitors, Chip, Wire Rectangle	**CAPCWR** + Body Length + Body Width **X** Height
Capacitors, Molded, Non-polarized	**CAPM** + Body Length + Body Width **X** Height
Capacitors, Molded, Polarized	**CAPMP** + Body Length + Body Width **X** Height
Capacitors, Aluminum Electrolytic	**CAPAE** + Base Body Size **X** Height
Ceramic Flat Packages	**CFP127P** + Lead Span Nominal **X** Height **-** Pin Qty
Column Grid Array's	**CGA** + Pitch **P** + Number of Pin Columns **X** Number of Pin Rows **X** Height **-** Pin Qty
Crystals (2 leads)	**XTAL** + Body Length **X** Body Width **X** Height
Dual Flat No-lead	**DFN** + Body Length **X** Body Width **X** Height – Pin Qty
Diodes, Chip	**DIOC** + Body Length + Body Width **X** Height
Diodes, Molded	**DIOM** + Body Length + Body Width **X** Height
Diodes, MELF	**DIOMELF** + Body Length + Body Diameter
Fuses, Molded	**FUSM** + Body Length + Body Width **X** Height
Inductors, Chip	**INDC** + Body Length + Body Width **X** Height
Inductors, Molded	**INDM** + Body Length + Body Width **X** Height
Inductors, Precision Wire Wound	**INDP** + Body Length + Body Width **X** Height
Inductors, Chip, Array, Concave	**INDCAV** + Pitch **P** + Body Length **X** Body Width **X** Height **-** Pin Qty
Inductors, Chip, Array, Flat	**INDCAF** + Pitch **P** + Body Length **X** Body Width **X** Height **-** Pin Qty
Land Grid Array	**LGA** + Pin Qty **-** Pitch **P** + Ball Columns **X** Ball Rows _ Body Length **X** Body Width **X** Height
LED's, Molded	**LEDM** + Body Length + Body Width **X** Height
Oscillators, Side Concave	**OSCSC** + Pitch **P** + Body Length **X** Body Width **X** Height **-** Pin Qty
Oscillators, J-Lead	**OSCJ** + Pitch **P** + Body Length **X** Body Width **X** Height **-** Pin Qty
Oscillators, L-Bend Lead	**OSCL** + Pitch **P** + Body Length **X** Body Width **X** Height **-** Pin Qty
Oscillators, Corner Concave	**OSCCC** + Body Length **X** Body Width **X** Height
Plastic Leaded Chip Carriers	**PLCC** + Pitch **P** + Lead Span L1 **X** Lead Span L2 Nominal **X** Height **-** Pin Qty
Plastic Leaded Chip Carrier Sockets Square	**PLCCS** + Pitch **P** + Lead Span L1 **X** Lead Span L2 Nominal **X** Height **-** Pin Qty
Quad Flat Packages	**QFP** + Pitch **P** + Lead Span L1 **X** Lead Span L2 Nominal **X** Height **-** Pin Qty
Ceramic Quad Flat Packages	**CQFP** + Pitch **P** + Lead Span L1 **X** Lead Span L2 Nominal **X** Height **-** Pin Qty
Quad Flat No-lead	**QFN** + Pitch **P** + Body Width **X** Body Length **X** Height **-** Pin Qty + Thermal Pad
Pull-back Quad Flat No-lead	**PQFN** + Pitch **P** + Body Width **X** Body Length **X** Height **-** Pin Qty + Thermal Pad
Quad Leadless Ceramic Chip Carriers	**LCC** + Pitch **P** + Body Width **X** Body Length **X** Height **-** Pin Qty
Quad Leadless Ceramic Chip Carriers (Pin 1 on Side)	**LCCS** + Pitch **P** + Body Width **X** Body Length **X** Height **-** Pin Qty
Resistors, Chip	**RESC** + Body Length + Body Width **X** Height
Resistors, Molded	**RESM** + Body Length + Body Width **X** Height
Resistors, MELF	**RESMELF** + Body Length + Body Diameter
Resistors, Chip, Array, Concave	**RESCAV** + Pitch **P** + Body Length **X** Body Width **X** Height **-** Pin Qty
Resistors, Chip, Array, Convex, E-Version (Even Pin Size)	**RESCAXE** + Pitch **P** + Body Length **X** Body Width **X** Height **-** Pin Qty
Resistors, Chip, Array, Convex, S-Version (Side Pins Diff)	**RESCAXS** + Pitch **P** + Body Length **X** Body Width **X** Height **-** Pin Qty
Resistors, Chip, Array, Flat	**RESCAF** + Pitch **P** + Body Length **X** Body Width **X** Height **-** Pin Qty
Small Outline IC, J-Leaded	**SOJ** + Pitch **P** + Lead Span Nominal **X** Height **-** Pin Qty
Small Outline Integrated Circuit, (50 mil Pitch SOIC)	**SOIC127P** + Lead Span Nominal **X** Height **-** Pin Qty
Small Outline Packages	**SOP** + Pitch **P** + Lead Span Nominal **X** Height **-** Pin Qty
Small Outline No-lead	**SON** + Pitch **P** + Body Width **X** Body Length **X** Height **-** Pin Qty + Thermal Pad
Pull-back Small Outline No-lead	**PSON** + Pitch **P** + Body Width **X** Body Length **X** Height **-** Pin Qty + Thermal Pad
SC89	**SC89** + Pitch **P** + Lead Span Nominal **X** Height **-** Pin Qty
SC90	**SC90** + Lead Span Nominal + Body Length **X** Body Width **X** Height
SOD (Example: **SOD3717X135 = JEDEC SOD123**)	**SOD** + Lead Span Nominal + Body Width **X** Height
SOT89 (JEDEC Standard Package)	**SOT89**
SOT143 & SOT343 (JEDEC Standard Package)	**SOT143 & SOT343**
SOT143 & SOT343 Reverse (JEDEC Standard Package)	**SOT143R & SOT343R**
SOT23 & SOT223 Packages (Example: **SOT230P700X180-4**)	**SOT** + Pitch **P** + Lead Span Nominal **X** Height **-** Pin Qty
TO (Generic DPAK - Example: **TO228P970X238-3**)	**TO +** Pitch **P** + Lead Span **X** Height **-** Pin Qty

Notes:

1. **All dimensions are in Metric Units**
2. **All Lead Span and Height numbers go two places past the decimal point and “include” trailing Zeros**
3. **All Lead Span and Height numbers go two place before the decimal point and “remove” leading Zeros**
4. **All Chip Component Body Sizes are one place to each side of the decimal point**
5. **All Pitch Sizes are two places to the right & left of decimal point with no leading Zeros but include trailing zeros**

3.2 PCB Libraries SMT Non-Standard Land Pattern Names

Amplifiers	**AMP_** Mfr.’s Part Number
Batteries	**BAT_** Mfr.’s Part Number
Capacitors, Variable	**CAPV_**Mfr.’s Part Number
Capacitors, Miscellaneous	**CAP_**Mfr.’s Part Number
Crystals	**XTAL_**Mfr.’s Part Number
Diodes, Miscellaneous	**DIO_**Mfr.’s Part Number
Diodes, Bridge Rectifiers	**DIOB_**Mfr.’s Part Number
Ferrite Beads	**FB_**Mfr.’s Part Number
Fiducials	**FID** + Pad Size X Solder Mask Size
Filters	**FIL_**Mfr.’s Part Number
Fuses	**FUSE_**Mfr.’s Part Number
Fuse, Resettable	**FUSER_**Mfr.’s Part Number
Inductors, Miscellaneous	**IND_**Mfr.’s Part Number
Keypad	**KEYPAD_**Mfr.’s Part Number
LEDS	**LED_**Mfr.’s Part Number
LEDS, Chip	**LED** + Body Length + Body Width
Liquid Crystal Display	**LCD_**Mfr.’s Part Number
Microphones	**MIC_**Mfr.’s Part Number
Opto Isolators	**OPTO_**Mfr.’s Part Number
Oscillators	**OSC_**Mfr.’s Part Number **-** Pin Qty
Relays	**RELAY_**Mfr.’s Part Number
Speakers	**SPKR_**Mfr’s Part Number
Switches	**SW_**Mfr.’s Part Number
Test Points, Round	**TP** + Pad Size (1 place left of decimal and 2 places right of decimal, Example **TP100** = 1.00mm)
Test Points, Square	**TPS** + Pad Size (1 place left of decimal and 2 places right of decimal)
Test Points, Rectangle	**TP** + Pad Length **X** Pad Width (1 place left of decimal and 2 places right of decimal)
Thermistors	**THERM_**Mfr.’s Part Number
Transducers (IRDA’s)	**XDCR_**Mfr.’s Part Number
Transient Voltage Suppressors	**TVS** + Body Length + Body Width
Transient Voltage Suppressors, Polarized	**TVSP** + Body Length + Body Width
Transistor Outlines, Custom	**TRANS_**Mfr.’s Part Number
Transformers	**XFMR_**Mfr.’s Part Number
Trimmers & Potentiometers	**TRIM_**Mfr.’s Part Number
Tuners	**TUNER_**Mfr.’s Part Number
Varistors	**VAR_**Mfr.’s Part Number
Voltage Controlled Oscillators	**VCO_**Mfr.’s Part Number
Voltage Regulators, Custom	**VREG_**Mfr.’s Part Number

3.3 IPC-7251 Through-Hole Land Pattern Names

Component, Category	**Land Pattern Name**
Capacitors, Non Polarized Axial Diameter Horizontal Mounting	**CAPAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Capacitors, Non Polarized Axial Rectangular	**CAPAR** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body Thickness + **H** Body Height
Capacitors, Non Polarized Axial Diameter Vertical Mounting	**CAPADV** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Capacitors, Non Polarized Axial Rect. Vert. Mounting.	**CAPARV** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body Thickness + **H** Body Height
Capacitors, Non Polarized Axial Diameter Horizontal Mounting	**CAPAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Capacitors, Non Polarized Axial Rectangular	**CAPAR** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body Thickness + **H** Body Height
Capacitors, Non Polarized Axial Diameter Vertical Mounting	**CAPADV** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Capacitors, Non Polarized Axial Rectangular Vert. Mtg.	**CAPARV** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body Thickness + **H** Body Height
Capacitors, Non Polarized Radial Diameter	**CAPRD** + Lead Spacing + **W** Lead Width + **D** Body Diameter + **H** Body Height
Capacitors, Non Polarized Radial Rectangular	**CAPRR** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body Thickness + **H** Body Height
Capacitors, Non Polarized Radial Disk Button	**CAPRB** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body thickness + **H** Body Height
Capacitors, Polarized Axial Diameter Horizontal Mounting	**CAPPA** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Capacitor, Polarized Radial Diameter	**CAPPR** + Lead Spacing + **W** Lead Width + **D** Body Diameter + **H** Body Height
Diodes, Axial Diameter Horizontal Mounting	**DIOAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Diodes, Axial Diameter Vertical Mounting	**DIOADV** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Dual-In-Line Packages	**DIP** + Lead Span + **W** Lead Width + **P** Pin Pitch + **L** Body Length + **H** Component Height + **Q** Pin Qty
Dual-In-Line Sockets	**DIPS** + Lead Span + **W** Lead Width + **P** Pin Pitch + **L** Body Length + **H** Component Height + **Q** Pin Qty
Headers, Vertical	**HDRV** + Lead Span + **W** Lead Width + **P** Pin Pitch + **R** Pins per Row + **L** Body Length + **T** Body Thickness + **H** Component Height
Headers, Right Angle	**HDRRA** + Lead Span + **W** Lead Width + **P** Pin Pitch + **R** Pins per Row + **L** Body Length + **T** Body Thickness + **H** Component Height
Inductors, Axial Diameter Horizontal Mounting	**INDAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Inductors, Axial Diameter Vertical Mounting	**INDADV** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Jumpers, Wire	**JUMP** + Lead Spacing + **W** Lead Width
Mounting Holes Plated With Support Pad	**MTGP** + Pad Size + **H** Hole Size + **Z** Inner Layer Pad Size
Mounting Holes Non-Plated With Support Pad	**MTGNP** + Pad Size + **H** Hole Size + **Z** Inner Layer Pad Size
Mounting Holes Non-Plated Without Support Pad	**MTG** + Pad Size + **H** Hole Size + **Z** Inner Layer Pad Size + **K** Keep-out Diameter
Mounting Holes Plated with 8 Vias	**MTGP** + Pad Size + **H** Hole Size + **Z** Inner Layer Pad Size + 8 Vias
Pin Grid Array's	**PGA** + Pin Qty + **P** Pitch + **C** Pin Columns + **R** Pin Rows + **L** Body Length **X** Body Width + **H** Component Height
Resistors, Axial Diameter Horizontal Mounting	**RESAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Resistors, Axial Diameter Vertical Mounting	**RESADV** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter
Resistors, Axial Rectangular Horizontal Mounting	**RESAR** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body thickness + **H** Body Height
Test Points, Round Land	**TP** + Lead Width
Test Points, Square Land	**TPS** + Lead Width
Test Points, Top Land Round & Bottom Land Square	**TPRS** + Lead Width
Wire	PAD + Wire Width

Note: All dimensions are in Metric Units and all numbers go two places past the decimal point

Amplifiers	**AMP**_Mfr.'s Part Number
Batteries	**BAT**_Mfr.'s Part Number
Bridge Rectifiers	**DIOB**_Mfr.'s Part Number
Converters	**CONV**_Mfr.'s Part Number
Crystals	**XTAL**_Mfr.'s Part Number
Diodes, Miscellaneous	**DIO**_Mfr.'s Part Number
Ferrite Beads	**FB**_Mfr.'s Part Number
Filters	**FIL**_Mfr's Part Number
Fuses	**FUSE**_Mfr.'s Part Number
Fuses, Resettable	**FUSER**_Mfr.'s Part Number
Heat Sinks	**HSINK**_Mfr.'s Part Number
Jumpers, Wire	**JUMP** + Distance between Pads in Metric
LED's	**LED**_Mfr.'s Part Number
Liquid Crystal Display	**LCD**_Mfr.'s Part Number
Microphones	**MIC**_Mfr.'s Part Number
Opto Isolators	**OPTO**_Mfr.'s Part Number
Oscillators	**OSC**_Mfr.'s Part Number
Regulators	**REG**_Mfr.'s Part Number
Relays	**RELAY**_Mfr.'s Part Number
Resistor Networks	**SIP** + Pin Qty
Shield, off the shelf	**SHIELD**_Mfr.'s Part Number
Shield, Custom	**SHIELD** + Body Length **X** Body Width in Metric
Speakers	**SPKR**_Mfr's Part Number
Stiffners	**STIF**_Mfr's Part Number
Switches	**SW**_Mfr.'s Part Number
Thermistors	**THERM**_Mfr.'s Part Number
Transducers (IRDA's)	**XDCR**_Mfr.'s Part Number
Transient Voltage Suppressors	**TVS** + Mfr.'s Part Number
Transient Voltage Suppressors, Polarized	**TVSP** + Mfr.'s Part Number
Transistor Outlines, Standard	**TO-** JEDEC Number
Transistor Outlines, Custom	**TRANS**_Mfr.'s Part Number
Transformers	**XFMR**_Mfr.'s Part Number
Trimmers & Potentiometers	**TRIM**_Mfr.'s Part Number
Tuners	**TUNER**_Mfr.'s Part Number
Varistors	**VAR**_Mfr.'s Part Number
Voltage Controlled Oscillator	**VCO**_Mfr.'s Part Number
Voltage Regulators	**TO-** JEDEC Number

3.4 Connector Land Pattern Names

Manufacturer	Land Pattern Name
3M™	3M_Part Number
AGILENT™	AGILENT_Part Number
AIRBORNE™	AIRBORNE_Part Number
AMPHENOL™	AMPHENOL_Part Number
AVX™	AVX_Part Number
BERG™	BERG_Part Number
BLOCKMASTER ELECTRONICS™	BLOCKMASTER_Part Number
CUI-STACK™	CUI-STACK_Part Number
E.F. JOHNSON™	JOHNSON_Part Number
ERNI™	ERNI_Part
FCI ELECTRONICS™	FCI_Part Number
FUJITSU™	FUJITSU_Part Number
HIROSE™	HIROSE_Part Number
ITT CANNON™	ITT_Part Number
JALCO™	JALCO_Part Number
JWT™	JWT_Part Number
JST™	JST_Part Number
KEYSTONE™	KEYSTONE_Part Number
KYCON™	KYCON_Part Number
LEMO™	LEMO_Part Number
MILL-MAX™	MILL-MAX_Part Number
MOLEX™	MOLEX_Part Number
NEUTRIK™	NEUTRIK_Part Number
PHOENIX™	PHOENIX_Part Number
PULSE™	PULSE_Part Number
RIA™	RIA_Part Number
SAMTEC™	SAMTEC_Part Number
SIEMENS™	SIEMENS_Part Number
SPEEDTECH™	SPEEDTECH_Part Number
STEWART™	STEWART_Part Number
SULLINS™	SULLINS_Part Number
SWITCHCRAFT™	SWITCHCRAFT_Part Number
TYCO™	TYCO_Part Number
YAMAICHI™	YAMAICHI_Part Number

3.5 Syntax Explainations

The **+** (plus sign) stands for "in addition to" (no space between the prefix and the body size)
The **_** (underscore) is the separator between the Prefix and the Mfr Part Number.
The **–** (dash) is used to separate the pin qty.
The **X** (capital letter X) is used instead of the word "by" to separate two numbers such as height **X** width like "Quad Packages".
Connector Libraries:
In large connector such as AMP, MOLEX and SAMTEC the "Series Number" is used and the pin qty.
Molex Example: **90663-60**
The "Connector" library will contain the manufacturer's name and part number

SUFFIXES For Every Common SMT Land Pattern to Describe Environment Use (This is the last character in every name)

- **M**......................Most Material Condition (Level A)
- **N** ....Nominal Material Condition (Level B)
- **L**.......................Least Material Condition (Level C)

Note: This excludes the BGA component family as they only come in the Nominal Environment Condition

SUFFIXES for Alternate Components that do not follow the JEDEC, EIA or IEC Standard

- **A** ....Alternate Component (used primarily for SOP & QFP when Component Tolerance or Lead Size is different)
- **B** ....Second Alternate Component

SUFFIXES for JEDEC and EIA Standard parts that have several alternate packages

- **AA, AB, AC**.....JEDEC or EIA Component Identifier (Used primarily on QFN and SON component families)

GENERAL SUFFIXES

- **_VIA ....Vias (Mounting Holes with 8 vias) - Example: MTG370X700_VIA**
- **_HS ....HS will be placed between the Pin Qty and the Environment - Example: TO254P1340X300_HS-6N**
- **_BEC ....BEC = Base, Emitter and Collector (Pin assignments used for three pin Transistors)**
- **_SGD ....SGD = Source, Gate and Drain (Pin assignments used for three pin Transistors)**
- **_321 ....321 = Alternate pin assignments used for three pin Transistors - Example: SOT95P285X240_321-3N**

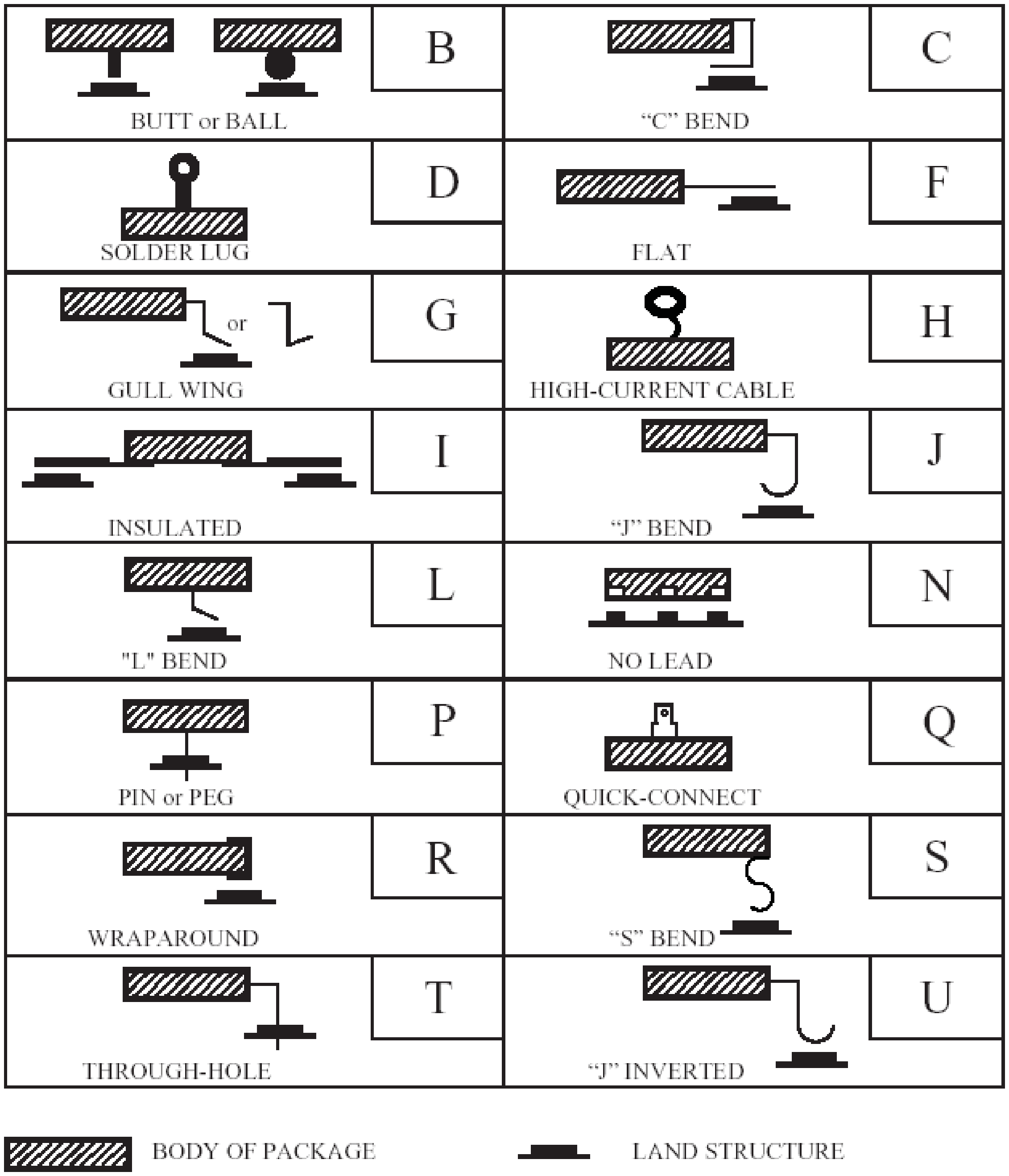
The CAD Library of the Future will use a Standard Land Pattern Naming Convention

4 COMPONENT LEAD FORMS

4.1 Standard JEDEC Component Leads

The chart below illustrates all the different component leads that must solder to a PCB board.

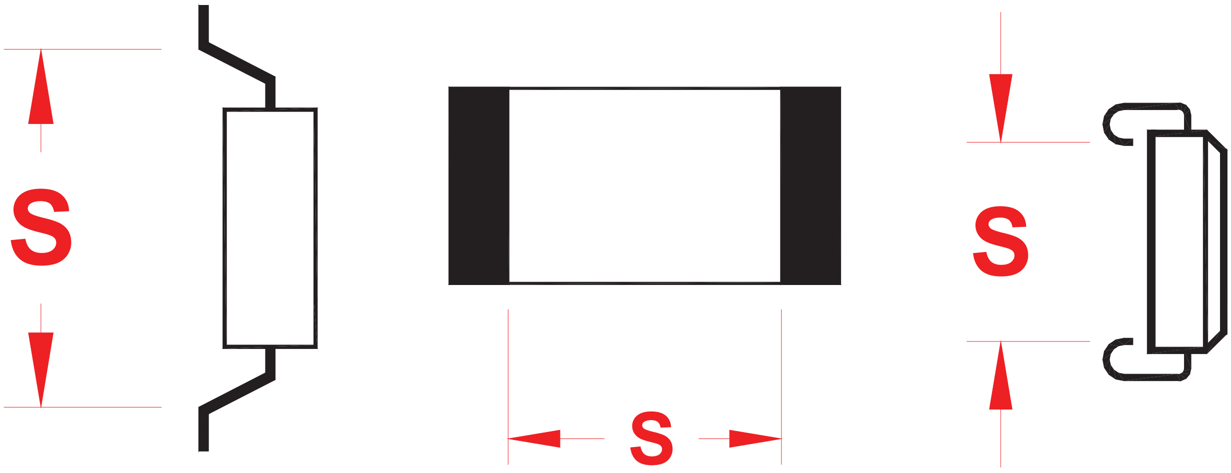
JEDEC Standard No. 30-B
Page 18



5 SOLDER JOINT TOLERANCE

5.1 Component Lead Space Tolerance

This Solder Joint Tolerance is for the inside dimension between the component terminal. It is normally represented by the “S” symbol. See the pictures below as a reference.



The “S” dimension is used to calculate the inside spacing of Component Terminal Leads and has Minimum & Maximum values referred to as the “S” Tolerance. The “S” dimensional tolerance has a direct affect on the Toe and Heel values which in turn affect the overall pad length.

For CAPC3216 (1206) example:
RMS tolerance accumulation = $\sqrt{(L_{tol})_2 + 2(T_{tol})_2}$

Where:
$L_{tol} = L_{max} - L_{min}$
$T_{tol} = T_{max} – T_{min}$

tol = tolerance
max = maximum
min = minimum

As an example, the SOIC with 16 leads has the following limits for the “L” (component length) and “T” (terminal length) dimensions:
L_{min} = 5.8 mm, L_{max} = 6.2 mm
$L_{tol} = L_{max} - L_{min}$ = 6.2 mm - 5.8 mm = 0.4 mm
T_{min} = 0.4 mm, T_{max} = 1.27 mm
$T_{tol} = T_{max} - T_{min}$ = 1.27 mm - 0.4 mm = 0.87 mm

Therefore, the calculations for “S” minimum and maximum dimensions are as follows:
$S_{min} = L_{min} - 2T_{max}$ = 5.8 mm - 2 (1.27 mm) = 3.26 mm
$S_{max} = L_{max} - 2T_{min}$ = 6.2 mm - 2 (0.4 mm) = 5.40 mm
$S_{tol} = S_{max} - S_{min}$ = 5.4 mm - 3.26 mm = 2.14 mm

The difference between S_{min} and S_{max} is 2.14 mm, which is probably a larger tolerance range than the actual range within which these components are manufactured. This worst-case scenario for the tolerance range for ''S'' can also be calculated by adding the tolerances for the component length and the two terminals:
$S_{tol} = L_{tol} + 2T_{tol} = 0.4 \text{ mm} + 2\ (0.87 \text{ mm}) = 2.14 \text{ mm}$

In order to arrive at a more realistic tolerance range, the RMS value is calculated using the tolerances on the dimensions involved (''L'' and ''T''):

$$\mathbf{S_{tol}\ (RMS) = \sqrt{(L_{tol})^2 + 2(T_{tol})^2} = \sqrt{0.4^2 + 2(0.87)^2} = 1.30 \text{ mm}}$$

The difference between worse case and the RMS value is 2.14 – 1.30 = 0.84. This variation is the difference between the two methods for tolerance analysis. In order to derive a new Maximum and Minimum dimension for "S" to determine land patterns, half of this difference is subtracted from the worse case S_{max} (5.4 - 0.42 = 4.98); and half the difference is added to the worse case Smin. (3.26 + 0.42 = 3.68). Thus, 4.98 to 3.68 becomes the variation (Max/Min) for the S dimension.

This technique is used so that a more realistic S_{max} dimension is used in the land pattern equations for calculating G_{min} (minimum land pattern gap between heel fillets).

5.2 Land Pattern Pad Length Tolerance

The "G" dimension is used to calculate the minimum and maximum inside spacing of the solder pad. The "Z" dimension is used to calculate the minimum and maximum outside spacing of the solder pad. See the following pictures.

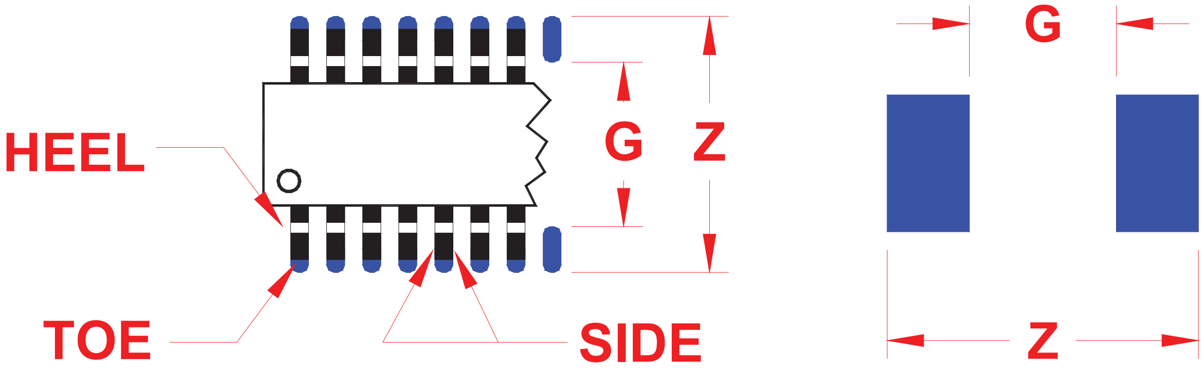


Figure 5.2.1

The "G" and "Z" values are used to determine the maximum and minimum values of the pad length. They take into consideration the component terminal length tolerance, the Toe value (the pad size on the outside of the component terminal) and the Heel value (the pad size on the inside of the component terminal).

Solving for Dimension ''G'' The inner dimensions between heel fillets on opposing sides are the most important. Inner dimensions are derived by:

a. Establishing the maximum outline of the component as measured from lead termination end to lead termination end. (This dimension is shown as ''L,'' and is provided by the manufacturer).

b. Establishing the minimum amount of the lead length as measured across the ''footprint'' (from heel to toe for gull-wing leads). (This dimension is ''T,'' and is provided by the manufacturer).

c. Subtracting twice the minimum lead length of (T) from the maximum overall component length of (L) to arrive at the maximum length inside the leads across the length

d. Three sets of tolerances are involved in the analysis described within three tolerances on the overall component, plus the tolerances for the lead on each end. Since not all three tolerances are considered at their worst case, a recommended method for determining the statistical impact is to summarize the squares of the tolerances and take the square root of their sum as the RMS (root-mean-square) tolerance difference.

For example:

RMS tolerance accumulation $= \sqrt{(L_{tol})^2 + 2(T_{tol})^2}$

Where:

$L_{tol} = L_{max} - L_{min}$

$T_{tol} = T_{max} - T_{min}$

tol = tolerance
max = maximum
min = minimum

As an example, the SOIC with 16 leads has the following limits for the ‘‘L’’ (component length) and ‘‘T’’ (terminal length) dimensions:

L_{min} = 5.8 mm, L_{max} = 6.2 mm

$L_{tol} = L_{max} - L_{min}$ = 6.2 mm - 5.8 mm = 0.4 mm

T_{min} = 0.4 mm, T_{max} = 1.27 mm

$T_{tol} = T_{max} - T_{min}$ = 1.27 mm - 0.4 mm = 0.87 mm

Therefore, the calculations for ‘‘S’’ minimum and maximum dimensions are as follows:

$S_{min} = L_{min} - 2T_{max}$ = 5.8 mm - 2 (1.27 mm) = 3.26 mm

$S_{max} = L_{max} - 2T_{min}$ = 6.2 mm - 2 (0.4 mm) = 5.40 mm

$S_{tol} = S_{max} - S_{min}$ = 5.4 mm - 3.26 mm = 2.14 mm

The difference between S_{min} and S_{max} is 2.14 mm, which is probably a larger tolerance range than the actual range within which these components are manufactured. This worst-case scenario for the tolerance range for ‘‘S’’ can also be calculated by adding the tolerances for the component length and the two terminals:

$S_{tol} = L_{tol} + 2T_{tol}$ = 0.4 mm + 2 (0.87 mm) = 2.14 mm

In order to arrive at a more realistic tolerance range, the RMS value is calculated using the tolerances on the dimensions involved (‘‘L’’ and ‘‘T’’):

S_{tol} (RMS) $= \sqrt{(L_{tol})^2 + 2(T_{tol})^2} = \sqrt{0.4^2 + 2(0.87)^2} = \mathbf{1.29\ mm}$

S_{tol} (RMS) is added to S_{min} to arrive at a maximum ‘‘S’’ dimension. This technique is used so that a more realistic S_{max} dimension is used in the land pattern equations for calculating G_{min} (minimum land pattern gap between heel fillets). In this example, the following calculation is used for S_{max}:

$$\begin{aligned} S_{max}\ (\text{RMS}) &= S_{min} + S_{tol}\ (\text{RMS}) \\ &= 3.26\text{ mm} + 1.29\text{ mm} \\ &= 4.55\text{ mm} \end{aligned}$$

In the previous example, the two joints should be rounded to a realistic number. Normally, a total Z dimension of 7.0 mm would be acceptable for a density level B land pattern providing a 0.4 mm land protrusion at either end of the SO16 component.

Solving for Dimension ''Z'' It should be noted that there are various options to determine the tolerances for the component (C), the fabrication allowance (F), and the placement tolerance (P). In determining the calculations for the example in Figure 5.2.1 for the dimension ''Z,'' one would note that the component ''SO16'' has an L_{max} equal to 6.20 mm, and an L_{min} equal to 5.80 mm. With the assumption that ''F'' is equal to 0.1 mm and ''P'' is equal to 0.2 mm, the following conditions would be used for determining the ''Z'' dimension:

$$Z_{max} = L_{min} + 2J_T + \sqrt{C_{L2} + F_2 + P_2}$$

$$Z_{max} = 6.20\text{ mm} + 2J_T + \sqrt{0.4_2 + 0.1_2 + 0.2_2}$$

''G'' dimension. This action results in a reduced land pattern at Least Material Condition (LMC). Thus, processing target values should be as close as possible to the basic ''Z'' and ''G'' dimensions at Maximum Material Condition (MMC). This concept also holds true for the width (X) of the land dimension which is specified at maximum size.

The variation between the dimensions Z, G, and X are indicated as a fabrication allowance (F). This fabrication allowance represents the maximum variation between the largest land pattern size (MMC) and the least land pattern size (LMC). This does not include material movement which is included in the assembly tolerancing since machine vision capability revaluates the true position of the land pattern.

In the above example, the two joints should be rounded to a realistic number. Normally, a total Z dimension of 7.0 mm would be acceptable for a density level B land pattern providing a 0.4 mm land protrusion at either end of the SO16 component.

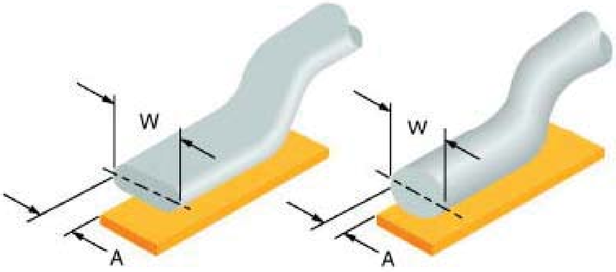
The CAD Library of the Future will use Component Lead, Fabrication and Assembly Tolerances to determine land pattern Pad Size

6 SOLDER JOINT ANALYSIS

6.1 Solder Joint Toe, Heel and Side Goal

The chart below provides an example of the typical Gull Wing component lead Solder Joint Goal

Round or
Flattened
Leads



Round or flattened (coined) leads (unit: mm)

Land pattern characteristics	**Maximum Level 1**	**Median Level 2**	**Minimum Level 3**
Toe-land protrusion	1,0	0,65	0,2
Heel-land protrusion	0,5	0,35	0,2
Side-land protrusion	0,1	0,1	0,1
Courtyard excess	0,5	0,25	0,05
Round-up factor	Nearest 0.5	Nearest 0.5	nearest 0.05

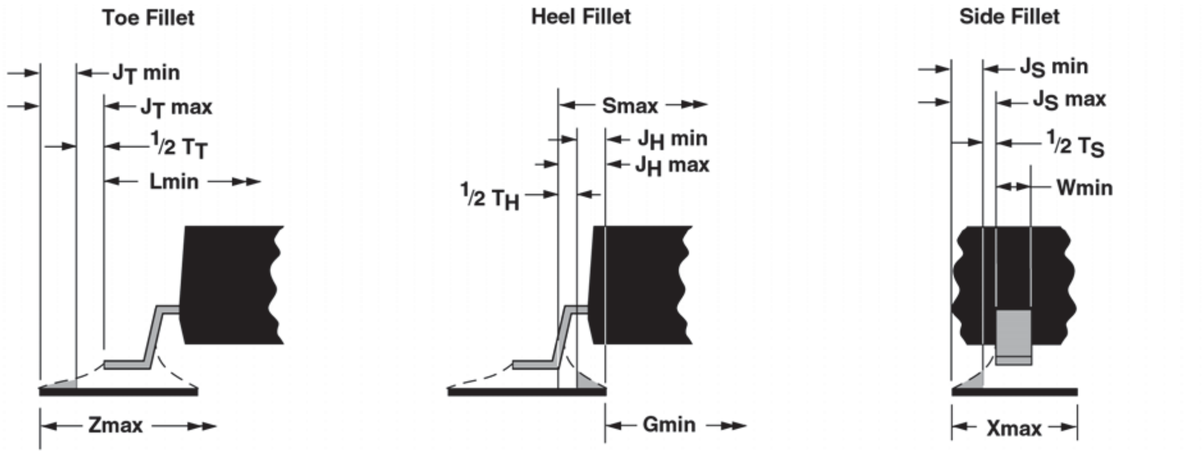
The chart below provides an example of the typical Gull Wing component lead Solder Joint Goal

Metal Electrical
Face

Cylindrical end cap terminations (MELF) (unit: mm)

Land pattern characteristics	**Maximum Level 1**	**Median Level 2**	**Minimum Level 3**
Toe-land protrusion	1,0	0,4	0,2
Heel-land protrusion	0,2	0,1	0,0
Side-land protrusion	0,2	0,1	0,0
Courtyard excess	0,5	0,25	0,05
Round-up factor	Nearest 0,5	Nearest 0,5	Nearest 0,05

The illustration below provides a graphical representation of the Gull Wing component lead to calculate the Toe, Heel and Side minimum and maximum values.



$Z_{max} = L_{min} + 2J_{T}min + T_T$

Where:

$J_{T}min$ = Minimum toe fillet

T_T = Combined tolerances at toe fillet

$G_{min} = S_{max} - 2J_{H}min - T_H$

Where:

$J_{H}min$ = Minimum heel fillet

T_H = Combined tolerances at heel fillet

$X_{max} = W_{min} + 2J_{S}min + T_S$

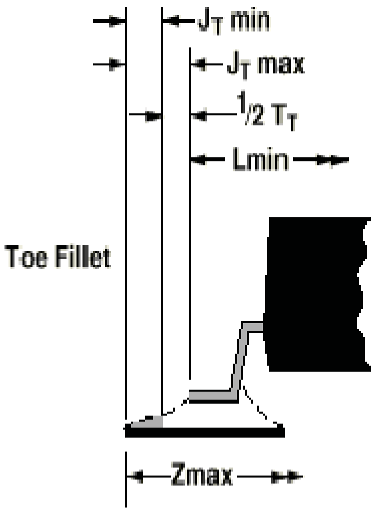
Where:

$J_{S}min$ = Minimum side fillet

T_S = Combined tolerances at side fillet

Solder Joint / Land Protrusion

- J is the desired dimension of solder fillet or land protrusion;
    - J_t is the solder fillet or land protrusion at toe;
    - J_h is the solder fillet or land protrusion at heel;
    - J_s is the solder fillet or land protrusion at side;



The CAD Library of the Future will use Solder Joint Analysis to determine the land pattern pad size

7 MANUFACTURING TOLERANCE

7.1 Fabrication Tolerances

When calculating a land pattern pad size, a fabrication tolerance must be applied to compensate for the etch-back of every feature on the outer layer of a PC board. To control the line width for impedance calculations, the PC board manufacturer might widen the trace width to compensate for the etch-back process, but they do not widen every surface mount pad size to compensate for the etch-back process.

A fabrication tolerance is added into the pad size equation. The standard fabrication tolerance is ± 0.05mm.

Figure 5.2.1 shows the land pattern for an SOIC with gull-wing leads intended to be a companion to the chip component dimensioning concepts shown in Figure 5.2.1. The basic "L" dimension is across the outer extremities of the component lead or terminal.

For the land pattern, dimension "Z" is at maximum size, while the inner extremities (dimension "G") are dimensioned at minimum size. Unilateral tolerances decreased the basic dimension for "Z" while increasing the basic "G" dimension. This action results in a reduced land pattern at Least Material Condition (LMC). Thus, processing target values should be as close as possible to the basic "Z" and "G" dimensions at Maximum Material Condition (MMC). This concept also holds true for the width (X) of the land dimension which is specified at maximum size.

The variation between the dimensions Z, G, and X are indicated as a fabrication allowance (F). This fabrication allowance represents the maximum variation between the largest land pattern size (MMC) and the least land pattern size (LMC). This does not include material movement which is included in the assembly tolerancing since machine vision capability revaluates the true position of the land pattern.

7.2 Assembly Tolerances

The assembly process also has a manufacturing tolerance that must be considered. The standard assembly tolerance allowance is ± 0.05mm.

Another part of the equation is the assembly variation defined by the letter "P."

This variation represents the location of the component in relation to its true position as defined by the design. The term diameter of true position (DTP) is used to describe this variation and is a single number that can be used in the dimensional tolerance analysis.

As an example, for establishing the target heel protrusion dimensions of the example shown in Figure 5.2.1, the following conditions would be true:

Where:

J is 0.5 mm (target heel fillet)

C is S_{tol} (RMS) = 1.29 mm (see previous calculations from component dimensions)

F is ±0.05 mm (assumed fabrication tolerance)

P is ±0.05 mm (assumed assembly equipment placement tolerance)

Therefore:

$$\begin{aligned} \mathbf{G_{min}} &= \mathbf{4.55\ mm} - \mathbf{2(0.5\ mm)} - \sqrt{(\mathbf{1.29})^2 + (\mathbf{0.1})^2 + (\mathbf{0.05})^2} \\ &= \mathbf{2.25\ mm} \end{aligned}$$

Another major condition for multiple-leaded components that must be considered in land pattern design is lead, termination, or castellation pitch. The pitch describes the basic dimension of the spacing of one component lead termination or castellation to its adjacent counterpart(s). No tolerance is assigned to pitch in the profile dimensioning concept. Differences in pitch are included in the width dimensions of the lead, termination, or castellation which are dimensioned as basic at the minimum size.

The worst-case criteria for determining a dimension would require that ''C,'' ''F,'' and ''P'' be added to the minimum dimension of the component length plus the solder joint requirements, in order to determine the maximum dimension of the outer land pattern.

Experience shows that the worst-case analysis is not always necessary; therefore statistical methods are used by taking the square root of the sum of the squares of the tolerances.

This method assumes that all features will not reach their worst case. The equations for determining component land pattern requirements are as follows:

$$Z_{max} = L_{min} + 2J_T + \sqrt{C_L^2 + F^2 + P^2}$$

$$G_{min} = S_{max} - 2J_H - \sqrt{C_S^2 + F^2 + P^2}$$

$$X_{max} = W_{min} + 2J_S + \sqrt{C_W^2 + F^2 + P^2}$$

Where:

Z is the overall length of land pattern

G is the distance between lands of the pattern

X is the width of land pattern

L is the overall length of component

S is the distance between component terminations

W is the width of the lead or termination

J is the desired dimension of solder fillet or land protrusion

  J_T is the solder fillet or land protrusion at toe

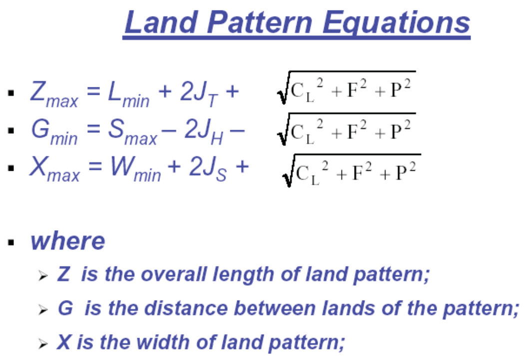
  J_H is the solder fillet or land protrusion at heel

  J_S is the solder fillet or land protrusion at side

7.3 Component Terminal Tolerances

Every component terminal lead has a manufacturing tolerance that the component manufacturer must hold to. The larger the component lead tolerance minimum and maximum values, the longer the land pattern pad must be to compensate for the component manufacturing tolerance.

Below is the mathematical formula for calculating the Z, G and X dimensional values by taking into consideration the Component, Fabrication and Assembly Tolerances.



Land Pattern Equations

- $Z_{max} = L_{min} + 2J_T + \sqrt{C_L^2 + F^2 + P^2}$
- $G_{min} = S_{max} - 2J_H - \sqrt{C_L^2 + F^2 + P^2}$
- $X_{max} = W_{min} + 2J_S + \sqrt{C_L^2 + F^2 + P^2}$
- ***where***
  - ***Z is the overall length of land pattern;***
  - ***G is the distance between lands of the pattern;***
  - ***X is the width of land pattern;***

Land tolerancing is used for lands in a manner similar to that of the components. All tolerances for lands are intended to provide a projected land pattern with individual lands at maximum size. Unilateral tolerances are intended to reduce the land size and thus result in a lesser area for solder joint formation. In order to facilitate companion dimension systems, the land pattern is dimensioned across outer and inner extremities.

The dimensioning concept in this standard uses limiting dimensions and geometric tolerancing to describe the allowable maximum and minimum dimensions of the land pattern. When lands are at their maximum size, the result may be a minimum acceptable space between lands; conversely when lands are at their minimum size, the result may be a minimum acceptable land pattern necessary to achieve the minimum required land protrusion. These thresholds allow for gauging of the land pattern for go/no-go conditions. The whole concept of the dimensioning system described in this document is based on these principles and extends to component mounting dimensions, land pattern dimensions, positioning dimensions, etc., so that the requirements may be examined using optical gauges at any time in the process in order to insure compliance with the tolerance analysis.

7.4 Dimension and Tolerance Analysis

In analyzing the design of a component/land pattern system, several things come into play, including the size and position tolerances of the component lead or termination, the tolerances of the land pattern, and the placement accuracy of the man/machine to center the part to the land pattern. The result is the land area available for a solder joint that provides a proper formation of a toe, heel, or side fillet.

System equations have been developed for chip components and multiple leaded parts. These concepts assume that the target values of parts and land patterns are maximized to reflect solder joint formation (i.e., outer dimensions of components at minimum size with outer dimensions of land patterns at maximum size). The equations use the following symbols:

C is the unilateral profile tolerance(s) for the component

F is the unilateral profile tolerance(s) for the board land pattern

P is the diameter of true position placement accuracy to the center of the land pattern

With the assumption that a particular solder joint or solder volume is desired for every component, some methods use C is the component tolerances.

C_L is the tolerance on component length

C_S is the tolerance on distance between component terminations

C_W is the tolerance on the lead width

F is the printed board fabrication (land pattern geometric) tolerances

P is the part placement tolerance (placement equipment accuracy)

The formula (the square root of the sum of the squares) is identical for both toe and heel solder joint formation (different tolerances are used, however). However, the desired solder joint dimension and the square root of the sum of the squares are added for outer land pattern dimensions and subtracted for inner land pattern dimensions. The result provides the final land pattern dimensions Z, G, and X.

The same concept is true for chip, multiple leaded or leadless components. Additionally, pitch with lead-to-land overlap (M) can be evaluated as well as the space (N) to reflect the clearance between a lead, termination, or castellation and the adjacent land(s). These latter values are not used in the equations to determine the land pattern sizes, but may be used to limit lead-to-adjacent land proximity and to adjust lead-to-land overlap.

The CAD Library of the Future will use Fabrication, Assembly and Component Lead tolerances

8 ZERO COMPONENT ORIENTATION

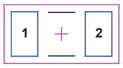
8.1 Pick & Place Machine Tape & Reel Orientation Requirements

The Component Zero Rotation relates to the Pick & Place machine tape and reel and component tubes. The rotation of the actual component in a tray or tape & reel is referred to as the Zero Rotation for the CAD Library part and how it should be built in the CAD library. All CAD Library parts should be built in the CAD system in the same rotation that the component is packaged in the tape and reel or assembly feeder tube.

The JEDEC JEP95 specification and the EIAJ / ANSI 481 are the industry guideline for component packaging information.

This is a list of the most commonly used parts in the world today and their correct Zero Rotation

1) Chip Capacitors, Resistors and Inductors (RES, CAP and IND) – **Pin 1 (Positive) on Left**



2) Molded Inductors (INDM), Resistors (RESM) and Tantalum Capacitors (CAPT) - **Pin 1 (Positive) on Left**

3) Precision Wire-wound Inductors (INDP) – **Pin 1 (Positive) on Left**

4) MELF Resistors and Diodes (DIOMELF) – **Pin 1 (Cathode) on Left**

5) Aluminum Electrolytic Capacitors (CAPAE) – **Pin 1 (Positive) on Left**

6) SOT Devices (SOT23, SOT23-5, SOT223, SOT89, SOT143, etc.) – **Pin 1 Upper Left**

7) TO252 & TO263 (DPAK Type) Devices – **Pin 1 Upper Left**

8) Small Outline Gullwing ICs (SOIC, SOP, TSOP, SSOP, TSSOP) – **Pin 1 Upper Left**

9) Ceramic Flat Packs (CFP) – **Pin 1 Upper Left**

10) Small Outline J Lead ICs (SOJ) – **Pin 1 Upper Left**

11) Quad Flat Pack ICs (PQFP, SQFP) – **Pin 1 Upper Left**

12) Ceramic Quad Flat Packs (CQFP) – **Pin 1 Upper Left**

13) Bumper Quad Flat Pack ICs (BQFP) – **Pin 1 Top Center**

14) Plastic Leaded Chip Carriers (PLCC) – **Pin 1 Top Center**

15) Leadless Chip Carriers (LCC Pin 1 in Center) – **Pin 1 Top Center**

16) Leadless Chip Carriers (LCCS Pin 1 on Side) – **Pin 1 Upper Left**

17) Quad Flat No-Lead ICs (QFNS, QFNRV and QFNRH) – **Pin 1 Upper Left**

18) Ball Grid Arrays (BGA) & Land Grid Arrays (LGA) – **Pin A1 Upper Left**

The CAD Library of the Future will use the above Component Zero Orientations

9 LAND PATTERN ORIGIN

9.1 CAD Library Part Origins

The land pattern origin is the component “Center of Gravity”, so in most cases it’s the Center of the library part. An example of where it’s not the center is the DPAK or TO-252 component.

The land pattern origin is the zero point in which all the features of the land pattern are derived. The origin is also the center of rotation. The point in which the land pattern rotates around is the Land Pattern Origin.

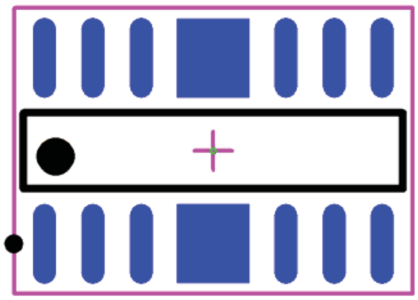
Before SMT parts came into existence, the common land pattern origin for through-hole parts was Pin 1. The main reason for this was a convenience to the PCB designer to keep the component pins on a common grid to make the routing phase of the PCB design layout easy.

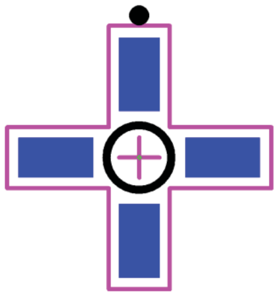
When the PCB designer provided X Y coordinate data to the assembly shop, the engineers at the assembly shop had to invent calculators for the various through-hole devices that relocated the part origin from pin 1 to the center of the part.

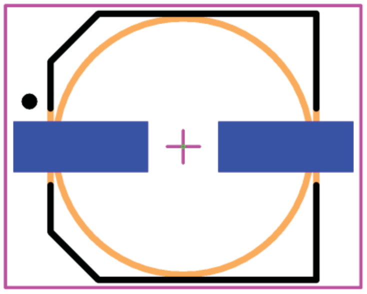
Today with SMT and Through Hole mixed technology and with the need to streamline and automate the assembly process, all land origins should be located in the part center. The only exception to this rule would be components or connectors that absolutely require hand assembly. Then the PCB designer can select the land pattern origin to whatever makes their job easier.

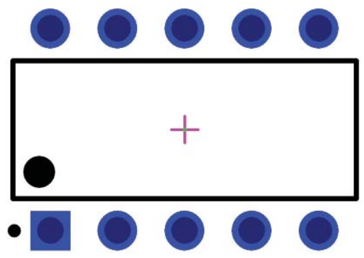
A good feature to add to the CAD library land pattern is a cross hair placed on a documentation layer so that it is visible to the PCB designer. This is a part placement aid. When the PCB Designer selects a component to move it, most CAD tools will make the part origin jump to wherever the cursor is. This is very annoying when you’re fine-tuning a part placement and your goal is just to tweak the placement. If you can visually see the cross hair on the origin, you can select the part at the cross hair location and the part will not jump.

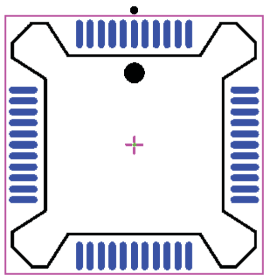
9.2 Sample Pictures of Land Pattern Origins











10 PLACEMENT COURTYARD

10.1 SMT Placement Courtyard

The placement courtyard was introduced by IPC in the IPC-SM-782 Surface Mount Design Land pattern Standard in 1987 and fine-tuned in the 2005 release of the IPC-7351.

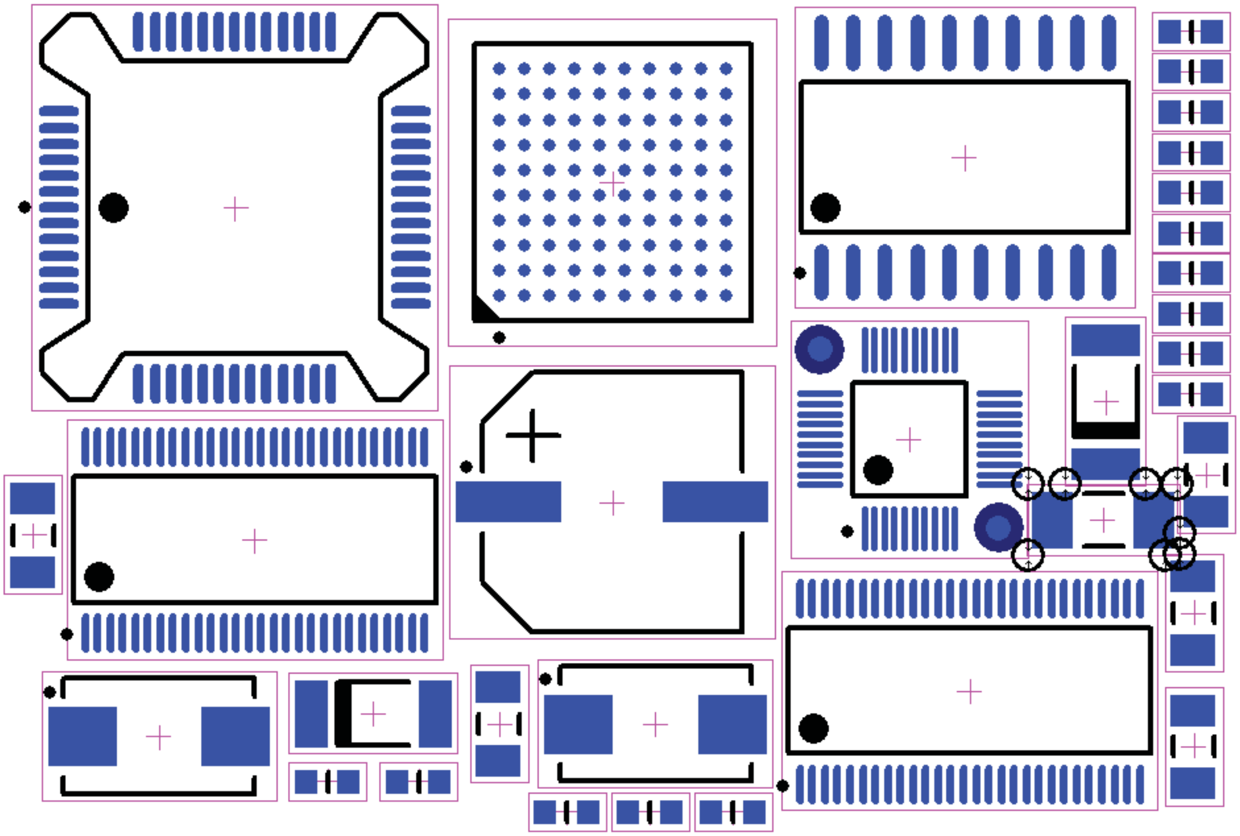
The primary use of the placement courtyard was to provide the PCB designer a guideline for placing land patterns next to each other with enough room to compensate for component tolerances.

Courtyard outlines are used to insure that all parts will fit, but they do not compensate for assembly machine heads and manufacturing allowances. Each assembly manufacturer has there own unique processes that require various allowances. Placement Courtyards are not meant to touch each other or overlap. They should have a space gap in-between them so when the PCB Designer runs a Design Rule Check for Body-to-Body clearance, there should be "No Errors Found".

The standard courtyard line width is 0.05mm and it's placed on a layer designated by the CAD vendor. The Placement Courtyard is used as a CAD visual graphic aid for part placement and never post processed.

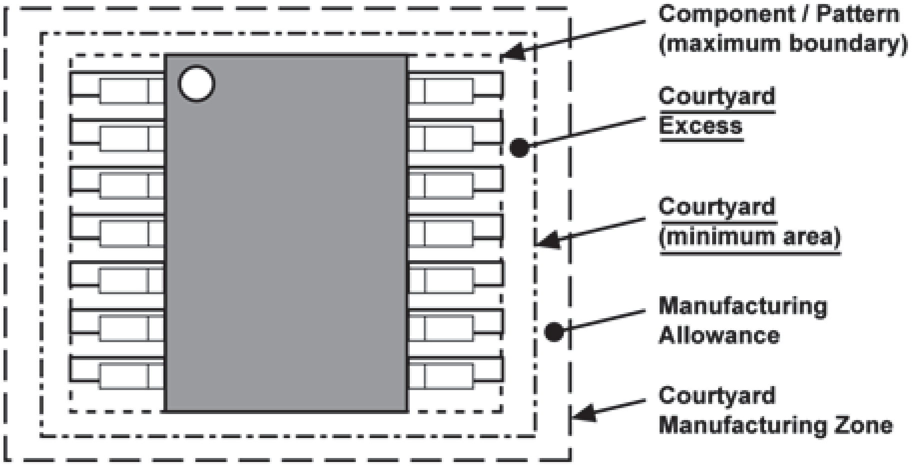
10.2 Sample Part Placement

The placement of parts below has a design rule of 0.05mm Body-to-Body. There is one component that violates to Body-to-Body spacing rule and produces error markers when a Design Rule Check is run.



10.3 Land Pattern Courtyard Determination

The illustration below shows the Component Boundary, the Minimum Courtyard Excess and the Manufacturing Allowance.



It's the Courtyard Manufacturing Zone that is critical for the assembly process. This is the Body-to-Body clearance that you set in your Design Rules for Design Rule Checking. The size of the manufacturing tolerance must come from the assembly shop that is going to be used to populate the parts on the PC Board. Every assembly shop has different assembly tolerances, but the average is 0.1mm.

The assembly process makes it very difficult to determine placement courtyards for through-hole components. It's easy to determine SMT to SMT and even Through-Hole to Through-Hole, but SMT to Though Hole gets complex, especially when placing Through-Hole parts on the Top Side and SMT parts on the bottom side. Since Through Hole parts require holes that go all the way through the PC Board, the Through Hole part Top Side courtyard would be different than the bottom side courtyard due to the wave solder process used to solder Through Hole component leads. If wave solder is used for the Through Hole component leads, the SMT parts mounted on the bottom side must have a 5mm clearance between the edge of the Through Hole pad and edge of the SMT pad. If a selective wave is used there is a different tolerance between the pads depending on the assembly shop requirements.

Therefore, building in placement courtyards for through-hole parts is almost impossible due to too many variables. A PCB designer must use common standard rules provided by the assembly shop when performing the part placement. The assembly shop should always approve the part placement prior to routing any traces on the board. This is an official check point that must not be avoided.

The CAD Library of the Future will have Placement Courtyards built into every SMD land pattern

11 SILKSCREEN OUTLINE & POLARITY

11.1 Silkscreen Outlines

Silkscreen outlines are used for cosmetic purposes only and are really not required by manufacturing.

Most CAD land pattern silkscreen outlines are not representative of the true component outline. Silkscreen outlines must avoid the exposed copper pad by 0.4mm for maximum clearance 0.3mm nominal or 0.25mm minimum.

The standard acceptable line width for silkscreen outlines is 0.2mm.

The silkscreen drawn by the PCB designer can be very complex, to illustrate their creative talent, or be very simple. In the end, it really doesn't matter because you can only see it when the physical PC board passes between the fabrication facilities to the assembly shop. Once the parts are assembled, all the silkscreen outlines are covered up and cannot be seen.

The silkscreen originated from the hand tape days. Back in the 1970s, PC boards did not have silkscreen outlines. Assembly drawings were created using rectangles and circles. Some PCB designers decided the assembly drawing would look good if it appeared on the PC board and the silkscreen was born.

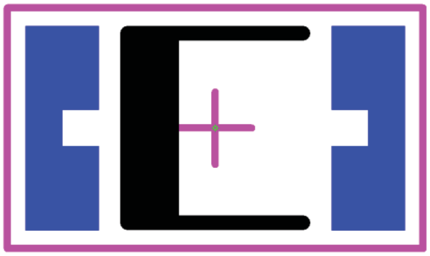
Now, most boards have part placements that are so tight that there's no room for silkscreen outside the part. It's my opinion, that with a one world standard library and full machine automation that the silkscreen will be a thing of the past. It's interesting to note that PC boards that go into outer space purposely do not have silkscreen to reduce the weight of the product.

When PCB designers start to use all the principles discussed in this outline, the manufacturing assembly process can be fully automated. The CAD Library of the Future will not require the use of silkscreen outlines.

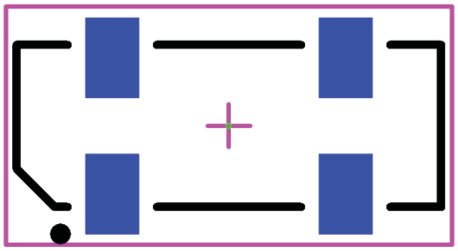
11.2 Silkscreen Polarity Markings

Some assembly shops or test engineers who are debugging a prototype might require silkscreen Polarity Markings. Silkscreen Polarity Markings are primarily used to illustrate the "Positive" terminal of a two-pin component. Polarity Markings are also used when there is a potential for inverting the part placement in the assembly process that would result in a malfunction of the component.

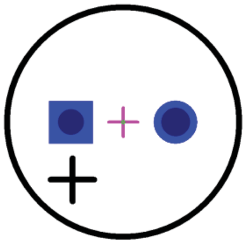
The term Polarity Marking came from its use to identify the Positive Pin on a "Polarized" capacitor. But polarity marking is also used on diodes to indicate the Cathode Pin. It's also used on connectors to illustrate the Pin 1 location. Below are some samples of Silkscreen Polarity Markings.



MELF DIODE



OSCILLATOR



CAPACITOR

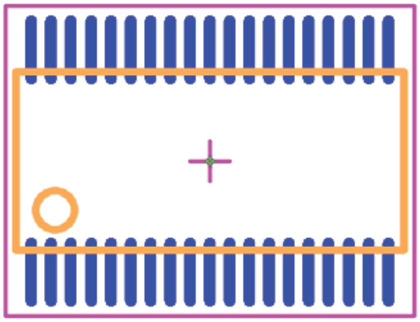
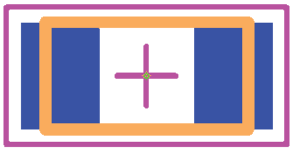
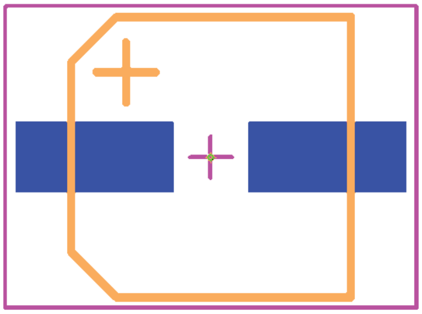
12 ASSEMBLY OUTLINE & POLARITY MARK

12.1 Assembly Drawing Outlines

The assembly drawing outline should represent the maximum outline of the component body. Unlike the silkscreen outline which has to be created to avoid solder pads (a fake component outline); the assembly outline only gets placed on an assembly drawing that goes to the assembly shop. There is no need to fake this outline.

Assembly outlines can be created with complex drawings to illustrate the actual physical component features or with a simple rectangle. It makes no difference to the assembly shop that has to interpret the assembly drawing. Drawing complex shapes for the assembly outline shows off the PCB designer's artistic creativity, but once the PC Board goes into production, it makes no difference because the assembly drawing is never used again. The CAD Library of the Future will have 1:1 scale component outlines in the assembly drawing.

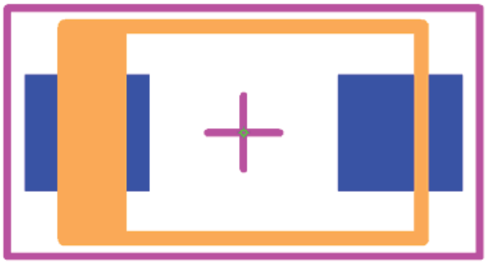
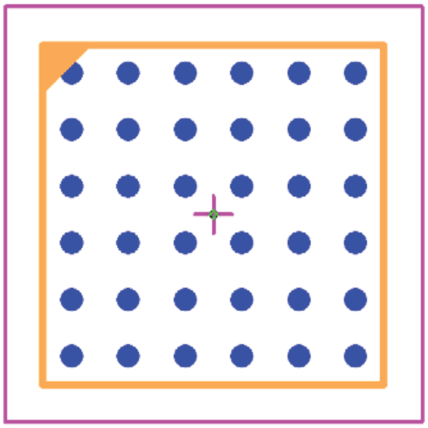
Here are some samples of assembly drawing component outlines in relationship to the solder pad.

12.2 Assembly Polarity Marking

The assembly Polarity Marking is sometimes totally different than the silkscreen Polarity Marking because the silkscreen must avoid touching the solder pad. Unlike the silkscreen, the assembly drawing can illustrate robust polarity markings to insure that the component is inserted with the correct rotation.

Here is some sample assembly drawing component Polarity Markings in relationship to the solder pad.

13 PADSTACKS

13.1 Surface Mount Padstack

The surface mount component padstack consists of a solder pad, solder mask and solder paste. We've already discussed the creation of the pad size. The solder mask and paste mask size is typically the same as the pad size.

Solder Mask - We allow the PC Board manufacturer to expand the solder mask size according the rule technology that the PCB designer used to design the PCB layout. If the design layout had a trace/space rule setting of 0.3mm (0.012"), then the manufacture could expand the solder mask size larger than if the design layout had a trace/space rule of 0.1mm (0.004").

In the past, PCB designers had a strict rule that the PC Board manufacturers not modify their Gerber data. But with today's CAM technology, board manufacturers often have more advanced design rule checking features than our CAD tools do. It's OK to let the board manufacturer adjust the solder mask size to accommodate their manufacturing equipment and solder mask application technique. It's probably better that PCB designers let the manufacturers do their job and to not try guess what the manufacturer needs.

The most important aspect is that all solder mask sizes be built in the padstack 1:1 scale so that the manufacturer can globally oversize all pads with the same oversize. All Solder Mask sizes are in increments of 0.05mm.

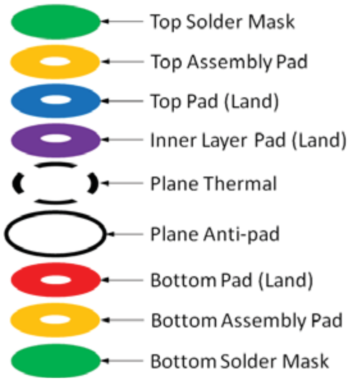
Solder Paste – We allow the stencil maker to oversize the solder paste to match the specifications of the assembly shop that the paste mask stencil is being made for. It is important that the Solder Paste size in the padstack be the same size as the pad to make the stencil creation process easy. If we make adjustments for BGA pad sizes or other SMT components, the stencil maker does not know this. It's much better to tell the solder paste stencil maker that all the pad size data is 1:1 scale to the Solder Paste data.

13.2 Through Hole Padstack

The Through-Hole Padstack is much more complex than the Surface Mount Padstack because it contains a drill size that goes all the way through the PC Board.

This is what a typical Through-Hole Padstack is built like:

Top Solder Mask
Top Assembly Pad
Top Pad
Inner Layer Pad
Plane Thermal Relief
Plane Anti-pad
Bottom Pad
Bottom Assembly Pad
Bottom Solder Mask
Drilled Hole



Solder Mask – The rule mentioned above is applicable to the Through-Hole Padstack.

Pad Size – The Pad Size is determined by two factors. 1) It is at least 0.25mm (0.010") larger than the Drilled Hole size. 2) It is capable of handling the electrical current of the component lead. The larger the component lead, the larger the hole size, the more potential for high current. Component manufactures do not make large component lead sizes unless they are intended to withstand a particular electrical current. The Pad Size must also be able to withstand that same current or it will become a fuse point that has the potential of heating up past the melting point temperature of the prepreg that the pad is fused to.

Anti-pad – The Power Plane Anti-Pad is the copper clearance around the drilled hole on an inner layer power or ground plane. The Anti-pad size is determined by two factors. 1) The PC Board manufacturer requires the anti-pad size to be at least a minimum of 0.5mm (0.020") larger than the drilled hole and a nominal size if 0.6mm (0.024") larger than the drilled hole. 2) The EE Engineer does not want you to make the anti-pad any larger than the PC Board manufacturers nominal size because the anti-pad = anti-copper or the removal of copper from the power or ground plane. It is very important in today's high speed design layouts that every critical signal has a clean return path. If the plane anti-pads are created too large, the signal traces pass over areas void of copper creating signal integrity problems. All Anti-pad sizes are in increments of 0.05mm.

Thermal Relief – The Power Plane Thermal Relief has five attributes. Thermal Relief's have an outside diameter, an inside diameter, a spoke width, a spoke rotation and 2 or 4 spokes. The Outside Diameter is typically the same size as the Anti-pad. The inside diameter is typically 80% less than the outside diameter. The spoke width is typically 4 times smaller than the outside diameter with 4 spokes or 3 times smaller than the outside diameter with 2 spokes. The spoke rotation is normally 45 degrees with 4 spokes. All Thermal Relief feature sizes are in increments of 0.05mm.

Drilled Hole – The Drilled Hole size is typically 0.3mm (0.012") larger than the longest portion of the component lead size and rounded up to the nearest 0.05mm (0.002"). All Drill Hole sizes are in increments of 0.05mm.

The IPC-7251 Level A chart below is the most commonly used Through-Hole component leads

Max Lead Dia	Minimum Finished Hole Diameter	Mounted Land	Internal Layer Land Diameter	Opposite Land	Solder Mask Top & Bottom	Assembly Top & Bottom	Plane Clearance Anti-pad Diameter	Thermal OD	Thermal ID	Thermal 4 Spoke Width
0.10	0.35	0.85	0.85	0.85	0.85	0.85	1.35	1.35	0.95	0.13
0.15	0.40	0.90	0.90	0.90	0.90	0.90	1.40	1.40	1.00	0.14
0.20	0.45	0.95	0.95	0.95	0.95	0.95	1.45	1.45	1.05	0.14
0.25	0.50	1.00	1.00	1.00	1.00	1.00	1.50	1.50	1.10	0.15
0.30	0.55	1.05	1.05	1.05	1.05	1.05	1.55	1.55	1.15	0.16
0.35	0.60	1.10	1.10	1.10	1.10	1.10	1.60	1.60	1.20	0.17
0.40	0.65	1.15	1.15	1.15	1.15	1.15	1.65	1.65	1.25	0.17
0.45	0.70	1.20	1.20	1.20	1.20	1.20	1.70	1.70	1.30	0.18
0.50	0.75	1.25	1.25	1.25	1.25	1.25	1.75	1.75	1.35	0.19
0.55	0.80	1.30	1.30	1.30	1.30	1.30	1.80	1.80	1.40	0.20
0.60	0.85	1.35	1.35	1.35	1.35	1.35	1.85	1.85	1.45	0.20
0.65	0.90	1.40	1.40	1.40	1.40	1.40	1.90	1.90	1.50	0.21
0.70	0.95	1.45	1.45	1.45	1.45	1.45	1.95	1.95	1.55	0.22

The CAD Library of the Future will have full padstacks built into every land pattern

14 3D COMPONENT OUTLINE

14.1 Component 3D Modeling

Every CAD tool has a different approach to handling 3D Models of component data. Some are much more elaborate than others.

The CAD tool that I use is PADS Layout and I own the IDF translator that is capable of extracting “Closed Polygon” data from the land pattern parts.

The PADS IDF translator has a requirement that the component outline must be a closed polygon and it must be on a layer that does not contain any other graphic features, just the component outline.

So in the PADS tool, we use Layer_25 to construct a closed polygon of the maximum body size of the component outline.

The line width for the component outline should be “Zero Width” but PADS does not have that feature so we use a 1 micron line width.

The Geometry Height of the component is stored in a Part-Type attribute called Geometry.Height.

The unit structure for the Geometry Height attribute is just a number for mil units. It must have “**mm**” following the number if the units are metric and the number must be followed by the **“** sign if the value is in inches.

When you run the IDF program using PADS File/Export, the program has a layer input field that the user enters and the program looks at all the library parts for the existence of a closed polygon on that layer.

If no closed polygon exists, the program will search through all the layers trying to find a closed polygon that is isolated on a layer.

If you do not have a closed polygon on an isolated layer with no other graphics, the program automatically draws a rectangular outline around the outside perimeter of the part extents and uses that shape to portray the 3D Model.

The IDF program produces two files, .emn and .emp which are imported directly into PRO-E for 3D Model illustration. SolidWorks has a translator that can be used to import the same data in their CAD tool.

The CAD Library of the Future will have 3D Model attributes built into every land pattern to use as a mechanical drafting aid for the reduction of errors in product packaging.

14.2 Sample 3D Model Using Solidworks

FIGURE 1

ROCABD, SILK SCREEN W/PADS

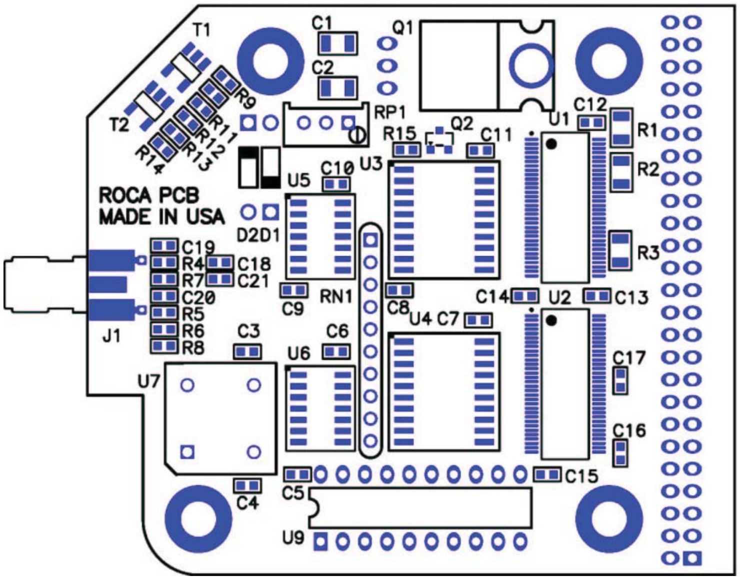


FIGURE 1: PCAD PCB Outline with silkscreen and top layer pads.

The IDF output from PCAD will be used by Circuitworks to define the 3D of the PCB created by Solidworks.

A library of corresponding 3D components to PCB components was previously created in Solidworks.

It is critical that PCB and 3D component definitions match in relation to a reference point, Zero Orientation and Seating Plane.

FIGURE 2

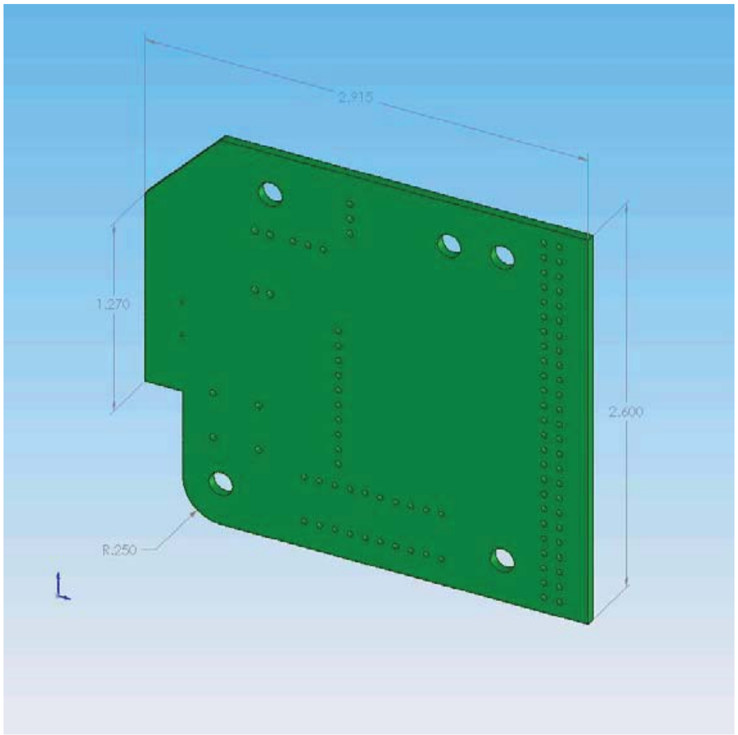


FIGURE 2: Circuitworks translation of IDF file from PCAD layout to 3D definition of PCB with holes.

Special Note: PCAD defines the outer layers of a PCB as the “Top” and “Bottom” Layers. When the IDF translation is finished, the 3D representation of the PCB layers is now defined as “Front” and “Back”, not “Top and “Bottom”.

This is a trimetric view of the bare (unpopulated) PCB. Zero-Zero reference is the lower left hand corner.

FIGURE 3

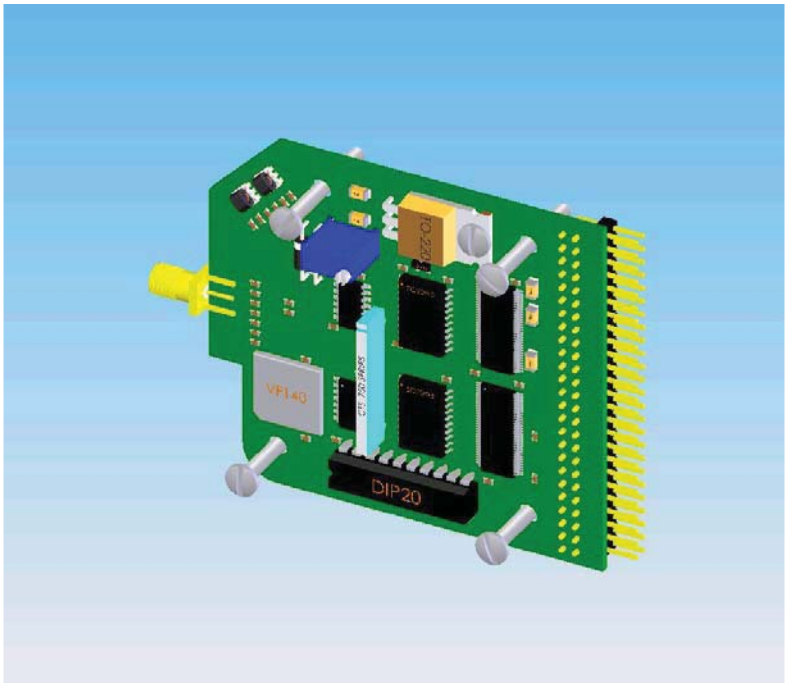


FIGURE 3: 3D definition of PCAD PCB with correct component plane orientation. Front and Back metal lids removed for clarity.

FIGURE 4

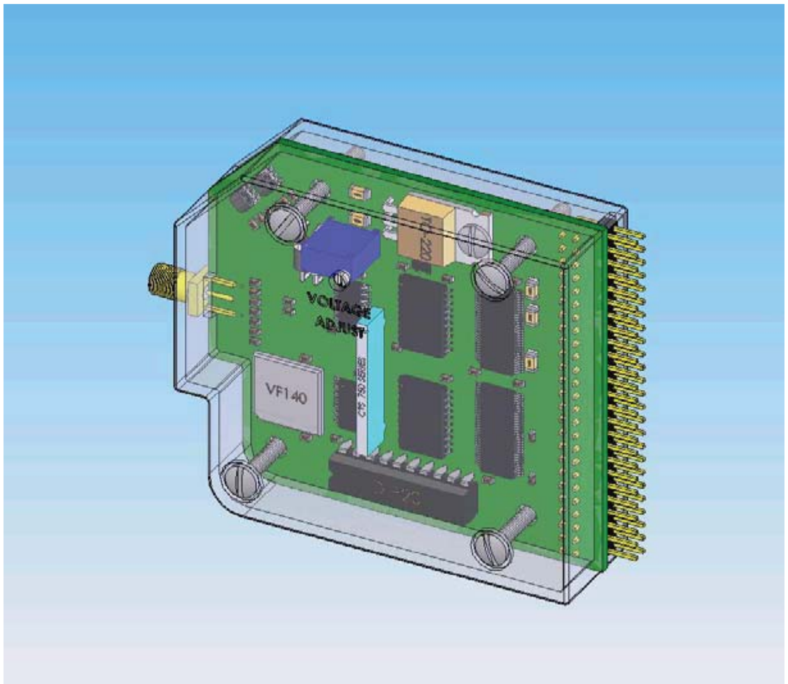


FIGURE 4: 3D definition of PCB with correct component plane orientation.

Front and back metal enclosure made transparent for clarity.

FIGURE 5

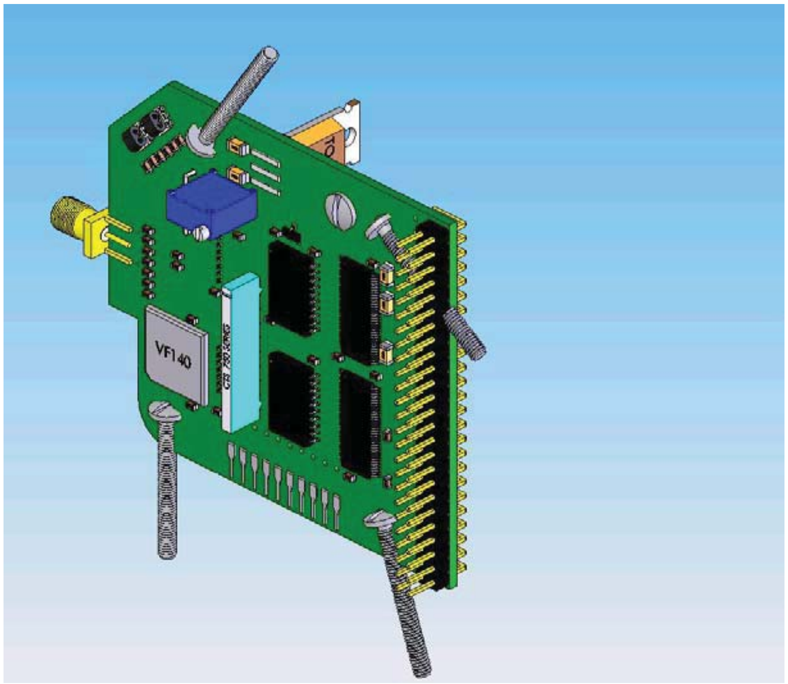


FIGURE 5: 3D definition of PCAD PCB with correct component plane orientation. Front and Back metal lids removed for clarity.

Note the mis-orientation of the following components: TO-220, DIP20, the 50 pin right angle header and the 4-40 X 1” hardware.

These components are oriented using the 2D PCAD definition of “Top” and “Bottom” instead of the 3D definition “Front” and “Back”.

FIGURE 6

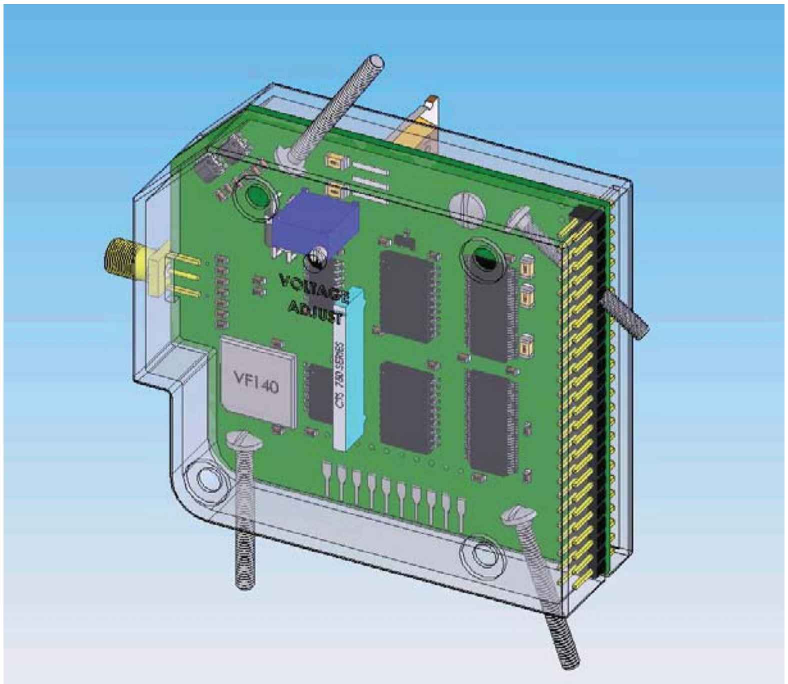


FIGURE 6: Same 3D definition of PCB as in FIGURE 5, but with front and back metal enclosure made transparent for clarity.

FIGURE 7

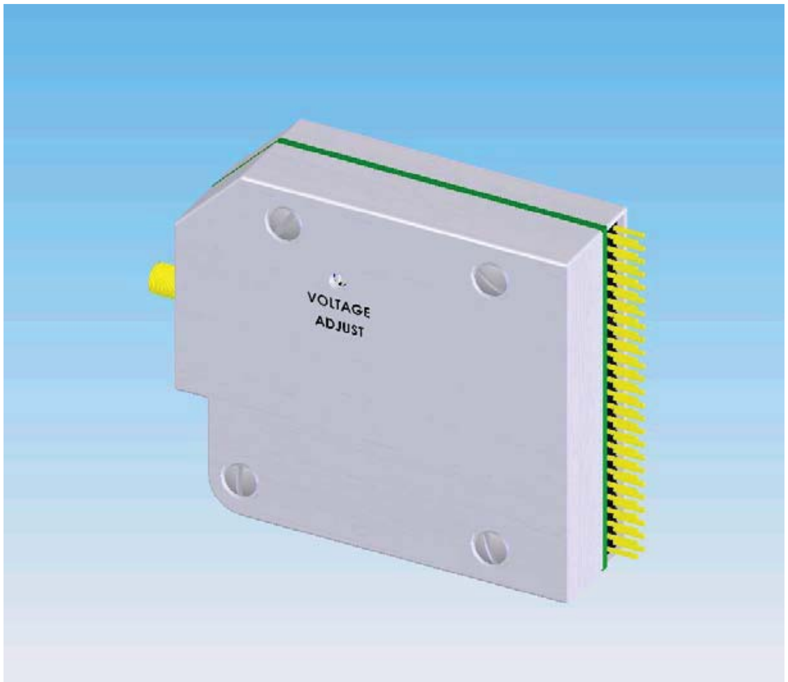


FIGURE 7: 3D of PCB with Front and Back Lids.

FIGURE 8

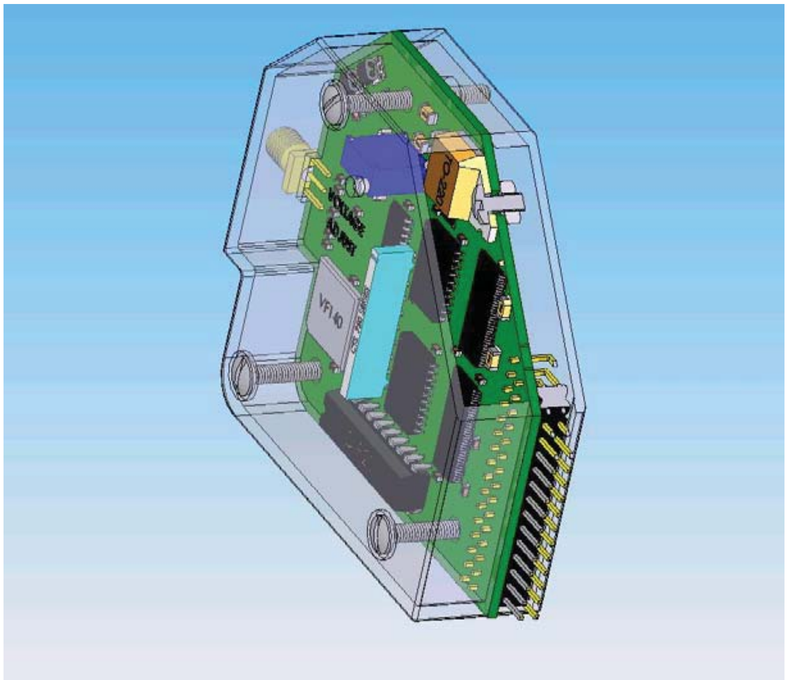


FIGURE 8: Sectional view of PCB shown with right plane angled at -45 degrees along Y axis with transparent metal enclosure.

FIGURE 9

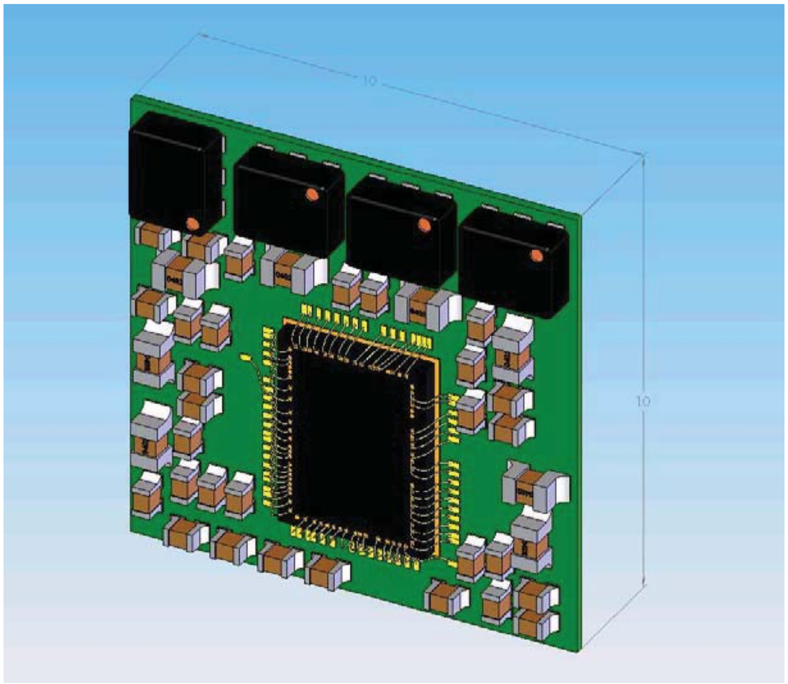


FIGURE 9: Another example of 3D capabilities.

MCM with wire bonds

FIGURE 10

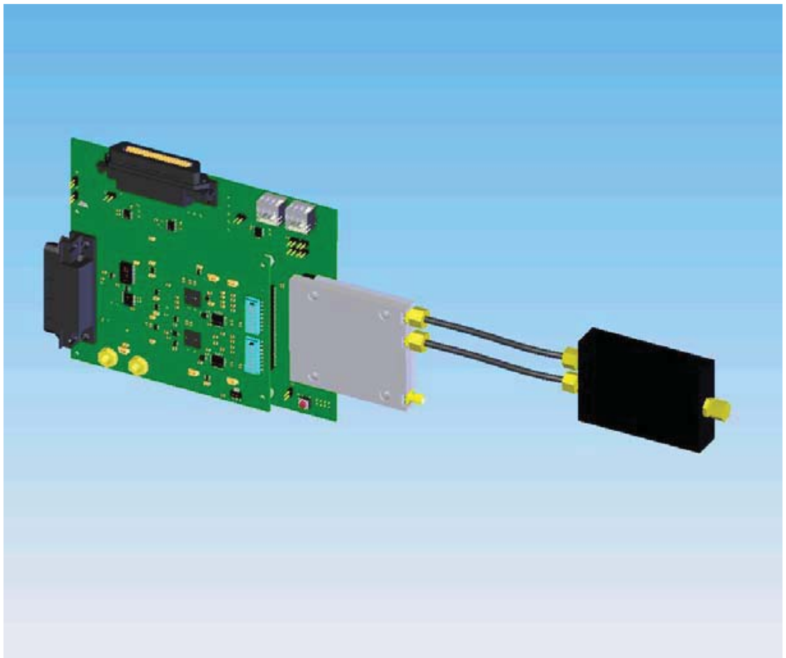


FIGURE 10: In this example, 3 PCB's are mated together showing a completed assembly being cabled over to a Mini-Circuits Hela-10 Amplifier.

15 IPC-7351 3-TIER LIBRARY SYSTEM

15.1 The IPC-7351 3-Tier Construction

The unique aspect regarding IPC-7351 specification is the 3-Tier CAD Library System.

Different electronic products have different requirements for reliability, maintainability and board density.

With the 3-tiered library construction concept, you can generate land patterns to meet those different requirements by varying the pad and courtyard dimensions.

Here are the three different tiers and how and when you should use them:

Three land pattern geometry variations are supplied for each of the device families; maximum land protrusion (Density Level A), median land protrusion (Density Level B) and minimum land protrusion (Density Level C).

Density Level A: Maximum (Most) Land Protrusion – For low-density product applications, the 'maximum' land pattern condition has been developed to accommodate wave or flow solder of leadless chip devices and leaded gull- wing devices. The geometry furnished for these devices, as well as inward and “J”-formed lead contact device families, may provide a wider process window for reflow solder processes as well.

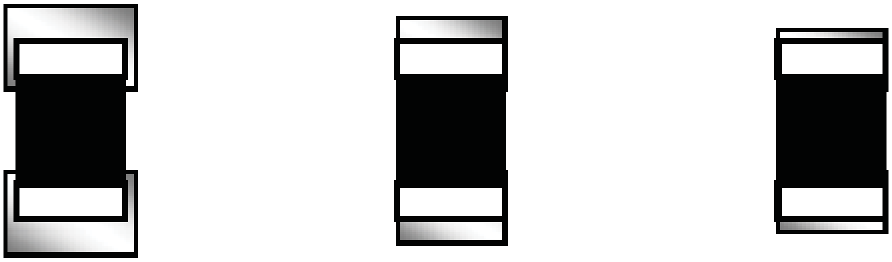
Density Level B: Median (Nominal) Land Protrusion – Products with a moderate level of component density may consider adapting the 'median' land pattern geometry. The median land patterns furnished for all device families will provide a robust solder attachment condition for reflow solder processes and should provide a condition suitable for wave or reflow soldering of leadless chip and leaded gull-wing type devices.

Density Level C: Minimum (Least) Land Protrusion – High component density typical of portable and hand-held product applications may consider the 'minimum' land pattern geometry variation. Selection of the minimum land pattern geometry may not be suitable for all product use categories. The use of classes of performance (1, 2, and 3) is combined with that of component density levels (A, B, and C) in explaining the condition of an electronic assembly. As an example, combining the description as Levels 1A or 3B or 2C, would indicate the different combinations of performance and component density to aid in understanding the environment and the manufacturing requirements of a particular assembly.

The 3-Tier library system affects this list of standard SMT parts:

- BGA
- QFP
- SQFP
- TQFP
- TSQFP
- SOIC
- SOP
- TSOP
- TSSOP
- SON
- QFN
- SOJ
- PLCC
- SOT
- MELF
- LCC
- CFP
- CQFP
- TO
- LGA
- Chip Resistor
- Chip Cap Polarized
- Chip Cap Non-Polarized
- Chip Inductor
- Aluminum Electrolytic Capacitors
- Molded Capacitor Polarize
- Molded Inductor
- Molded Resistor
- Molded Diode
- Wire Wound Inductor
- D-PAK
- CWR06 Capacitors
- TO Packages
- JEDEC Standard Components
- IEC Standard Components
- EIA Standard Components
- Chip Array RES, IND, CAP
- Crystal Oscillators

Land Pattern Variations for Rectangular Two Terminal Devices



The CAD Library of the future will use the 3-Tier construction approach

15.2 IPC-7351 Specification

In addition to the 3-Tier specification, the electronics industry and the IPC-7351 specification will also standardize on the following CAD Land Pattern features:

- Correct pad size that allows for manufacturing tolerances
- Correct pad spacing the allows for accurate solder joints
- Correct Zero Rotation for pick and place machine automation
- A good land pattern naming convention that standardizes the process of building schematic symbols with a link to the correct CAD Land Pattern
- Part Placement Courtyard boundaries
- The correct land pattern origin for pick and place machines
- Silkscreen and exposed copper allowance

16 IPC-2581 NEUTRAL CAD FORMAT

16.1 Electronic Product Hardware Design Automation

True electronic product hardware design automation cannot be achieved until the electronics industry creates and accepts two basic fundamental standards.

1. A guideline specification for all CAD Land Pattern Library creation (**IPC-7351**) mentioned in chapter 15.

2. A neutral CAD format that is universal and can be interpreted (Imported and exported) by every CAD tool and manufacturing tool (**IPC-2581**). In order to fully explain the importance of the IPC-2581, we first must identify the key players in the electronics industry.

16.2 The Electronics Industry

Who and what is the "**Electronics Hardware Industry**"?

It's a combination of the following groups:

- Electronic Engineers
- PCB Designers
- PCB Manufacturers
- PCB Assembly Shops
- CAD Vendors
- CAM Vendors
- Standards Groups
- Component Manufacturers

A standard CAD Land Pattern Library is at the center of electronic product development automation because it has a direct affect with all the above groups.

PCB Design Engineering:

All EE engineers require a standard land pattern name that links with their schematic symbol to automate the process of providing the PCB Designer with accurate data. An engineer that has a good schematic library that is linked to the correct IPC-7351 Land Pattern data, can reduce both the engineering design cycle and the potential error rate.

PCB Design Layout:

All PCB Designers need a CAD Land Pattern Library to perform their job function. The better the CAD Library the better the PCB. It is a fact that a good and complete CAD Library can reduce the PCB Design Layout process by as much as 20%.

PCB Fabrication:

The CAD Land Pattern library has built in features that drive the PCB manufacturing processes. 80% of all manufacturing errors and/or cleanup are directly related to poor CAD Library construction. Some of these items include: inadequate inner layer plane anti-pads (too large or too small), silkscreen outlines that intersect with exposed copper pads, inadequate annular rings on pads and many other items that could be avoided with a good CAD Library.

PCB Assembly:

The CAD Land Pattern library has built in features that drive the PCB assembly process. 80% of all assembly problems occur from errors that are related to poor land pattern construction. Some of these items include: Incorrect hole size for the component lead, incorrect pin pitch for the pad spacing, SMT pads that are too small or too large, poor solder mask allowances, incorrect Zero Rotation for pick and place machines, unknown component origins, non-standard land pattern naming conventions, inadequate placement courtyards that allow for component and manufacturing tolerances and many other things that have a direct affect on the assembly automation process.

PCB CAD Vendors:

The CAD vendors historically have provided CAD Libraries with their tools, however a major consensus has revealed that the majority of all PCB designers do not use the stock vendor CAD library for several reasons. Normally, the CAD vendor cannot keep up with the component industry and their libraries get old and useless. The CAD vendor library does not come with any documentation, so it leaves the PCB designer guessing on which library part to use. The day has come when CAD vendors must make a decision to get out of the CAD library business and refer their customers to existing 3rd party CAD Land Pattern libraries.

The top CAD Vendors are: Mentor Graphics, Cadence, Altium, Zuken and Intercept Technologies.

PCB CAM Vendors:

The CAM vendors are the last quality control front where the CAD Land Pattern library parts are checked for manufacturability. This is where many the CAD Land Pattern library parts errors are discovered and the manufacturing process has to stop and send the error report back to the PCB designer to correct the errors before proceeding the manufacturing process. Unfortunately, most CAM software DRC checks only detect fabrication errors and not assembly errors.

The key CAM Vendors are: Valor, CAM350, GerbTool, CAMtasia, Lavenir, Infinite Graphics and GC CAM

Standards Organizations:

The Standards Groups are responsible for producing guidelines and specifications for proper CAD Land Pattern construction. Unfortunately, they cannot keep pace with the rapidly expanding growth of the electronic component industry. So the only alternative for the standards groups is to create the two items mentioned above to aid with the process of standardization of the creation of a one world standard CAD Land Pattern library.

The key Standards Organizations involved with the creation of a “One World CAD Library” are: IPC, IEC, JEDEC and NIST

Component Manufacturers:

The Component manufacturers have the option of using predefined standard component package data, but often ignore the standards for several reasons. The primary reason to create a unique package that requires a unique Land Pattern is so the customer who purchases the components is forced to use that specific vendor's device and cannot substitute the device with alternative price competitive devices. Also, the reality of the burden of providing CAD Land Patterns should fall on the component manufacturers. The component manufacturer should provide the component dimensional data, the land pattern library part (in a neutral CAD data format) and the land pattern dimensional data to their customers.

The American component manufacturers belong to the organization called NEMI. The Asian component manufacturers belong to the organization called JEITA.

16.3 IPC-2581 Neutral CAD Database Format

A neutral CAD database format has always been a known fact to support electronic product design and development, failure to create and accept a neutral CAD database format has stifled the automation process. The IPC-2581 neutral CAD database format will fulfill a 30 year search for a universal acceptable format. This one single aspect can greatly accelerate the process of all electronic product development because it is the common language between all machines: The CAD system, the fabrication equipment and the assembly equipment. The IPC-2581 also provides the component manufacturers a mechanism to build their own CAD land patterns using a single intelligent format that can be imported into every CAD tool. This will eliminate millions of man hours spent on CAD Land Pattern Library creation. Used in conjunction with the IPC-7351 land pattern guideline specification, all CAD Land Pattern parts can be created using the same identical universal standard.

The IPC-7351 and the IPC-2581 are the key components that will ultimately standardize The CAD Library of the Future and once and for all put an end to the chaos that has stifled electronic product development automation.

It is important to note the key contributors to the development of the IPC-7351 and IPC-2581 standards. The group of representatives is called the IPC 2-17 subcommittee and it consists of the 16 following corporations:

- Celestica
- Sanmina-SCI
- Teradyne
- Lockheed Martin
- Valor
- Lucent Technologies
- Agilent Technologies
- Solectron
- Toppan
- Ohio Design
- Router Solutions
- PCB Libraries, Inc.
- Mentor Graphics
- Cadence
- IPC
- NIST

17 TRANSITIONING TO THE METRIC SYSTEM

17.1 Metrication of the PCB Design Industry

The United States is now the only industrialized country in the world that does not use the metric system as its predominant system of measurement.

Congress, recognizing the necessity of the United States' conformance with international standards for trade, included new encouragement for U.S. industrial metrication in the **Omnibus Trade and Competitiveness Act of 1988**. This legislation amended the Metric Conversion Act of 1975 and designates the metric system as the preferred system of weights and measures for United States trade and commerce. The legislation states that the Federal Government has a responsibility to assist industry, especially small business, as it voluntarily converts to the metric system of measurement.

The current effort toward national metrication is based on the conclusion that industrial and commercial productivity, mathematics and science education, and the competitiveness of American products and services in world markets, will be enhanced by completing the change to the metric system of units. Failure to complete the change will increasingly handicap the Nation's industry and economy.

Companies sometimes ask whether they must convert to the metric system of measurement. The simple answer is no— the law does not require conversion and the government cannot force businesses to convert. Competitors (especially overseas competitors) might even prefer that U.S. companies not convert. Finally, some workers may be relieved to hear they do not need to learn a new system, and companies may wish to postpone transition expenses (although the competitive reality is that postponement will be very temporary and subsequent costs may be higher).

A better answer is yes—yes to a conscious and strategic decision to convert. Companies that delay conversion will lose some of the future economic benefits that will ultimately surpass any short-term costs. Companies should convert if they make or sell any product or service that they or anyone else might want to sell in foreign markets, if they want to be assured of being able to sell to the government in the future, and if they want to begin to enjoy a long-term return on their investment in the transition. In short, companies should actively plan and manage their transition, and not wait for circumstances that will force it. By then, it may be too late for some firms to survive in the increasingly competitive business climate.

Clearly, U.S. companies that do not produce products or services to metric specifications will risk being increasingly noncompetitive in world markets. Japan has identified the U.S. lack of metric usage as a strategic impediment to access of U.S. products to the Japanese home market. In addition, consolidation of the European market product standards will make sales of non-metric products increasingly difficult and uncertain. Most U.S. companies understand that using metric units is essential to future economic success. Their hesitation may be due to uncertainty as to when and how to convert.

Through their actions, federal agencies are demonstrating an increasing determination to use the metric system of units in business-related activities. The results are not yet very visible to the public, which is not a direct target of current federal transition activities. Industry is the target, and is becoming increasingly aware of and generally welcomes the government's progress.

Industry acceptance of the wisdom of proceeding with the metric transition is due partly to the realization that producing to metric specifications and surviving in tomorrow's economic environment are synonymous. Industry also understands that government agencies are committed to working cooperatively with industry.

All the World Standard Groups involved in the electronics industry (IPC, IEC, NIST, JEDEC, EIAJ & JEITA) have made the transition to the metric measurement system. They formed an alliance to stop using English units and all the data they publish is in metric units. The “CAD Library of the Future” will be in metric units.

18 CONCLUSION

IPC, in conjunction with IEC and the world electronics industry standards groups, are in the process of establishing the IPC-7351 standard for CAD Land Pattern specifications.
The IPC-7351 specification introduces the following standards for CAD Libraries:

1. A strict Land Pattern Naming Convention which will help the standardization of electronic schematic symbols for engineering.
2. Zero Component Rotation so that all CAD Land Patterns are built with the same rotation for the purpose of assembly machine automation.
3. 3-Tier specification that supports various levels of product complexity. The 3-Tier CAD library system supports the following:
    a. Least Environment Land Pattern for miniature devices where the land pattern has the least amount of solder pattern to achieve the highest component packing density.
    b. Nominal Environment Land Pattern for normal everyday consumer devices. The solder pattern is average size.
    c. Most Environment Land Pattern for high shock, high vibration or life support systems. The solder pattern is robust and can be easily reworked.
4. Placement Courtyard has been redefined to accommodate the 3-Tier specification.
5. Silkscreen and polarity marking sizes, copper to ink clearances and locations have been clearly defined.
6. Land Pattern origins to aid pick and place machine automation has been defined.
7. Mathematical algorithms to determine pad sizes and spacing have been defined for the 3-Tier environment. These algorithms account for fabrication and assembly tolerances and component tolerances to calculate a precise land pattern.
8. 3D Modeling for mechanical verification using maximum component outlines and maximum component height has been defined.

The IPC-7351 defines all the properties necessary for standardization and acceptability of a “One World CAD Library”. The main objective in defining a one world CAD library is to achieve the highest level of “Electronic Product Development Automation”.

On the other hand, not incorporating a standard CAD library specification will only prevent the highest level of “Electronic Product Development Automation” from happening.

Many large firms have spent millions of dollars creating and implementing their own unique standards for their own “Electronic Product Development Automation”. These standards are proprietary to each firm and are not openly shared with the rest of the industry. This has resulted in massive duplication of effort costing our industry millions of man hours in waste and creating industry chaos and global non-standardization.

The IPC-7351 puts an end to “Proprietary Intellectual Property” and introduces a world standard so every electronics firm can benefit from Electronic Product Development Automation.

The IPC-7351 LP Viewer allows the User to view all standard components and land pattern dimensional data. It also has a powerful search engine for quickly locating parts.

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