THE pcb design MAGAZINE

March 2016

an I·Connect007 publication

Strategies to Increase Profit

The Top 10 Ways

Designers Can Increase Profits

by Mark Thompson, pg. 10

The Need for Speed: Strategies for Design Efficiency

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD AUSTRALIA

Years of experience with one EDA tool obviously develops efficiency, whether the tool be high-end feature-packed or basic entry-level. And one becomes accustomed to the intricacies of all the good and bad features of their PCB design tool. However, there comes a time, with the fast development pace of technology, that one should really consider a change for the better to incorporate the latest methodologies. This month, I will look at productivity issues that impede the PCB design process.

The choice of PCB design tools, until now, has been limited to either high-end, enterprise-level solutions that are expensive and have the added cost of an extended learning curve and setup time, or entry-level desktop solutions that are fast to pick up but limited in capability and error-prone. Mentor Graphics' new PADS Professional has addressed this by providing the best of both solutions. Based on proven Xpedition technology, PADS Professional focuses on ease of adoption, ease of use and affordability but is still packed with all the features today's designers need for the most complex designs.

Typically, a high-speed computer-based design takes two or three iterations to develop a working product. However, these days the product life cycle is very short and therefore time-to-market is of the essence. One board iteration can be expensive, depending on your overheads.

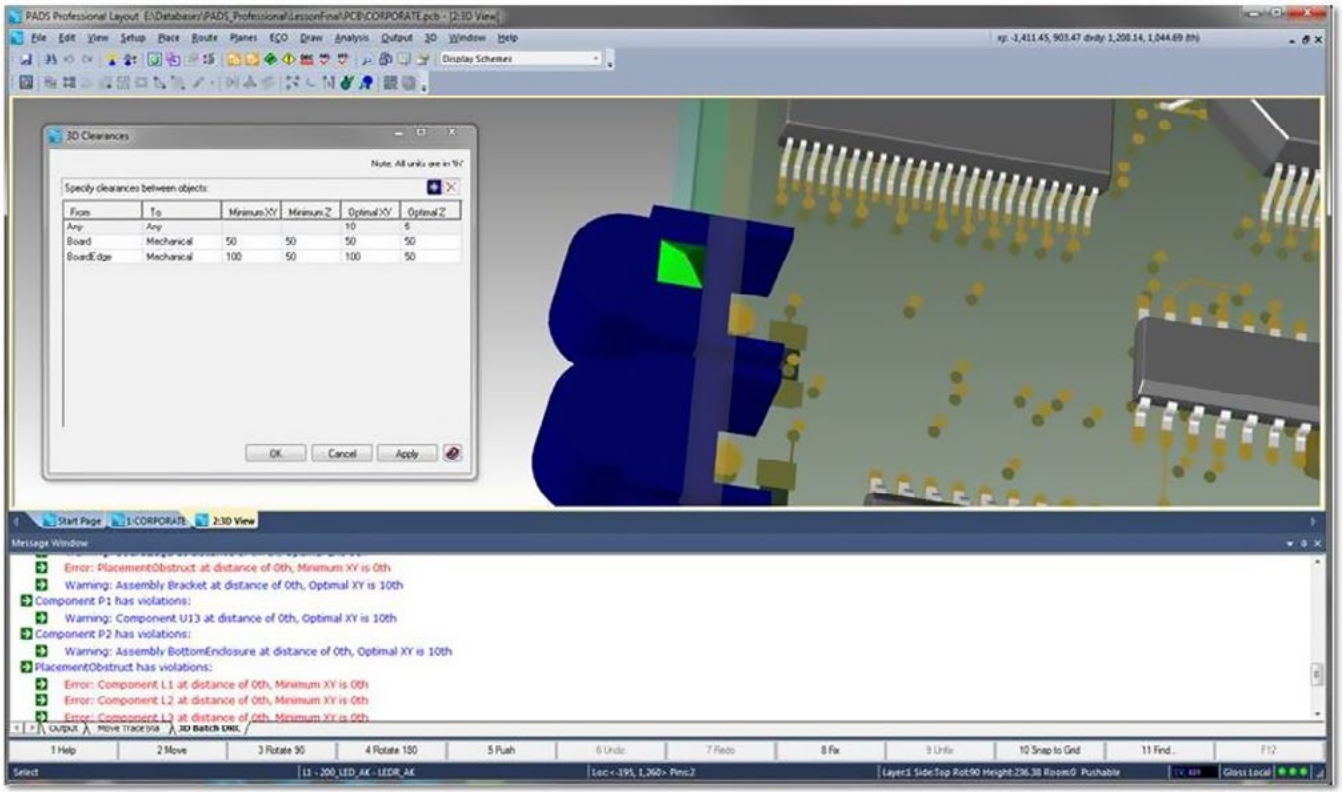


Figure 1: 3D interference validation.

We should not only consider the engineering time but also the cost of delaying the products market launch. This missed opportunity could cost your company hundreds of thousands of dollars, if not the total loss of market share.

In a previous column, Introduction to Board-Level Simulation and the PCB Design Process, I mentioned that the cost of development is dramatically reduced if simulation is employed during the design cycle. The design changes that occur early in the design process are less expensive compared to those that take place after it is introduced into full-scale production. The cost of the change increases with development time.

Fundamentally, the design changes can be classified into pre-production and post-production modifications. The pre-production changes can happen in the conceptual, design, prototype, or the testing stage. The post-production stage change will happen almost immediately when the product is introduced into production or worse still, be recognized only when the product reaches the market. The later the stage, the more expensive the issue is to fix. The advantage of virtual prototyping is that it identifies issues early in the design process so they can be rectified before they become a major problem.

For years, entry-level tools allowed us to quickly design and build a prototype, some of these based on chip vendor reference designs. Unfortunately, those days are long gone and development teams are finding that they need to employ analysis tools to verify their design before release. One cannot rely on reference designs to actually work in the operating environment. These designs are generally built by R&D teams who have high academic qualifications but little appreciation of design for reliability or manufacturability—the real world.

This in-circuit design, find-and-fix methodology is imperative in today's design environment, where multiple fast rise-time signals propagate at faster and faster speeds with the implementation of each new technology. We no

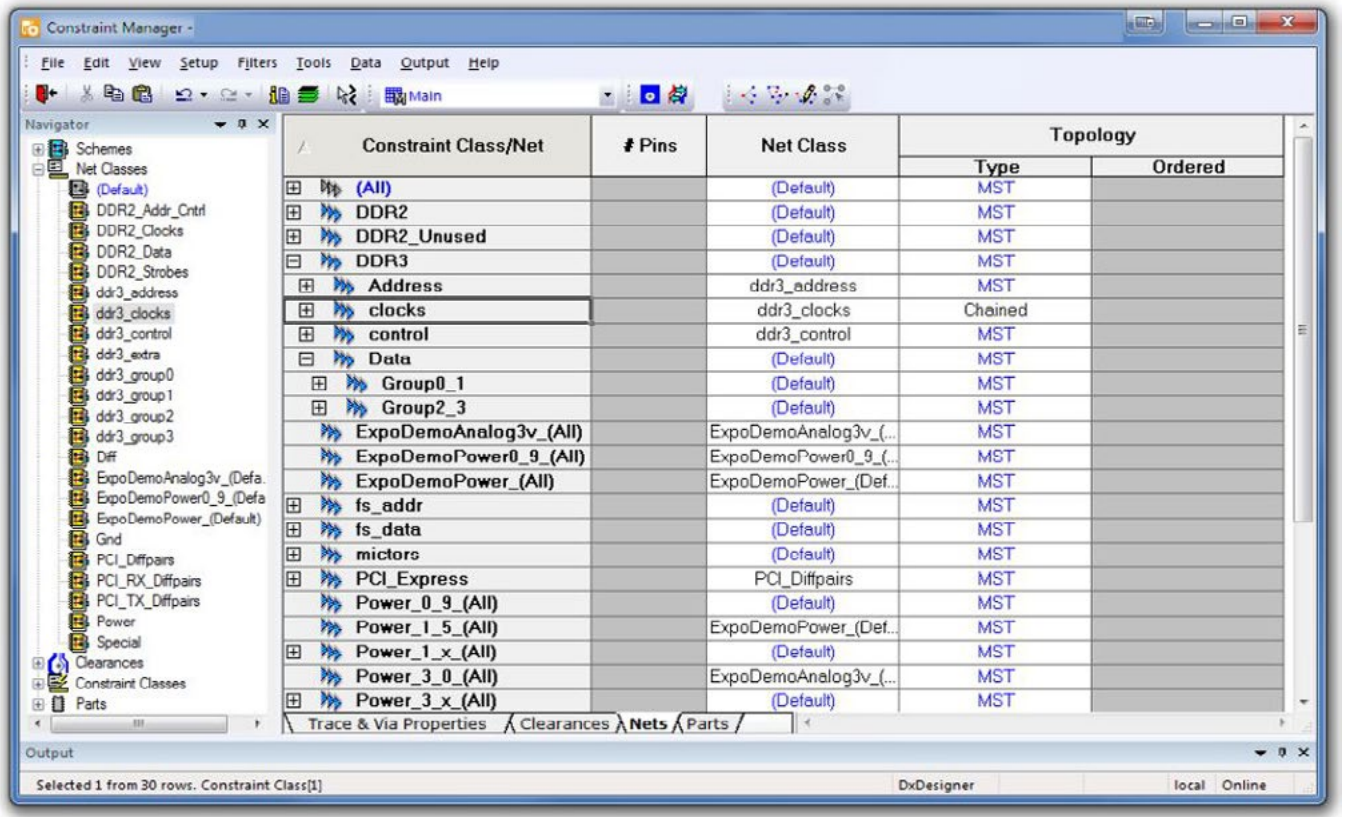


Figure 2: Constraints planning at the schematic level.

longer have the luxury of building a prototype, testing and then revising the approach where necessary. Virtual prototyping, including signal and power integrity, thermal analysis, DFM and 3D interference validation, impart fewer design spins and are essential for design efficiency. 3D interference validation is shown in Figure 1. 3D clearances can be setup then the 3D clearance checking displays violations and automatically zooms in on the selected violation.

Entry-level tools tend to rely on the skills of the engineer and PCB designer to detect possible issues as they arise during the design process. However, these days a more constraint-driven, correct-by-construction approach is required for complex designs. Once the rules are established, they will be followed by downstream tools and validated to conform by the various design rule checkers (DRCs).

Figure 2 illustrates typical constraints planning and definition for a high-speed DDR2 & 3 design. The constraints should be defined at the schematic level and flow through to the layout process. The advantage of this approach is that the engineer can convey his intent, to the PCB designer, without misinterpretation. Alternatively, the independent engineer (the guy who does everything) can manage the constraints, throughout the design process, using the same consistent management tool. Also, the reuse of constraints from a previous proven design not only ensures consistent rules but also minimizes the possibility of errors.

Net classes are used to organize and speed-up the definition of routing constraints for nets with similar properties. For each net class, the layers allowed for routing, the corresponding trace width range for these layers, and the via types allowed can be defined. For differential pairs, a layer-dependent differential pair gap can be defined based on the calculated impedance to ensure uniform impedance across all layers.

Proper grouping and definition of net classes and constraint classes in the early stages of the design process simplifies constraint definition and management significantly. Grouped constraints can increase layout efficiency, reducing design time and, ultimately, lower PCB design costs.

Pre-layout simulation allows the designer to predict and eliminate signal and power integrity, crosstalk and EMC issues early in the design process. This is the most cost-effective way to design a board with fewer iterations, rather than starting with the post-layout simulation. One

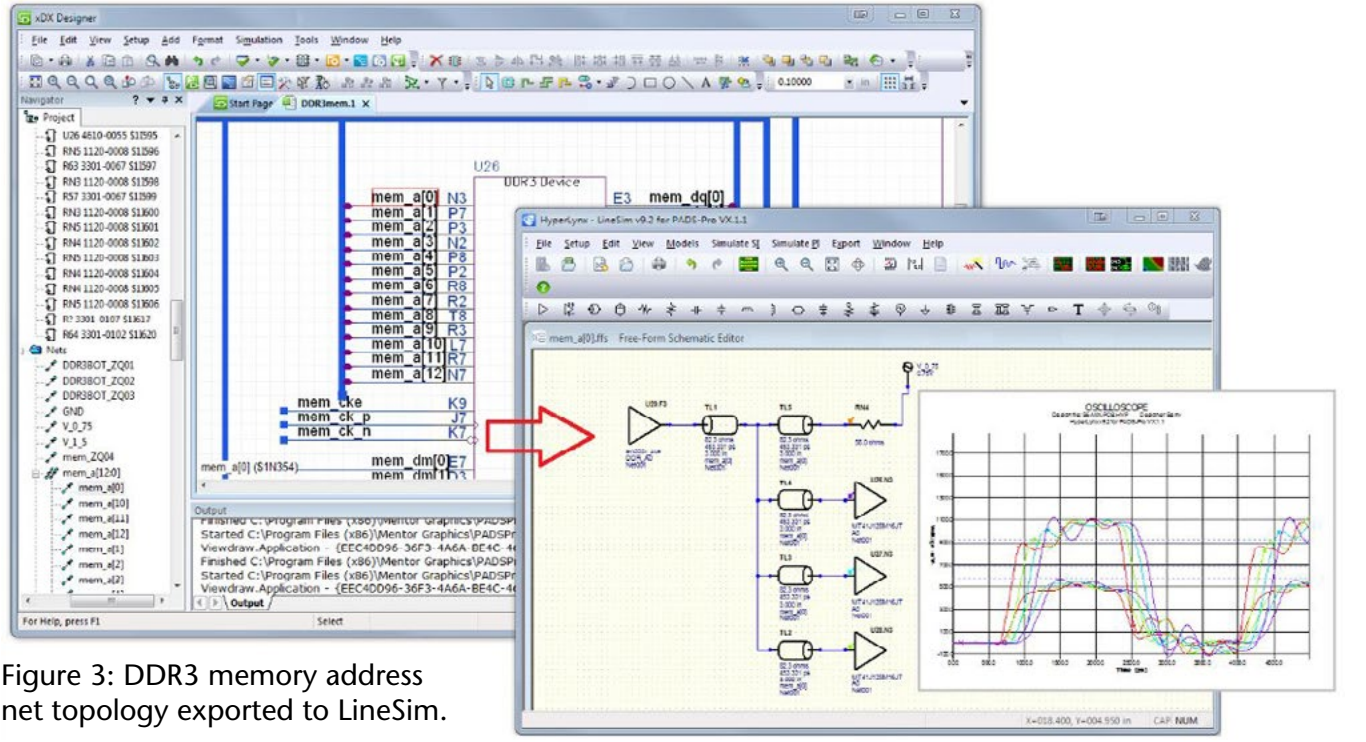


Figure 3: DDR3 memory address net topology exported to LineSim.

can quickly simulate complex interconnect scenarios including ICs, transmission lines, connectors and passive components to identify which scenario is best suited to a particular design.

An integrated correct-by-construction component library also ensures that once a part is defined, the symbol, cell and part mappings will be in sync. This approach eliminates a major cause of design iterations commonly found in netlist driven design paradigms.

Apart from the use of signal and power integrity analysis tools, most designers still rely on eye-balling to pick up many inconsistencies in the layout. HyperLynx DRC, for instance, can verify complex design rules that are not easily simulated, such as EMC constraints. With support for DRCs of such items as traces crossing split planes, reference plane changes, shielding and via checks, one can quickly detect and rectify issues that may later on causes intermittent signal and power integrity issues. The DRCs can also be customized to allow users to create constraints for any check that they may otherwise perform manually eliminating human error.

Today's high-performance processors, with sub-nanosecond switching times, use low DC voltages with high transient currents and high clock frequencies in order to minimize the power consumption and hence heat dissipated. However, fast rise times, low output buffer impedance and the simultaneous switching of busses create high transient currents in the power

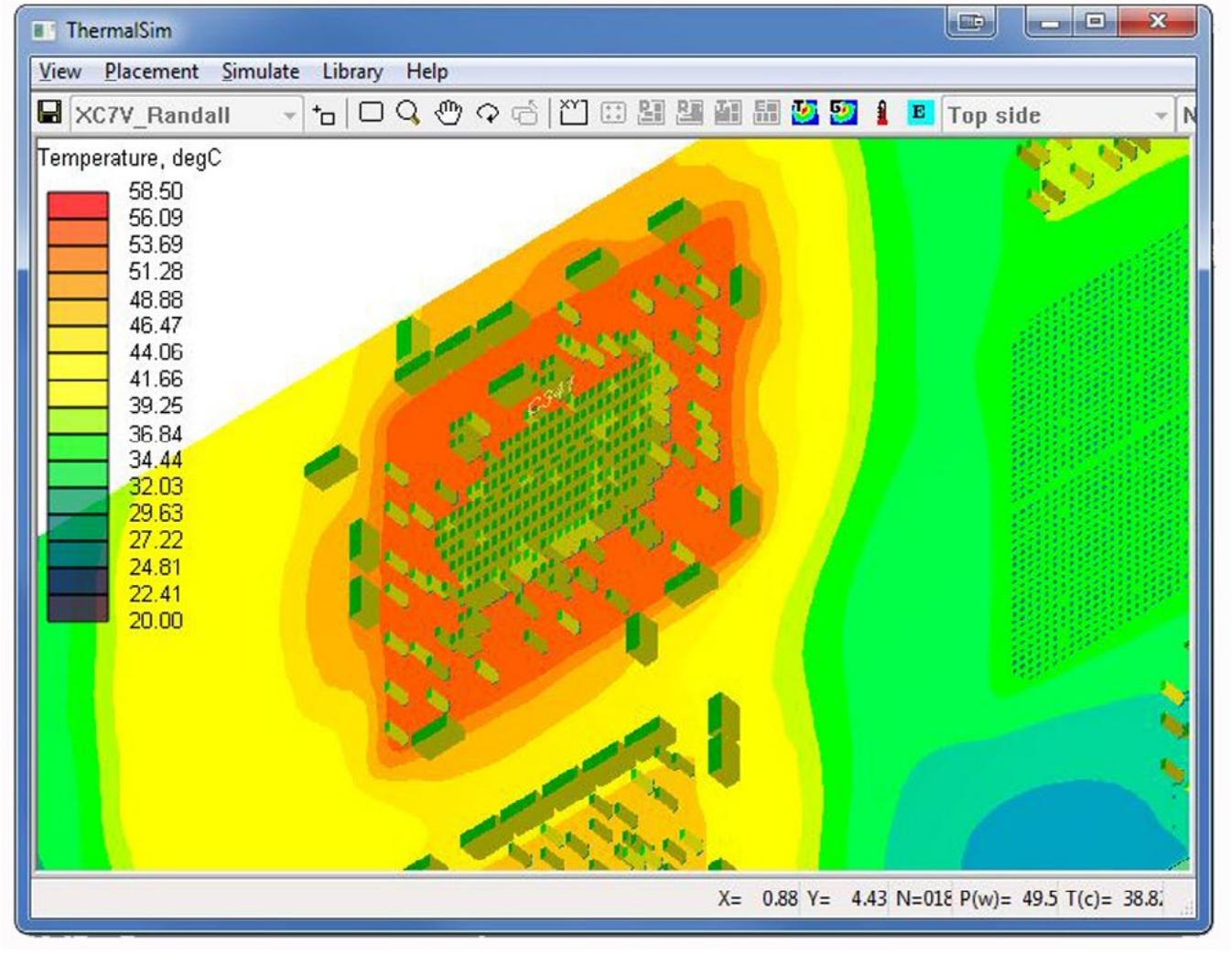


Figure 4: Thermal simulation of hotspots on the bottom of the PCB.

and ground planes. This in turn, degrades the performance and reliability of the product. There is also a high risk of thermal failure in adverse operating environments. Independently from power integrity analysis, thermal analysis can detect hotspots, overheated components and other thermal issues that may degrade the product. Thermal simulation can be run by itself or co-simulated with DC voltage drop. Thermal-only simulation takes into account the heat dissipated from ICs and other components, the environmental air flow and ambient temperature. Thermal/DC drop co-simulation additionally includes the heat produced by current flowing through copper connecting the voltage regulator module (VRM) and DC sink component pin models.

Of course, the use of today's advanced routing technology can provide stunning productivity gains, particularly with the latest high-speed DDR4 memory interfaces requiring your undivided attention to detail. Once set up with constraints defined for all critical signals, routing can be completed and verified in a fraction of the time required using manual techniques.

In conclusion, the use of virtual prototyping including signal and power integrity, thermal analysis, DFM and 3D validation, is now becoming imperative in order to reduce design iterations, meet aggressive schedules and stay ahead of the competition, But, what about the cost? One could choose an enterprise solution that would undoubtedly do the job, or you could consider an affordable bundle of tools that are comparatively priced to desktop solutions, yet provide all the necessary tools required for the most demanding design. Is it time to look at more efficient alternatives?

Points to Remember:

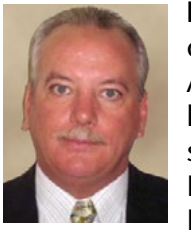
- The choice of PCB design tools, until now, has been limited to high-end, enterprise-level solutions or entry-level desktop solutions.
- A typical a high-speed computer based design takes two or three iterations to develop a working product, costing engineering time and delaying time-to-market.
- The design changes that occur early in the design process are less expensive when compared to those that take place after it is introduced into full scale production.
- Development teams are finding that they need to employ analysis tools to verify their design before release.
- Virtual prototyping, including signal and power integrity, thermal analysis, DFM and 3D interference validation, impart fewer design spins and are essential for design efficiency.
- Entry-level tools tend to rely on the skills of the engineer and PCB designer to detect possible issues during the design process. A more constraint-driven, correct by construction approach is required for complex designs.
- The reuse of constraints, from a previous proven design, not only ensures consistent rules but also minimizes the possibility of errors.
- Net classes are used to organize and speed-up the definition of routing constraints for nets with similar properties.
- Designers still rely on eye-balling to pick up many inconsistencies in the layout. However, DRC tools can verify complex design rules that are not easily simulated, such as EMC constraints.
- Independently from power integrity analysis, thermal analysis can detect hotspots, overheated components and other thermal issues that may degrade the product.
- Today's advanced routing technology can provide stunning productivity gains. **PCBDESIGN**

References

1. Barry Olney Beyond Design columns: Introduction to Board Level Simulation and the PCB Design Process, Design for Profit.

2. Steve Hughes, Mentor Graphics PADS Professional documentation, Why Impose Design Constraints?

3. For information about PADS Professional, click here.



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.