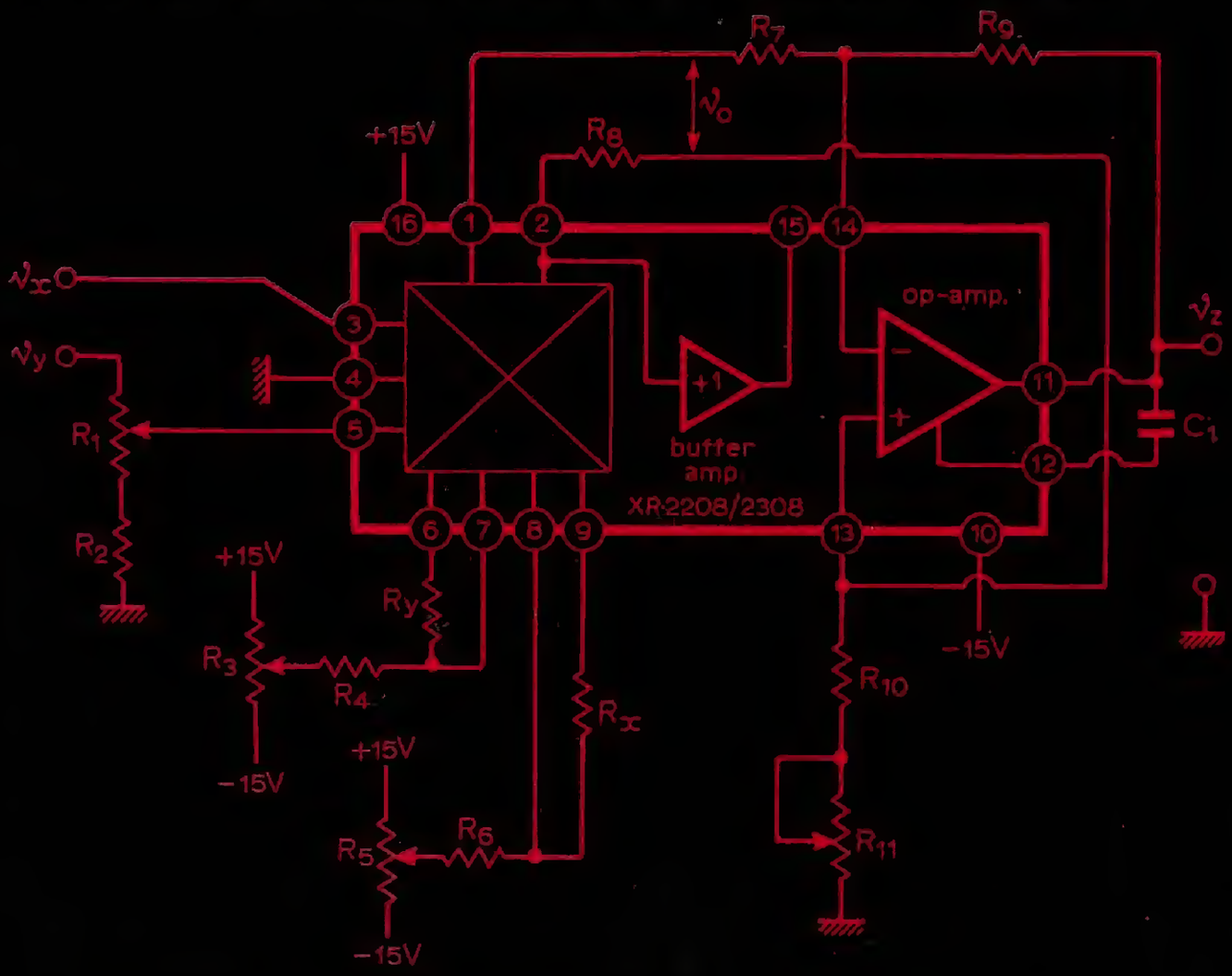
circuit designs

3

Collected Circards

P Williams / J Carruthers / J H Evans / J Kinsler



A WIRELESS WORLD PUBLICATION

circuit designs 3 P Williams / J Carruthers / J H Evans / J Kinsler

THIS BOOK is for those who design, use or understand electronic circuits. It contains the information previously included on sets 21 to 30 of Circards, corrected where necessary, and supplemented with ten pages of new circuits. Introductory articles originally published in Wireless World complement each section.

In October 1972, Wireless World launched a circuit information system called Circards. The system was based on issued sets of 8 × 5in cards suitable for personal filing systems. Published in conjunction with introductory articles in Wireless World, Circards gave the subscriber descriptions of circuit operation, component values and ranges, circuit limitations and modifications, performance data and graphs.

Circuit Designs No.1 and No.2, containing information on Sets 1 to 10 and 11 to 20 respectively, are now out of print. However, sets of cards are still available at £2 per set, supplied post free in plastic wallets.

circuit designs

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Contents

Preface

While writing Circards we have often felt like acting out the parts of latter-day Canutes as the tide of innovations sweeps in. There is the feeling that the tide must be halted long enough at least to learn to swim. The biggest worry in electronics can be to pace the learning process so that new knowledge is both absorbed and applied. Too little reading and study, and the designer is continually forced back on a standard repertoire of solutions; too much and there is no time left to apply that knowledge.

The analogy is appropriate in other ways: new developments come in waves, each building on the ones before. A single technical article or new device can set a whole generation of designers off with fresh momentum, each contributing to that tide. In an age when power is assumed to reside only in organizations it is cheering to note how often the origin of such a sequence of waves can be traced to a few individuals. Just as Blumlein in an earlier age provided new and fundamental innovations such as the Blumlein integrator and the long-tailed pair, so in the i.c. age Bob Widlar changed the whole approach to design by such innovations as the current-mirror and band-gap regulators. Some of the most useful and innovative designs in the last couple of years have come from Barrie Gilbert, whose papers are always a source of ideas (if you are going to steal an idea at least steal a good one). The common feature to such designers is their ability to approach problems in a more open way—a state of mind that says "what happens if . . .?"

This approach is refreshingly present in much published work in recent years. It would have been all too easy as integrated circuits were produced for particular purposes to close the mind to other alternatives or applications. Fortunately the manufacturers are continually forced to broaden the range of applications of each device. From a production standpoint the i.cs have to be as standardized as possible with the fewest possible connections and simplest processing. A good example is the three-terminal voltage regulator aimed initially at on-card regulation in digital systems. No sooner had it appeared than the applications engineers were set to work to show that it could also be used for variable voltage regulation, as a switching regulator, a current limiter and so on.

It is important for each of us to continue that spirit of controlled curiosity. In Circards we have tried to provide an optimum blend of standard and novel circuits. Clearly with readers having a wide range of interests and expertise we will offend some with out naivety, and baffle others with our obtuseness. Our hope is that the circuits will be useful, but that in addition they will include sufficient new ideas to start a few fresh waves. The nearest tide to sweep in on the analogue shore, that of the functional blocks such as multipliers, V-f and d/a converters, presents a superb opportunity for good design and good designers. To mix the metaphor a little, the alternatives are to sit in the deck-chair or start surfing.

We would like to acknowledge the continuing support and encouragement of the Principal and Governors of Paisley College, the help and advice of colleagues; the excellent judgement of *Wireless World* in supporting this project; and the apparently limitless patience of our wives and families. To these last, this book is dedicated with love.

Peter Williams

Set 21 : Voltage-to-frequency converters

You may not find many voltage-to-frequency converter circuits classified as such. They are likely as not to be found under such headings as voltage-controlled oscillators, frequency modulators, astable circuits, and even waveform generators, as the following article—an elementary introduction to their operation—points out. Decisions on which kind to use may often centre on linearity. The closed loop designs generally have better linearity, typically 0.1 to 0.5%, than the simpler open-loop designs, especially the "charge dispensing" kind, discussed in the article (see, for example, page 19). The unijunction type, page 10, also crops up on pages 116 & 130, and a further $\Delta\Sigma$ circuit on page 117.

Voltage-to-frequency converters

Voltage-controlled oscillators—astable multivibrators—waveform generators—frequency modulators: under each of these headings one finds circuits that have an important common property, that the output frequency is a function of some reference or control signal. Such circuits are multi-variable systems in which several parameters of the output waveform are controlled singly or in various combinations by other parameters at the input. Thus the same circuit can appear under different headings depending on which input/output relationship is of priority concern.

As an example, some recent integrated circuits have been designed as waveform generators with square/triangle/sine wave outputs. If the output waveform is of no particular concern, the fact that the frequency of each output is proportional to a direct control voltage assumes a greater importance. The circuit can then be called a voltage-controlled oscillator. Now assume that the control voltage is set to a particular quiescent value with a smaller alternating voltage superimposed. Then the output frequency is modulated by the a.c. input, with the carrier frequency corresponding to the quiescent value of control voltage. The label for this circuit is frequency modulator.

In set 21 of Circards the primary property of interest is the relationship between an input voltage or current and the frequency of the output, with much less importance being attached to the wave shape or amplitude. A particularly desirable property is that the voltage-to-frequency relationship be linear, and in extreme cases departures from linearity of as little as 0.01% may be desired. In the process of achieving this, the output pulse height and width may have to be equally well controlled but these are a means to the end and not an end in themselves. There are other cases where the frequency needs to be varied only over a limited range, demanding only a small linear region to the *V/f* characteristic. A good example is found in the design of v.c.os for high-frequency phase-locked loops. Restriction of the frequency range and of linearity is a compromise accepted more or less willingly in exchange for a speed capability that matches that of the associated digital circuits.

In nearly all of these examples, the basic timing mechanism is that of charging a capacitor from a control voltage or current. The voltage change across the capacitor is sensed by some level-detecting circuit which activates an electronic switch to discharge the capacitor and restart the cycle. Two categories of circuit can be clearly distinguished:

- where the discharge time of the capacitor is made short compared with the shortest charging time and need not be under the control of the input voltage, and
- where both charge and discharge times are controlled in common by the input. The first-mentioned circuits produce sawtooth waveforms across the capacitor and short duration output pulses, while the last-mentioned commonly develops a triangular wave across the capacitor, in association with a square wave at a separate output.

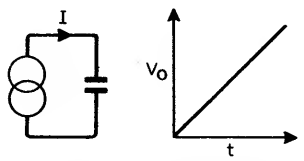

Fig. 1. Constant charging current allows repetition frequency to be made proportional to current.

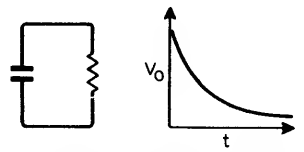

Fig. 2. To cause charging cycle to recommence, a low-value resistor is switched across the capacitor to discharge it quickly.

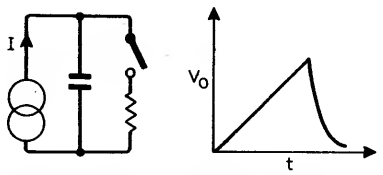

Fig. 3. If discharge time is made small enough the charging current can remain connected. Level of capacitor voltage is used to operate discharge switch.

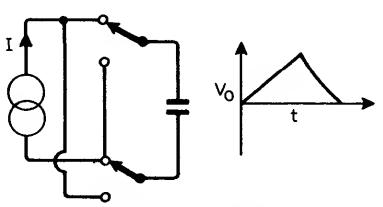

Fig. 4. Triangular waves with repetition frequency proportional to current are produced by reversing capacitor charging current.

These ideas are illustrated in Figs 1 to 4. In Fig. 1, constant current results in a constant rate-of-change of voltage across the capacitor, i.e. the time taken to charge to a given p.d, will be inverse to the charging current. If that level can be sensed and caused to end the cycle or half-cycle, then the repetition frequency (being inverse to the period of the waveform) will be proportional to the current and a linear *I/f* converter results. The simplest way of causing the cycle to recommence is to place a low-value resistor across the capacitor to discharge it in the shortest possible time. If the discharge current is large compared to the charging current, then it is immaterial whether the charging current is disabled or not and Fig. 3 represents the basic principle of many *V/f* converters, with the switch periodically closing at the instant when the p.d. across the capacitor reaches a defined value.

An alternative principle is shown in Fig. 4. The current generator is applied to the capacitor in the reverse direction giving an opposing slope to the ramp but of equal magnitude. The resulting waveform is triangular with the repetition frequency linearly related to the current if the points at which switching is initiated are defined. The provision of a purely electronic two-pole change-over switch is difficult, and the reversal of current direction is more often achieved by using a single-pole switch or its equivalent to control the current generator directly.

A second problem that often arises is that the changing p.d. across the capacitor affects the nominally constant current. This is obvious in terms of the non-linearity of the ramp, but may not affect the linearity of the

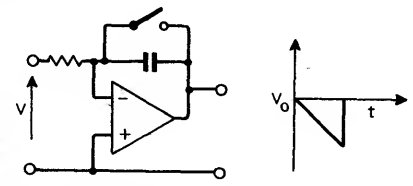

Fig. 5. Using the charging capacitor in an op-amp integrator ensures current is independent of capacitor p.d.

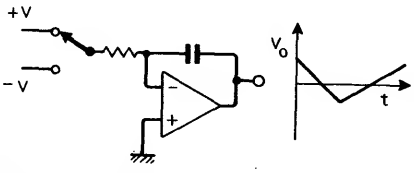

Fig. 6. Simple form of triangular-wave generator uses principle of Fig. 5.

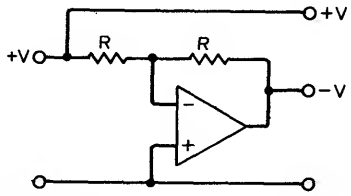

Fig. 7. Circuit provides equal $+V$ and $-V$ inputs for Fig. 6 with an op-amp of -1 gain.

V/f function provided the waveshape is well controlled, e.g. accurate *V/f* conversion is possible with simple *R-C* charge and discharge circuits though the wave shape is highly non-linear. Where waveshape is also of importance, the capacitor forms part of an operational amplifier integrator circuit, with the virtual earth action ensuring that the charging current is independent of the p.d. The discharge element now has no point connected to ground which can raise problems in activating it. (Fig. 5.)

This technique leads to a simple form of triangular-wave generator shown in Fig. 6 where both the $+V$ and $-V$ inputs have to vary together if the slopes are to remain of equal magnitude. By using both the input and the output of an amplifier with a voltage gain of -1 this is readily achieved (Fig. 7). Alternative methods include the design of amplifiers whose voltage gain is switched from $+1$ to -1, and of integrators in which the direction of capacitor current is reversed by a switch while the magnitude is controlled by a single input voltage.

In all of these circuits there remains the problem of the level sensing circuitry that is to determine the instant of switching; both switching speed and accuracy of level are important making the design of a fast, accurate *V/f* converter a difficult one.

The term charge-dispensing is a big one in the literature on precision *V/f* converters. A feedback system is set up in which the output pulses from a generator (basically monostable in form) are arranged to feed back a constant amount of charge for each output pulse. If these units of charge are combined at the input of the system with the control signal, and the overall feedback is negative, then the pulse rate will be proportional to the control signal.

In block-diagram form in Fig. 8, the principle is illustrated by a combination of *V/f* and an *f/V* converter. Assuming that the amplifier gain is high, and that the *f/V* convertor is very linear then the feedback overcomes any non-linearities in the *V/f* converter, i.e. $V_o = V$ to a high accuracy because of the feedback while $V_o \propto f$ ensuring that $f \propto V$ without reference to the linearity of the *V/f* converter. The *f/V* converter might be of the diode-pump variety which with suitable design can transfer a fixed charge into a load for each output pulse rate.

A level-sensing monostable gives an output pulse when the input level rises above a critical value. If the input then falls a second pulse is generated on the next excursion through the set level in the same sense. An important restriction is that the capacitor shall have been completely discharged prior to the second pulse—otherwise the time taken for recharging will be shortened and the output pulse-width reduced. The output of such a monostable would ideally be a train of constant-amplitude constant-width pulses, which could be smoothed and fed back to the input amplifier as in Fig. 9.

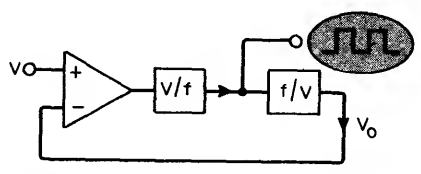

Fig. 8. In this "charge-dispersing" system, a constant amount of charge for each output pulse is fed back so that pulse rate can be proportional to the control signal.

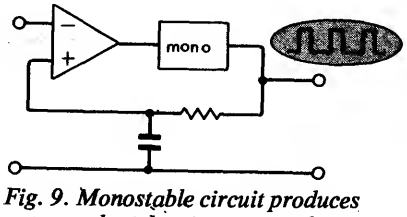

Fig. 9. Monostable circuit produces output pulse when input exceeds a certain level, in either sense.

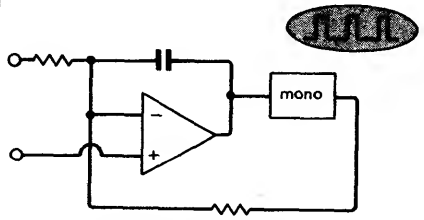

Fig. 10. An alternative arrangement is to dispense charge into a summing integrator. Output pulse rate is a linear function of control voltage or current.

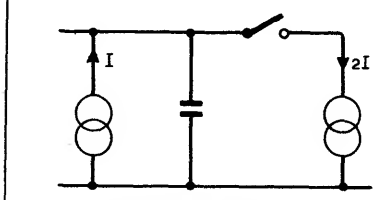

Fig. 11. Technique of using two current sources, but switching only the one having twice the value of the other, is used in some i.cs.

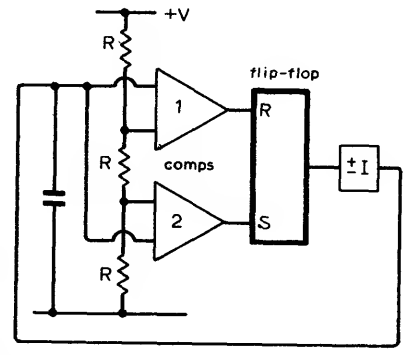

Fig. 12. Triangular wave generator using technique of Fig. 11. Comparator reference inputs are set to 2V/3 and V/3, the capacitor voltage ranging between these limits.

A better arrangement dispenses these units of charge into a summing integrator—Fig. 10. For positive pulses a negative control voltage is required, the integrator output ramping up until a pulse is produced from the monostable. The charge dispensed into the summing junction causes the output of the integrator to fall, again rising slowly under the action of the control current. On average, the net charge inflow has to be zero, the charge dispensed per pulse is constant and hence the pulse-rate is a linear function of the control voltage/current.

Other recent i.cs revert to the separate constant current circuit for timing circuits and waveform generators, and the resulting *I/f* linearity can be accurate enough for many applications. One technique is to have two current sources one set by the external control voltage, the other of opposite polarity but of twice the magnitude—Fig. 11. Keeping the former permanently on and switching the latter on and off makes the net current in the capacitor change from $+I$ to $-I$. A circuit configuration to use this technique to produce a triangular-wave generator is shown in Fig. 12.

Two comparators sense the capacitor voltage, their reference inputs being set to $+V/3$ and $+2V/3$ by an internal potential divider. Assume the current at I; the capacitor charges until its p.d. reaches $+2V/3$. Comparator 1 changes its output and resets the flip-flop. This reverses the direction of current flow until the capacitor discharges to $+V/3$. The comparator 2 operates setting the flip-flop into its original state and restarting the cycle.

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Unijunction voltage-to-frequency converter

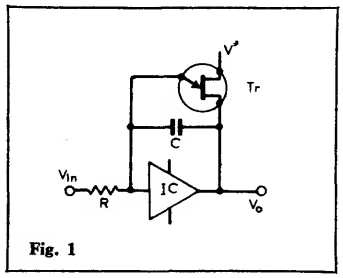


Fig. 1

Components
IC 741, ±15V supplies
Tr 2N2646
C 10nF
R 100kΩ
V′ 3.3V
V_{in} see graph
V_o see graph

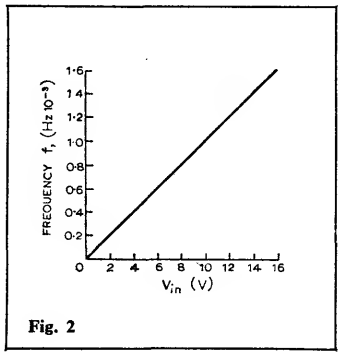


Fig. 2

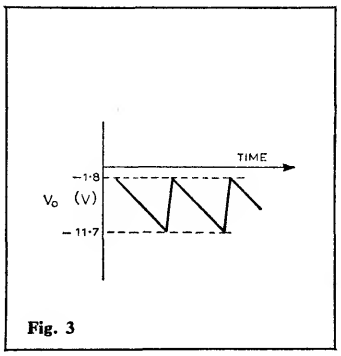


Fig. 3

Circuit description
With the removal of the unijunction transistor the circuit of Fig. 1 is simply an integrator which, with a positive V_{in}, gives a negative-going ramp V_o. If the i.c. gain is sufficiently high then V_o is $-V_{in}t/RC$. The unijunction serves to discharge the capacitor each time the voltage between e and b_1 reaches the unijunction trigger voltage. The circuit therefore goes through the cycle shown right. Upper limit of −1.8V is the voltage at which the unijunction reverts to being an open circuit. Lower limit of −11.7V is arbitrary and is the result of choosing V′, R and C so that V_{in}=10V gave a frequency of 1kHz. With ±15V supplies this obviously cannot be extended beyond 15V.
The degree of linearity in the plot of frequency against V_{in} shown in Fig. 2 is quite high e.g. 10V gave 1kHz, 5V gave 498Hz, 1V gave 96Hz and 0.15V gave 16Hz.
Rise time of the output waveform (Fig. 1 circuit gave the waveform of Fig. 3) corresponding to the time when C is discharging, was 15μs i.e. 1.5% of the period at 1kHz, so the circuit cannot be recommended for much higher frequencies.
But from the expression for the downward ramp it is clear that the same frequency range can be achieved by the use of different values of R and C, and also of V′. It will, of course, be generally desirable to keep R relatively high to give high input impedance.

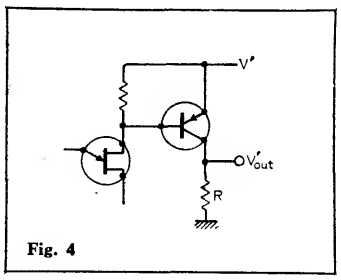
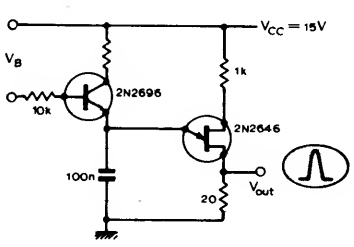


Fig. 4

Circuit modifications
The modification shown in Fig. 4 to the circuitry around the unijunction transistor will provide a pulse train at V'_o, the frequency being the same as that of the main circuit. The leading edge of this pulse train will correspond to the rising edge of V_o shown in Fig. 3. This V'_o will, of course, have the advantage of going much closer to zero in the time between the pulses.
An alternative voltage-to-frequency converter reported by Swarup and Banerjee is shown in Fig. 5. It is basically a unijunction oscillator with constant-current drive to the capacitor, this current being proportional to the voltage V_B.
A linear relationship between V_B and the output frequency is claimed in the range 0 to 500Hz. The basic action of the unijunction oscillator and modifications to reduce the discharge time of C are fully described in Circards set 3 (waveform generators) card 4.

Reference
Swarup & Banerjee, Linear voltage to frequency and voltage to pulse width converters using unijunction transistors. *Int. J. Electronics*, vol. 32, 1972, pp. 377-81.

Fig. 5



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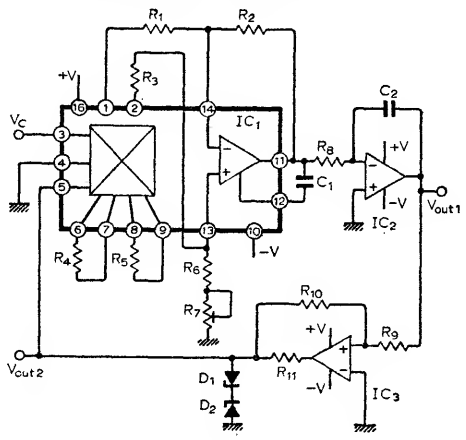
Multiplier voltage-to-frequency converter

Fig. 1



Typical performance
Supplies ±15V, ±8.5mA
IC_1 XR2308 IC_2, IC_3 741
D_1, D_2 3.3V Zeners R_1, R_3 22kΩ
R_2, R_6 330kΩ R_4, R_5 68kΩ
R_7 100kΩ R_8, R_9, R_{10} 10kΩ
R_{11} 2.2kΩ C_1 22pF, C_2 1nF
See Fig. 3 for graph of f/V_c and Fig. 2 for waveforms.

Fig. 2

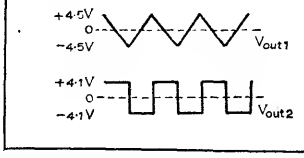


Fig. 3

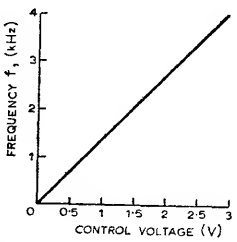


Fig. 4

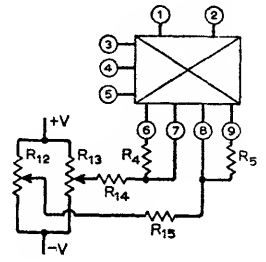
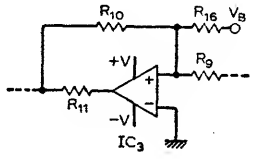


Fig. 5



Circuit description
The circuit of Fig. 1 is basically a closed-loop integrator-comparator square-triangle generator, comprising IC_2 and IC_3, with a multiplier (IC_1) inserted in the loop to provide control of frequency. The value of the output voltage from the multiplier is a scaled version of the product V_{out2} and the control voltage V_C. Thus the amplitude of the signal to be integrated is directly proportional to a scaled value of the control voltage. A positive voltage applied to the inverting integrator charges C_2 with its output end negative relative to the input end (held close to 0V by negative feedback through C_2 and the high gain of IC_2). Thus, V_{out1} goes negative until the current it feeds through R_9 exceeds the positive current in R_{10}, resulting in a negative current to the non-inverting input of the Schmitt comparator. V_{out2} then rapidly switches to a negative value due to positive feedback applied to IC_3, causing the multiplier output to go negative (V_c is always positive). The output from the integrator then starts rising until it reaches a positive voltage sufficient to make the comparator change its state again, returning V_{out2} and the multiplier output to their original positive values. Hence, V_{out1} is a triangular wave and V_{out2} a square wave with frequency linearly dependent on the control voltage

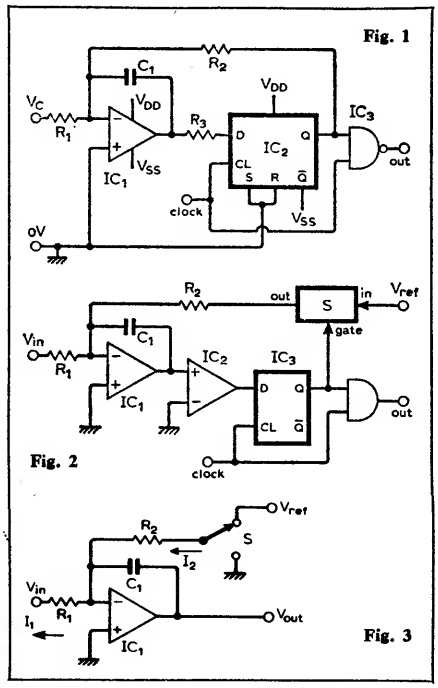
Component changes
Useful range of supplies: ±7 to ±16V.
Increase C_2 to reduce upper frequency limit.
Useful range of V_c is about 0 to +11V.
Changing IC_3 to a 301 type op-amp increases slew-rate capability.
R_9 can have a wide range of values the lower limit being imposed by heavy loading of IC_2 and the upper limit by the failure of IC_3 to switch before it saturates.

Circuit modifications
- Accuracy of frequency control largely depends on the nonlinearity and offset voltages in the multiplier part of the loop. Output offset adjustment is provided by R_7 and independent adjustment of the offset voltages at the multiplier's X and Y inputs (pins 3 and 5) can be obtained by the 25-kΩ potentiometers R_{12}, R_{13} shown in Fig. 4, where R_{14}, R_{15} are 100kΩ.
- For a given value of control voltage frequency depends on the scale factor of the multiplier. Adjusting this allows the output frequency to be made a simple linear function of V_c. The factor can be adjusted in three ways: (1) by adjusting the op-amp gain in the multiplier block by means of R_2, (2) by adjusting the gain of the multiplier block by varying R_4 and R_5, and (3) by connecting the V_{out2} signal to the Y input of the multiplier (pin 5) through a ground-referred potentiometer.
- Asymmetry in the output waveforms due to mismatched Zener diodes can be corrected by applying a bias voltage V_B of suitable polarity to the comparator input via R_{16}, as shown in Fig. 5. Alternatively, this arrangement with $V_B = \pm V$ and $R_{16} = 10k\Omega$ can be used to purposely introduce a d.c. offset into the output waveforms.
- Other methods may be used to limit the amplitude of the output voltage from the comparator, e.g. by using a diode bridge limiter or by replacing IC_3 with an op-amp of the type providing access to the drive point of its output stage, such as a 748. This allows the comparator output to be clamped by zener diodes or suitably-biased transistors connected to the output stage drive point.
- For higher frequency operation the multiplier/op-amp block can be replaced by a separate multiplier (MC1495) and inverting amplifier (LM318), the 741-type integrator replaced by an LM318 integrator and the Schmitt replaced by an LM311.

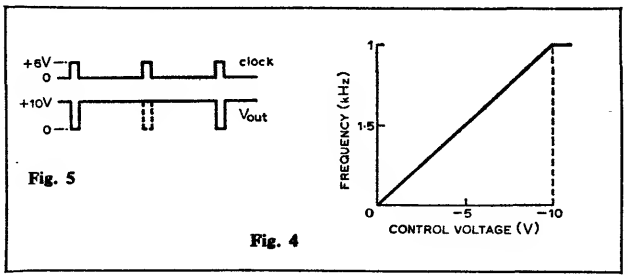
Further reading
Graeme, J. G. Applications of operational amplifiers, McGraw-Hill 1973, pp. 161/2.
Graeme, J. G., Tobey, G. E. & Heulsman, L. P. Operational amplifiers, McGraw-Hill 1971, pp. 237-51.
XR-2208/2308 operational multiplier data sheet, EXAR Integrated Systems Inc. 1972.

Cross references
Set 2, card 1
Set 3, cards 1, 5
Set 13, card 9
Set 17, cards 3, 6
Set 21, card 4

Delta-sigma voltage-to-frequency converter



Typical performance of Fig. 1
IC_1 741, IC_2 $\frac{1}{2}\times$CD4013AE
IC_3 $\frac{1}{4}\times$CD4011AE
Supplies V_{DD} +10V
V_{SS} −10V
R_1, R_2 100kΩ
R_3 1kΩ
C_1 100nF
Clock 6V positive pulses,
p.r.f. 1kHz, duty cycle 10%
See Figs 4 and 5.



Circuit description

A class of voltage-to-frequency converter gives an output in the form of a pulse train where the repetition frequency is directly proportional to the instantaneous value of the control voltage but the pulses are generated asynchronously. The output from a delta-sigma encoder is again a pulse train but its average pulse repetition frequency is proportional to the control voltage and the pulses are generated in synchronism with a clock pulse waveform.

The basic form of a delta-sigma modulator is essentially a voltage-to-pulse ratio converter (Fig. 3). The circuit maintains a constant voltage across C_1 as the input voltage is varied, which requires that the charging current from the voltage reference source to be switched into C_1 at a repetition rate that attempts to keep the net change in voltage across C_1 at zero. Thus the rate at which the reference current must be switched into the capacitor must be proportional to the input voltage. If the reference current is switched under the control of a stable clock-pulse generator the output pulses will be proportional to V_{in} and synchronized with the clock pulse source. Assuming that the net voltage across C_1 is zero, that V_{in} is negative, that V_{ref} is positive and IC_1 is a high-gain op-amp then $I_1=I_2$, V_{out} (mean) $=0$ and I_{out} (mean)$=0$. As the inverting input of IC_1 is a virtual earth, $I_1=V_{in}/R_1$ and $I_2=kV_{ref}/R_2$ where k is pulse duty cycle required to keep $I_2=I_1$. Equating these currents gives

$$\frac{V_{in}}{R_1}=k\frac{V_{ref}}{R_2},$$

where k is the ratio of the output pulse repetition rate (f) to the clock pulse repetition rate (f_c). Hence

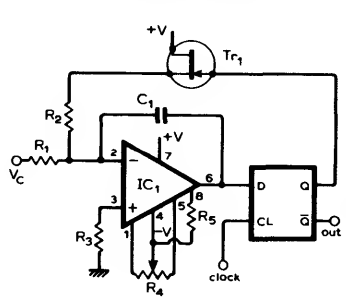
$$f=\left(\frac{R_2 f_c}{R_1 V_{ref}}\right) V_{in}.$$

By making $R_2=R_1$ and $V_{in(max)}=V_{ref}$ the maximum output p.r.f. is that of the clock source and the average output pulse rate is proportionally smaller for smaller values of V_{in}.

The arrangement of Fig. 2 uses an analogue transmission gate to realize the switch S. IC_2 is a precision comparator which determines when the reference voltage source is to be switched to R_2 by monitoring the polarity of the output from the integrator IC_1. This switching action is synchronized to the clock pulses by using gating pulses derived from the output of a D-type flip-flop which receives the comparator's output at its data input.

The circuit of Fig. 1 is that to which the typical performance data refers. This is a simplified form of the arrangement previously discussed with the electronic switch, separate reference source and precision comparator removed. (Note that whilst the integrator used both positive and negative supplies the D-type flip-flop is connected only across the positive supply.) As the D-type produces output pulses equal in amplitude to the V_{DD} rail voltage only when its data input receives a positive pulse from the integrator, a separate switched reference is not essential. Also, the precision comparator can be replaced by R_3 which limits the negative-going pulses to the data input of the D-type which acts as the comparator. Average frequency/V_c graph (Fig. 4) has a linearity of ±0.1% up to $f=f_c$ when $V_c=V_{DD}$. No further increase in frequency is possible except by increasing the p.r.f. of the clock source. Output pulse waveform of Fig. 5, inverted by IC_3, is of $V_c=V_{DD}/2$, the dashed pulse only being present when V_c is raised to V_{DD}.

The circuit of Fig. 6 is another simplified form of the more general system where the comparator had been omitted and the electronic switch is realized by a junction f.e.t. The positive supply rail is used as the voltage reference source and the output is taken from the $\bar{Q}$ terminal of the D-type flip-flop IC_2, which is a complementary m.o.s. version to conserve power. This circuit is capable of linear v-to-f conversion within ±0.05% almost independently of temperature changes. Typical values are:
V ±2.7V
IC_1 LM4250C
IC_2 $\frac{1}{2}\times$MC14013CL
R_1, R_2, R_3, R_4 100kΩ
R_5 5.6MΩ, C_1 100nF
Tr_1 2N4396



Further reading

Defreitas, R.Low-cost way to send digital data, *Electronics Design*, pp. 68-73, Jan. 18. 1974

Ross, P. J. Simple accurate voltage to frequency converter. *Jnl. of Physics E*, vol. 7, pp. 706/7.

Alusten, B. Calculate with a v-f converter, *Electronics Design*, June 7, 1974, pp. 130-2.

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Set 21: V to f converters—4

Sinewave voltage-to-frequency converters

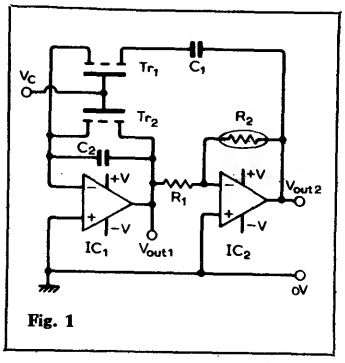


Fig. 1

Typical performance
Supplies ±15V
IC_1, IC_2 741
Tr_1, Tr_2 1/6×CD4007AE
R_1 150Ω
R_2 thermistor type R13
C_1, C_2 100nF
V_{out1} 520mV pk-pk
V_{out2} 1.04V pk-pk
See graph for f/V_c (Fig. 2)

Circuit description
This circuit (Fig. 1) is one of the many forms of Wien bridge oscillators with Tr_1 and C_1 forming the series-connected frequency-dependent arm with Tr_2 and C_2 forming the parallel connected arm of the bridge. For oscillation to occur the closed-loop gain must be unity, the required amount of gain being provided by the inverting operational amplifier IC_2, the gain being determined by the ratio R_2/R_1. With this configuration the common-points of the frequency-determining resistors are connected to the virtual-earth inverting input of IC_1. This is a convenient arrangement for replacing these resistors with elements which have a resistance that can be controlled by a ground-referred voltage source. In the above circuit these elements take the form of a pair of matched c.m.o.s. transistors which have gate-source resistances that depend on the control voltage V_c. Linearity of the voltage-to-frequency conversion characteristic is not particularly good over a wide range of frequencies but may be adequate for many purposes where only a restricted frequency range is required. Resistance of the f.e.ts depends on their drain-source signal voltages as well as on the control voltage V_c but this can be reduced, and the linearity of f.e.t. resistance-to-control voltage characteristic linearized, by using local feedback around the f.e.ts as shown in Fig. 3, where R_3, R_4, R_5 and R_6 may be of the order of 1MΩ.

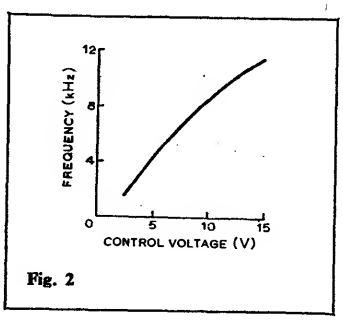


Fig. 2

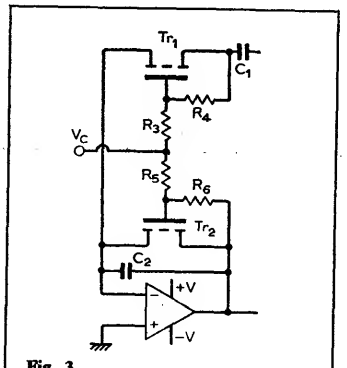


Fig. 3

If the closed-loop gain deviates from unity the amplitude of oscillation will vary with time, so to avoid extremely precise setting of gain it is initially set slightly high and then automatically controlled the a.g.c. being achieved with a thermistor in the above circuit. In addition to the use of local feedback on the f.e.ts, these elements could be connected to form only part of the frequency-determining resistances with bulk of the values in the form of series-connected resistors which would tend to swamp out the non-linearities in the f.e.t. whilst restricting the range of control.
The f.e.ts could be replaced by matched photoconductive resistors or by bipolar transistors which are switched on and off by current pulses to the bases, the mean collector-emitter resistance being controlled by the pulse repetition frequency.
A voltage-to-frequency converter using a pair of all-pass active networks is shown in Fig. 4. These networks, using A_1 and A_2, have a constant gain magnitude but a phase shift given by $\phi_1 = -2\tan^{-1}(\omega CR_1) - 180°$ and $\phi_2 = -2\tan^{-1}(\omega CR_2) - 180°$ respectively. With the 180° phase shift through the a.g.c. amplifier A_3 the circuit will oscillate at a frequency $1/(2\pi C\sqrt{R_1R_2})$Hz, which shows that a voltage-to-frequency conversion may be obtained by making R_1 or R_2 or both voltage-dependent resistors, e.g. f.e.ts. For a wide range of frequency variations R_1 could be a voltage-dependent resistor and R_2 a range-switching resistor. For $R = R_1 = R_2$ the outputs are generated with a controllable phase difference $\phi = (\phi_1 - \phi_2) = -2\tan^1(\omega CR)$.
Circuit of Fig. 5 uses two active integrators and two multipliers to produce a voltage-to-frequency converter having quadrature outputs that can have a very fast response to changes in V_c provided a fast a.g.c. system is added to the basic circuit. Under this condition the circuit will oscillate at a frequency which allows the double integration to take place without changing the amplitude of the signal. Multiplier M_2 provides an output $V_2 = +V_c.V_{out1}/10$ and M_1 gives an inverted output, to maintain the loop phase shift, of $V_1 = -V_c.V_{out2}/10$. With the 1/10 scaling factor, frequency of oscillation is $V_c/20\pi RC$. Multiplier M_1 could be replaced by an inverting operational amplifier.

Fig. 4

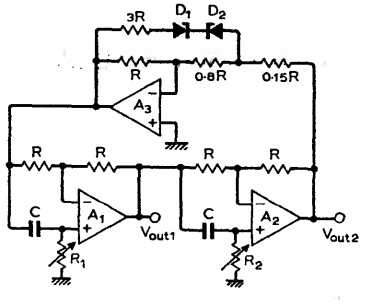
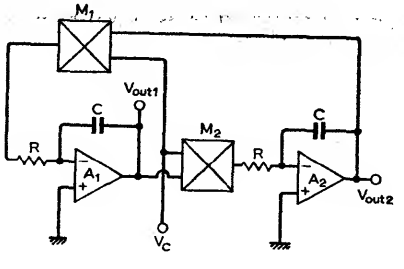


Fig. 5



Further reading
Von Ow, H. P., Reducing distortion in controlled attenuators using FETS. *Proc. IEEE*, 1968, pp. 1718/9.

Multiphase voltage-to-frequency converter

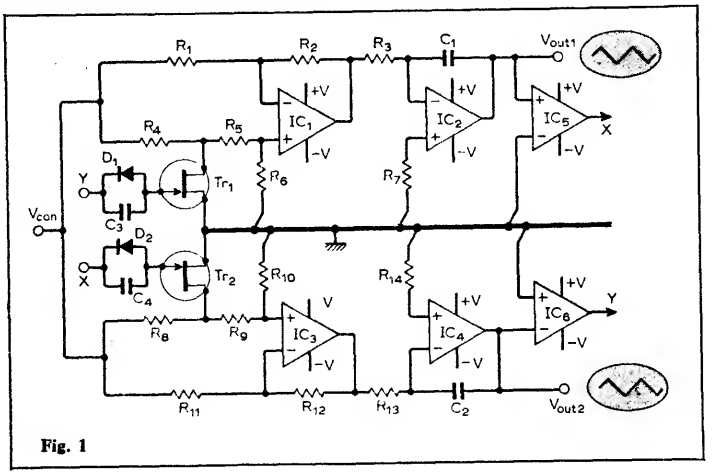


Fig. 1

Typical data
IC_1 to IC_6 74IC
Tr_1, Tr_2 2N5457
R_1, R_{11} 20kΩ
R_2, R_3, R_{12}, R_{13}, R_6, R_7, R_{10}, R_{14} 10kΩ
R_4, R_5, R_8, R_9 2.7kΩ
C_1, C_2 47nF
C_3, C_4 68pF
D_1, D_2 1N914

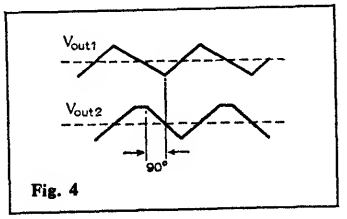


Fig. 4

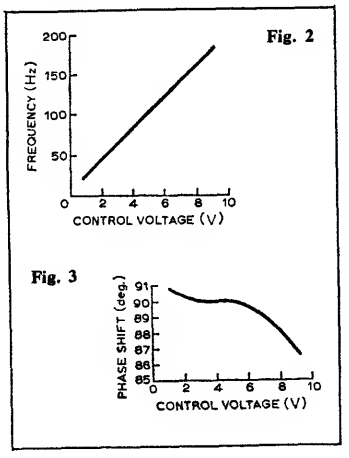
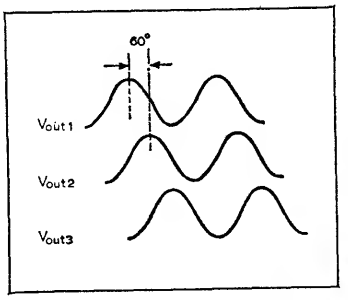


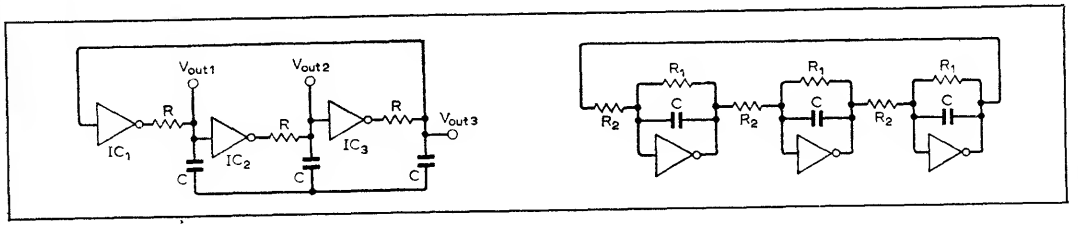
Fig. 2

Fig. 3



Circuit description
This is a twin circuit based on R-C integration to provide the triangular waveform and level sensing to provide a square wave which operates an electronic switch controlling polarity applied to the integrator. Outputs X and Y are cross-connected giving control of electronic switches Tr_2 and Tr_1 respectively and triangular waveforms which are 90° out of phase. IC_5 and IC_6 provide high open-loop gain, and at low frequencies provide faster switching than comparators. V_{out1} is a positive-going ramp until Tr_1 changes state and this occurs at the instant of zero-crossing of V_{out2}, which then switches IC_6. V_{out1} then ramps down and changes the state of Tr_2 when a zero-crossing point is reached. The time taken to go from say a positive peak to zero level depends on the RC time constant and the value of $V_{control}$. It should be noted that as no amplitude controls for the output are imposed, one or other of the integrators will reach saturation before the other output reaches its zero crossing point.

Circuit modifications
- Use a switched integrator rather than a switched gain amplifier. This makes IC_1, IC_3 redundant (Circard Set 3, No. 5). LM3900 quad package may be now arranged to provide the two outputs.
- Phase shift oscillator (above) provides three outputs with 60° phase relationship.
IC_1–IC_3: 1/6×CD4049,
R: 10kΩ, C: 2700pF,
frequency: 13kHz.
As the c.m.o.s. gates are being used in their linear region, both the n- and p-type transistors will be conducting and hence power consumption will depend on the supply voltage. Typically the total current drain from the supply for the above network is
$V_{DD}-V_{SS}$= 3V I_T=0
$V_{DD}-V_{SS}$=10V I_T=12mA
$V_{DD}-V_{SS}$=15V I_T=30mA
Frequency may be controlled by substituting voltage-dependent resistors for each R_1 and maintaining as close a ratio as possible between the R values. Frequency is approximately $1/3RC$.
Note that with the CR values necessary for 60° phase shift at a specific frequency, the output of each buffer stage is attenuated by about one half and hence the minimum gain of each stage must be >2.
- An alternative arrangement is shown above right, using similar c.m.o.s. buffer inverters. In this case the resistor ratio is critical and theoretically for infinite gain amplifiers $R_2=R_1/2$ and a much better approximation to sinusoidal outputs is obtainable from each buffer, again phase shifted by 60°. Typical values R_1:100kΩ, R_2: 33 to 39kΩ, C: 2700pF, $V_{DD}-V_{SS}$=6V, frequency 1kHz.

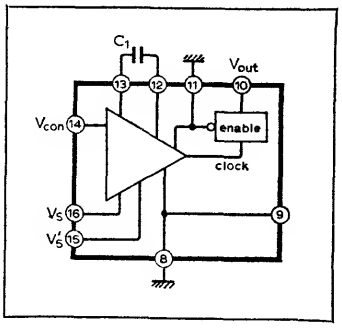


These buffers have gain-frequency responses which give higher gains for lower supply voltages. Typically 50dB at +3V up to 100Hz, and 30dB at +10V up to 100kHz. Hence since the gains are finite, then R_2 must be less than $R_1/2$. But at the lower values of the supply range 3 to 15V, some flexibility of this value between each R_2 is permitted. At higher levels the ratio is more critical, R_2 may be replaced by f.e.ts employed as v.c.r. to obtain a restricted frequency range.

Further reading
Voltage controlled two-phase sawtooth oscillator, *Wireless World*, June 1973, p. 285.
AN-88 CMOS Linear Applications, National Semiconductor, p. 170.
Frequency controllable 3-phase sinewave generator, *Electronic Engineering*, July, 1974.

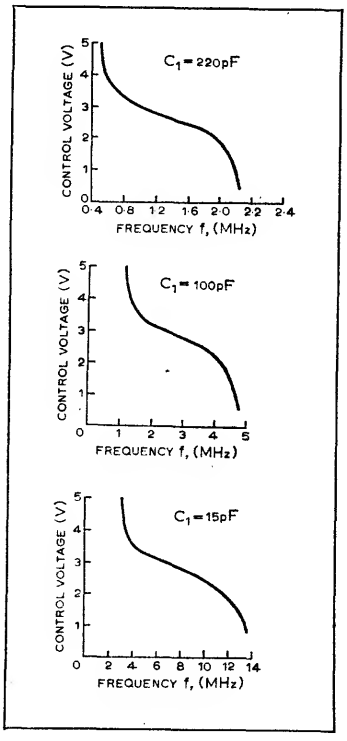
Cross references
Set 11, card 6.
Set 8, card 1.

Monolithic voltage-to-frequency converters



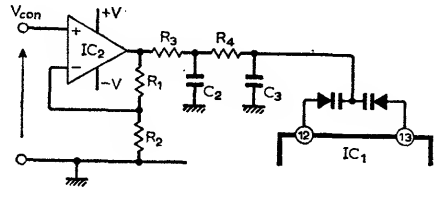
Typical data
IC ½SN74S124N
C_1 220pF
$V_s = V'_s$ +5V d.c.
Frequency range 0.7 to 1.8MHz (approx. linear)

Circuit description
An emitter-coupled astable multivibrator uses a single capacitor for timing. The circuit has high switching speed because charge storage effects are avoided by using the transistors in a non-saturated mode. This circuit is the basis of the above medium-scale integration package, where variable frequencies are obtained by charging the external capacitor at different rates via an internal voltage-controlled current source. The i.c. package contains two identical networks, but if only one is being used, it is essential that both ground connections (pins 8 & 9) are earthed to ensure earthing of the substrate and good isolation. The enable terminal (no. 11) must be grounded for continuous output at the output terminal. Output is disabled if this terminal is taken to logic high or open-circuited.



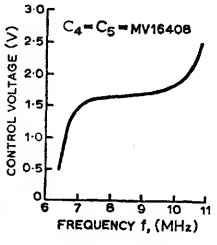
Graphs opposite indicate linearity over a restricted range for each capacitor value, and waveform deteriorates at very low values of C_1, and thus at high frequencies.

Circuit modification
- Emitter-coupled astable output swings are usually restricted. An additional output stage supplied via V'_s permits the output swing to be approximately 0V up to V'_s and hence t.t.l. compatibility is easily achieved, i.e. V'_s and V_s need not be the same.
- Variable-capacitance diodes may provide a wider frequency range, depending on type (see over). Supply voltage 4.5 to 6.5V, frequency maintained constant.



Components (circuit above)
Supply ±10V
IC_1 SH74S124N IC_2 LM301
R_1 R_2 10kΩ
R_3 R_4 100kΩ
C_2 C_3 1μF
C_4 C_5 MV16408

IC_2 is connected as a non-inverting amplifier with a voltage gain of two, so that the biasing voltage in this case is twice the control voltage. This gain can be altered for appropriate voltage range.
A claimed frequency range of 2 to 20MHz using varactors MV1403 and MC1456 for IC_2 is documented in the referenced literature.

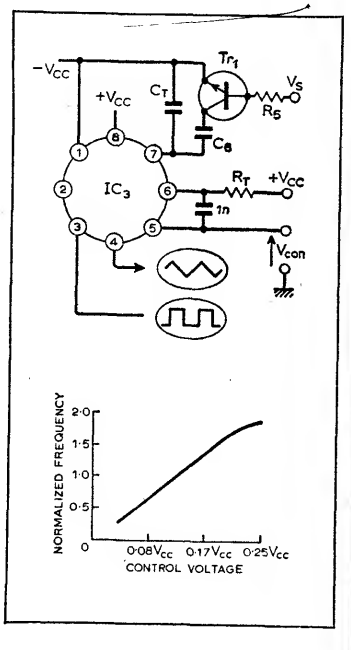


Components (circuit right)
IC_3 LM566, SE/NE566
General-purpose voltage-controlled oscillator.
C_T 4.7nF C_6 0.047μF
R_5 4.7kΩ R_T 10kΩ
Maximum sweep rate 1MHz
R_T and C_T are the frequency range determining components. For a fixed value of C_T 10:1 variation in frequency is possible via a variable input at $V_{control}$ which should be within the range 3 to 5.5V for $V_{cc} = \pm 6$V.

The above values provide for a maximum free-running frequency of about 10kHz for Tr_1 off. For $V_s = -3$V, Tr_1 is saturated, hence increasing timing capacitor 10 times, free-running frequency is then approximately 1kHz.

Control voltage measured between pins 8 and 5 should be in the range 0 to $0.25V_{cc}$. (It is this voltage divided by R_T which defines capacitor charging current.) Frequency is

$$\frac{2(V_{cc} - V_{control})}{R_T C_T V_{cc}}$$

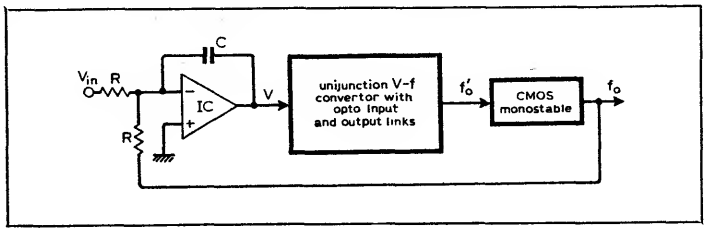


Further reading
Klein, E. Medium-scale integration for instrumentation and control, *Semiconductors* (Motorola) vol. 2 no. 1 1971, p. 20.

Signetics: SE/NE566 function generator data sheet.

Cross references
Set 17, card 3
Set 8, card 9

Linearized voltage-to-frequency converter



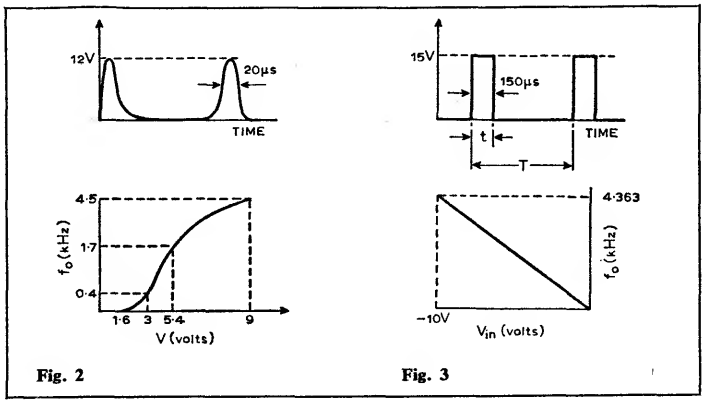


Fig. 2 Fig. 3

Components
R 100kΩ, C 0.22μF
IC 741
Unijunction V-f'o—see over, centre. Monostable—see over, right V_{in} 0→−10V

Performance
Graphs of f'o and fo are shown in Figs. 2 and 3. Graph of V against fo, corresponding to open-loop v-f conversion, is shown in Fig. 2. with V_{in} against fo shown in Fig. 3. Linearity achieved was better than 0.5%—clearly much better than the open-loop performance.

System description
If the loop gain of a closed-loop system is high then the effect of non-linearities in the forward path is much reduced. In this case we have a highly non-linear V to fo converter and an integrator/error detector is then included to provide the feedback. In d.c. terms, the integrator can be regarded as having infinite gain since for finite input voltage the output voltage after infinite time is infinite, ignoring the effect of saturation. Alternatively: $\Delta V =$

$$1/RC \int_0^T V_{in}dt + 1/RC \int_0^t 15dt$$

The steady-state condition of constant fo can only occur when V is constant and this occurs when ΔV is zero i.e. when the integral of the input signal and the integral of the feedback signal exactly cancel. Hence exact correspondence between V_{in} and fo can be expected if the integrator and feedback signal are "perfect". Immediate improvement in the system would be effected if an i.c. with much lower input current requirements were used e.g. 308. Further improvement would be obtained by the use of a low-loss capacitor. The c.m.o.s. monostable was included to give an output pulse train of well defined height and width and overall shape. A better f'o to fo converter could have been used. It should be noted that the overall characteristics are now dictated by the feedback signal and the integrator so that forward path changes, causing changes in fo, will be completely cancelled, apart from transient effects. Changes in the shape of fo, e.g. impulse height and width, will however have an effect on fo, although not linearity.

System modification
Effectively, the combination of the monostable and integrator is an f'o to v converter. The system could therefore be changed to that shown in Fig. 4. K would be chosen to be sufficiently high such that the linearity of the overall system is equivalent to that of the f to v converter. This is only satisfactory if the shape of the f'o pulses is satisfactory.

Element description
The circuit of Fig. 5 shows the detail of the unijunction v to f converter (card 1) used. The opto-elements are included to show that their inherent isolating properties can be used not least to produce a very non-linear v to f'o characteristic. This is because D_1 requires approximately 1.6V to conduct and there is non-linearity in the device current transfer ratio.

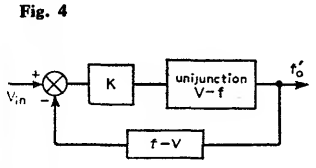
Resistor R_2 is included to protect the transistor and R_4 is large to produce a sufficiently large pulse to trigger the monostable. Resistor R_1 may be reduced to allow much lower input voltages to be used. The limit is set by the opto-diode input current. Any opto-isolator may be used e.g. TIL112.

Components
R_1 2.2kΩ, R_2 1kΩ, R_3 100Ω
R_4 10kΩ
Opto-isolators 4350 (Hewlett-Packard)
U.j.t. 2N2646 V_s 15V
C 0.01μF

Circuit of Fig. 6 is the c.m.o.s. monostable used. It is identical in format to that described in set 18, card 8 but includes an extra diode to allow the capacitor to discharge closer to zero volts to improve linearity.

Components
R 100kΩ
C 2.2nF
D 1N914
IC CD4013E

Fig. 4



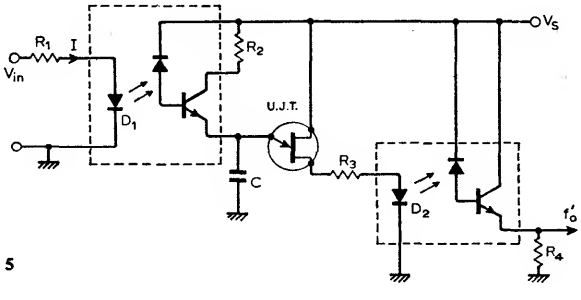


Fig. 5

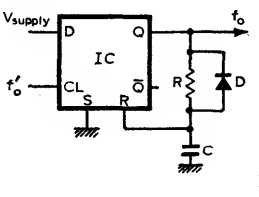
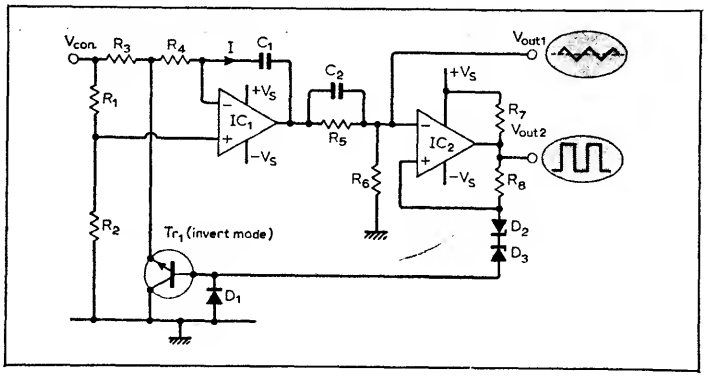
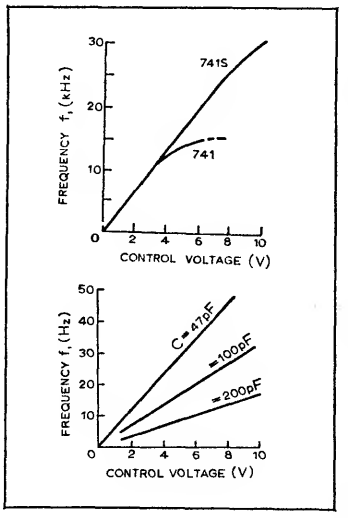


Fig. 6

Linear voltage-to-frequency converters



Typical performance data
Supply ±15V
IC_1 741S IC_2 LM311
Tr_1 ME4002
R_1 68kΩ, R_2 22kΩ, R_3 33kΩ
R_4 15kΩ R_5, R_7 3.3kΩ
R_6 12kΩ R_8 4.7kΩ all ±5%
C_1 100pF C_2 1nF
D_1 1N914
D_2, D_3 reference diodes 6.8V e.g. BZY88
$V_{control}$ range 0 to 10V
Triangular output ±8V peak
Frequency range 30Hz to 33kHz



Circuit description
The circuit comprises an integrator whose output ramps toward positive and negative target values defined by diodes D_2 and D_3 i.e. the potential at the non-inverting input of comparator IC_2 is $V_{D_2}+V_{D_3}+V_{BC}$ (or V_{D1}) about ±9V. When the transistor is off (V_{o_2} negative), capacitor current is

$$I=\frac{V_{control}\left(1-\frac{R_2}{R_1+R_2}\right)}{R_3+R_4} \quad (1)$$

When Tr_1 conducts, I is

$$I=-V_{control}\left(\frac{R_2}{R_1+R_2}\right)/R_4 \quad (2)$$

For equal slopes at the triangular output, V_{o_1}, the current magnitudes are equal, provided

$$\frac{R_1}{R_2}=1+\frac{R_3}{R_4}$$

If V_{o_2} is positive, Tr_1 is on, and integrator output rises towards +9V at which level the comparator IC_2 switches over to make V_{o_2} negative, bringing Tr_2 out of conduction. C_1 charges according to the first equation, and integrator output ramps towards −9V, when comparator again changes state.
Components C_2, R_5, R_6 form a phase-advance network to compensate for the switching delays of IC_2 and Tr_1 at the higher frequencies. The invert mode of Tr_1 provides a very low collector-emitter drop (few millivolts), i.e. the effect on the second equation is neglected.
Linearity is better than 0.5% over the range of control voltage, 0.1V to 8V, based on deviation from 6V value.

Component changes
This slew rate is typically 10V/μs. If 741 used, slew rate (0.5V/μs) restricts higher frequency to which linearity is maintained (see graph).

Range of C_1: Typically 47 to 200pF. Frequency variation shown on graphs. Frequency is power supply dependent, hence need for good stability of supply.

Vary mark/space ratio of output at V_{o_2} by R_2/R_1 ratio change; this also modifies frequency.
Range of R_2, R_1 22 to 68kΩ
Range of mark/space 1:1 to 1:3.

Circuit modifications
● A variable output voltage is obtainable via the circuit shown in Fig. 1. Comparator hysteresis can be changed by varying the fraction fed back via a potentiometer RV_1. This will control the output amplitude. The triangular output is shaped by the circuit of Fig. 2. Potentiometer RV_2 is adjusted for a minimum even-harmonic content, to provide an approximate cisoidal wave form at V_{out}.

● The field-effect transistors of Fig. 3 provide a similar switching action to Tr_1 in first circuit to provide the integrator capacitor current charging paths. IC_3 as an integrator employs a speed-up network of 150pF in series with 10MΩ resistor.
Transistors Tr_2 and Tr_3 controlled by square-wave output from the Schmitt circuit of IC_4. When Tr_2 is on, Tr_3 is off and C_3 charges via Tr_2 and 10kΩ resistor. With Tr_2 off, and Tr_3 on, current reverses through the capacitor with magnitude defined by $V_{control}/2R_9$. RV_3 should be adjusted to provide a symmetrical square-wave output when $V_{control}$ is 5mV.
Input control voltage range: 5mV up to 5V.
Frequency range 10Hz to 10kHz.

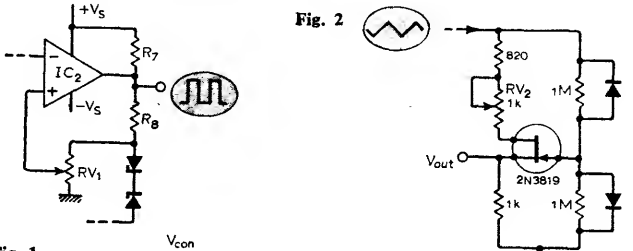


Fig. 1

Fig. 2

Components
IC_3 LM301A
IC_4 LM311
Tr_2 2N3972
Tr_3 2N5019
D_1, D_2 1N457
D_4, D_5 1N751
V_S ±15V

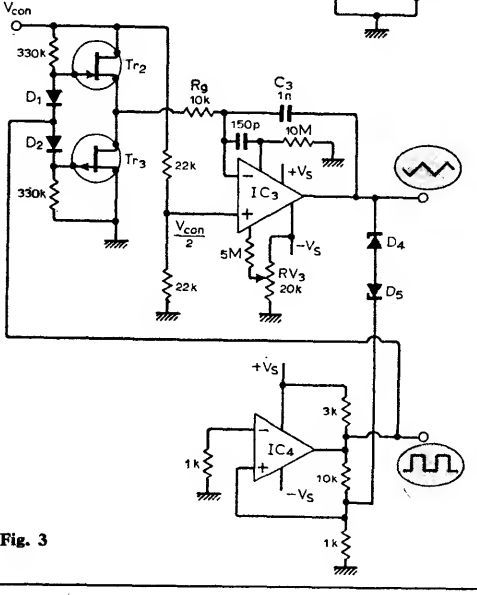
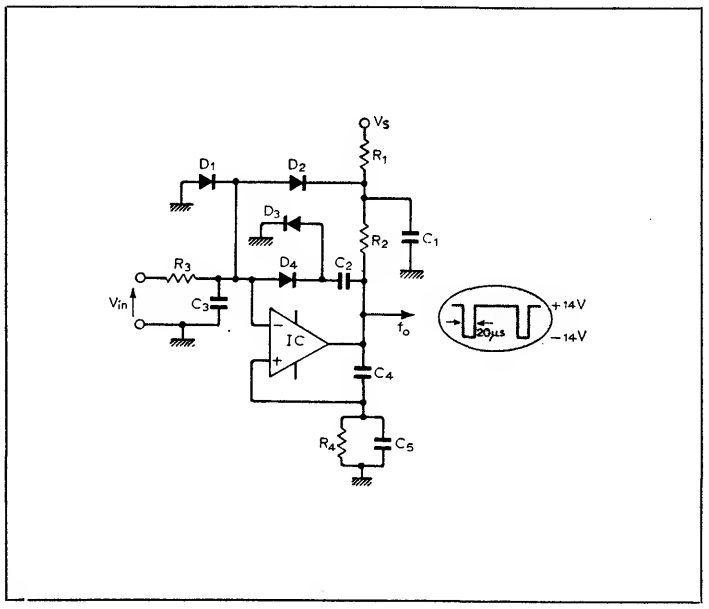


Fig. 3

Further reading
Wright, M.J. Linear voltage to frequency converter, *Electronic Engineering*, July 1973.
Linearize your v-f converter, *Electronic Design*, Nov. 1973.
Applied Ideas, *Electronic Engineering*, Jan. 1975, p. 17.
Linear Integrated Circuits, National Semiconductor, 1972, p. 255.

Cross references
Set 3, cards 1, 5, 11
Set 17, card 3

Diode-pump voltage-to-frequency converter



Components
Supplies ±15V
IC 748C
R_1 12kΩ, R_2 3.9kΩ
R_3 10kΩ, R_4 4.7kΩ
C_1 4.7μF, C_2 1nF
C_3 33μF, C_4 56pF
C_5 500pF
D_1 to D_4 1N914

Performance
V_{in}: 0 to +4.00V
Output pulse train: pulse width about 20μs swinging from +14V to −14V with a maximum frequency of around 14kHz, corresponding to a mark-space ratio approaching 3:1.
Linearity better than 0.3% over two decades.

Circuit description
Elements R_1, R_2, D_1, D_2 and C_1 are not basic to the action of this circuit and will be ignored initially. Suppose the i.c. output is sitting at +14V. Then C_2 will have been charged to this level via D_3.
However as C_3 charges via R_3 under the influence of V_{in}, the negative terminal of the i.c. eventually reaches 0V and the amplifier output swings negative. The network comprising C_4, R_4 and C_5 provides sufficient positive feedback to make this swing very rapid—hence the use of a high speed op-amp. Capacitor C_2 then deposits its charge via D_4 into C_3 in a diode pump fashion thereby lowering the voltage across C_3. However the positive feedback network consists of elements with a short time constant and the voltage on the positive terminal quickly becomes less negative than the negative terminal voltage and so the amplifier voltage swings back to +14V. In the −14V period the circuit is acting rather like a monostable, the delay being fixed by the C_4, R_4, C_5 network and by the R_3, C_3 network. Because there is again positive feedback the rising edge will be equally sharp but the period will be difficult to define accurately, partly because of the complexity of the CR networks and partly because two voltages both going in the same direction (positive) are being compared.
This, however, is not serious since the pulse width does not affect the amount of charge on C_2, and it is this charge which is being balanced by the current in the input network.
The maximum frequency we obtained was close to the limit of the op-amp but the mark-space ratio could have been made even lower if required by reducing C_3, R_3 or lengthening the time constant of C_4, R_4, C_5.
The network comprising R_1, R_2, C_1 and D_2 prevents the device from locking into a saturated condition by too large an input voltage (positive). Diode D_1 prevents the negative input terminal being overdriven by a negative input voltage.

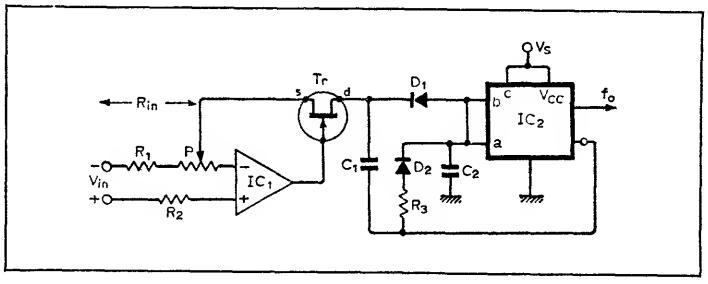
Circuit modifications
- A high-speed comparator would be preferable to an op-amp which was used in our experiments.

- The pulse width does not theoretically affect the result but the pulse height does. A c.m.o.s. buffer amplifier could be included to give a well defined output pulse height—see reference 2.

- An alternative approach to the pulse height problem is to use internal clamping of the output level—see references 3.

References
1 Pease, R. Ultra-linear voltage-to-frequency converter, *Electronic Engineering*, March 1971.
2 Set 3 (waveform generators) card 11.
3 Set 3, card 1.
Set 2, card 1.

Differential input voltage-to-frequency converter



Components
Supplies ±15V
IC_1 741, IC_2 NE555
Tr 2N5457
R_1 270Ω
R_2 1.2kΩ
R_3 47Ω
C_1 1nF
C_2 22nF
D_1, D_2 1N914

Circuit description
The above circuit is of a form published by Woodward but with what appear to us as corrections, although we have to admit to not achieving the performance claimed in his article, viz linearity better than 0.05% from 10Hz to 10kHz. The results we achieved are shown roughly in Fig. 2, measured linearity being 0.15% over the two decades, 100Hz to 10kHz.
Pin c of IC_2 is the R (reset) terminal and its action is not necessary in a brief explanation. Pins a and b are the trigger and threshold terminals of the i.c. When the C_2 capacitor voltage goes below the trigger potential, $V_s/3$, the output swings high, and when the voltage exceeds the threshold voltage, $2V_s/3$, the output swings low—see waveforms of Fig. 3.
The basic principle is that of charge dispensing in which a current proportional to a voltage is balanced by the periodic charging of a capacitor to a precise voltage. In this case, the current through the f.e.t. is fixed by the input voltage at V_{in}/R_{in}. This current flows for time T as a result of the charging of C_2 from $V_s/3$ to $2V_s/3$. Thus

$$\frac{V_{in}}{R_{in}}\ T = C_2\frac{V_s}{3}$$

and $$f_o = \frac{3V_{in}}{R_{in}C_2V_s}.$$

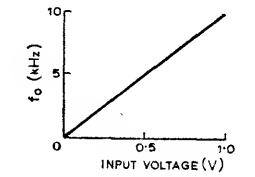
This expression is valid so long as T is large compared with the pulse width.
When the output goes high C_2 charges via R_3 and D_2 from $V_s/3$ toward V_s. During this period D_1 is reverse biased and at the same time C_1 is providing some current to the f.e.t.
When C_2 reaches $2V_s/3$ the output goes low, D_1 conducts, C_1 and C_2 share the charge on C_2 and the parallel combination discharges linearly through the f.e.t. Diode D_2 is reverse biased in this period.
The sharing of the charge between C_1 and C_2 causes the sharp drop in the C_2 voltage when $2V_s/3$ is reached. The discharge is linear because the f.e.t. current is fixed by the input voltage.
The results obtained required adjusting of the op-amp offset voltage to zero. Common-mode rejection ratio is independent of input resistor match and is dictated by the op-amp used. However, common-mode voltage should not exceed ±2V.

Component changes
The charging time depends on C_2R_3 and should be short without R_3 being so low as to overload IC_2. This is not difficult to achieve since it is the open collector terminal which is used to charge C_2. Capacitor C_1 serves to cut off D_1 whilst C_2 is charging, so its value is not critical. Generally speaking though it should be less than C_2 to minimize the drop in C_2 voltage when D_1 starts conducting again, thereby keeping the slope of the downwards ramp as large as possible and clearly defining the time at which the voltage drops below $V_s/3$. Actually, C_1 and D_1 can be removed altogether without complete failure of the circuit, although linearity and output pulse shape are affected.
Diodes D_1 and D_2 can be any general-purpose diodes unless very high speed operation is required.
Reducing the values of the op-amp input resistors and choosing a suitable op-amp will allow values of V_{in} in the millivolt region to be used to give the same output frequencies.

Circuit modifications
Any circuit which will successfully draw constant current from the junction of C_1 and D_1 will produce the same result and such a circuit is shown in Fig. 4. The photodiode current is proportional to light intensity so an intensity-to-frequency converter would be produced by this arrangement. The differential input aspect is lost, however, unless one puts a second photodiode, connected the opposite way round, across the one shown.

Reference
Woodward, W. S. Simple 10kHz voltage-to-frequency converter features differential inputs, *EDN*, Oct. 20, 1974, p. 86.

Fig. 2



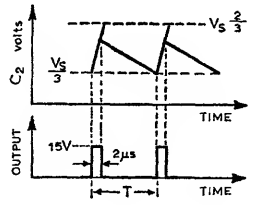


Fig. 3

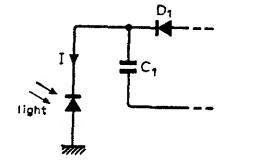


Fig. 4

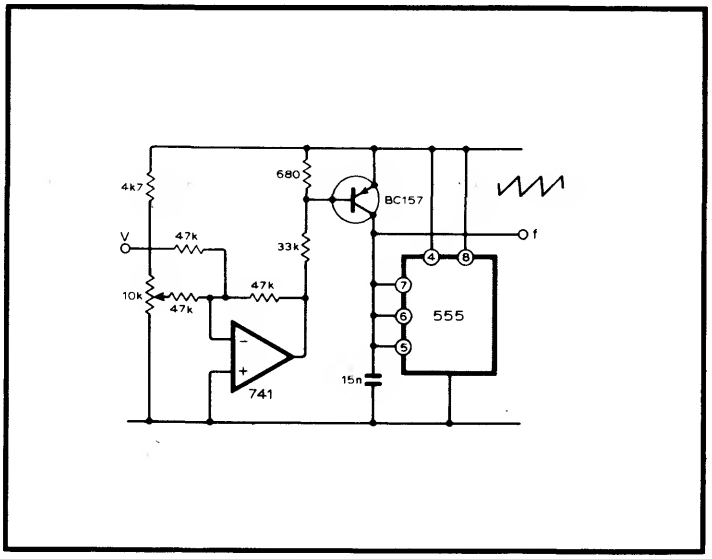
wireless world circard

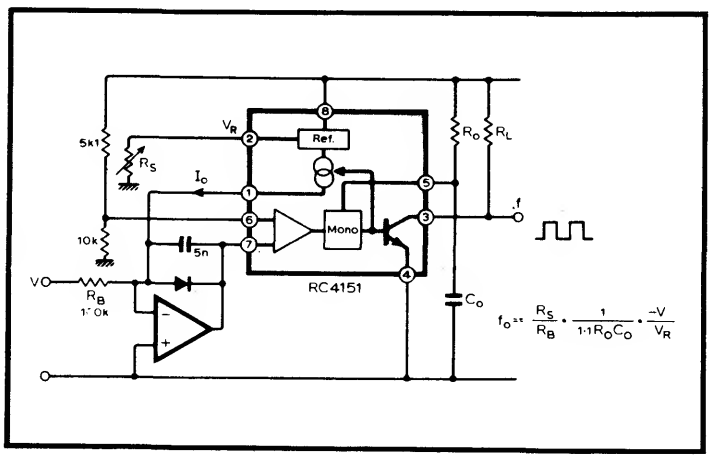
Most of the circuits described have been aimed at linearizing the v-f conversion, as in measurement of modulation systems. Sometimes it is required to have a converter in which the v-f conversion is highly non-linear with the frequency following, for example, an exponential or logarithmic function or sharply changing at some threshold voltage. The circuit indicates a simple way of changing the frequency over a claimed five-decade range.

A linear voltage variation is applied to the base-emitter junction of a transistor to charge a capacitor. The capacitor forms part of an astable circuit based on the well-known 555 timer, with a sawtooth waveform generated across the capacitor swinging between $V/3$ and $2V_s/3$. The reference indicates additional components to set the frequency to zero for $V=0$ and for buffering the output waveform. More generally a linear v-f converter is combined with a non-linear amplifier whose non-linearity is predictable, rather than introducing non-linearity into the conversion process itself.

Reference

Brice, J. L. Voltage-controlled ramp generator, *Wireless World*, June 1976, p. 72.



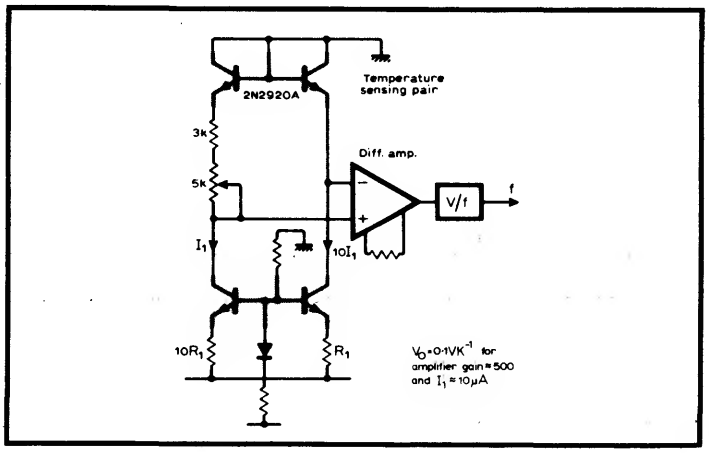


The new generation of linear integrated circuits includes complete v-f modules that will compete with the hybrid and modular versions for many applications. One such monolithic device RC4151 is in line of succession to the 555. It includes a monostable comparator and output stage, but adds a switched current generator. It can be used without additional active devices, but for improved linearity is combined with an op-amp to form a charge-balancing system. The input current to the summing junction is balanced by the constant-height constant-width current pulses returned by the monostable ensuring a linear relationship. A zero-offset voltage fed to the non-inverting terminal ensures that f→0 as V→0. Resistor R_s sets the scale-factor for 0–10kHz corresponding to 0→10V.

Reference

Cate, T. IC V-f converters readily handle other functions such as f-V, A-D, *EDN*, Jan. 5, 1977, pp. 82–6.

The same article shows amongst other applications a linear thermometer, with some similarity to the band-gap reference circuits of set 23. The temperature-sensing pair are forced to operate at a 10:1 ratio of collector currents giving a ΔV_{BE} that is a controlled linear function of temperature. The precise scaling factor is set by the 5kΩ resistor. The amplifier requires to be a true differential input amplifier of controlled gain. Again the overall function is split into two parts: a linear v-f converter, and a separate circuit to provide the linear or non-linear response. It would be proper to describe this as a T-V-f converter.



Set 22 : Amplitude modulators

The term amplitude modulation here includes modulation with either one or two sidebands, with or without a carrier present, by one of four methods—multiplication, switching, non-linearity, or direct tuned-circuit modulation in a class C amplifier.
The circuits using 741s are limited to use with carrier frequencies of a few tens of kilohertz, but two other i.c. designs—the modulated crystal osillator of page 27, the "micropower" circuit of page 32 and those of page 24—operate with carriers of the order of megahertz. And examples of v.h.f. modulators are given on page 33.
The i.c. modulator of page 24 can double as a with-carrier or suppressed-carrier circuit, and uses a biased gating-control input for the modulation. Balanced i.c. modulators appear in place of circuit modifications on this page (see also page 31).
Operating conditions for the lower circuit on card 7, originally omitted, have been added and further reading for the bridge modulator added.

Amplitude modulators

If the amplitude of a high-frequency sinusoidal carrier, $c(t)=A\cos\omega_0 t$ is made to vary in sympathy with the instantaneous value of a low-frequency signal $x(t)$ an amplitude-modulated signal is generated which has a spectrum concentrated in the vicinity of the unmodulated carrier frequency, f_0. The effect is to shift, or frequency-translate, the spectrum of the modulating signal to produce a pair of sidebands symmetrically disposed with respect to f_0 as shown in Fig. 1. The resulting wave may be described by: $y(t)=[A+x(t)]\cos\omega_0 t$, so if, for example, $x(t)$ is a pure tone modulating signal represented by $x(t)=A_1\cos\omega_1 t$ the a.m. output becomes $y(t)=[A+A_1\cos\omega_1 t]\cos\omega_0 t$ which may be written as $y(t)=A[1+m\cos\omega_1 t]\cos\omega_0 t$ where $m=A_1/A$ is the modulation index, or modulation depth, and has a value $\leqslant 1$ if over-modulation is to be avoided.

The amplitude modulated waveform is shown in Fig. 2, and if this is displayed on an oscilloscope the modulation index may be found from $m=(B-C)/(B+C)$. As well as measuring the modulation index, the oscilloscope may be used to examine the linearity of the modulation process if it has an X-Y facility. If the amplitude modulated wave is applied to the Y-amplifier and the low-frequency modulating signal applied to the X-amplifier a Lissajous figure of $y(t)/x(t)$ is obtained as shown in Fig. 3.

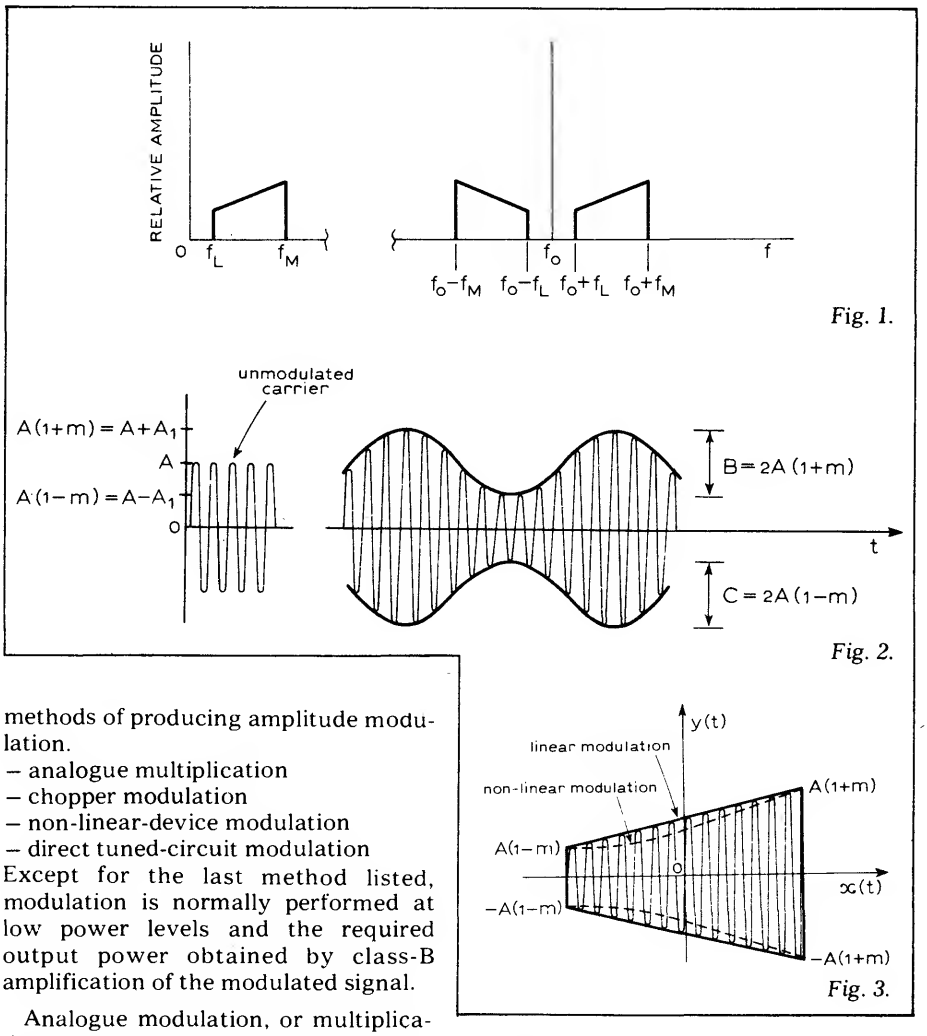
The above process is what is generally accepted as understood when referring to a.m. However a family of processes may together be considered as amplitude modulation techniques which include

- a pair of sidebands with carrier (a.m.)
- a pair of sidebands without carrier (d.s.b. or d.s.b.s.c.) or with diminished carrier (d.s.b.d.c.)
- an upper or lower sideband without carrier (s.s.b.) or with diminished carrier (s.s.b.d.c.)
- a pair of single sidebands with independent modulation (i.s.b.)
- one sideband, carrier and a vestige of the other sideband (v.s.b.)

In general, the above systems depend in some way on the use of four basic methods of producing amplitude modulation.

- analogue multiplication
- chopper modulation
- non-linear-device modulation
- direct tuned-circuit modulation

Except for the last method listed, modulation is normally performed at low power levels and the required output power obtained by class-B amplification of the modulated signal.



Analogue modulation, or multiplication, is obtained by applying the modulating signal and the carrier to a circuit providing an output which is a function of the product of its inputs. Output from the multiplier or balanced modulator is ideally a d.s.b.s.c. signal. This arrangement is often convenient for producing an s.s.b.s.c. signal by removing the unwanted sideband and any residual carrier by means of band-pass sideband filter.

Many multipliers or balanced modulators are available in the form of purpose-designed integrated circuits for operation at carrier frequencies of at least 100MHz. Depending on the nature of the modulating signal, the carrier frequency and the required degree of unwanted-sideband and carrier suppression, the filter can be realized using L-C networks, quartz crystal lattice networks, ceramic disc resonators or mechanical filters. If the same signal is applied to both inputs of a multiplier it acts as a squarer and it, or any other square-law device, may be used to produce an a.m. output as shown in Fig. 4 if $v_1(t)=A+x(t)$ and $v_2(t)=V\cos\omega_0 t$.

Chopper modulation is obtained by chopping the modulating signal at the carrier rate, using either a sinusoidal or a square-wave carrier, and then passing the resulting wave through a band-pass filter centred on the carrier frequency.

The bandpass filter will normally remove the component at the modulating frequency as well as the sidebands centred on the harmonics of the carrier frequency. To ease the requirements of the band-pass filter a balanced chopper modulator removes the low-frequency modulating signal component. The carrier-driven switches are normally realized using diode bridges or field-effect transistors.

Modulation using a non-linear device is achieved by adding the modulating- and carrier-frequency components and then passing the resultant through a bandpass filter centred on the carrier frequency to extract the a.m. signal. The non-linear device should have non-linearity not exceeding second-order and the highest significant modulation frequency should not exceed one-third of the carrier frequency.

Direct tuned-circuit modulation is achieved by controlling the voltage across a parallel-tuned circuit, tuned to the carrier frequency, by means of the modulating signal and pulsing the tuned circuit at the carrier rate with a high-power, class-C amplified carrier pulse. If modulating frequency is too high its rate of increase can be such as to cause the envelope of the a.m. wave to become distorted due to the failure to follow the modulation.

The modulation techniques discussed above which use band-pass filters must provide a filter bandwidth suited to the transmission of the desired signal whilst rejecting all unwanted components. For a.m. and d.s.b. this bandwidth must be twice the highest modulating frequency and for s.s.b. it must be equal to the bandwidth of the modulating signal. In virtually all these cases the sharp cut-off required from the bandpass filter is only obtainable if the centre frequency of the filter is relatively low. Normally the filtration is achieved in the region of 50Hz to about 1MHz and the resulting modulated wave heterodyned, or frequency translated, to the required carrier frequency for transmission.

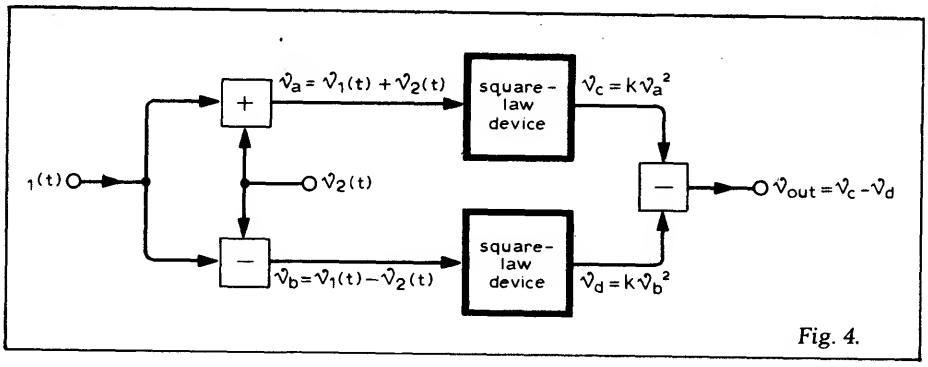
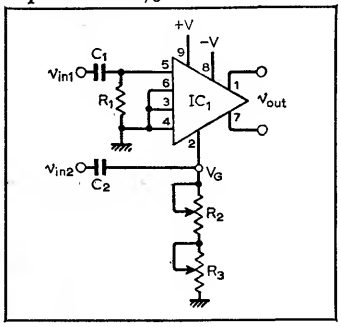


Fig. 4.

Another way is the phasing method of generating an s.s.b. signal which avoids the problems associated with filter design, but replaces them with the problem of designing a pair of networks (A and B) which are required to maintain a constant 90° phase difference between their outputs whilst their output amplitudes are held constant over the bandwidth of the modulating signal. Selection of either sideband is achieved by reversing the output from one of the balanced modulators or by reversing the phase of either the carrier or the modulation to one balanced modulator. Because of the relative ease of inverting an audio signal, the modulating signal reversal is normally the simplest to accomplish in practice.

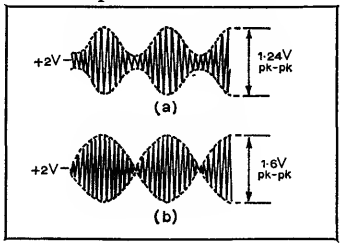
I.C. package modulators

Typical performance
Supplies ±10V, 10mA
IC_1 MC1445L
R_1 47Ω
R_2 4.7kΩ, R_3 220Ω
C_1, C_2 100nF
Amplitude modulator
V_G 2V d.c.
v_{in1} (carrier) 130mV pk-pk
f_c 1MHz
v_{in2} (modulation) 1.3V pk-pk
f_m 10kHz, to produce maximum useful modulation depth of ≈78%.



v_{out} (pin 1 or 7) 800mV pk-pk unmodulated, see waveform opposite.
Balanced modulator
V_G 2.5V d.c. to balance out carrier
v_{in1} (carrier) 130mV pk-pk
f_c 1MHz
v_{in2} (modulation) 2.4V pk-pk (max)
f_m 10kHz
v_{out} (pin 1 or 7) see waveform opposite.

Circuit description
Many integrated circuit packages are available either in the form of purpose-designed modulators for producing a.m. or d.s.b. outputs or in the forms which can be readily adapted to these applications. An example of the latter type is the gate-controlled, two-channel-input wideband amplifier shown. This integrated circuit consists of a pair of differential-input amplifiers having a constant current switched between them under the control of a gating signal which cuts off one amplifier when the other is conducting. The output from each of these amplifiers is available via low-output-impedance Darlington emitter followers. Although the gating signal would normally be at t.t.l.-compatible logic levels, the characteristics of the gate circuit allows the i.c. to be used as an amplitude modulator



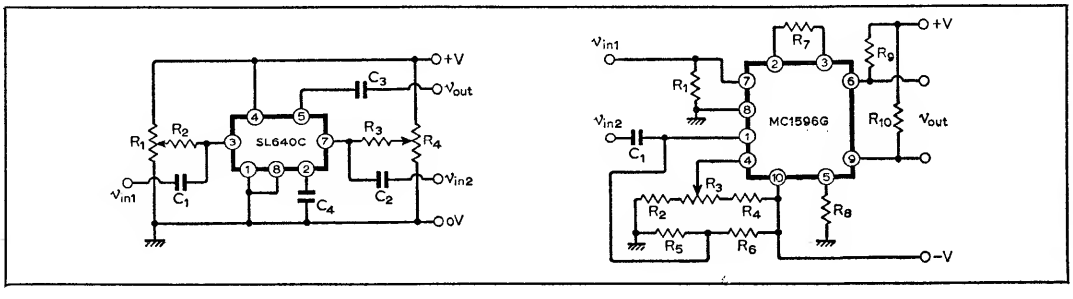
when connected as shown. Although the voltage/gain/gate voltage characteristic is far from linear over the full gate voltage range, it is virtually linear over a range of a few hundreds of mV with respect to a suitable d.c. bias. This bias is obtained by connecting a coarse/fine control (R_2, R_3) between the gate (pin 2) and ground. The low-frequency modulating signal is superimposed on this bias by coupling it to the gate through C_2 and the carrier input is coupled via C_1 and R_1 to either of the input channels, pins 5 or 6 (as shown) or pins 3 and 4 (unused in circuit shown). The amplitude modulated output is available at either output, pin 1 or pin 7. With defined input signal levels, the output modulation depth may be varied using R_2 and R_3.

A double-sideband suppressed-carrier signal may be produced by applying the carrier simultaneously to both channels of the input differential amplifiers which then have their outputs cross-coupled. The resulting balanced modulator is as shown. but with pin 5 earthed and the junction of R_1 and C_1 taken to pins 6 and 3. If the carrier has sufficient amplitude to switch these channels completely off and on, the modulating signal is switched between the channels at the carrier frequency, which is equivalent to multiplying the modulating signal by a switching function—the required condition for producing a pair of side-frequencies and suppressing the carrier. If a reduced-amplitude carrier is required, this can be produced by slightly changing the d.c. bias applied to the gate terminal by means of R_3.

Component changes
Useful range of supply ±4 to 12V
Maximum useful carrier input ≈280mV pk-pk producing unmodulated carrier output of ≈3.3V pk-pk
f_c(max) ≈ 75MHz
Maximum load current ≈ 25mA.
Examples of integrated circuits purpose-designed as balanced modulators are the MC1596G and the SL640C. These packages are essentially intended to replace diode-bridge or ring modulators with transistor double-balanced modulators to overcome the disadvantages of the former type of less than unity gain the need for a high level signal at one input and the need to use up to three transformers. The inherently good matching of the monolithic transistors ensures that excellent carrier suppression is obtained with little need for balancing by external components when the devices are used as double-sideband suppressed-carrier generators.
An arrangement of the SL640C for this purpose is shown Typically, V = +6V, R_1 R_4 10kΩ, R_2 R_3 330kΩ, C_1 C_2 and C_3 should have low reactance compared with the source and output resistance, except for high frequency applications (i.e. f_c approaching 75MHz) where the modulation source resistance should be low and C_2 of comparable reactance C_4 is a base-decoupling capacitor and must have a very low reactance at all frequencies used to minimize carrier and modulation feed-through. Resistors R_1 and R_2 are adjusted to minimize modulation and carrier leakage respectively.
The circuit below shows the MC1596G used as an amplitude modulator.
Typically V ±8V, R_1 47Ω R_2, R_4, R_5, R_6, R_7 1kΩ R_3 470Ω, R_8 6.8kΩ, R_9 R_{10} 3.9kΩ, C_1 1μF.

Further reading
Microelectronics Databook: MC1445, MC1596 data sheets and AN-475, 2nd edition, Motorola 1969.
Integrated Circuit Databook, Plessey 1973. pp.103-5.
SL600-Series Application Manual, 2nd edition, Plessey 1974, pp. 29-34.

Cross reference
Set 21, card 2.



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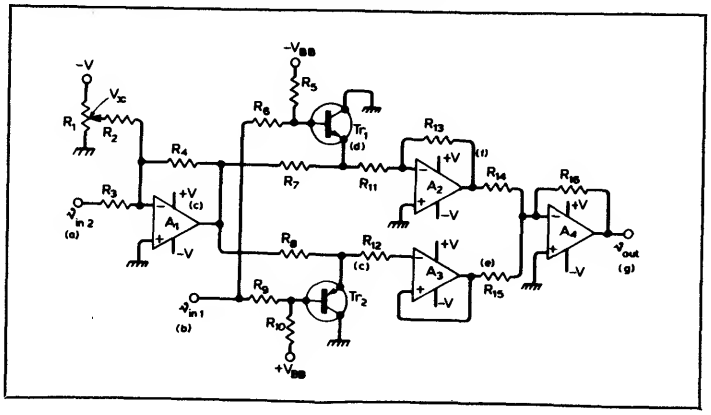
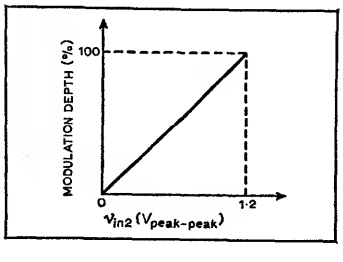
Linear amplitude modulator

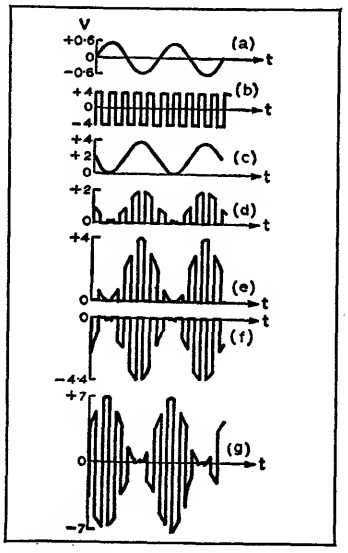


Typical performance

Supplies ±15V+7.5mA, −9.3mA, V_{BB}±5V 0.75mA
A_1 to A_4 741
R_1, R_3, R_7, R_8, R_{11}, R_{12} 10kΩ
R_2 100kΩ R_4 33kΩ
R_5, R_{10} 4.7kΩ R_6, R_9 1.5kΩ
R_{13}, R_{14}, R_{15} 22kΩ R_{16} 39kΩ
Tr_1 BC125 Tr_2 BC126
V_x −5.5V

v_{in1} (carrier) 8V pk-pk square wave at f_c 10kHz.
v_{in2} (modulation) 1.2V pk-pk sinewave at f_m 1kHz to produce a.m. output with 100% modulation (see graph right) v_{out} see waveforms opposite for 100% modulation.





Circuit description

The modulating signal (v_{in2}) is applied via R_3 to the inverting, summing operational amplifier A_1 and receives a gain of $-R_4/R_3$. Although this input is bipolar in nature the output from A_1 is not permitted to go more negative than 0V due to the presence of a d.c. bias obtained from the −V rail via R_1 (V_x) which receives an inverting "gain" of R_4/R_2. This composite, positive signal is applied over separate paths to the inverting input of A_2 (via R_7 and R_{11}) and to the non-inverting input of A_3 via R_8 and R_{12}. The junctions of these pairs of resistors are connected to ground through Tr_1 and Tr_2 when these "chopper" transistors are switched on by the square-wave carrier (v_{in1}).

In the absence of a carrier input, Tr_1 is held off by the reverse bias on its base from the $-V_{BB}$ supply via R_5 and Tr_2 is held in the off state by the reverse base bias from the $+V_{BB}$ rail through R_{10}. With $R_5 \approx 3R_6$ and $R_{10} \approx 3R_9$ a square-wave carrier having a peak value slightly less than V_{BB} is sufficient to overcome the reverse base voltages in the transistors and drive them hard into conduction. On positive half-cycles of the carrier, Tr_2 remains off and Tr_1 is switched on causing the junction of R_7 and R_{11} to fall to within V_{CEsat} of ground, effectively removing the modulation input to A_2. On the following negative half-cycles of the carrier, Tr_1 is switched off and Tr_2 switches on taking the junction of R_8 and R_{12} to within V_{CEsat} of ground, effectively removing the modulation input to A_3. Thus, the signals applied to A_2 and A_3 are in the form of the modulating signal which has been chopped at the carrier rate. As the inverting input of A_2 is a virtual earth and $R_7 = R_{11}$ the signal applied to A_2 is effectively of half the amplitude at the output of A_1. Hence, the output from A_2 is an inverted form of the signal at Tr_1 emitter which receives a gain of R_{13}/R_{11} and by making this gain 2 the output from A_2 has the amplitude of that at A_1 output. A_3 is connected as a unity gain follower so the signal applied to its non-inverting input is fed to a high-impedance point. Therefore, although Tr_2 chops the modulating signal at the carrier rate the full peak-to-peak A_1 output is applied to A_3 and this chopped signal appears at the follower's output. A_2 and A_3 therefore provide equal-amplitude anti-phase chopped output signals. These two outputs are applied through equal resistors (R_{14} and R_{15}) to the inverting, summing amplifier A_4 which, with component values shown, provides a gain of magnitude 1.77 to produce a composite output signal which is the linear sum of its inputs.

The output waveform will contain the original carrier frequency and its harmonics with sets of upper and lower sidebands centred around each of the carrier components. For a pure amplitude-modulated wave the output waveform should be passed through a bandpass filter centred on the input carrier frequency and having a bandwidth sufficient to accommodate the sidebands of the highest modulating frequency.

As shown left, modulation depth is a linear function of the modulating signal input voltage, 100% modulation being achieved when the peak value of the modulation at A_1 output is equal to the d.c. bias at that point.

With the low-cost operational amplifiers shown the circuit can function with carrier frequencies up to about 25kHz. Higher carrier frequencies can be used if operational amplifiers having a high gain-bandwidth product than the 741 are used, and in principle, the circuit should operate with carrier up to several MHz.

With suitable adjustment of the input signal levels and bias voltages the circuit can work from supplies between about ±4 and ±18V. For the circuit as shown the maximum and minimum useful carrier-frequency inputs are approximately 11V pk-pk and 6.4V pk-pk respectively.

Further reading

Linear modulator has excellent temperature stability, Electronic Circuit Design Handbook, Tab, 1971, 4th edition, p.405.

Cross reference

Set 22, card 3.

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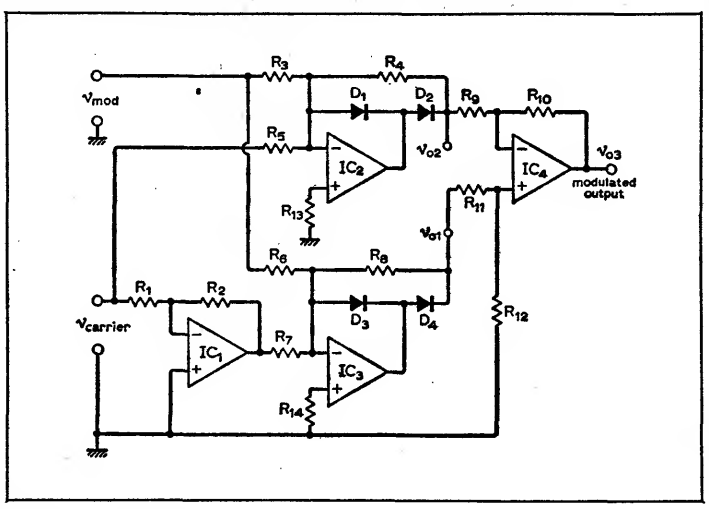
Modulator using precision rectifiers



Circuit description

IC_1 acts as inverter for the carrier signal. The lower frequency modulation signal v_m is summed with the carrier and its inversion, via the absolute half-wave rectifier circuits of IC_3 and IC_2 respectively. When the summed input is positive, the output of IC_3 tends toward a negative level due to inverter action and hence D_3 is forward biased. Therefore the negative peak outputs are clipped to a level approaching zero because D_3 is in the feedback loop. The output is characterized by V_{o1}, that at V_{o2} being similar, but of course the carrier is inverted. Non-linearity of the rectifier impedances introduces some distortion which is evident in the troughs of the modulated output and very slightly distorted at the higher levels of modulated carrier, though not the peaks of the envelope. Output filtering is unnecessary and hence drift of carrier-frequency offers no great problem.

Component changes

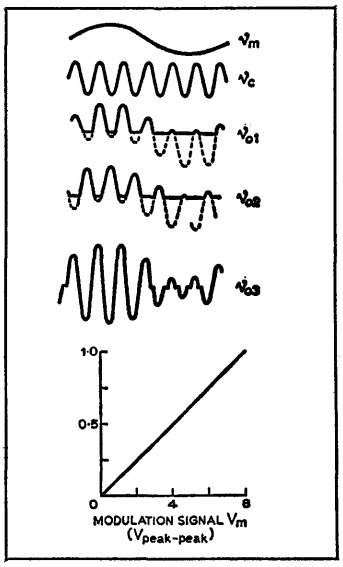
Maximum carrier amplitude to obtain 100% modulation 8V pk-pk ($v_m \approx 8$V pk-pk).
Maximum carrier frequency 23kHz before peaks distort (measured at $f_m = 1$kHz and $m = 1$).
Maximum f_m at this f_c to minimize phase errors about 4kHz; then minimum carrier amplitude 8V.
Maximum carrier amplitude 8.8V.
Use 741CS for faster slew-rate and slightly greater carrier frequency capability. R_1 fairly critical. Maximum variation of $\pm 200\Omega$. Other resistors variable over wide range provided ratios maintained. R_{10}, R_9 etc i.e. accurately matched resistors are suggested. Use centre-tapped transformer to provide carrier and its inverted form, as shown above.
Useful range of this modulator is in the audio band, provided that the non-linearity is not significant. Crossover distortion will be minimized for high carrier frequencies, and large peak-to-peak carrier excursions.

Circuit modifications

High-frequency performance is limited by slew rate and gain of the op-amp in turning off say diode D_1 and turning on diode D_2. This switching speed is increased by the circuit shown middle. Additional gain is added during the switching transition of the order of 250 up to 30kHz obtained with the addition of Tr_1 to Tr_4 circuitry. At the switching instant, D_1 and D_2 are off, thus opening the feedback loop, and do not shunt this additional network. When conduction recommences, one diode heavily conducts, shunts the high output impedance of this additional stage giving again an overall gain of near unity. Low-value resistors provide small time constants for stray capacitance. Frequency response will be above that of op-amp when additional stage driven from supply currents of the i.c. This reduces peak-to-peak swing requirement of amplifier and should be within slew-rate limit at higher frequencies. Typical data Small-signal bandwidth 30kHz to 300kHz
IC_1 BB3500B.
R 100Ω. Chosen to limit rated output current for a 1V swing at output. Other components as before.

Typical data

Supply ± 10V
IC_{1-4} 741
R_{1-10}, R_{12} $10k\Omega$
R_{11} $4.7k\Omega$
R_{13}, R_{14} $3.3k\Omega$
D_{1-4} 1N914
v_{mod} 1V pk-pk at 1500Hz
$v_{carrier}$ 2V pk-pk at 10kHz

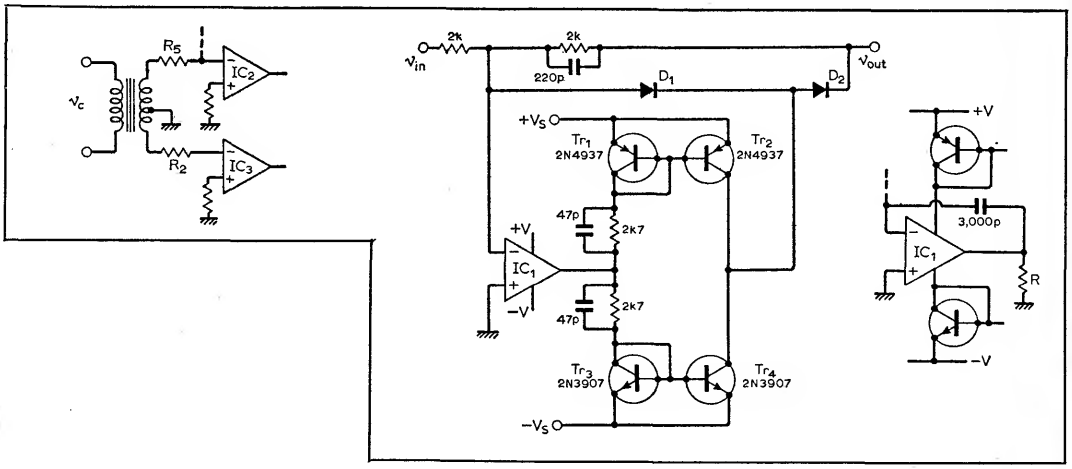


Further reading

Inexpensive AM modulator, *Electronic Design*, vol. 20, Sept. 27, 1974.
Graeme, J. Applications of operational amplifiers—third generation techniques, McGraw-Hill, 1973.
Graeme, J. Boost precision rectifier BW above that of op-amp used. *EDN*, July 5, 1974.

Cross references

Set 4, card 3
Set 22, cards 2, 5
Set 15, card 1



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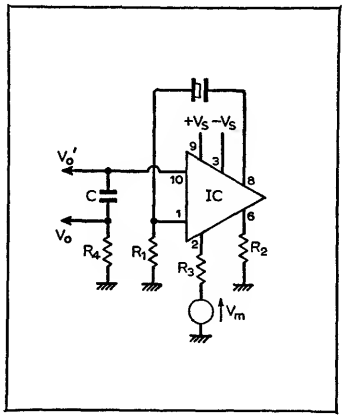
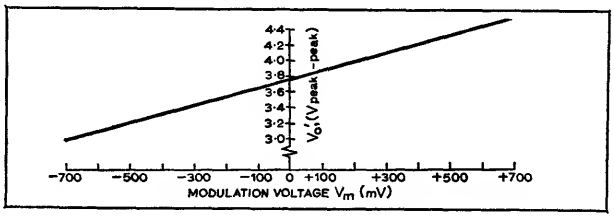
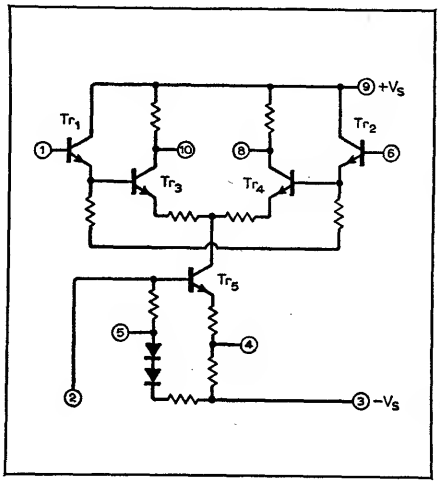
Modulated crystal oscillator



Components

Crystal 1MHz	V_s 6V
R_1, R_2 1kΩ	IC CA3000
R_3 600Ω	C.r.o. probe used had
R_4 100kΩ	impedance of 10MΩ in parallel
C 27pF	with 10pF.





Performance

Graph shown of v'_o (not v_o) was obtained with d.c. values of v_m and indicates a modulation sensitivity of 1.07V/V and a modulation depth of approximately 25% over the range shown. Range was limited by the fact that increasing v_m beyond +700mV caused limiting on the negative peaks of v'_o. Lower limit was very much lower than that shown but there is no point in going beyond a symmetrical condition.

With the c.r.o. probe on v_o the modulation depth fell to 11% (due to the loading of the probe) and this was maintained from d.c. to approximately 2kHz without appreciable distortion. Higher frequencies caused phase distortion.

With R_1 set at 500Ω no carrier oscillations were obtained. With higher R_1, however, little effect was observed, e.g. R_1=10kΩ produced a modulation depth of 10.5% although with approximately 12% increase in carrier amplitude.

Variation of R_2 in the range 1.5Ω to 1500Ω produced very little effect; thereafter limiting occurred.

Description

The CA3000 is a d.c. amplifier in a 10-pin T0-5 package. The schematic is shown above. Emitter follower inputs Tr_1 and Tr_2 provide high input impedance (0.2MΩ), the remainder of the circuit being conventional long-tailed pair (Tr_3 and Tr_4) differential amplifier design with constant-current tail (Tr_5). With external connections as shown in the main diagram the circuit becomes a crystal oscillator with feedback to pin 1. These oscillations are modulated by v_m which controls the tail current. Output at pin 10 contains the (carrier) oscillations plus harmonics modulated by v_m, plus v_m itself, plus d.c. The high-pass filter consisting of C and R_4 eliminates the d.c. and v_m, leaving the amplitude modulated signal.

Since the oscillator is a crystal oscillator the frequency of oscillation is extremely well defined so variations in other components, supply voltages etc. will produce very little frequency modulation.

Modifications

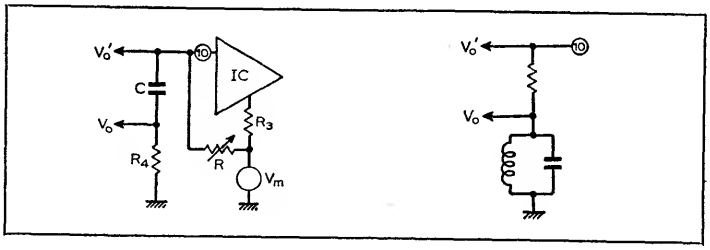
Due to the symmetry of the CA3000 one can reverse the roles of pins 10, 8 and pins 1, 6; no advantage or disadvantage accrues.

All the unwanted terms in v'_o (including carrier harmonics) can be removed by use of a suitable bandpass filter.

Because the output impedance of the amplifier is high (8kΩ) a tuned L-C filter may be used as shown below in our case with a carrier of 1MHz and modulating signal of 2kHz a Q of 250 is permissible but would reduce the modulation depth by 0.707 at 2kHz.

Since the modulation depth is inherently low, a lower Q would appear advisable and if possible one would be better with a more rectangular bandpass filter.

If one simply wants to remove the modulating signal from v'_o, the arrangement shown below can, with suitable adjustment of R simply cancel the offending term. We achieved this with a value of R of approximately 15kΩ. This has the additional effect of reducing the carrier at v_o by approximately 30% but enabled one to increase the modulation depth to approximately 43%, v_m being 6.8V pk-pk. C and R_4 were retained for direct comparison but obviously do not help to give the max. obtainable. Modulation depth of approximately 47% at v_o was achieved by increasing the positive supply to 12V. Alteration of the negative supply had little effect. No change in carrier amplitude was observed with this increased supply. One cannot guarantee this performance since the device is being driven outside the manufacturer's recommendations. Presumably if the alterations of modification no. 1 were used it would be the negative supply which would require alteration.



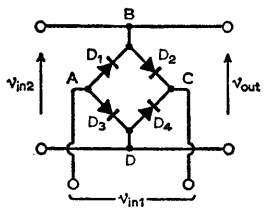
References

RCA applications notes ICAN5030.

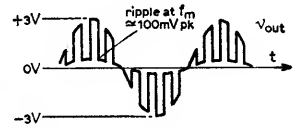
Card 8, this set.

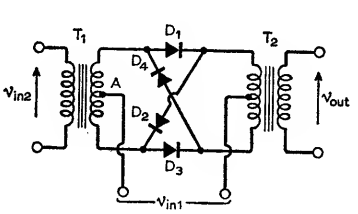
Low-cost 2-stage circuit forms versatile a.m. oscillator. 100 Ideas for Design, Hayden, 1966

Diode bridge modulators

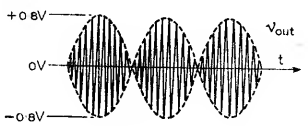


Typical performance
D_1 to D_4 PS101
V_{in_1} carrier 10V pk-pk sinewave at f_c 10kHz, from 600-Ω source.
V_{in_2} modulation 6V pk-pk sinewave at f_m 200Hz from 600-Ω source.
V_{out} see waveform below.





Typical performance
D_1 to D_4 PS101, T_1, T_2 RS type T/T1, ratio 1:1
V_{in_1} carrier 1.2V pk-pk sinewave at f_c 4kHz from 600-Ω source.
V_{in_2} modulation 2V pk-pk sinewave at f_m 200Hz from 600-Ω source.
V_{out} see waveform below

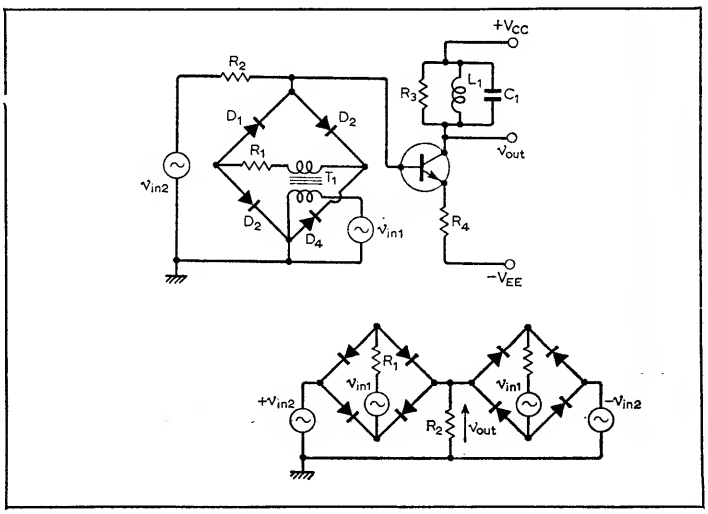


Component changes
D_{1-4} Any general purpose, discrete or monolithic silicon, germanium or Schottky types. A square-wave carrier source may be used in either circuit together with an output filter. A floating source for carrier in Cowan modulator (left) can be simulated from grounded-type using a transformer.

Circuit descriptions and modifications
Both modulators are widely used at low carrier frequencies. In the Cowan arrangement diode switching in the bridge is under the control of the carrier alone provided that its amplitude is much greater than that of the modulating signal. Assuming this condition exists, then during the half-cycles of the carrier when point C is positive with respect to point A, the diodes will be reverse-biased and they present a high impedance shunted across the path between the modulation source and the output. When the carrier goes through its other alternate half-cycles, point A is positive with respect to point C, the diodes become forward-biased and the bridge provides a low-impedance shunt path across the modulation source. The higher frequency carrier voltage therefore causes the diode bridge to act as a single-pole single-throw switch which passes the modulating signal to the output during one half-cycle of the carrier and attenuates the modulation during the other half-cycle. As the magnitude of the modulating signal increases the carrier controlled switching of the diodes becomes less perfect (see waveform and a ripple appears on the output waveform at the modulation frequency. This ripple is due to the larger-amplitude modulating signal causing some small amount of conduction on the diodes during their off state. When V_{in_2} polarity makes point B positive with respect to point D a diode leakage path exists through D_2, the carrier source and D_3, and through D_1, the carrier source and D_4, when B becomes negative with respect to D. This modulator produces an output waveform containing the original modulating-frequency components and sets of upper and lower sidebands centred on the original carrier frequency and its harmonics, all of which are ideally suppressed. To remove all components except the sidebands around the original carrier frequency a band-pass filter must be incorporated at the output.
A simple method of achieving this filtration, at the same time isolating the output from the bridge and simulating the floating-source carrier by means of a transformer is shown top. In this arrangement R_2 should be about $10R_1$; $(1+h_{fe})\,R_4$ should be much greater than R_2, and R_3 chosen to damp the output tuned circuit sufficiently to pass the desired sidebands.
The double-balanced bridge-ring modulator obtained its name from its ability to suppress both the original modulating signal and the carrier from its output. Hence it is to be preferred to the Cowan modulator when the carrier frequency does not greatly exceed the highest modulating frequency. In the circuit shown, when point A is positive with respect to point B, D_1 and D_3 are forward-biased and D_2 and D_4 reverse-biased. When B becomes positive with respect to A, D_2 and D_4 are forward-biased with D_1 and D_3 reverse-biased. Hence the modulating signal will pass from Tr_1 to Tr_2 over two different paths during alternate half cycles of the carrier causing a 180° phase shift of the output after each carrier half-cycle. When wideband transformers are used the output waveform consists of sets of upper and lower sidebands centred on the original carrier frequency and its harmonics, all of which are, ideally, suppressed.
The output waveform differs from the above due to the use of a.f. transformers with a 10-kHz carrier so that very little of the sidebands of harmonic carrier frequencies are present at the output due to transformer imperfections.
Many other forms of bridge ring modulators exist, the basic form of one type using two diode bridges to simulate the effect of a reversing switch

Further reading
Clarke, K. K. & Hess, D. T. Communication Circuits: Analysis & Design, chapter 8, Addison-Wesley, 1971.
Bell Telephone Labs. Transmission Systems for Communications, 4th edition, 1971, pp. 125-8.

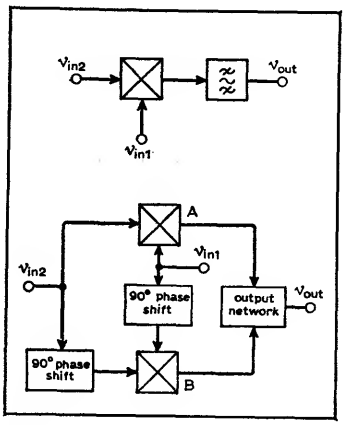
Cross reference
Set 22, card 3.



Single sideband generation

Filter method

A single-sideband signal can be produced by feeding the carrier v_{in_1} and modulating signal v_{in_2} to a balanced modulator to produce a double-sideband suppressed-carrier output which is then passed through a bandpass filter to select either the upper or lower sideband as required. The degree of carrier suppression depends on the design of the balanced modulator and the rate of cut of the sideband filter, which must have a bandwidth equal to that of the baseband modulating signal. A number of different filter realizations may be used, their suitability depending on the carrier frequency at which the filtration is performed. The use of L–C ladder filters is normally restricted to carriers in the approximate range of 20kHz to about 100kHz due to the relatively low Q-factor values obtainable with low-cost inductors. The much higher Qs obtainable with quartz crystals allow the design of bandpass filters using a lattice structure at frequencies above about 500kHz. Ladder-type mechanical filters provide much higher Qs than L-C resonant circuits, which give them excellent selectivity characteristics in a useful carrier range of about 50kHz to 1MHz. Ceramic elements using the piezo-electric effect, but having lower Q values than quartz crystals, can be used in a ladder structure over a carrier range of about 250kHz to 1MHz. Whatever the nature of the bandpass filter the same filter could be used to select either the upper sideband or the lower sideband by shifting the carrier frequency to the appropriate edge of the filter response, assuming the filter to have a similar rate of cut at both edges. The balanced modulator could be replaced by an amplitude modulator in certain applications, the degree of carrier suppression depending on the filter attenuation characteristic.



The unwanted sideband can be removed without the use of bandpass filters by means of phase shift techniques. The basic form of a phasing method s.s.b. generator is shown below. The carrier frequency is applied to balanced modulators A and B with a 90° phase shift introduced in one path. The modulating signal is also applied to both balanced modulators, to A directly and to B via a wideband 90° phase-shifting network. The output signals from the modulators, when combined, result in the suppression of one sideband. If the other sideband is required instead this can be achieved by reversing the phase of the carrier applied to one modulator, or by reversing the phase of the modulating signal to one modulator, or by reversing the output of one of the modulators. Of these methods the second is usually preferred due to the relative ease of inverting a.f. signals. In this method of s.s.b. generation, the modulating signals applied to both balanced modulators should ideally differ by 90° over their complete frequency range whilst retaining equal magnitudes. This is virtually impossible to achieve in a single network as shown over, so practical forms use a pair of networks to more closely approach the ideal requirements as shown below.

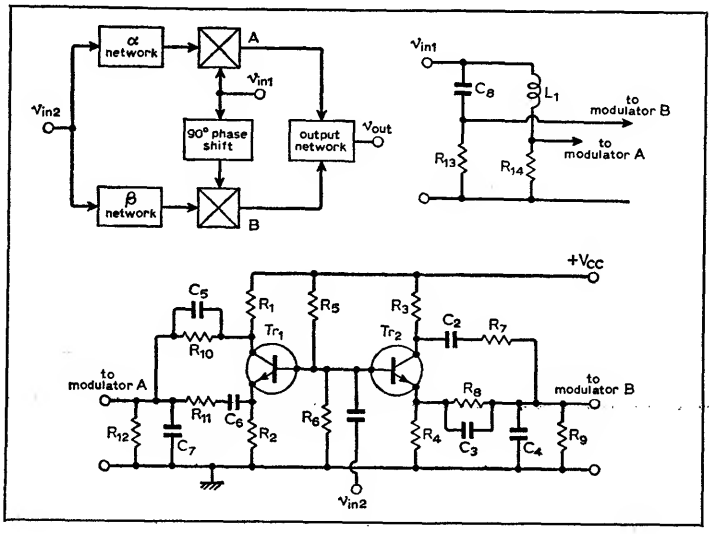
The number of different networks that could be used to realize the α and β-networks is almost limitless, but to meet the required conditions over a range of frequencies indicates the need to combine an all-pass characteristic with a non-uniform time delay as a function of frequency over the required frequency range, which results in a type of ladder structure.

An example of such a realization is shown above. This configuration is capable of maintaining the phase difference at the outputs to within about $\pm 1°$ of the desired 90° phase difference over a frequency range of about 10:1. For the speech bandwidth of approximately 300Hz to 3kHz typical values are given below.

Supply +15V, Tr_1, Tr_2 general-purpose, reasonably well-matched silicon n-p-n transistors.

R_1, R_2, R_3, R_4 680Ω
R_5 15kΩ, R_6 6.8kΩ, R_7, R_{11} 1.775kΩ, R_8, R_{10} 10kΩ
R_9, R_{12} 4.02kΩ, C_1 100nF
C_2 45.9nF, C_3 8.2nF, C_4 21nF
C_5 32.4nF, C_6 181nF, C_7 83.1nF.

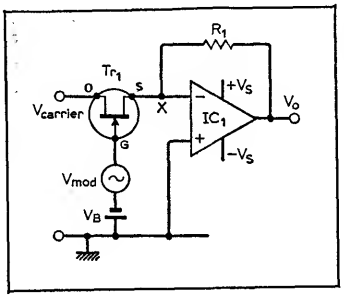
The required 90° phase shift between the carrier frequency inputs to the two balanced modulators can be achieved in a number of different ways, for example from a quadrature sinusoidal oscillator. A simple arrangement for a fixed carrier frequency using a parallel pair of L-R and C-R branches is shown right, the 90° phase shift occurring at the frequency where the inductive and capacitive reactances equal R_{14} and R_{13} respectively. For example with R_{13}, R_{14} 50Ω C_8 8nF and L_1 20μH the carrier should be set to 397.89kHz with v_{in_1} derived from a 600-Ω source.



Further reading

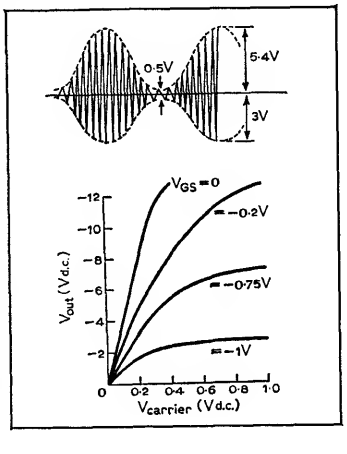
Pappen, E. W. *et al.* Single Sideband Principles and Circuits, McGraw-Hill 1964.
Proc. I.R.E. Dec. 1956—special issue on s.s.b. techniques.
Dome, R. B. Wideband phase-shift networks, *Electronics*, Dec. 1946, pp.112-5.
Betts, J. A. High-frequency communications, E.U.P., 1967, chapter 5.

FET modulators



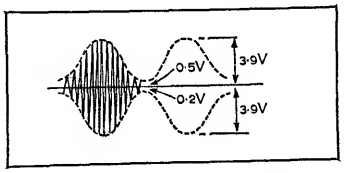
Typical data
IC_1 741, Tr_1 2N5457
Supply ±15V
R_1 10kΩ
v_{mod} 1V pk-pk f_{mod} 1kHz
$v_{carrier}$ 100mV pk-pk
$f_{carrier}$ 10kHz
$v_B \approx 0.75V$
Output at v_o as shown top.
D.C. transfer function between input carrier and v_o, for varying V_{GS} of f.e.t., provides information on linear regions.

Circuit description
This circuit uses an n-channel junction f.e.t. in its voltage-controlled resistance mode, and hence the gain of the inverter-amplifier will be dependent on the slope resistance of Tr_1. The drain-source conductance g_{DS} of Tr_1 is fairly well defined by $g_{DS}=2I_{DSS}/-V_P+2I_{DSS}V_m/V_P^2=K_1+K_2\ V_m$ provided $|V_{DS}|<100mV$.
I_{DSS} is the drain current for $V_{GS}=0$ and $V_{DS}=-V_P$.
In this circuit $V_{GS}=V_{mod}+V_B$, and if $V_B=|V_P|$, then $g_{DS}=(2I_{DSS}/V_P)\ (V_{mod}/V_P)$.
The output from IC_1 is V_o and is $-R_1\ g_{DS}\ V_{carrier}$ hence $V_o=-R_1\ 2I_{DSS}/V_P^2\ (V_{carrier})\ (V_{mod})$
i.e. proportional to the product of the carrier and modulation signals. Note that point x is a virtual earth point and $|V_{carrier}|=|V_{DS}|$. This restricts the carrier to a maximum of 100mV pk-pk to limit distortion. Positive values of V_{mod} much greater than $|V_P|+0.7V$ will forward-bias the gate-source junction, hence this determines the maximum allowable modulating signal.



Component changes
R_1 10 to 20kΩ to provide increased output.
Carrier peaks can be equalized by biasing carrier with V_x, say. For V_x=29mV, other parameters as before, output envelope is shown below.

Circuit modification
● Operational amplifier may be replaced by a single transistor in circuit shown (ref. 1). Output will contain a signal proportional to the carrier and modulating signal product which can be applied to a bandpass filter centred at f_c. C is large enough to be an a.c. short-circuit for the carrier frequency. I_E is chosen to make h_{1b} of the transistor small, given by $h_{1b}=26/I_{E(mA)}$. This ensures that $v_{carrier} \approx v_{DS}$.



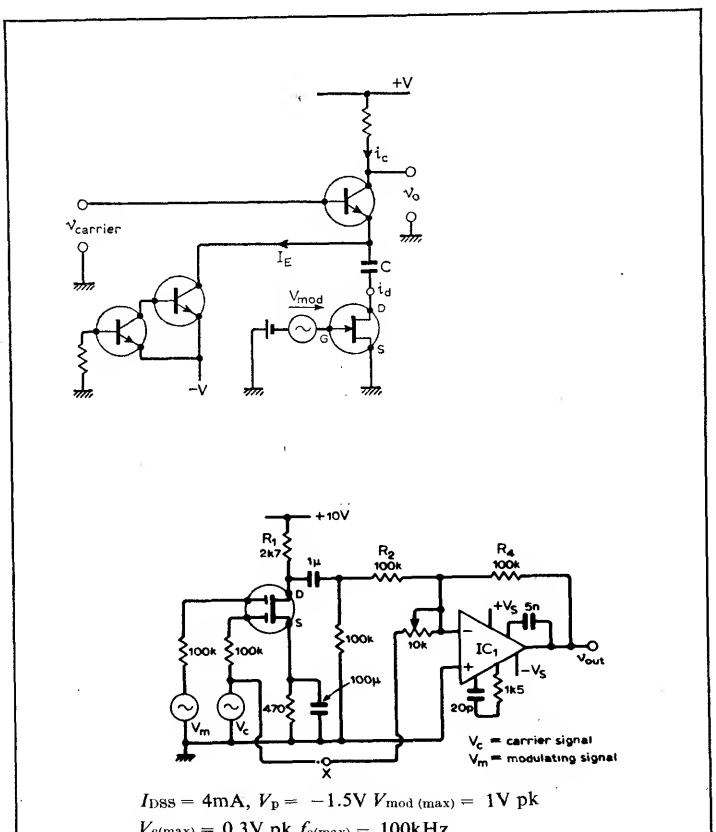
Also, since $i_d=g_{DS}\ v_{mod}$ and $i_c=\alpha(I_E+i_d)$ then $v_o=V_{CC}-\alpha I_E\ R_L-\alpha g_{DS}\ R_L\ v_{carrier}$. This provides, an a.c. product of $2\alpha R_L\ I_{DSS}/V_P^2\times(v_{carrier})\ (v_{mod})$. Similar limitations to levels apply in this circuit (α common base current gain).

● Figure (bottom) comprises a combination of a dual gate m.o.s.f.e.t. and inverting amplifier.
Tr_1 40841, IC_1 SN72709
supply ±12V.
For double-sideband suppressed-carrier operation, the carrier is fed forward through R_4.

If $v_{mod} \gg v_{carrier}$, then gain V_{DS} is given by $-(K_1+K_2v_{mod})\ R_1v_C$ i.e. $V_{DS}=-K_1R_1v_c-K_2R_1v_m\ v_C$.
Provided $(R_4/R_3)v_c=(R_4/R_2)K_1R_1v_c$,
then the above condition is obtained, i.e. v_{out} is proportional to the product of the two signals.
To obtain amplitude modulation the circuit is opened at X. Modulation depth must be limited to around 60%. At these levels of carrier and modulating signals where v_m is no longer much greater than v_C the g_m of the f.e.t. is a function of both signals causing unwanted harmonics.
Modulation depth may be increased if output filters are employed. Note that other analogue multipliers may be used as amplitude modulators, but an important limitation will be their frequency responses.

Further reading
1. Clark, K. K. & Hess, D. T. Communication circuits—analysis and design, Addison-Wesley 1971.
Ideas for design, *Electronic Design*, January 4, 1973, p.98.

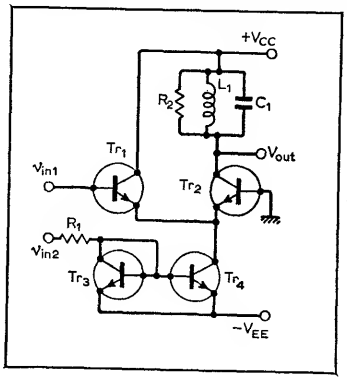
Cross reference
Set 22, card 1.



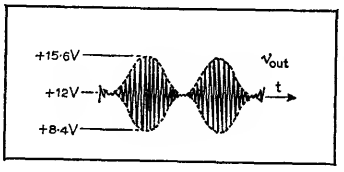
I_{DSS} = 4mA, V_p = −1.5V $V_{mod\ (max)}$ = 1V pk
$V_{c(max)}$ = 0.3V pk $f_{c(max)}$ = 100kHz

wireless world circard

Long-tailed pair modulators

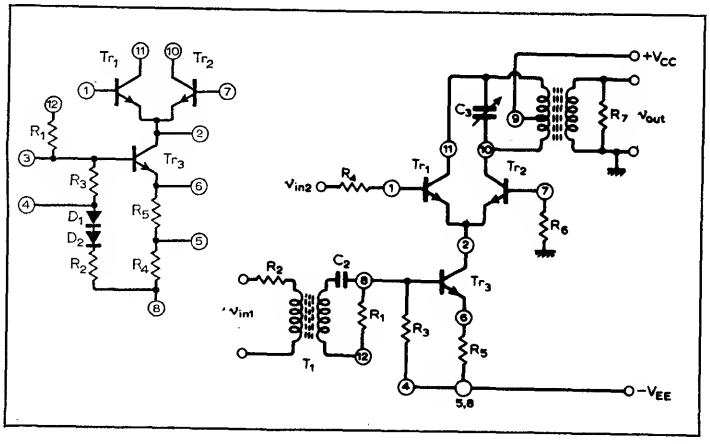


Typical performance
Supply ±12V, ±2.7mA
Tr_1 to Tr_4 1/5 of CA3086 (pin 13 substrate connected to $-V_{ee}$)
R_1, R_2 4.7kΩ



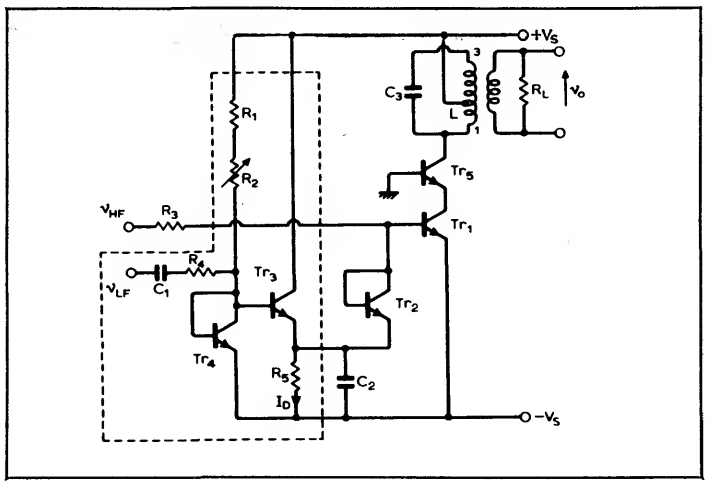
L_1 10μH, C_1 1nF
v_{in1} carrier 100mV pk-pk sinewave at f_c 1.61MHz to produce unmodulated carrier output from tuned circuit of 3.6V pk-pk.
v_{in2} modulation 25V pk-pk (max) sinewave at f_m 1kHz to produce approximately 100% modulation depth output from tuned circuit.
v_{out} see waveform left.

Circuit description
Circuit shown above is an example of an amplitude modulator having one input channel which is linear and the other channel highly non-linear. Although the multiplication from such a circuit is far from ideal, amplitude modulation can be obtained by applying the carrier to the non-linear input channel, applying the modulating signal to the linear input channel and taking the output across a bandpass filter centred on the carrier frequency. In this circuit the collector current of Tr_2 is a linear function of the common tail current but a highly non-linear function of the voltage between the bases of Tr_1 and Tr_2 due to the voltage drive from the carrier source to Tr_1 base. Transistors Tr_3 and Tr_4 form a current mirror that acts as a current source for the differential pair Tr_1 and Tr_2. Quiescent tail current is determined by R_1 with the single-ended (grounded) modulation source v_{in2} set to zero. This quiescent current is then varied by the modulating signal. The collector current of Tr_2 thus contains the modulating signal as well as the carrier and its sidebands, together with carrier harmonics and their sidebands due to the non-linear relationship between the collector current and the carrier drive voltage between Tr_1 and Tr_2 bases.
To obtain an output amplitude-modulated wave the bandpass filter, in this case the parallel tuned circuit $L_1C_1R_2$, must have a sufficiently high loaded Q-factor to remove the modulation-frequency components and the harmonic carrier and sideband components. For the circuit shown the theoretical value of the centre-frequency for the tuned circuit is $f_0 = 1/2\pi\sqrt{L_1C_1}$ Hz=1.592MHz which is within 1% of the value in practice. The loaded Q-factor is $Q_L = 2\pi f_0 R_2 C_1 = 47$ which provides a passband (to 3dB down points) having a width of $f_0/Q_L = 33.87$kHz which is suitable for audio modulation, up to 15kHz. By suitable choice of L_1 and C_1 carrier frequencies up to about 100MHz may be used, with adjustment of Q_L by means of R_2 to provide a suitable bandwidth for the highest modulating frequency.
Whereas the above circuit is formed by interconnecting the monolithic individual transistors to produce the long-tailed pair, other integrated circuits are manufactured in the long-tailed pair configuration. Examples of these are the CA3004, CA3005 and CA3006 the last type being particularly suited to use as a balanced modulator due to the small input offset voltage (typically 1mV). The internal structure of this integrated circuit is shown. The i.c. consists of a well-balanced differential-input amplifier Tr_1 and Tr_2 fed from a constant-current source Tr_3. Due to the versatile biasing arrangements a number of different operating modes may be used but pin 8 must be connected to the most negative direct voltage in the circuit and pin 9 to the most positive direct voltage used. Pin 12 is normally connected to ground.
A typical balanced modulator circuit using this integrated circuit is shown below
In this application, the diodes, R_2 and R_4 of the integrated biasing network are short-circuited, the modulating signal is applied between the differential pair bases v_{in2} and the carrier applied to the base of the constant-current transistor Tr_3 via transformer T_1. The differential-output double-sideband suppressed-carrier signal between Tr_1 and Tr_2 collectors is converted to a single-ended output by the tuned transformer T_2 which suppresses the unwanted output components. Attention should be paid to careful printed circuit layout and screening to obtain the best performance. Typically the carrier suppression is around 25dB below the wanted double-sideband output when v_{in2} is adjusted to produce 16mV r.m.s. at pin 1 and v_{in1} adjusted to produce 31.5mV r.m.s. across the primary winding of T_1 at a frequency of 1.75MHz. Typical values: Supplies V_{CC} +6V, V_{EE} −6V, R_1, R_3, R_5 part of i.c., R_2, R_4, R_6, R_7 50Ω, C_1 560 to 870pF, C_2 10nF, C_3 90 to 400pF, T_1 9.6:1 step-up, T_2 bifilar wound 9:1 step-down with primary tapped 3:1.
This degree of carrier suppression may make the circuit suitable for double-sideband systems requiring the transmission of a pilot carrier. For applications requiring a higher degree of suppression an improvement may be obtained by increasing the modulation signal input and decreasing the carrier input voltage.



Further reading
Clarke, K. K. & Hess, D. T. Communication circuits: analysis and design, Addison-Wesley, 1971, chapters 3, 4 & 8.
RCA Solid-State Databook SSD-201B, 1973, pp.183-8.
Solid State Databook, RCA, SSD-202B, '74 Series, Nov. 1973, pp.108-33.
Cross reference
Set 20, card 4

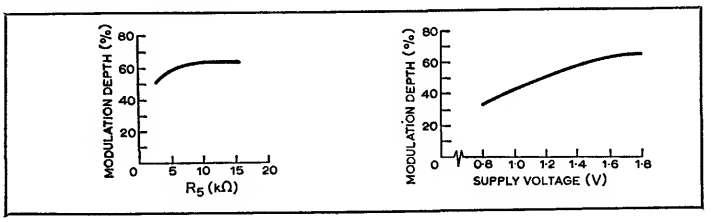
Micropower amplitude modulator



Components

R_1 33kΩ, R_2 5kΩ
R_3 1MΩ, R_4 5.6kΩ
R_5 see graph
R_6 10kΩ load resistor

C_1 47μF, C_2 1.5nF
C_3 250pF, L 490μH (total)
C_3 and L tuned for 460kHz
Transistors from CA3086 i.c.

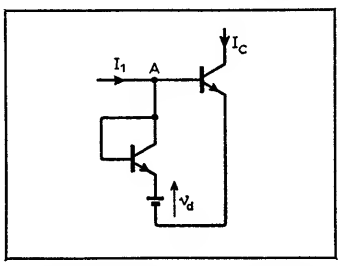


Performance

V_s was set to 1.5V, v_{if} to zero and the carrier frequency adjusted to give maximum v_o; this occurred at about 460kHz. v_{if} was then adjusted to give maximum modulation depth, m, and R_5 was varied. It was found that maximum m occurred at 1V pk-pk for v_{if} for all R_5. The resulting graph of m versus R_5 is shown above centre. Higher values of R_5 produced non-linear modulation and lower values gave a rapidly diminishing value of m. Maximum carrier amplitude was 1.32V pk-pk with R_5=15kΩ. The modulating frequency was 400Hz and linear modulation was maintained over the frequency range 10Hz to 1kHz typical. Maintaining R_5 at 6.8kΩ, the frequency of v_{if} at 400Hz, and altering the magnitude of v_{if} at all points to produce maximum m produced the graph of m versus V_s, above right. The lower limit of 0.8V was chosen as being that of the end-of-life voltage of a dry cell. The corresponding range of v_{if} was 0.48 to 1.25V pk-pk. Power consumption is less than 500μW throughout the voltage range; considerably so at the lower end.

Circuit description

This circuit is due to Venkateswavlu & Sonde (see ref.) who claim slightly better results than we achieved. Consider first the circuit shown above. This is a gain-stabilized block for which

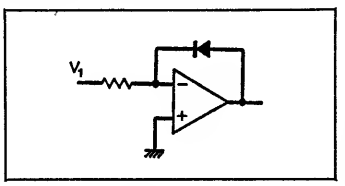


$I_C/I_1 \approx \exp(\lambda V_D)$ (Ref. 1)

over a wide range of operating conditions (λ having the usual connotation). To understand the circuit in a simplified manner assume that both base currents are negligible. Both transistors are governed by the same exponential relationship such that for a given Δv_{be} (which must be the same for both transistors) the collector currents change by the same percentage. Hence, if V_d sets different initial values of collector currents, which it will, a signal V at A will result in the same ratio of a.c. to d.c. in each transistor. As the direct current ratio is fixed by V_d (at e.g. 10:1), the ratio of a.c. is also fixed and since the collector current of the diode connected transistor is approximately equal to the input current I_1, then the current gain I_C/I_1 both small signal and large signal is likewise fixed or stabilized. Clearly changes in V_d cause changes in I_c if I_1 is fed from a current source, i.e. I_c can be modulated. It can be shown (see ref.) that

$m = \Delta I_c/I_c = \exp(\lambda \Delta V_d) - 1.$

The above block can be seen in the main diagram in the form of Tr_1 and Tr_2. V_d is produced across R_5, C_2 simply acting as a short to carrier frequency signals. The section of the main diagram enclosed



by the broken line is, after a fashion, a mirror image of the gain-stabilized block and produces

$\Delta V_d \approx (1/\lambda)\ln(1+v_{if}/R_4 I_D)$

Substituting this in to the expression for m produces

$m \approx v_{if}/R_4 I_D$.

v_{if}/R_4 is the modulating input current leaving I_D as the only variable. I_D is the quiescent current in R_5 and is dependent on the biasing arrangements in the dotted section. m was found to be insensitive to variations in R_1 and R_2 and the graph of m versus R_5 shows m to be somewhat insensitive to R_5 also. This is not surprising as Tr_3, Tr_4 is a stabilized block in the same way that Tr_1 and Tr_2 is.

Note from the expressions quoted that Tr_3, Tr_4 etc comprises a linear-log converter and Tr_1 and Tr_2 effectively take the anti-log. Tr_5 is a casc ded transistor to improve the voltage gain characteristics and may be omitted at the expense of reduced m.

The tapped transformer is included to minimize the loading effect of R_L, again improving voltage gain characteristics. A straightforward L-C circuit could be used at the expense of reduced m.

Circuit modifications

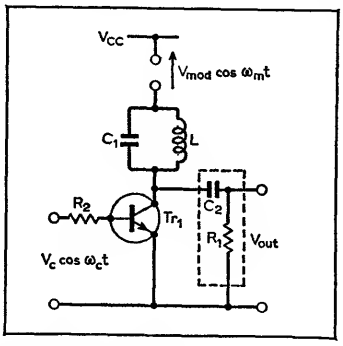
Possible modifications in respect of Tr_5 and the transformer have already been mentioned. In addition it appears possible to remove R_1, R_2 and C altogether and simply current drive Tr_3 and Tr_4 by increasing R_4.

Any linear to log converter may be used e.g. the circuit above right may be used although the micro power aspect is lost and a bias signal would be required with V_1.

Reference

Venkateswavlu, V. & Sonde, B. S. Micropower amplitude modulator, *Proc. IEEE*, July 1971, pp.1114-6.

Direct tuned-circuit modulator



Circuit description

This circuit demonstrates the principle that may be used to perform the initial modulation of a carrier signal, which may then be used to drive a power amplifier. Transistor Tr_1 is driven hard into conduction once every carrier-cycle so that its base-collector junction is forward biased. The related collector current pulses excite the tank circuit LC_1 which is tuned to the carrier frequency which therefore rings between pulses at a frequency f_c. The waveform at the transistor collector or across the tuned circuit is shown opposite at (b). The envelope is approximately the superposition of $V_{CC}+v_{mod}$ and is of the form $(V_{CC}-V_{CEsat})(1+m\cos\omega_m t)$ where the modulating index $m=v_{mod}/(V_{CC}-V_{CEsat})$ To maintain approximately 100% modulation for variation of V_{CC}, the modulating signal is linearly related as shown in graph.

Circuit notes

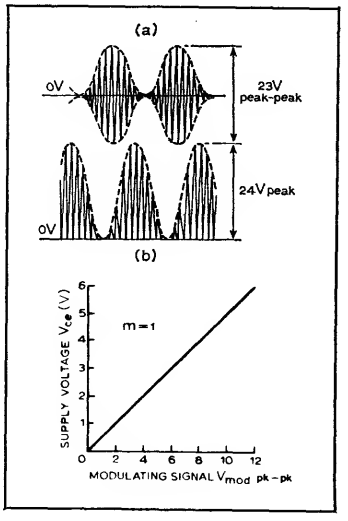
- Tuned circuit Q in the range 30 to 50.
- Filter circuit (high pass) of C_2R_1 provides useful demonstration technique only. Normally output coupled out via tapped-down transformer where L is the primary.
- R_1 value chosen empirically to minimize phase shift of positive and negative carrier peaks of waveform.
- Frequency range of modulating signal 1Hz to 20kHz, but some reduction in R_1 is necessary at the higher frequency to maintain symmetry of waveform.

Applications

In certain situations, a.m. is performed at low power levels, and power levels suitable for transmission are developed by power amplifiers. An example of such a circuit is shown over[2], top. To preserve a wideband performance a push-pull configuration of Tr_1, Tr_2 minimizes unwanted harmonic content. Typical performance data:

V_{CC}: 12.5V
Peak envelope power: 40W
Modulation: 95%
Carrier frequency: 118 to 136MHz
Carrier input power: 5mW.

A similar concept but at a low power is described in the circuit[4] shown over, bottom. Typical output 100mW depending on transistor at a carrier frequency of 27MHz (US citizens band). Collectors are supplied push-pull, but the bases are paralleled, as distinct from above circuit.



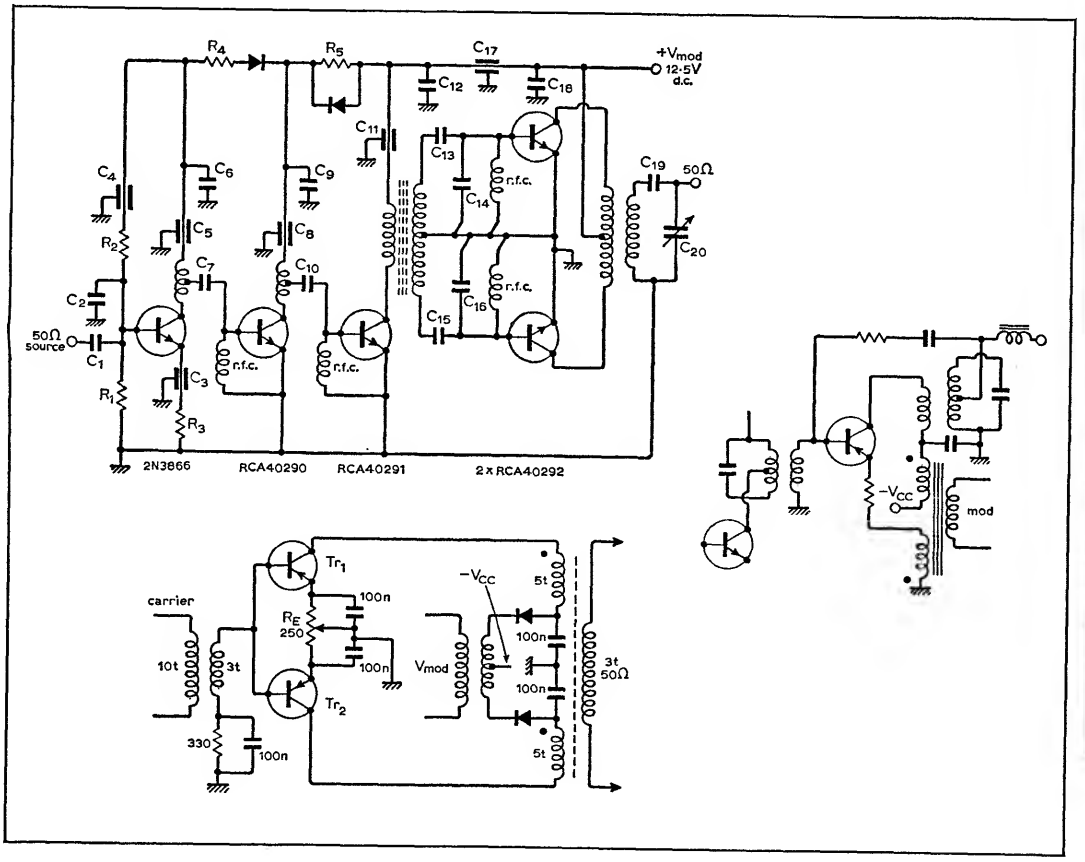
R_E permits balancing of transistor characteristics to cancel carrier.
Circuit right is one in which modulation is applied both to collector and emitter[5].

Further reading

1 Clarke, K. & Hess, D. Communication circuits: analysis and design. Addison-Wesley 1971.
Getting transistors into single-sideband amplifiers. Motorola application report AN-150.
2 RCA application note AN-3749, 1968.
3 100 ideas for design, no. 4, Hayden 1964.
4 Stokes, V. O. Radio transmitters, Van Nostrand 1970.
5 100 ideas for design, no. 3, Hayden 1964.

Cross reference

Set 7, card 6.



wireless world circard

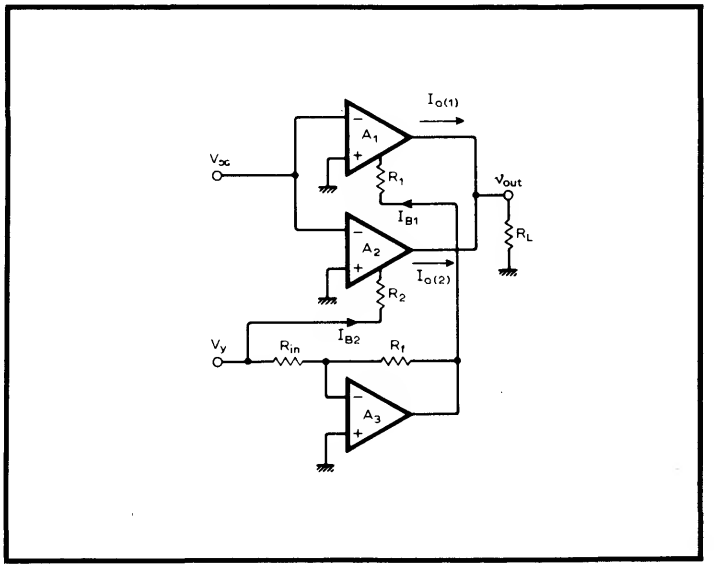
The transconductance operational amplifier triple array CA 3060, when connected as a four-quadrant multiplier may be used as a modulator in the arrangement shown.
The output current from amplifier 1 and 2 is in the form $I_{out} = g_m V_{IN}$ where g_m is the forward transconductance.
Hence $I_{0(1)} = -g_1 V_x$ and $I_{02} = +g_2 V_x$.
$V_{out} = (I_{0(1)} + I_{0(2)})\ R_L = V_x R_L\ (g_2 - g_1)$.
Because the g_m is almost proportional to bias current, I_B, then

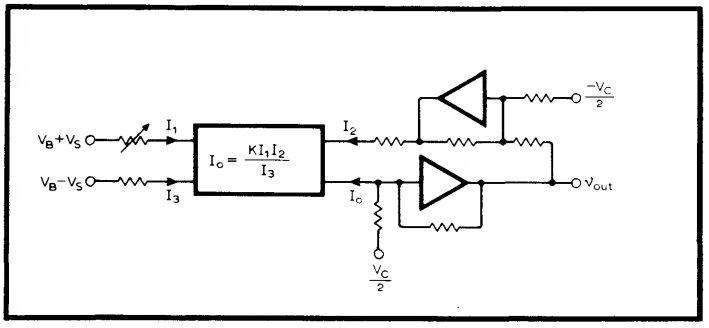
$$I_{B2} \approx \frac{V_y - (-V_s)}{R_2}$$

where $-V_s$ is the negative supply.

Therefore
$g_2 = k_1 I_{B2} = k_2(V_y + V_s)$.
Because the bias current for A_1 depends on $-V_y$, then $g_1 = k_2(-V_y + V_s)$. This means that the output voltage is approximately $2k_2 R_L V_x V_y$, or $V_{out} \propto V_x V_y$. Fuller circuits are given in the reference, allowing for gain equalization and examples of modulated waveforms are shown.

Reference
RCA Integrated Circuits 1976, p. 171.





The analogue multiplier/divider is assumed to have a characteristic given by $I_0 = K I_1 I_2 / I_3$ where I_1, I_2, I_3 are input currents, I_0 is the output current and where K is a parameter dependent on temperature, device ageing etc. Such a circuit is suitable as a precision modulator, where a product term should be generated to an accuracy of around 0.1%. For this condition, the effects of K must be eliminated. The above configuration using negative feedback is shown to provide an a.c. gain proportional to a modulating signal, but independent of the constant K.

Reference
Faulkner, E. A. *Electronics Letters*, 11th Nov. 1976, vol. 12,

Set 23: Reference circuits

First described by one of the authors a little over a decade ago, the ring-of-two reference has become almost a classic constant voltage reference, with many variants coming to light since (See also set 6, especially card 5). The article reminds readers that zener diodes are not the only reference component; any device with a slope or dynamic resistance sufficiently different from its static resistance can be used. And as well as presenting measured characteristics of four zener types, the set includes characteristics of other kinds of device—v.d.rs, conventional diodes and l.e.ds.
Some circuits shown may be familiar under their alternative names—the amplified diode for the technique of page 40, and a constant current diode for the f.e.t. of page 46. (This last-mentioned page has some changes incorporated from the original card.)
And band-gap reference circuits are briefly explained in the article on page 36. (Owners of set 23 of Circards will have noticed that Figs 1 & 2 on page 39 were originally in error on card 2.)

Reference circuits

Some semiconductor devices have highly non-linear characteristics, in which the non-linearity is well-defined with predictable and small dependence on temperature. If a region of the characteristic is found for which the slope resistance is either very much greater than or very much less than the static resistance then the device can be used as a current or voltage reference respectively.

In Fig. 1 (a) there is an extended region over which the voltage varies little for large changes in current. Fig. 1 shows the dual characteristic with current being maintained constant against changes in bias voltage. The most commonly used device belonging to the former category is the zener diode, the reverse characteristic having a sharp breakdown region. There are two physical mechanisms that can control the reverse conduction of a p-n junction: zener breakdown and avalanche breakdown.

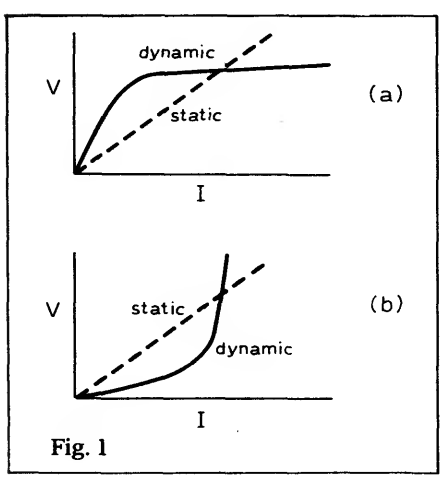


Fig. 1

Zener breakdown is a field effect which dominates for heavily-doped narrow junctions, where even small p.ds of three or four volts can provide a sufficiently intense field for the direct production of hole-electron pairs. The observed characteristics are that the current increases steadily as the operating region is approached, with a rounded knee, and with a temperature drift of about -2mVK^{-1}. To a first order the slope resistance of such diodes is inverse to the quiescent current.

At higher p.ds, which can only exist with more lightly doped broader junctions where the zener effect is unable to limit the voltage, thermally generated holes and electrons are accelerated by the field. If the p.d. is large enough some will gain sufficient kinetic energy before colliding with other atoms, to produce further hole-electron pairs by collision. These in turn may generate further pairs and at a particular voltage there is a very sharp increase in current. Below breakdown the current is negligible, while above it the slope resistance is low. The voltage changes with temperature by less than $+0.1\%\ \text{K}^{-1}$.

There is an intermediate doping level resulting in breakdown voltages between five and seven volts where both processes contribute significantly to the total current. The proportion is dependent both on the junction and on the current level, but it is possible for diodes between 5.5 and 6.5V to have negligible drift with temperature if biased correctly (lower currents for the higher voltage devices). An identical breakdown occurs in the base-emitter region of a transistor, and planar silicon transistors can be used as low-current zener diodes with good slope resistance. Breakdown voltage for the base-emitter junction is typically 6 to 10V, varying little for a given device. (Breakdown diodes are commonly described as zener diodes regardless of which physical process dominates.)

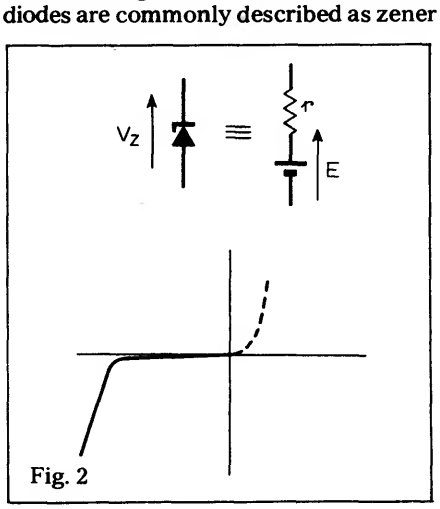


Fig. 2

A simplified equivalent circuit for such a diode if biased into the low slope region is shown in Fig. 2. It consists of a constant e.m.f. in series with a small resistance. The resistance is assumed constant i.e. the characteristic is approximated to by the 'piecewise linear' graph shown. A circuit for a simple zener diode regulator is shown in

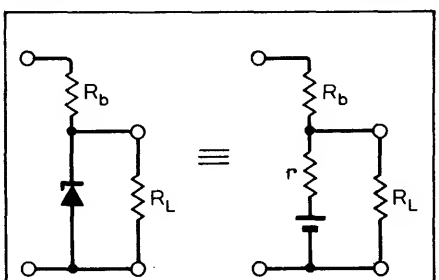


Fig. 3

Fig. 3. For changes in the supply voltage, load current etc the constant e.m.f. may be suppressed e.g. for an input voltage change ΔV_S, the output voltage changes by

$$\left(\frac{\frac{rR_L}{r+R_L}}{Rb+\frac{rR_L}{r+R_L}}\right)\Delta V_S$$

Since $r \ll R_L$ and $r \ll R_b$ are reasonable assumptions for a correctly designed circuit, the result simplifies to $\Delta V_o/\Delta V_S \approx r/R_b$. Similarly the output resistance is $\approx r$.

Where the diode is used simply to produce a stable reference voltage, the load current can usually be arranged to be negligible, or at least reasonably constant. This leaves only supply voltage and temperature variations to be dealt with, though for high-stability designs ageing of the device may be equally important in bringing long-term drift. The two problems require different solutions.

The effect of supply voltage is determined by the circuit design, while temperature effects can be minimized by choosing the right diode. In some

cases the reference diode may have one or more forward-biased diodes added in series. By selecting as the reverse-biased diode, one with a breakdown voltage >7V, its positive drift can be balanced against the negative drift of the forward-biased diode(s). In the circuits of Figs 4 to 7 the single zener diode could be replaced with any such combination.

Though the diode has a low slope resistance its voltage stability will be ideal if fed from a constant current (Fig 4). A practical way of realizing this is to use a transistor with a fixed base-potential and large emitter resistor. Any variation in supply voltage causes only a small variation in the transistor current and hence a still smaller change in the output voltage. An extension of the method, the ring-of-two reference (Fig. 5) has two zener diodes each controlling the constancy of current fed to the other. In this and other related circuits the variation in output voltage due to supply charges can be reduced to a few tens of microvolts – generally far lower than the variation due to temperature changes.

Most i.c. voltage reference/regulator circuits are based on similar principles while exploiting the matched-characteristics of adjacent transistors as in Fig. 6. The transistors Tr_1 and Tr_2 comprise a current mirror forcing the zener diode current to equal the current in R_E, which in turn is closely defined by the zener voltage. Both circuits contain a positive feedback loop, clamped by the zener, but they are essentially bistable in nature i.e. all devices could remain non-conducting indefinitely. To inhibit this condition the resistor R_S (which can be very much greater than R_E) provides a starting current without significantly impairing the regulation.

Where the reference voltage is of an inconvenient value then a voltage amplifier may be added as in Fig. 7. Further advantages accrue from this approach. The current drawn from the diode is reduced to negligible proportions; the output current capability is increased without forcing the zener to operate at a high current; the output impedance is very low because of the shunt-derived negative feedback; the diode can be biased either from a separate supply, or from the amplifier output provided it is sufficiently greater than the zener voltage. This last method is of the same nature as those adopted in the circuits of Figs 5 and 6 viz that the zener voltage indirectly controls its own bias current. The stability can be extremely high, but the non-conducting state can also occur and may require a separate starting circuit.

Although zener diodes are the most common voltage reference units, they can be replaced by any element conforming to Fig. 2). Examples include forward-biased silicon diodes, assymetric voltage dependent resistors (down to 1V), forward and reverse biased

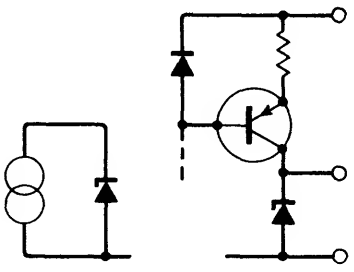


Fig. 4

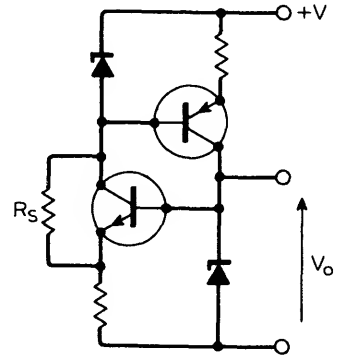


Fig. 5

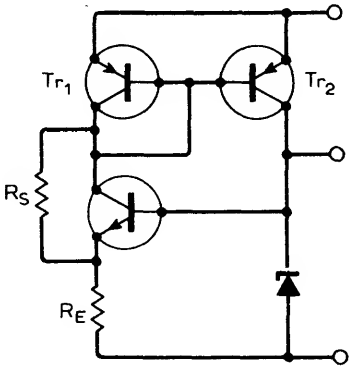


Fig. 6

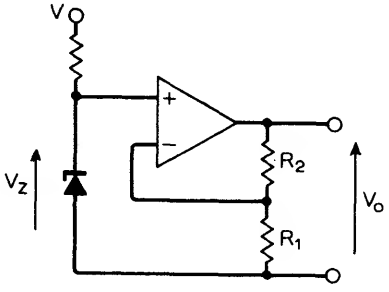


Fig. 7

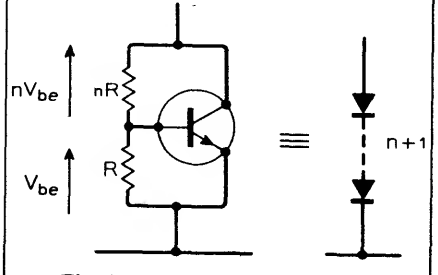


Fig. 8

junctions of transistors. A useful circuit where high stability can be sacrificed in exchange for flexibility is the amplified diode circuit of Fig. 8. If a transistor is biased by a potential divider between collector and emitter then under certain constraints, the terminal p.d. approximates to that of $(n+1)$ diodes in series. The current in the potential divider must be much greater than the transistor base current, but not much in excess of the collector current. Note that n need not be an integer and that by replacing the base-collector resistor with a variable control, we have a simple variable zener diode. The temperature drift is relatively large, about $+0.3\%K^{-1}$, but an overall stability of a few percent is readily achievable under laboratory conditions.

A completely different principle is embodied in the circuit of Fig. 9. While the V_{be} of a transistor falls as the temperature rises, ΔV_{be} between two identical transistors operated at different currents has a positive coefficient. The circuit, a much simplified form of that used in recent i.c. regulators, has a terminal p.d. of $V_{be}+n\Delta V_{be}$. A study of the transistor equations shows that this sum equals the energy-band gap of silicon at the point where the temperature drifts cancel. This voltage is about 1.23V and is scaled up by suitable amplifying circuits where required. The forward characteristics of devices can reasonly be expected to offer better long-term stabilities than in the breakdown region, and this principle is well-established in i.c. reference circuits of the highest ouality.

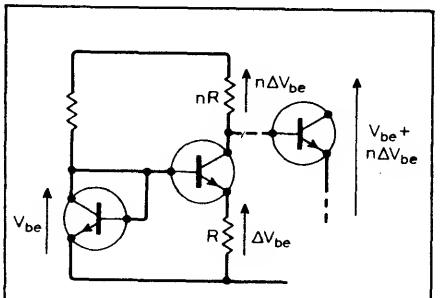
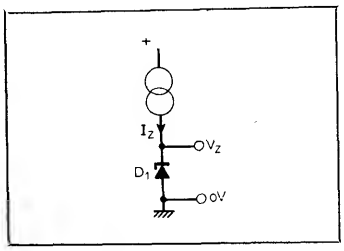
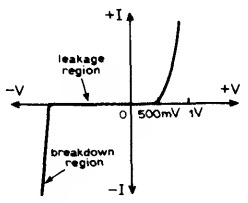


Fig. 9

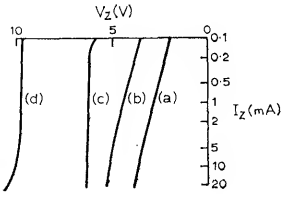
Zener diode characteristics



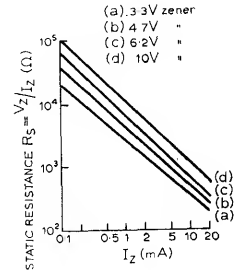
Performance (see graphs)
Constant current source: 0-20mA from commercial generator, ±0.05%.
V_Z measured with 5-digit d.v.m.
D_1 (a) BZX83C3V3
(b) BZX83C4V7
(c) BZX83C6V2
(d) BZX83C10.



Graph 1



Graph 2



Graph 3

Description

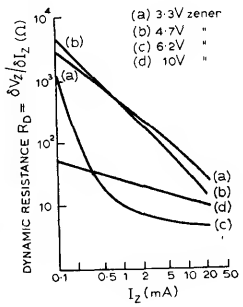
The zener diode exhibits three distinct regions: forward, leakage and breakdown. The forward-bias region is virtually identical with a normal diode, the forward-voltage temperature coefficient for a constant forward current being about −1.4 to −2.0mV/degC.
Under reverse bias, up to the breakdown region, a leakage current exists which, although being temperature dependent, is normally less than 1μA over the whole temperature range. When the reverse bias reaches some definite value, which depends on the p-n junction doping levels, the diode current rapidly increases and the breakdown or zener region has been reached. This region is the one used to provide a d.c. reference voltage by supplying the device from a constant-current source, as shown above left. At the onset of breakdown the resistance of the zener diode will be high but as the current increases the number of breakdown sites increases and the resistance falls to a small value. The reverse-breakdown characteristics for several zener diodes are shown at upper right, and their corresponding typical plots of static resistance as a function of zener current are shown lower right. The corresponding plots of slope or dynamic resistance are shown above, extreme left, The curves were obtained by setting I_z to a defined value and then reducing it instantaneously by 20% of the set value to obtain $R_D = \delta V_z/\delta I_z$. A sensitivity factor S of the dependence of zener voltage or current can be defined as $S=(\delta V_z/\delta I_z)/(V_z/I_z)$ and the reciprocal of S used as a figure of merit for the device ($F=1/S=R_S/R_D$), typical plots being as shown above, centre left. This figure of merit refers to the device only and will be degraded to a degree dependent on the circuit in which it is used and the zener current flowing. These figures may be used to assess the ability of the circuit to maintain a desired reference voltage against supply variations. Thus, if I_z changes by x% due to supply variation the reference voltage will change by approximately (x/F)% if the current source resistance is much larger than that of the zener diode. This would indicate the use of high-voltage supplies and high-voltage zener diodes operated at relatively low current levels. However, high voltages are not necessarily available and a compromise must normally be made between wasted volts and required stability of the reference voltage. Often the stability of the reference voltage against temperature changes is of prime importance and the choice of zener diode will depend on its temperature coefficient. Typical plots at room temperature are shown above centre right which indicate the use of diodes having a breakdown voltage of about 5V. Note that all these curves indicate that a positive temperature coefficient may be a distinct advantage as all the curves merge at a temperature coefficient exceeding about +4mV/degC. Thus a temperature-stable reference may be produced by replacing the single zener diode with a temperature-compensated reference unit consisting of the reverse-biased zener diode in series with n forward-biased normal diodes which exhibit a negative temperature coefficient of about 2mV/degC. If the zener diode has, for example, a temperature coefficient of +6mV/degC it could be series-connected with three forward-biased diodes.

Further reading

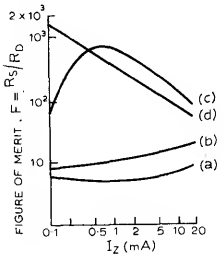
Patchett, G. N. Automatic Voltage Regulators and Stabilizers, 3rd edition, chapter 6, Pitman, 1970.
Buchanan, J. K. *et al.* Zener Diode Handbook, Motorola 1967.

Cross references

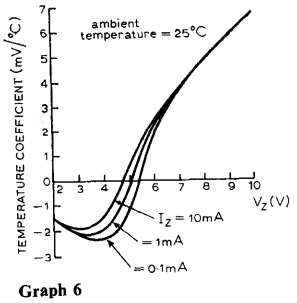
Set 23, cards 2, 3, 4



Graph 4



Graph 5



Graph 6

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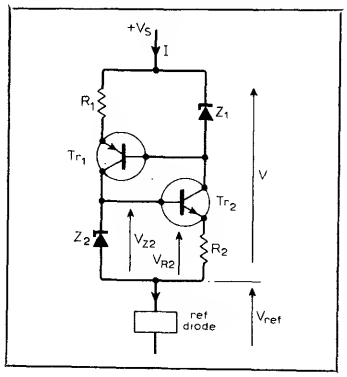
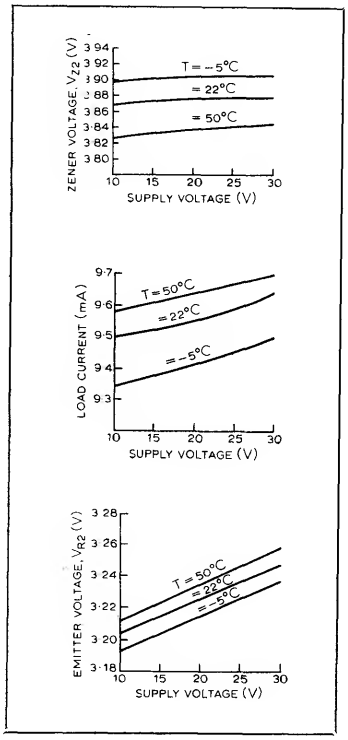
Williams ring-of-two reference



Typical data
Tr_1 BC126, Tr_2 BC125
Z_1, Z_2 BZY88 (3.9V)
R_1, R_2 680Ω
For test requirement, I was determined by measuring voltage across a standard resistance 50Ω±0.05% with a 5 digit voltmeter. Temperature levels obtained in a controlled oven.
Minimum $V_S \approx 10V$.

Circuit description
This circuit may be used to supply a constant current to a high capability reference diode, which is itself used as the voltage reference source. If it is assumed that diode Z_2 provides a constant voltage at the base of transistor Tr_2, then this forces a constant current to flow through the emitter resistor R_2. For reasonably high gain transistors, the collector-current will almost equal the emitter current, and hence the current through Z_1 will be constant. But this diode will maintain a constant potential at the base of transistor Tr_1, which in turn forces a constant current through R_1, Tr_1 to operate the original diode Z_2, which was initially assumed to provide a stable voltage. The total current drawn by the circuit is the sum of the collector currents and is substantially constant.
An increase in the supply voltage V_S largely appears between the collector and emitter of the transistors.
At 22°C, change in V_{Z2} 6.4mV
change in V_S 20V
Stability $\Delta V_S/\Delta V_Z \approx 3300$
At V_S=20V, ΔV_Z = +84mV for overall temperature change from 50°C to −5°C.
Temperature coefficient is −1.5mV/degC.

Note that the graph plots are obtained from a circuit using unselected diodes, and no attempt was made at temperature compensation.
Maximum supply voltage allowable will depend on permitted V_{CE} of transistors.
For V_S=20V, I=0.224mA for T=55°C.
$\Delta I/\Delta T \approx 4\mu A$/degC
At 22°C, ΔV_S=20V,
$\Delta I = 128\mu A$
$\Delta I/\Delta V_S \approx 4\mu A/V$
Percentage change ≈ +1.3%
Note. If self-starting difficulties arise, a resistor between bases or resistors across collector-emitter terminals may be used.



Circuit modifications
Stabilization ratio $\Delta V_S/\Delta V_z$ of 10^5: 1 is claimed for the circuit (Ferranti) using reverse biased base-emitter junctions of transistors ZTX303/300 as reference diodes. Tr_2 ZTX302, Tr_1 ZTX500. Circuit current 1mA for R_1, R_2 6.8kΩ. Supply range 14 to 25V.
The voltage reference circuit of Fig. 1 may provide a stability factor of the order of 10^6 for a voltage range of 20-40V.
Z_1, Z_2 6V planar zeners
Tr_1 2N3702, Tr_2 2N3820
Tr_3 2N3819, Tr_4 2N3707

Circuit Fig. 2 uses forward biased diodes as references to achieve a low voltage reference[2] Stability is maintained down to 1.1V supply.
Temperature change compensation is obtained by matching forward voltage drift on the silicon diode against that of base-emitter junction of germanium transistor. The circuit of Fig. 3 includes diode connected transistors to offset the base-emitter voltage variation with temperature[1]. As temperature also affects the transistor common emitter current gains, this effect is minimized by feeding these via op-amps[1]. Notice in Fig. 4 current feedback is to inverting inputs. Also slight variations in base current will still affect the collector currents. The use of junction f.e.ts in Fig. 5 reduces this dependence.

Further reading
Williams, P. Ring-of-two reference, *Wireless World*, July 1967. See also *Proc. IEEE*, January 1968.

References
1 Applied Ideas, *Electronic Engineering*, December 1974.
2 Williams, P. Low-voltage ring of two reference, *Electronic Engineering*, November 1967.
3 Ferranti E-Line Transistor Applications, June 1969.
4 Williams, P. D.C. reference voltage with very high rejection of supply variation, *Proc. IEEE*, January 1968.

Cross references
Set 23, card 1
Set 6, card 5

Fig. 1

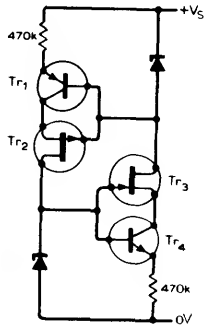


Fig. 2

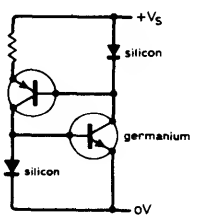


Fig. 3

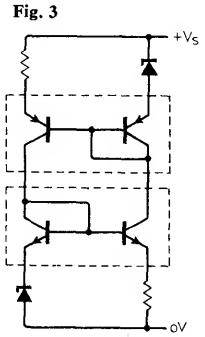


Fig. 4

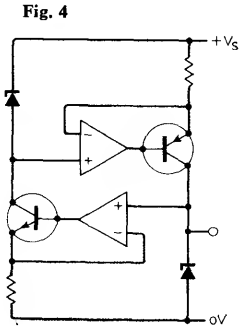
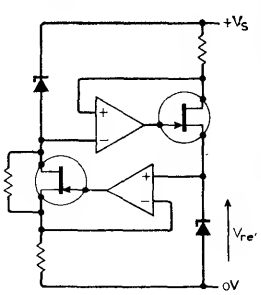
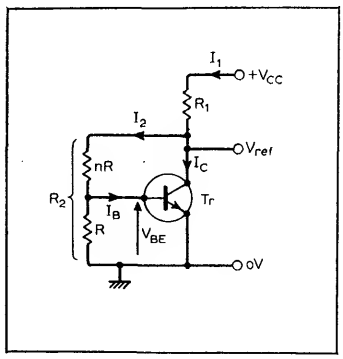


Fig. 5

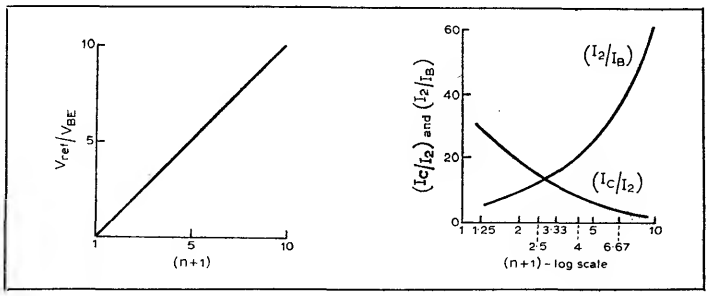


wireless world circard

Variable reference diodes



Typical performance
$+V_{cc}$ +15V
R_1 4.7kΩ±5%, R_2 10kΩ multiturn ±1%, linearity ±0.1%
Tr_1 BC125
Currents for $n=1$ condition
I_1 2.91mA, I_C 2.77mA
I_2 144.6μA, I_B 16μA
(see graph opposite)
Voltages for $n=1$ condition
V_{BE} 644mV, V_{REF} 1.371V
(see graph opposite)



Description
Although the zener diode is the most common device used to produce a stable reference voltage, may be replaced by any device, combination of devices or circuit that behaves as a two-terminal element having a stable p.d. across it and some internal resistance. Like the zener diode, such elements can normally only produce a definable, fixed reference. Many instances arise, especially under laboratory conditions, where a variable reference voltage is required and which has a range of required values that are not necessarily available from a single device or a combination of devices.
The circuit shown above left is an example of a simple d.c. reference which can often meet these requirements. If the transistor is assumed to have infinite current gain, I_B tends to zero, and the current I_2 in R_2 will produce p.ds across R and nR proportional to the current flowing. The p.d. across R is V_{BE}, which is dependent on the transistor current, and the p.d. across resistor nR will be n times that across R, i.e. nV_{BE}. Hence, the reference voltage will be $V_{BE}+nV_{BE}=(n+1)V_{BE}$. Since the factor $(n+1)$ cannot be less than unity the circuit is normally referred to as the amplified diode or the V_{BE} multiplier. In practice most commonly-available transistors have sufficiently high current gain to allow predictable performance. Departure from the ideal condition of $V_{REF}=(n+1)V_{BE}$ will occur at both high and low current levels, the first because I_B eventually becomes an appreciable part of the current in the bias resistors and the second because the collector current becomes a relatively small part of the total current and ceases to exercise control of the voltage. In most applications R will be held constant and nR will be a variable resistance used to set V_{REF} to the desired value. The major advantage of this circuit is that V_{REF} can be made almost any number of times greater than V_{BE} including non-integral values. The graphs shown overleaf show the linearity obtainable in practice between desired value of $(n+1)$ and actual value of (V_{REF}/V_{BE}) up to $(n+1)=10$. This graph was obtained by keeping R_2 fixed, by using a potentiometer, and varying the ratio of nR to R. The second graph overleaf shows the corresponding ratios of collector current to bias-chain current and bias-chain current to base current. Whilst the design aim should be to keep the bias-chain current much greater than the base current and the collector current much greater than the bias-chain current the last requirement is not nearly so important. The temperature dependence of V_{REF} is related to that of V_{BE} of Tr_1 which is typically −2mV/degC so V_{REF} will have a temperature coefficient of approximately $-2n$ mV/degC.
The current source to feed the amplified diode can be realized by a current mirror so that three transistors in an i.c. transistor array may be used. At the expense of raising the lower limit of V_{REF} a zener diode with a suitably chosen positive temperature coefficient can be included in series with the emitter as shown in Fig. 1. To provide a negative, variable reference voltage a p-n-p transistor and zener diode are connected as shown in Fig. 2. Circuits of the amplified diode type are available in monolithic, integrated circuit form which can be operated over a wide range of voltages and currents and which have a definable temperature coefficient. An example of this form is the General Electric D13V which is a combination of a Darlington-type transistor pair and a zener diode. The internal circuitry and normal connection arrangements are shown in Fig. 3.

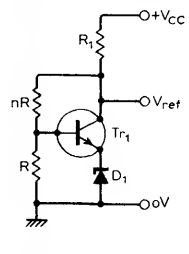


Fig. 1

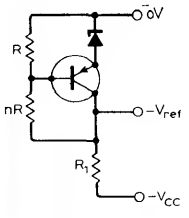
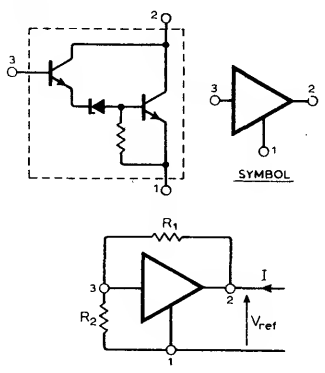


Fig. 2

Fig. 3

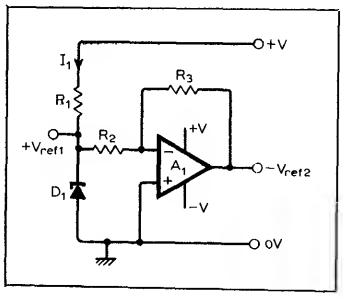


Further reading
Williams, P. The Amplified Diode, *Design Electronics* January 1968, pp. 32-4.
General Electric D13V data sheet, 1970.
Glogolja, M. Biasing circuit for the output stage of a power amplifier, *New Electronics*, 17 Sept. 1974, pp. 20 24.

Cross references
Set 6, card 4
Set 23, cards 1, 6
Set 7, card 8

wireless world circard

Bipolar references

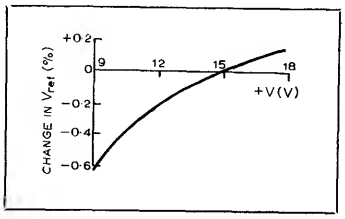


Typical performance
Supply ±15V, +3.4mA, −1.8mA
A_1 741, D_1 BZX830, 6.2V
R_1 4.7kΩ ±5%
R_2, R_3 22kΩ ±5%
I_1 1.94mA
V_{REF_1} V_z +6.16V
$-V_{REF_2}$ −6.20V

Circuit description
The reference element is the zener diode D_1, the basic reference circuit consisting of R_1 and D_1 in series, the current in D_1 being determined by R_1 for a given positive supply voltage. In the above arrangement the positive supply to the zener is, for, convenience, made the same as that provided for the operational amplifier A1. The reference voltage V_{REF_1}, which is positive and equal to the zener voltage, is fed to the inverting operational amplifier so that $V_{REF_2} = -V_{REF_1}R_3/R_2$. Thus, with $R_3 = R_2$, a simple bipolar reference circuit is obtained with outputs having the same voltage magnitude. In the experimental arrangement, the resistors were ±5% tolerance types which were not selected for equality resulting in $V_{REF_2} = -1.0065 V_{REF_1}$.
A close match between the reference voltages can be obtained by carefully matching R_2 and R_3. Note that whilst V_{REF_1} is fixed for a given zener diode and choice of supply and component values, $-V_{REF_2}$ may be varied over a wide range by adjusting the ratio R_3/R_2. However, the values of these resistors should not be so small as to appreciably load V_{REF_1}. The negative reference voltage output can be much more heavily loaded than the V_{REF_1} output, since the former is available from the low-output-resistance operational amplifier. The change in the values of the reference voltages with temperature changes are essentially due to the zener diode characteristics, since the operational amplifier drift is very small in comparison and with $R_3 = R_2$ the resistor temperature coefficients match to maintain a unity gain inversion of V_{REF_1}.

Circuit modifications
To allow the V_{REF_1} output to be more heavily loaded an operational amplifier voltage follower may be added to the basic circuit as shown in Fig. 1; this reference then being available from a low-output-resistance source.

Although this arrangement makes the current in the zener diode independent of the load currents taken from the V_{REF_1} and V_{REF_2}, the zener current is still subject to



variations in the positive supply rail voltage. Since an operational amplifier is a device which provides an output voltage that is inherently isolated from supply rail variations, the circuits above can be improved by supplying the direct voltage to R_1 from an operational amplifier instead of directly from the supply rail.
Irrespective of how the zener diode is supplied, its operating current may be more precisely defined and made independent of loading by placing the zener diode in the feedback path of an operational amplifier. This technique also allows the ability to provide a pair of opposite-polarity reference voltages having a summation equal to the zener voltage, including the particular case where they have equal magnitude. The basic form is shown in Fig. 2.
In this circuit R_1 again supplies the current to R_2 and R_3 as well as the zener diode current. Since the junction of R_2 and R_3 is a virtual earth, the output voltages are given by $V_{REF_1} = V_z R_2/(R_2 + R_3)$ and $V_{REF_2} = -V_z R_3/(R_2 + R_3)$ so with $R_2 = R_3$, $V_{REF_2} = -V_{REF_1} = V_z/2$. The operational amplifier must be capable of sinking all currents except the load current at the V_{REF_1} output. If the operational amplifier is to be an inexpensive type a transistor current booster can be added as shown in Fig. 3.
The operational amplifier now only has to supply the base current to Tr_1. Diode D_2 is included to ensure that the amplifier turns on correctly.
A complete bipolar reference circuit using booster transistors at each output and having the zener current supplied from an operational amplifier is shown in Fig. 4.
In this circuit the magnitude of each output is equal to V_z.
Typical component values are
±V ±15V, A_1, A_2 301A
Tr_1 2N3964, Tr_2 2N2222
D_1 1N829 (6.2 volt zener)
D_2, D_3 1N914, R_2, R_3 6.2kΩ
R_1 826Ω, R_4, R_5 300Ω
R_6 3.1kΩ

Further reading
Miller, W. D. & Defreitas, R. E. Op.amp. stabilizes zener diode in reference-voltage source, *Electronics* Feb. 20, 1975 pp. 101-5.

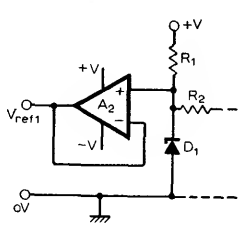


Fig. 1

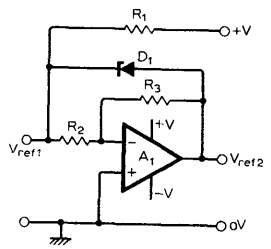


Fig. 2

Fig. 3

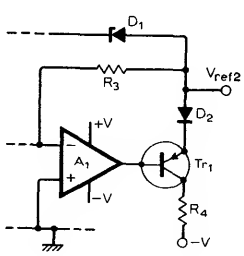
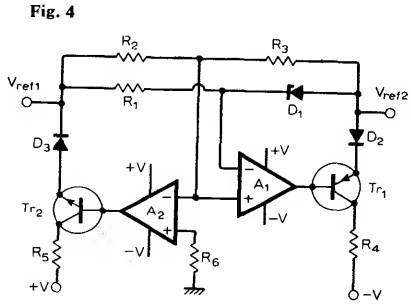
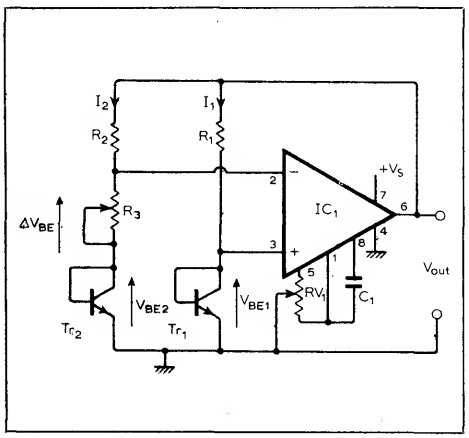


Fig. 4



Low temperature coefficient voltage reference



Typical data
Tr_1, Tr_2 Matched pair or $\frac{2}{5}$ CA3086
IC_1 CA3130AT
R_1 4.7kΩ, R_2 47kΩ
R_3 10kΩ (variable)
RV_1 100kΩ
C_1 1000pF
V_S +10V
At ambient temperature:
V_{out}=600mV+10.(26mV)(2.3)=1200mV

Circuit Description

Transistors Tr_1 and Tr_2 have identical parameters and hence similar saturation currents whose ratio is therefore temperature independent. The op-amp gain may be considered infinite and therefore the potentials of terminals 2 and 3 can be considered equal, for a finite output, V_{out}.

$V_{out}=V_{BE1}+I_2R_2$
$=V_{BE1}+\Delta V_{BE}R_2/R_3$

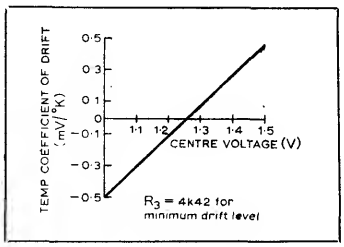
It is arranged by choice of R_1 and R_2, that I_1 is about ten times R_2.

Since $V_{BE}=(KT/q)\ln(I/I_S+1)$ and $V_{BE}=V_{BE1}-V_{BE2}$, then

$V_{out}=V_{BE1}+(R_2/R_3).(KT/q)\ln(I_1+I_{s1}/I_2+I_{s2}).I_{s2}/I_{s1}$
$=V_{BE1}+(R_2/R_3).(KT/q)\ln R_2/R_1$

because I_1/I_2 is in the ratio of R_2/R_1 and $I_{s2}=I_{s1}$. For $R_2/R_1=10$, then V_{out} is approximately defined at 1.2V at room temperature, for $R_2/R_3=10$. See typical data.

The base emitter junction voltage is also approximately given by $V_{go}-CT$ where V_{go} is gap energy voltage at 0 K and C is a constant. When the negative temperature coefficient of V_{BE1} and the positive temperature coefficient of the second term above, cancel, then $V_{out}=V_{go}$, and is then essentially temperature independent. Quoted value at 300K for V_{out} is 1.236V. Although the op-amp used in this circuit has temperature drift in excess of bipolar op-amp, it has the advantage of operating from a single-ended supply and provides the facility of strobing such that a pulsed output is clamped between 0V (due to the c.m.o.s. output stage) and the temperature independent reference level. Centre voltage is the value at ambient, adjusted by R_3. Temperature range imposed on transistor package was +70° to −30°. Minimum drift obtained at $V_{out}\approx 1.25$V.



Component changes

Supply voltage 10V-19V maximum. Change in V_{out}=0.75%.

Op-amp has heavy negative feedback and hence output impedance is low. This allows full current capability of op-amp to be drawn.

Typically
$I_{out}=0$, $V_{out}=1.251$V
$I_{out}=10$mA, $V_{out}=1.249$V
Maximum $I_{out}=22$mA.

Percentage sensitivity graph based on initial supply voltage $V_s=+9$V. Effective over load current range 0 to 20mA.

Bipolar-op-amp using positive and negative power supplies would improve overall drift, once offset is nulled.

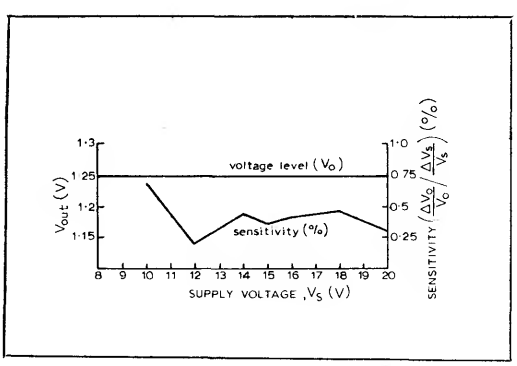
Increasing R_1 to 10k, R_2 to 100k demands R_3 increased to 9k to maintain same reference level: i.e. values not too critical provided same ratio maintained.

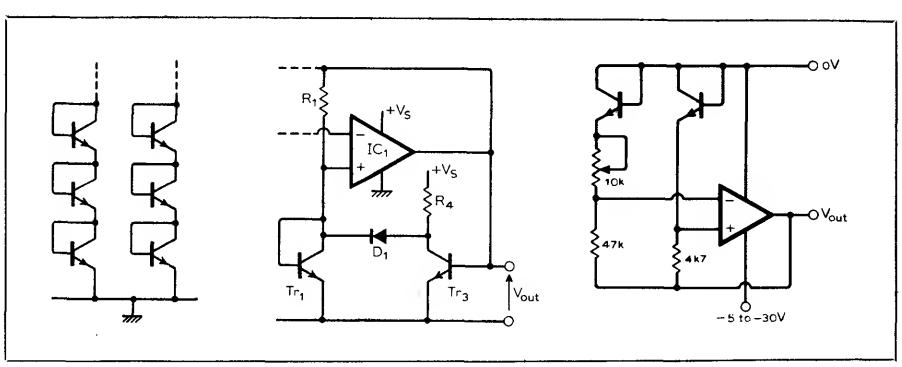
Circuit modification

Transistors can be series connected to increase available reference voltage—see middle e.g. eight diodes per chain will provide output ≈ 10V (Ref. 1). This will also allow a bipolar op-amp to be used from a single-ended supply because the inputs are held well above ground potential. Certain operational amplifiers will operate with inputs close to the most positive supply rail. This permits the dual configuration on diagram extreme right. V_{out} −1.25V. If self-starting difficulties occur the circuit shown middle right can be used. When the supply is switched on, the output of IC_1 may remain at zero volts and hence there is no supply for transistors Tr_1 and Tr_2. With the addition of diode D_1 and transistor Tr_3, D_1 will conduct if V_{out} is low and Tr_3 is therefore off. This means the collector of Tr_1 will rise and because it is connected to the non-inverting input of IC_1, V_{out} will then increase to bring transistor Tr_3 into conduction. Op-amp CA3130 has a strobe terminal which is connected to the gate of its c.m.o.s. inverter output stage. When this terminal is connected to V_S via an external gating network, e.g. $\frac{1}{3}$ CD4007, the pulsed reference facility is obtained.

Further reading

1. Kuijk, K. E. A precision reference voltage source. IEEE Journal of Solid State Circuits, Vol. SC-8, No. 3, June 1973.





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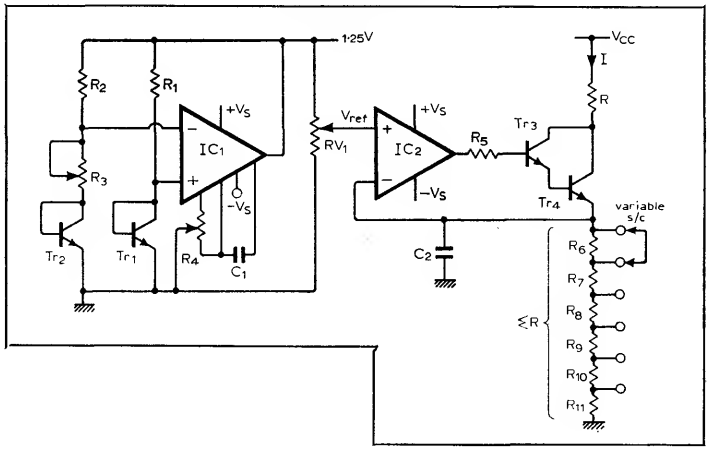
μA—mA/mV—V/calibrator



Typical data
Supply ±10V, IC_1 3130AT
IC_2 741, Tr_1 to Tr_4 use CA3086
R_1 4.7kΩ, R_2 47kΩ, R_3 10kΩ pot.
R_4 100kΩ, R_5 1kΩ, R_6 100kΩ
R_7 10kΩ, R_8 1kΩ, R_9 100Ω
R_{10} 10Ω, R_{11} 1.11Ω, RV_1 10kΩ
C_1 1nF, C_2 10μF tantalum
R variable load. For measurement, standard resistance used (±0.05%) and five digit digital voltmeter across R.
V_{ref} Adjusted for 1.000V

Fig. 1

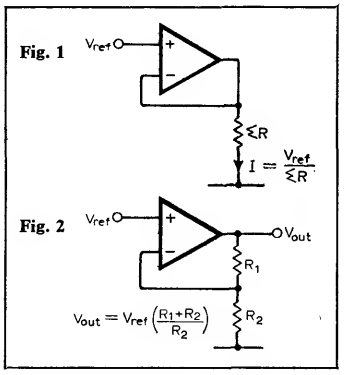
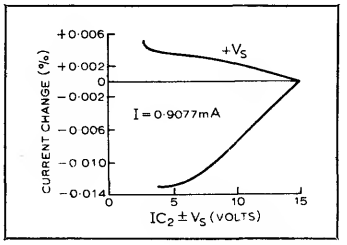
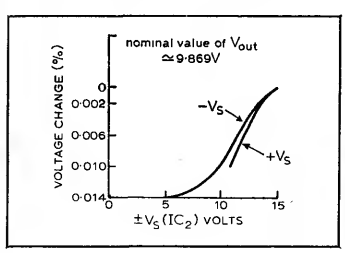


Fig. 2



Circuit description
When used as a current reference the circuit above simplifies to Fig. 1, and as a voltage reference, Fig. 2 shows the relationship between the output voltage and the input reference. The potential difference between the inverting and non-inverting inputs of IC_2 is very small for a high gain amplifier used in this negative feedback mode, and hence V_{ref} appears across the resistor chain R_6 to R_{11}. The current drawn from the V_{cc} supply depends on $V_{ref}/\Sigma R$, giving for the above values, a range from about 10μA to a safe maximum of 10mA (approx.) if R_6 - R_8 are shorted. Operation is such that if I did tend to increase, the voltage across ΣR increases, which would thus tend to increase the voltage applied to the non-inverting terminal of IC_2. This will reduce base drive to transistor Tr_3 and compensate for the assumed increase. Different values of current are achieved by varying RV_1 in association with varying the shorting points across ΣR.



Resistor R_{11} is chosen to provide an integer-multiplier for the voltage calibrator function. In this case the junction of R_6 and R_7 is connected to the inverting input of IC_2. This provides a ratio of exactly ×10 for the values chosen, and a case for 1% tolerance resistors is justifiable for an accurate source. Continuous variation of the output from 0-10V is available for this arrangement.

Component changes
Graph over indicates percentage current variation (100k and 10kΩ short-circuited) within ±0.01% for power supply variations of IC_2 up to 50% in ±V_S.
Range of V_S 3.5 to 20V for above setting. Minimum value depends on current required and load R.
Graph left shows change of output voltage for 30% change in ±V_S is within −0.01%.
Change in V_S of IC_2 changes power dissipation of its input transistors and hence changes chip temperature. This slightly alters offset voltage due to unbalanced heating of input pair.

Fig. 3

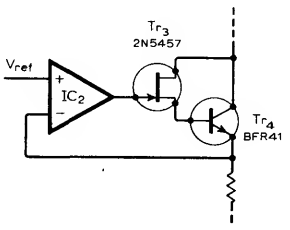


Fig. 5

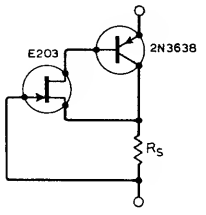
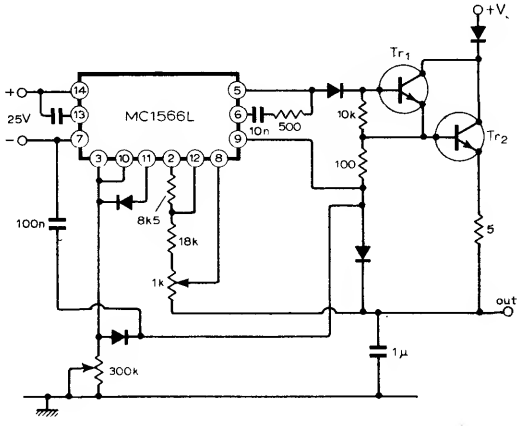


Fig. 4



Value of R_5 not critical because drive current is a small percentage of load current e.g. R_5 1kΩ, I_B 0.3μA, I_{LOAD} 10mA, R_5 100kΩ, I_B 0.365μA

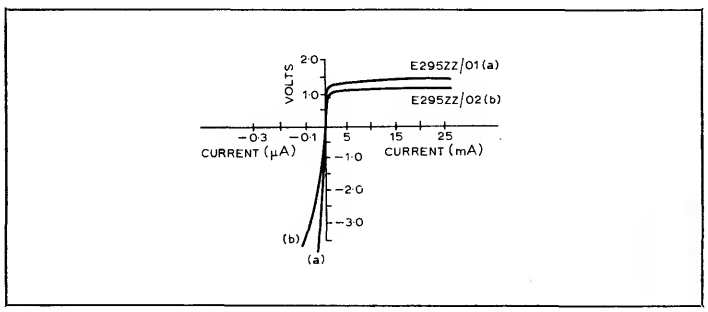
Circuit modifications
- Drive current error can be minimized by using a f.e.t./bipolar combination as Fig. 3. Current capability can be increased provided appropriate transistors used for Tr_3 Tr_4 combination e.g. Darlington package.
- IC MC1566L allows a variable constant current adjustable from 200μA to 100mA (depending on rating of output transistor Tr_2). A simpler current reference, programmed by resistor R_S, is shown right and uses a combination of bipolar p-n-p and n-type junction f.e.t. to provide a low cost arrangement with claimed drift better than 0.03%/degC at 20mA.

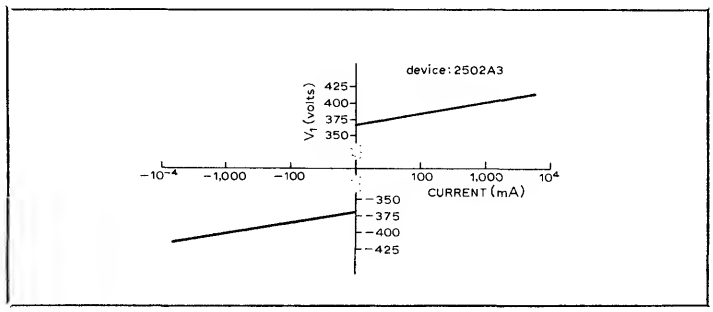
References
1. IC constant-current source at 750V, *Electronic Engineering*, May 1974.

Further reading
CA3130 Data Sheet 817, RCA.
Constant-current regulator 10m to 100mA, *Electronic Engineering*, July 1973.

Cross references
Set 23, cards 3, 5
Set 6, card 1

Non-zener device characteristics





1. Asymmetric voltage dependent resistors—low voltage

Non-linear resistors are made of certain polycrystalline materials having a voltage-current relationship given by

$V = CI^{\beta}$

where C and β are constants. This can be expressed as

$\log V = \beta \log I + \log C$

giving on log-log paper a straight line of slope β and intercept C.

In the case of asymmetric devices β and C change with current direction and a zener diode type characteristic can be obtained as shown above. The particular devices shown have knee voltages intermediate between that of zener diodes and that of Si or Ge diodes. The temperature coefficient of forward voltage for both these types is −0.2% per degC maximum.

2. Symmetrical voltage dependent resistors—high voltage

These devices have the same form of relationship as that of the asymmetric device but are essentially simpler in that C and β do not change with current direction. They are frequently used as transient suppressors or over voltage protection devices in high power systems but may be used to regulate supplies. They are also used in some control applications where the non-linear characteristic is used intentionally. The characteristics shown are those obtained for a Z502A3 metal-oxide varistor. The temperature stability is claimed to be excellent, our device at 500μA on test giving a temperature coefficient of −0.13mV per degC.

3. Semiconductor diodes

All semiconductor diodes are governed by the same form of exponential equation over a wide range of currents. Below is shown the characteristic curves that are obtained as a result of replotting current on a log. scale. The slopes differ according to the material used as do the approximate constant voltages obtained across the diodes when conduction starts. The voltage obtained falls in general by 60mV for each decade drop in current although falls of up to 120mV per decade of current can occur at very high or very low values of current. Again for semiconductor junctions the temperature drift is of the order of −2mV per degC, no matter the material, although this increases at lower current densities.

The range of voltages to be expected from Si diodes is 0.5 to 0.8V and from Ge diodes is 0.1 to 0.3V. Schottky diodes are intermediate.

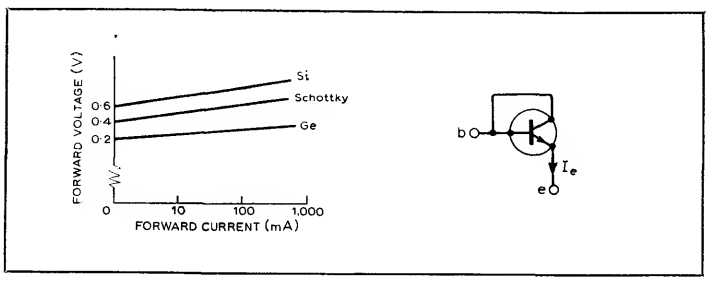
The diode connected transistor shown above will exhibit an exponential relationship between I_e and V_{be} over a much wider range of currents than is usual with simple diodes. The exponential relationship falls off at very low and very high currents due to loss of gain since basically it is I_e and V_{be} which are exponentially linked and the relationship between I_e and V_{be} being exponential depends on I_b being negligible.

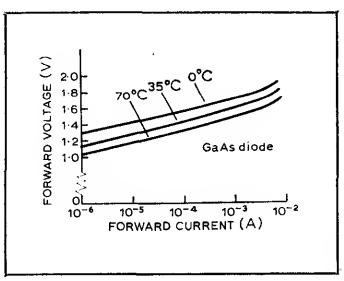
4. Light emitting diodes

Light emitting diodes are semiconductor diodes which tend to be used for their light emitting properties rather than for their other properties which are identical in form to those of any semiconductor diode.

They happen to have larger knee voltages than Si etc diodes, values in the range from 1.5V to 2.2V being common for medium current operation (several mA usually). This knee value is reduced by the normal 60mV per decade of current. Low current operation may extinguish the light but does not alter the simple exponential action. As before the temperature drift is −2mV per degC.

The graph shows the results from a GaAs l.e.d. Higher knee voltages are obtained with the other common l.e.d. material viz GaAsP.





wireless world circard

Set 23: Reference circuits—8

Compensated reference circuits

Fig. 1

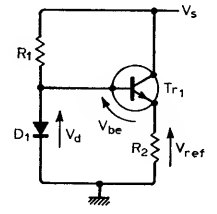


Fig.2(a)

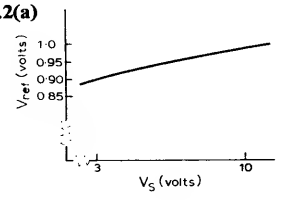


Fig.2(b)

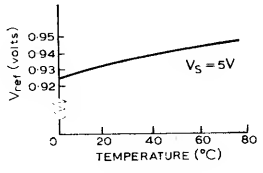
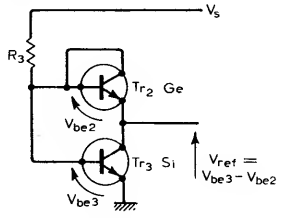


Fig. 3



Circuit 1

Components

R_1 470Ω, R_2 220Ω
Tr_1 BC125
D_1 5082-4850 (Hewlett Packard)
Performance—see graphs 1 and 2

Description

V_{ref} is given by $-V_{be}+V_d$ i.e. $-0.7+1.6=0.9$V to a first order approximately. The variation of V_{ref} with respect to supply voltage changes is shown in Fig.2(a). From this we observe a variation of approximately 10% in V_{ref} over the range shown so that compensation with respect to V_s is poor. The graph is approximately linear with slope +12mV per volt of V_s. Fig.2(b) shows the variation of V_{ref} with temperature, V_s being 5V. The graph is linear in the range shown with slope +0.27mV/degC. The variation of an independent p-n junction with temperature is approximately −2mV/degC. Clearly there is an element of temperature compensation involved, arising from the fact that V_{ref} is the difference in two junction voltages. In this case the effect of temperature variation on V_{be} is greater than the effect on V_d. For any junction the variation of junction voltage with temperature is dependent on the voltage itself and is approximately $+3\mu$V/degC for each change of +1mV. Hence, increasing the l.e.d. current and/or decreasing the transistor current could improve the drift due to temperature. This can be done by decreasing R_1 and/or increasing R_2.

Component changes

For any given V_s, R_1 and R_2 are not critical if only first-order temperature compensation is required. R_1 effectively controls the l.e.d. current since the transistor base current will be negligible and obviously R_1 should not be so high as to prevent l.e.d. conduction. Likewise R_2 carries the transistor current and should not be so low as to cause saturation of the transistor. Hence R_1 and R_2 are dictated by the particular l.e.d. and Tr_1 used.
Most l.e.ds and Si transistors will give the same reference voltage but if the transistor is replaced by a Ge transistor V_{ref} will become 1.3V approximately.

Circuit 2

The first circuit is not well compensated for supply voltage changes. In Fig. 3 Tr_2 is a Ge transistor and Tr_3 is a Si transistor and, hence, V_{ref} is approximately 0.4V—giving the circuit the added attraction of being a very low voltage reference. Ref. 1 quotes regulation 1% over supply current ranges of 100:1; the reason for this excellent regulation is that both transistors carry the same current so that the effects on V_{be} due to different currents (or different values of V_s) are the same for both transistors.
For the same reasons as before the circuit is also temperature compensated and indeed if the difference in the extrapolated band gaps at 0K is 0.43V complete temperature compensation is obtainable (Ref. 2). Achieving this requires selection of appropriate transistors.

Fig. 4

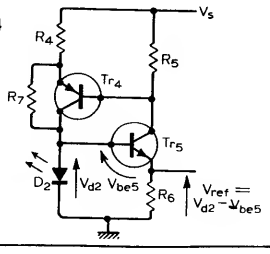
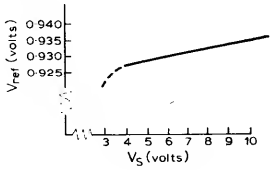


Fig. 5



Circuit 3

Components

R_4, R_6 220Ω
R_5 560Ω, R_6 22kΩ
Tr_4 BC126, Tr_5 BC125
D_2 5082-4850 (HP)

Performance

Fig. 5 shows the regulation achievable with this circuit viz 1.5mV per volt of V_s in the range 4 to 10V. For lower values of V_s saturation of the transistors occurs.

Description

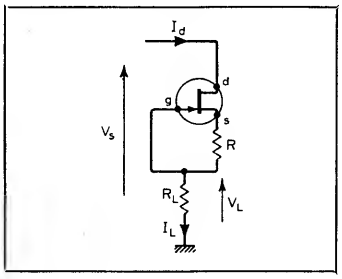
Fig. 4 shows a different approach to achieving simultaneous temperature compensation and supply voltage insensitivity. In this case the l.e.d. and transistor of Fig. 1 are incorporated in a ring-of-two reference circuit (Ref. 4). As in Fig. 1, V_{ref} is given by V_d-V_{be} so that similar ambient temperature compensation is effected. In addition however, the current through Tr_4 is largely independent of the supply voltage so that effects due to varying V_s are minimal. The action of the ring-of-two circuit is independent of V_s and is briefly as follows. Suppose D_2 is made to conduct (insured by presence of R_4 and R_7). Then V_{d_2} is approximately 1.6V and Tr_5 will conduct with V_{be} approximately 0.7V. The current in R_7 is, therefore, defined by $V_{d_2}-V_{be_5}$ and this current all flows through R_5 (ignoring base currents). This defines the voltage across R_5 and this voltage and the V_{be} of Tr_4 defines the current in R_4 which is the current in D_2 (ignoring current in R_7). Hence, once D_2 conducts the current through it is fixed and so are all the other currents. Hence $V_{d_2}-V_{be_5}$ is supply insensitive. Only the transistor collector-emitter voltages are supply dependent.

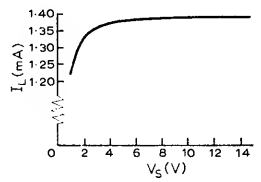
References

1 Very low voltage d.c. reference, P. Williams, *Electronic Engineering*, June 1968, pp. 348-349.
2 National Semiconductor LM311 voltage comparator data sheets.
3 Set 6, card 5

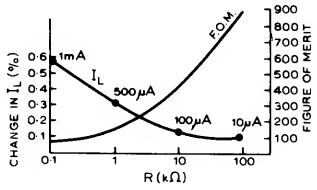
wireless world circard

Simple current reference

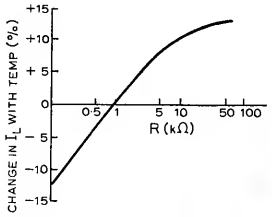




Graph 1



Graph 2



Graph 3

FET 2N5457

Performance

Graph 1 was obtained with $R_2 = 10\Omega$ and $R = 0$

Graph 2 was obtained with $R_2 \approx 1k\Omega$. V_s was set at 10V and I_L noted; V_s was then changed to 15V and the new I_L noted. From this was obtained the graph of % change in I_L for various values of R, the marked values of I_L on the graph being those at $V_s \approx 10V$. The figure of merit (f.o.m.) shown is defined as the slope resistance $\Delta V_s/\Delta I_L \div$ static resistance (V_s/I_L at $V_s = 10V$).

For a perfect current source this should be ∞ (see main text). As R increases the quiescent current I decreases but the f.o.m. increases, so we see clearly that the arrangement works best as a current source at low values of I_L. Note that from the graph of % change in I_L we can deduce the static and slope resistances which ranged from 8.1kΩ and 794kΩ to 1MΩ and 10^3MΩ respectively over the range of R shown.

Graph 3 shows the percentage change in I_L, as a result of a temperature change from −5°C to +70°C, for various R. This was obtained with $R_L = 1k\Omega$ and $V_s = 11.4V$ (a choice intended to produce 10V across R_L with $R = 0$, but of no material significance). In this respect it should be noted that although V_s is constant neither V_{dg} not V_L is constant because of the varying I_L. The main point, however, is that a temperature independent condition is achieved at approximately $R = 1k\Omega$ for the particular f.e.t. that we used. Whilst graph 3 shows the effect of a large temperature change, results were taken at intermediate temperatures. These indicated that to a first approximation, for any given R, the change in I_L is proportional to the change in temperature.

Circuit description

No matter the value of R, the gate current in a f.e.t. is negligible so that I_L and I_d can be equated. With $R = 0$ V_{gs} is zero and graph 1 is simply the normal f.e.t. characteristic for this value of V_{gs}. With increasing R more and more negative current feedback is used and consequently, the circuit behaves more like a current source with the ensuing drop in output as graph 2 shows.

Some explanation of the figure of merit used seems in order because some people use different figures of merit (Ref. 1 & 2) and notably slope resistance is at least implied as being all important. Consider Fig. 1 and the device characteristics shown, all passing through the same operating point, X. From this most people would agree that

OCD = perfect voltage source
OFG = imperfect voltage source
OAB = perfect current source
OHJ = imperfect current source
OE = indeterminate case.

From this we conclude that for a current source then (1) the slope resistance must be greater than the static resistance (HJ closer to horizontal than OE) (2) given 1 then the greater the slope resistance the better.

From this, one is tempted to conclude that slope resistance is all important. Consider, however, Fig. 2 where we have the same slope resistance but different static resistances at points P and Q. Is the device whose characteristic is ORPQ a better current source at P or at Q? At P we find that the angle between the given characteristic and the indeterminate case (OP) is β and clearly $\beta > \gamma$ i.e. at P we have a better current source. We could propose the figure of merit $(\alpha+\beta) \div \alpha$, which becomes larger as the device approaches a perfect current source but is rather devoid of meaning. However is we take tan $(\alpha+\beta) \div$ tan α we obtain the same overall picture with the merit that tan $(\alpha+\beta) \div$ tan = slope resistance ÷ static resistance. Since slope resistance and static resistance are meaningful we adopt this as our figure of merit. The inverse of this we would adopt for a voltage source since we want any f.o.m. to become bigger the more the source resembles a perfect source.

With regard to the temperature dependence of the circuit one should note that to a first order approx. the temperature independent condition is, in any f.e.t, obtained when $V_{gs} = V_p + 0.63$

For our circuit this can be achieved when

$$R = \frac{|V_p - 0.63|}{I_0} \times \frac{V_p^2}{0.63^2}$$

where V_p is the pinch-off voltage and $I_o = I_d$ when $V_{gs} = 0$. The usefulness of these formulae is restricted because of the large range of V_p and I_o quoted by the manufacturer for any device and the difficulty of measuring both for any single device. However, Graph 3 has been plotted over a very large range of R and consequently tends to exaggerate the effect of temperature.

References

1 I.R.C. zener diode handbook.
2 Motorola zener diode handbook.

Fig. 1

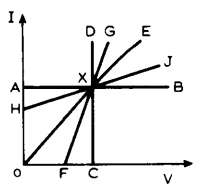
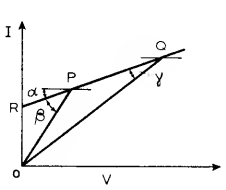


Fig. 2



Reference circuits

Fig. 1

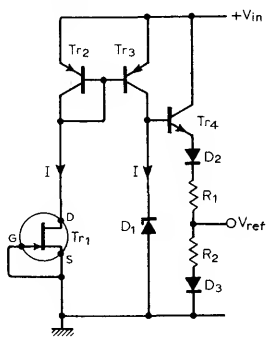
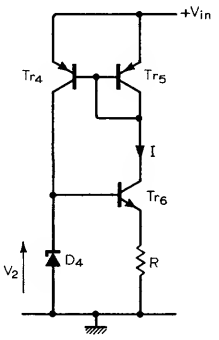


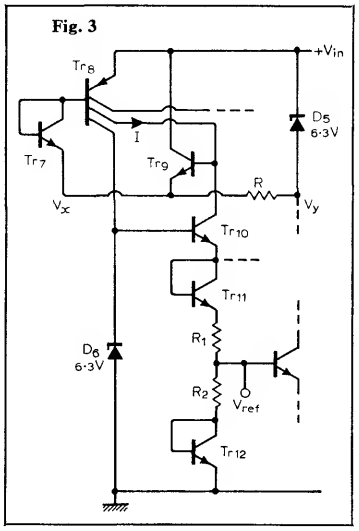
Fig. 2



Circuit description

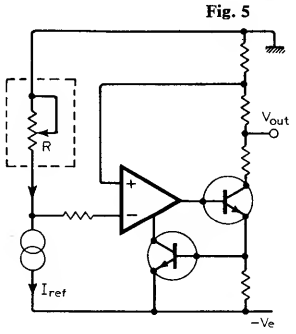
Internal reference circuits are based on the simpler voltage reference shown in Fig. 1, found in the low-cost LM376 voltage regulator. The self-starting technique used here employs a f.e.t. Tr_1, with gate-source connected to ensure a constant current from drain to source. Tr_1 will draw current initially via the base emitter-junctions of transistors Tr_2 and Tr_3. These transistors are therefore turned-on, and due to the current-mirror connection the current I through avalanche diode D_1 is defined, and hence its voltage. This turns on transistor Tr_4 and now produce a current through the D_2, R_1, R_2, D_3 chain. The circuit has no feedback loop, and an alternative is shown in Fig. 2. As it stands, this is not inherently self-starting, but with Tr_4 conducting, the voltage V_Z developed across avalanche diode D_4, will maintain a constant current through resistor R. The collector current I of Tr_6 is mirrored in the collector of Tr_4 again to maintain a constant current through D_4 thus completing the loop. This is shown more detailed in Fig. 3, reference circuit contained in the LM100 voltage regulator. The multi-collector transistor Tr_8 in conjunction with Tr_7, Tr_9 forms a closed loop. The V_{BE}'s of these transistors will be essentially similar, and their collector currents closely related, but dependent on relative collector area, but if one collector current is stabilized the others must be. If I is assumed to increase, the base drive of Tr_9 would increase and hence divert current away from Tr_7, since current through R is constant $(V_x - V_y)/R$. This would imply a reduction in the base current of Tr_8, which negates the original assumption. D_5 in association with $2V_{BE}$ drops across Tr_8, Tr_7 provide self-starting. The reference terminal can have a 0.1μF to ground to bypass possible noise from zener diode D_7. An alternative low impedance voltage reference point is available if the output and feedback terminal via a 2.2kΩ resistor. The internal circuit in principle is shown in Fig.4 where 5 and 6 are the base terminals of transistors connected as a long-tail pair. Diode connected transistors Tr_{11}, Tr_{12} and resistors R_1, R_2, R_3 provide a temperature compensation which is optimized to about 1.8V. Fig. 5 is a function block for the LM104 negative voltage regulator which uses an internal current reference network. An external 2.4kΩ resistor provides a current I_{REF} of 1mA. When this conducts through an external programming resistor R, the output voltage available is regulated up to zero volts.

Fig. 3



Type	Nominal ref. voltage (V)	Standby current (mA)	Temperature range (°C)	Input voltage range (V)	Temperature stability (%)
LM100	1.7	1	−55 to 125	8.5 to 40	0.3
LM300	1.7	1	0 to 70	8.5 to 30	0.3
LM305	1.7	0.8	0 to 70	8.5 to 50	0.3
LM304	—	1.7	0 to 70	−8 to −40	0.3
LM309	5	0.5	0 to 70	7 to 35	—
LM723	7.15	1.3	−55 to +125	9.5 to 40	coeff. 0.002%
LM723C	7.15	1.3	0 to 70	9.5 to 40	coeff. 0.003%
MC1723	7.15	2.3	0 to 75	9.5 to 40	coeff. 0.002%
MCC1463	−3.5V	—	0 to 75	up to −40	
MCC4060A	4.1	3.7	−10 to +75	9 to 38	coeff. 0.003%

Fig. 5



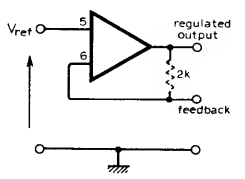


Fig. 4

If the output voltage is a linear function of temperature, then the temp-coefficient of voltage is a constant, and the total change in voltage (often called the stability) is the product of temperature coefficient and the total temperature change $dV = (\delta V/\delta T)dT$

The temperature coefficient of voltage changes with temperature because it results from a number of different sources of drift, and the actual $\delta V/\delta T$ at a given temperature might be greater or smaller than the average value implied by overall stability figure.

Further reading

Linear applications—National Semiconductor Corporation.
Linear Integrated Circuits—National Semiconductor Corporation.

Cross reference

Set 23, card 1.

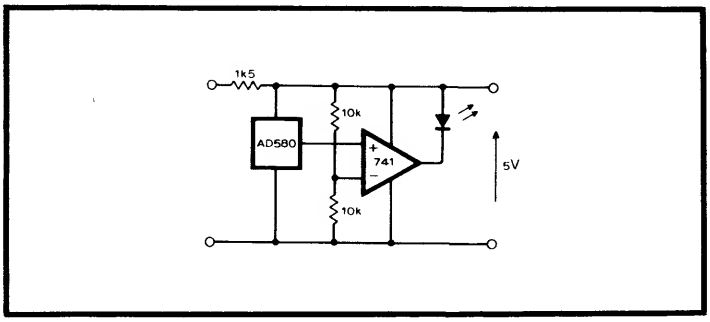
wireless world circard

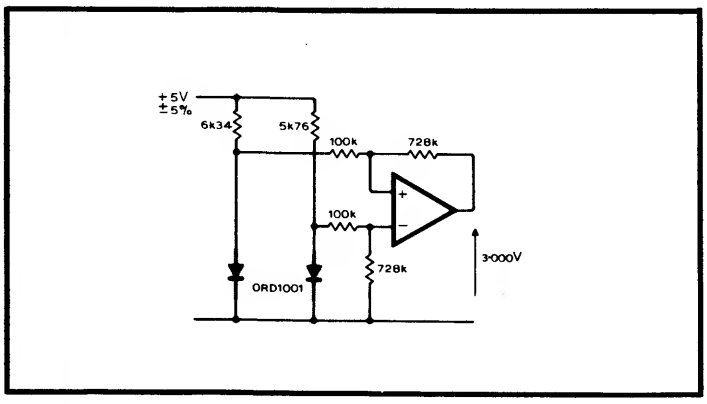
Set 23: Up-date

The strongest trend in reference designs in recent years has been that toward band-gap techniques. This is particularly true for low-voltage applications where zener diodes cannot be used. When dissimilar junctions or similar junctions with different current densities are used to generate a reference voltage, then temperature-independence is observed when that voltage is related to the band-gap voltages of the semiconductor materials. Two related approaches led to three-terminal reference elements as in the circuit shown or two-terminal devices such as LM113 or ZN423. These last-mentioned have a terminal voltage equal to the band-gap of silicon, about 1.2V. The three terminal devices can accept a wide range of input voltages with a fixed output voltage scaled up from the band-gap voltage internally. The output of the device shown is 2.5V but 5V and 10V versions have also been reported. The circuit shows a simple means of converting to other output voltages with the additional advantages that (i) both reference unit and amplifier are supplied from the stabilized output markedly reducing supply dependence (ii) visual indication is provided by the l.e.d. whose main purpose is to keep the op-amp output terminal within its linear range.

Reference

Jung, W. C. Programmable voltage reference is stable yet simple, *EDN*, Nov. 5, 1975, pp. 99/100.





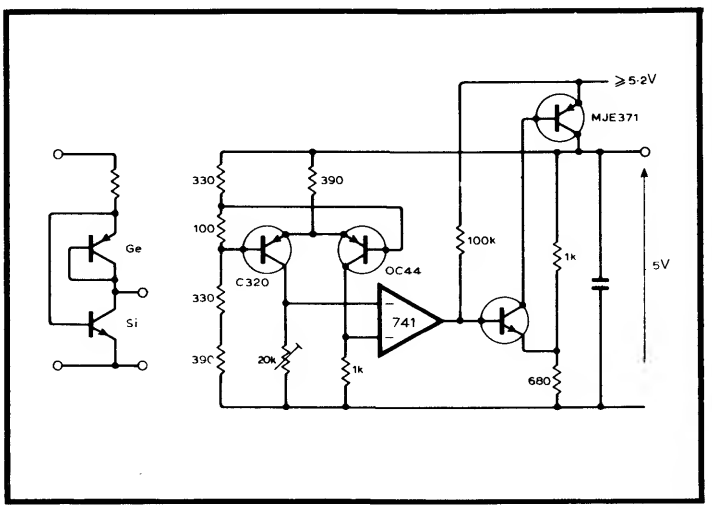
One special device that has been reported, contains a pair of silicon p-n junctions. One is so heavily doped that its band-gap voltage is reduced to that of germanium. The voltage difference is then temperature stable at around 0.41V, the difference between silicon and germanium band-gap voltages. The configuration of the circuit is not particularly novel, but the temperature coefficient is < 10p.p.m. K^{-1}, over the full military temperature range.

The Si-Ge band-gap circuit using only two transistors is the simplest capable of negligible variation against both supply and temperature changes. It requires a match between the Si and Ge transistors such that ΔV_{BE} equals the band-gap difference of ~ 0.43V. This is an acceptable limitation in return for its simplicity and very low voltage requirement (< 1V). If the transistor current densities can be adjusted then any pair of transistors can be used without prior matching. The circuit exploits this idea with the 20k potentiometer being adjusted to force 0.43V across the 100Ω resistor hence meeting the stability condition. Although the example shown is for a 5V output this can be reduced, and there is the further advantage that the temperature coefficient can be made either positive or negative as required by readjusting the current densities.

References

Verster, T. C. Regulated low-voltage power supply with controllable temperature coefficient, *Rev. Sci. Instrum.*, vol. 44, August 1973, pp. 1127/8.

Dubow, J. Low-voltage reference is ultra-stable, *Electronics*, Feb. 7, 1974, pp. 133/4.



Set 24 : Voltage regulators

This set covers integrated-circuit regulators with and without foldback on the one hand, and discrete-component series and shunt types on the other, but with some special cases in between. The exceptions are two dual-polarity circuits, a switching regulator and one using a current differencing or Norton amplifier.
On card 7 the field-effect transistor was wrongly drawn; page 56 shows the correct wiring, and on card 1 the last equation should have shown a product and not a difference.
Incidentally, on this set and others, unnumbered circuits on the bottom half of the page generally refer to items under circuit modifications and are in the same sequence as the text, unless made otherwise obvious.

Voltage regulators

The regulator is divided into the reference section and a d.c. power amplifier. These both require supply voltages; the convenience of having a single supply may outweigh the improved stability that can be obtained. The output current can cause the amplifier supply to vary: the source impedance including increased ripple if it is a rectified a.c. supply. Because the current required by the reference circuit is low and constant, it is easier to avoid any serious ripple/regulation effects. It is essential that the d.c. amplifier have (a) an accurately defined voltage gain, (b) a low output resistance, (c) a sufficiently high output current/voltage capability, (d) a temperature drift that is either low or of the appropriate sign and magnitude to compensate for any drift in the reference section.

A simple configuration that meets these requirements in principle is shown in Fig. 1 . The amplifier can be a standard operational amplifier if the output current is not much in excess of 10mA, and single-ended supply operation is permissible in many cases. The method is extended in Fig. 2 to the provision of output voltages that differ from the reference voltage. The output voltage is of opposite polarity to the reference voltage requiring a separate negative supply. The op-amp can be replaced by any circuit meeting conditions (a) to (d) above. Before turning to detailed study of possible configurations it is important to consider an alternative viewpoint.

A discrete component circuit that has all elements of a practical regulator is given in card 3. Three transistors comprise a voltage amplifier of gain (R_4/R_5+1) with high input- and low output-impedance (alternatively Tr_1, Tr_2 are the error amplifier and Tr_3 the series-pass transistor).

A serious problem arises in all regulators with emitter-follower outputs. The minimum input-output differential includes the V_{be} of Tr_3 plus the voltage-drop across R_2. This figure is markedly increased when Tr_3 is replaced by compound transistors for greater output current capability. This property has serious implications for the maximum efficiency of which the circuit is capable, and also for the maximum dissipation the output stage may be called on to tolerate.

A possible solution is to replace Tr_3 by a common-emitter p-n-p transistor, driving its base from the collector of Tr_1 to restore the feedback condition (Tr_3 would then be providing an additional inversion). A simplified form of the circuit for which this is not possible is shown in Fig. 3.) The effective reference voltage in this circuit is (V_z+V_{be}) and for best temperature stability, V_z would be chosen to have a drift of $+2mV\ K^{-1}$ to cancel the negative V_{be} drift. This circuit is the basis of a large number of commercial regulators, though the functional similarity may be hard to recognize amongst the welter of extra functions such as current limiting variable output voltage etc.

Although the basic form can be designed for output currents of 100mA+, any further increase forces the base current of Tr_2 too high – normally Tr_1 collector current has to be at least as great as the base current of Tr_2. It may not be convenient for the zener current to exceed about 10mA since the regulation is impaired. To keep the zener/error amplifier current low, it is sufficient to replace the output stage by a pair of transistors connected to give increased current gain.

A major problem in the design of voltage regulators is to protect against load resistances falling below specified levels, and the size and cost of transistors, heatsinks and power supplies is dictated by the occasional fault condition rather than by the ratings into any intended value of load. For this reason the technique described as foldback or re-entrant current limiting was devised. The resulting characteristic is shown in Fig. 4(b), with the current falling back to a short-circuit value close to zero as the short-circuit condition is approached. The technique involves a current-limit reference voltage which depends on the output voltage. As soon as the current-limit circuit is activated the output voltage begins to fall simultaneously reducing the current as shown.

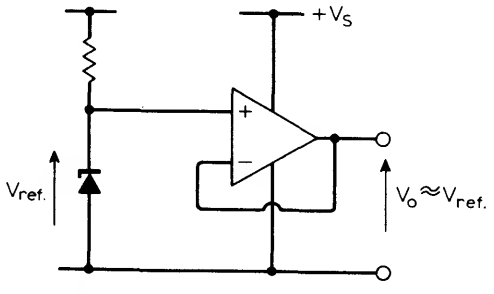


Fig. 1

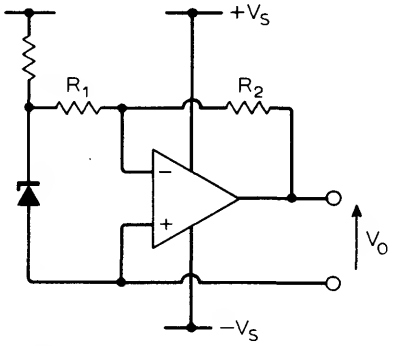


Fig.2

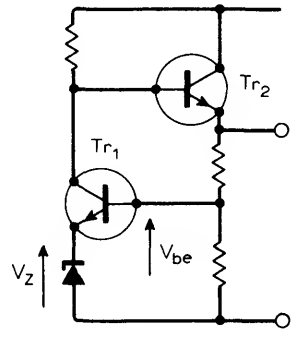


Fig.3

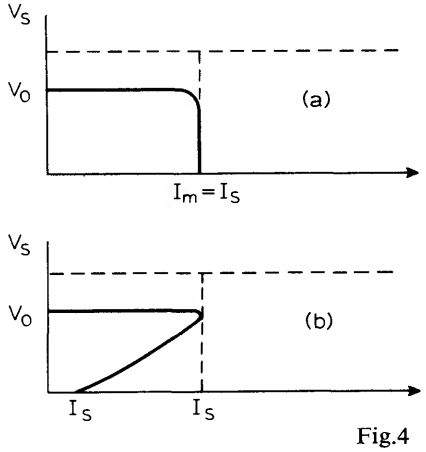


Fig.4

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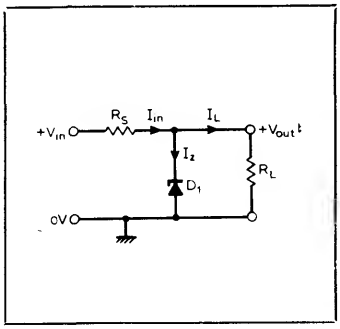
Zener diode shunt regulator



Typical performance
$I_L$constant, V_{IN}variable
D_1 BZY96C9V, I_L 50mA
$V_{IN(min)}$ 12V, $V_{IN(max)}$ 18V
R_S 54Ω (39Ω+15Ω)
R_L 195Ω (3×56Ω+27Ω) to set I_L at 50mA

Measured results

V_{IN}(V)	V_{OUT}(V)	I_L(mA)	I_Z(mA)	P_Z(W)
12	9.16	48	1	0.009
15	9.49	49	48	0.46
18	9.72	50.5	106.5	1.03

Typical performance
V_{IN}constant, $I_L$variable
D_1 BZY96C9V, V_{IN} 15V
$I_{L(max)}$ 100mA, $I_{L(min)}$ 80mA
R_S 39Ω+15Ω
R_L 95Ω to set I_L at 100mA
R_L 124Ω to set I_L at 80mA

Measured results

I_L(mA)	V_{OUT}(V)	I_Z(mA)	P_Z(mW)
102	9.27	7	64.9
80	9.56	26	248.6

Description
A voltage regulator should ideally provide a form of buffer action which makes its output voltage independent of changes that occur in its input voltage or its load current. The extent to which a particular regulator circuit approaches this ideal usually depends on the complexity of the electronic regulation element used. The simplest form of electronic shunt regulation element is the zener diode which may be considered to consist of an internal reference voltage source (V_Z) in series with an internal resistance (r_z), both of which have values that depend on the operating point and junction temperature.
The basic form of a zener diode shunt regulator is shown above where the input voltage must be larger than the required regulated output voltage. The input voltage will often be derived from the a.c. mains by rectification and will have a value that varies with mains input voltage and with load current, due to imperfect power supply regulation. The current in R_S is the sum of the load current (I_L) and the zener diode current (I_Z). If V_{IN} increases, the current in the zener diode and the load increases. But at the same time, a shift occurs in the zener diode operating point causing its internal resistance to fall. Thus the combined effects of the increase in I_Z and the decrease in r_z tends to maintain the output voltage at its former value. Similar but opposite effects occur if V_{IN} decreases. Ability of the circuit to maintain the output voltage depends on the zener resistance and on the temperature coefficient of the zener voltage. The output voltage will not, in general, be equal to the nominal zener voltage because V_Z and r_z have values that depend on I_Z and junction temperature.
In some applications the load current may be virtually constant and in others it may vary over a wide range. If the load current decreases, the current shunted by the zener diode will increase, and vice versa, resulting in a substantially constant output voltage.
Protection against excessive load current can be obtained with a fuse, but protection of the zener diode under light loading or open-circuit load conditions must be catered for by choosing a diode that can safely dissipate the power generated when $I_L \to 0$, if there is any possibility of the load being removed.
The design of this shunt regulator therefore becomes a matter of determining the value of R_S and the maximum power dissipated in the zener diode under specified conditions of variable V_{IN} and/or variable I_L. Although more precise results can be obtained by measuring and plotting the zener diode characteristics, for all practical purposes the nominal value of V_Z can be used to approximate the value of V_{OUT} in order to determine the component values. The Kirchhof voltage equation for the circuit is

$$V_{IN} = I_{IN}.R_S + V_Z$$

$$\therefore R_S = (V_{IN} - V_Z)/(I_Z + I_L),$$

as $I_{IN} = I_Z + I_L$
and $I_Z = (V_{IN} - V_Z)/R_S - I_L$
and the diode dissipation is

$$P_Z = I_Z.V_Z = [(V_{IN} - V_Z)/R_S - I_L]\,V_Z$$

Determination of suitable values for R_S and $P_{Z(max)}$ depends on the specification. The value of R_s must be such that the zener current will not fall below some minimum value, $I_{Z(min)}$, required to keep the diode in the breakdown region so that V_Z is maintained. Minimum zener current occurs when V_{IN} is a minimum, V_Z is a maximum and I_L is a maximum, so that

$$R_S = \frac{V_{IN(min)} - V_{Z(max)}}{I_{Z(min)} + I_{L(max)}}$$

Using the nominal zener voltage V_Z and an empirical factor of 10% of $I_{L(max)}$ for $I_{Z(min)}$ gives

$$R_S = \frac{V_{IN(min)} - V_Z}{1.1 I_{L(max)}}$$

for the condition where either V_{IN} or both V_{IN} and I_L are variable. When only I_L is variable

$$R_S = \frac{V_{IN} - V_Z}{1.1 I_{L(max)}}$$

Having determined R_S, $P_{Z(max)}$ can be found from

$$\left[\left(\frac{V_{IN} - V_Z}{R_S}\right) - I_{L(min)}\right] V_Z$$

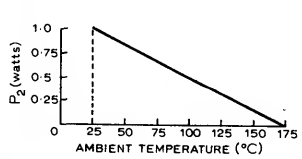
for constant V_{IN} and variable I_L.

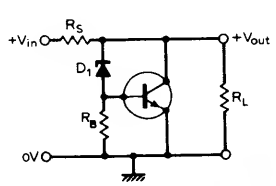
$$\left[\left(\frac{V_{IN(max)} - V_Z}{R_S}\right) - I_L\right] V_Z$$

for constant I_L and variable V_{IN}.

$$\left[\left(\frac{V_{IN(max)} - V_Z}{R_S}\right) - I_{L(min)}\right] V_Z$$

for I_L and V_{IN} variable.
A zener diode is then chosen having the desired nominal voltage and capable of safely dissipating this maximum power. It may be necessary to design a heat sink of suitable area and/or to derate the diode's dissipation capability as a function of ambient temperature. Most zener diodes are rated at a temperature of 25°C, a typical derating curve for a 1 watt diode being as shown on this card.
For increased power capability the zener diode can be connected in the base of a power transistor as shown.

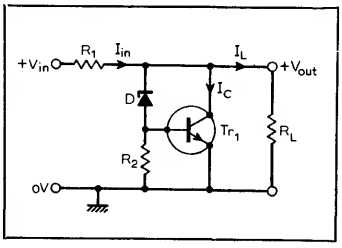




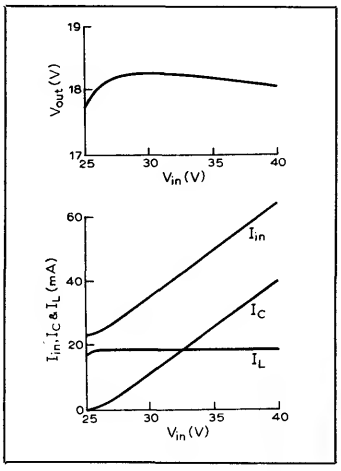
Further reading
Zener Diode Handbook, Motorola 1967.
Patchett, G. N. Automatic Voltage Regulators and Stabilizers, chapter 6, Pitman, 1970 (3rd edition).

Cross references
Set 23, card 1.
Set 24, cards 3, 4.

Simple transistor regulators



Typical performance
Tr_1 BFR41, D_1 ESM18
R_1 330Ω, 3W; R_2 100Ω
R_L 1kΩ, ¼W
V_{IN} 32.5±7.5V
V_{OUT} see graphs opposite



Description
Although less efficient than series regulators, the shunt regulator is normally a simpler circuit and is useful where an existing supply is to be used to provide a lower-value regulated output voltage. A simple regulator is shown above which includes a zener diode reference-voltage element and a transistor, in shunt with the load, acting as the regulator element. Note that the circuit is simply a common-emitter d.c. amplifier. The value of R_2 is chosen to provide a current in D_1 that is greater than the minimum value required to maintain the zener diode in its breakdown region without exceeding the rated dissipation. Output voltage remains essentially constant because the transistor collector current changes as the input voltage and/or the load current changes, causing a corresponding change in the p.d. across R_1. Transistor Tr_1 must be chosen to accommodate the maximum dissipation that can occur under specified input voltage and load current variations, including open-circuit load if this is a possibility.

Fig. 1

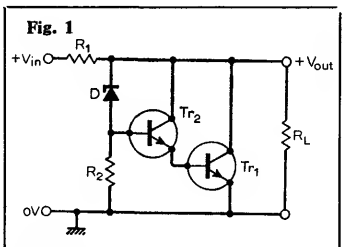


Fig. 2

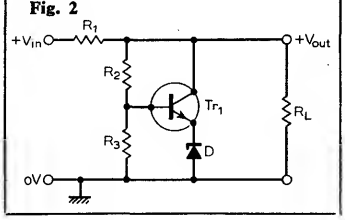
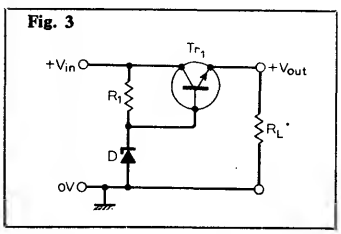
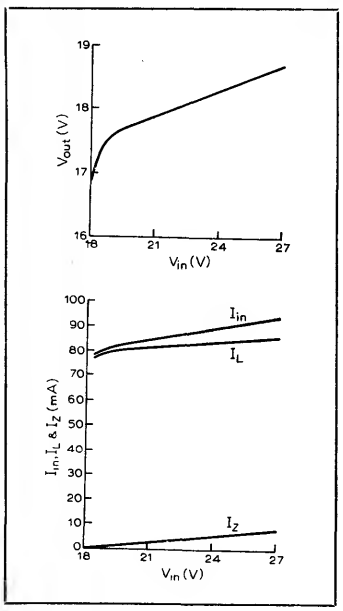


Fig. 3





Circuit modifications
To reduce changes in zener diode current, due to Tr_1 base current, cascaded transistors may be used to increase the current gain of the regulating element, as Fig. 1. The base current of Tr_2 is then only $\approx I_{B1}/h_{FE2}$ which can be made much smaller than the zener diode current by choice of R_2.
An alternative form of simple shunt regulator is Fig. 2 where the zener diode is in series with Tr_1 emitter.
A fraction of the output voltage $V_{OUT}R_3/(R_2+R_3)$ is compared with V_Z. If V_{OUT} increases the base potential rises causing an increase in collector and emitter currents and hence a larger p.d. across R_1 which tends to return V_{OUT} to its previous, lower value. The zener current is now the emitter current of Tr_1 which is much larger than the base current, and to make I_Z less dependent on I_E a resistor can be added between D_1 cathode and V_{OUT}. Note that V_{OUT} is now adjustable over a wide range, for a given zener voltage by choice of the ratio R_2: R_3.
The Fig. 3 circuit is a simple transistor series voltage regulator, i.e. the regulating element Tr_1 is in series with the load.
Note that the circuit is an emitter follower d.c. amplifier where ideally $V_{OUT}=V_Z$ but in practice $V_{OUT}=(V_Z-V_{BE})$.
If the output voltage tends to decrease due to changes in input voltage or load current, the base-emitter voltage of Tr_1 increases causing the transistor to feed a larger current to the load which will tend to restore V_{OUT} to its previous value. The current in the zener diode can be made much larger than the base current of Tr_1 by choice of R_1 and this current, hence V_Z and V_{OUT}, will be subject to variation as V_{IN} changes. The circuit is inherently safe with open-circuit loads but Tr_1 must be chosen to dissipate the maximum power generated under $V_{IN(max)}$ and $R_{L(min)}$ conditions.

Fig. 4

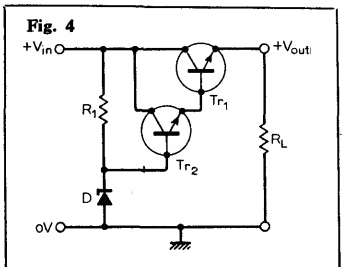
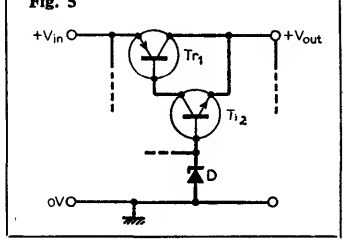


Fig. 5



Typical performance
Tr_1 BFR41, D_1 ESM18
R_1 1kΩ, ¼W; R_L 200Ω, 3W
V_{IN} 22.5±4.5V
V_{OUT} see graphs above
The variation of current in the zener diode with base current can be reduced by replacing Tr_1 by a Darlington pair as in Fig. 4, where the base current of Tr_2 is then only $I_L/[(1+h_{FE1})(1+h_{FE2})]$.
This principle can be extended to a number of emitter followers or a complementary pair may be used, Fig. 5, to keep $V_{OUT}=(V_Z-V_{BE})$.

Further reading
Patchett, G. N. Automatic voltage regulators and stabilizers, chapter 6, Pitman, 1970 (3rd edition).
Zener Diode Handbook—Motorola, chapter 6, 1967.

Cross references
Set 24, card 4.
Set 23, card 1.

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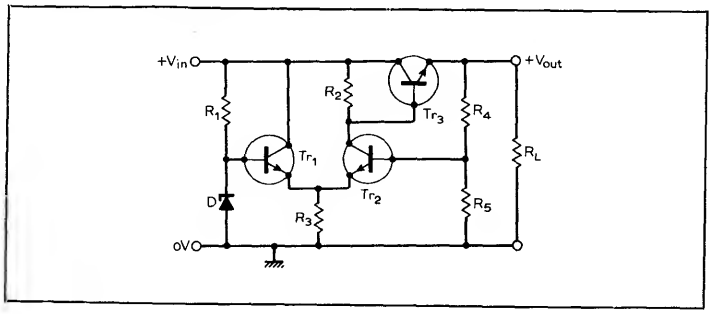
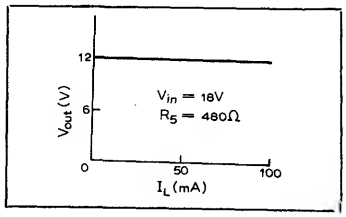
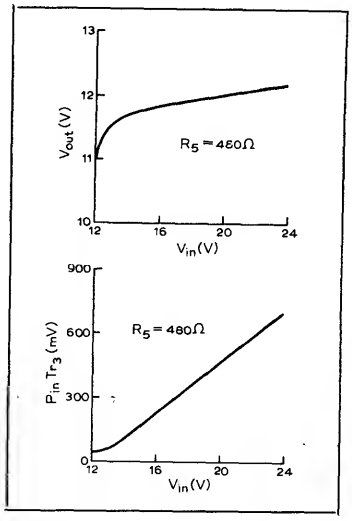
Feedback series regulators

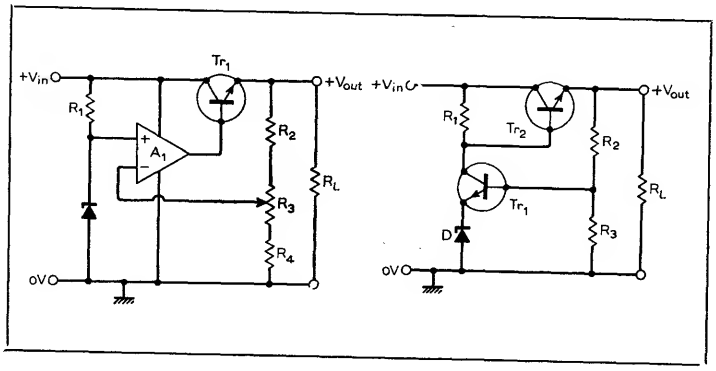


Typical performance
Tr_1, Tr_2 BC125 Tr_3 BFR41
D_1 BZY88C5V6
R_1 560Ω, R_2 1kΩ
R_3 220Ω, R_4 + R_5 1kΩ
R_L 250Ω 1W
V_{IN} 18V ±6V
V_{OUT} see graphs opposite





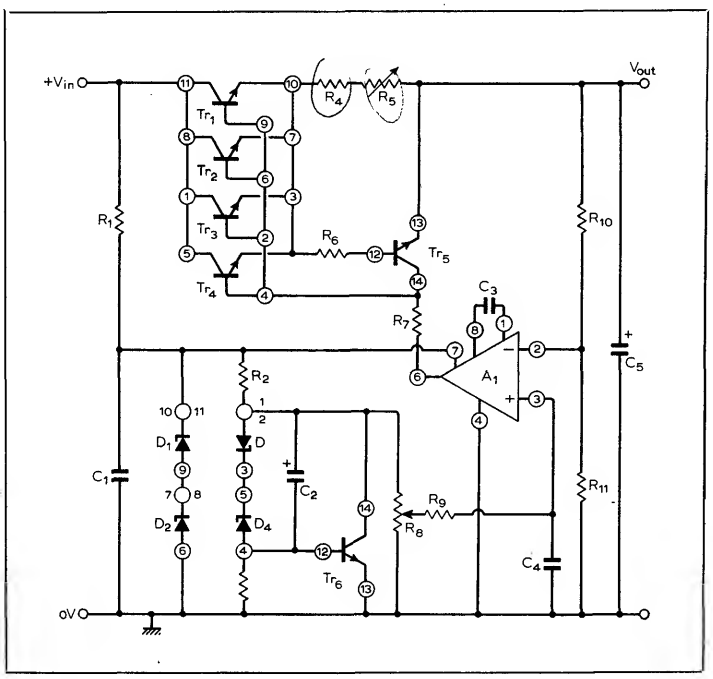
Long-tailed pair regulator
A very common type of feedback voltage regulator is shown above where the control amplifier is in the form of a long-tailed pair, or differential-input amplifier containing transistors Tr_1 and Tr_2. Resistor R_1 and D_1 act as a simple voltage reference circuit making Tr_1 base potential V_Z. The base potential of Tr_2 is a fraction of the output voltage, determined by the ratio of the resistors in the potential divider R_4 and R_5, so that the output voltage is continuously monitored. The output from the long-tailed pair is taken from Tr_2 collector and controls the base drive to the series transistor Tr_3 (an emitter follower). The differential amplifier attempts to keep its two inputs equal by altering the p.d. across the series transistor in order to hold the regulated output voltage constant despite changes that occur in the input voltage or load current. With a load current of 50mA, the circuit shown typically provides a load regulation of about 0.03% and a line regulation of approximately 0.5% for a ±20% change in V_{IN}.
For a fixed input voltage the output voltage may be varied conveniently by realizing R_4 and R_5 in the form of a potentiometer e.g. with $(R_4+R_5)=1k\Omega$ and R_5 varied over the range 100 to 900Ω. V_{OUT} may be varied over the range 16.86 to 6.4V.
Frequency stability is important in the design of feedback regulators. Because negative feedback is used in the control amplifier element, a total phase shift around the loop (including the series element) of 180° at high frequencies can result in oscillations unless the closed-loop gain is less than unity. Therefore, at the frequency where the total phase shift is 180°, provision should be made to reduce the closed-loop gain to less than unity. The use of shunt capacitance at the output, or elsewhere in the amplifier section produces the required gain "roll-off" with frequency. The degree of voltage stabilization depends mainly on the stability of the reference voltage, best results being obtained when Tr_1 and Tr_2 are a matched pair.
The differential-input amplifier is the basis of most operational amplifier designs so the long-tailed pair may be replaced by such an amplifier as shown below. In this arrangement the operational amplifier isolates the zener reference from load changes improving the load regulation. Potentiometer R_3 allows the output voltage to vary over a limited range. Typical performance is A_1 741, Tr_1 SE3035, D 1N4611, R_1 12kΩ, R_2, R_4 1.2kΩ, R_3 2.5kΩ. With V_{IN} of +30V, V_{OUT} may be varied over the range 9 to 25V with load currents up to 100mA. Output impedance is less than 0.1Ω. Useful minimum V_{IN} 20V.
Another type of feedback regulator in common use is the d.c. feedback pair shown below. In this circuit the effective reference voltage is V_Z+V_{BE} of Tr_1 and for best results, the temperature stability of the effective reference source should be optimized by choosing a zener diode that provides a temperature drift of approximately +2mV/degC to cancel the negative drift in the V_{BE} of Tr_1. In the basic form shown, load currents of up to about 100mA can be accommodated and for higher output currents Tr_2 can be replaced by a higher-current-gain transistor pair.



Further reading
English, M. Applications for fully compensated op.amp.i.c. *EEE*, January 1969, pp. 63-5.
Potted power, *Design Electronics*, January 1971, pp. 34/5.

Cross references
Set 24, cards 1, 4, 5, 6.
Set 23, card 3.
Set 20, cards 1, 2, 4, 10.

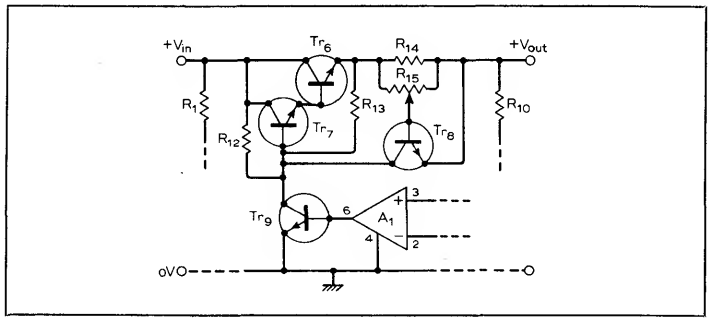
Bipolar/c.m.o.s. op-amp regulator



Typical performance
A_1 CA3130
Tr_1-Tr_6 1/5 × CA3086
D_1-D_4 1/5 × CA3086
R_1 390Ω, R_2 2.2kΩ, R_3 62kΩ
R_4 3Ω, R_5 R_6 R_7 1kΩ
R_8 50kΩ, R_9 100kΩ
R_{10} 20kΩ, R_{11} 30kΩ
C_1, C_4 10nF, C_2 25μF, 15V
C_3 56pF, C_5 5μF, 25V
With V_{IN} 20V, V_{OUT} variable in range 0 to 13.9V at I_L 40mA
Full load regulation <0.01%
Line regulation 0.02%/V
Standby current 8mA

Circuit description
The voltage regulator shown above uses three monolithic integrated circuits. A_1 is a bipolar-c.m.o.s. hybrid operational amplifier, Tr_1 to Tr_5 are contained within one bipolar array package, and D_1 to D_4 plus Tr_6 are contained in another identical package. Diodes D_1, D_2 and D_4 are bipolar transistors with collector and emitter strapped and operating in reverse bias in the breakdown region to serve as zener diodes having a zener voltage of about 7.3V. Diode D_3 is forward-biased and consists of a transistor in the same package with its collector and base strapped. Resistor R_1 and the series-connected zener diodes D_1 and D_2 act as a simple shunt regulator across the input to provide a regulated supply of $2V_Z$ for the CA3130 operational amplifier. The output from this part of the circuit also serves as a pre-regulated input to the low-impedance, temperature-compensated voltage reference source consisting of R_2, D_3, D_4, R_3 and Tr_6—the diodes and transistor being part of the same monolithic structure. The output from this reference source is taken to the non-inverting input of the error amplifier via potentiometer R_8 which allows the amplifier's reference to be varied continuously over the range 0V to about 8.3V allowing the output voltage to be controlled over the range 0V to about 13.9V. A fraction of the output voltage is fed to the inverting input of the error amplifier by means of the potential divider R_{10} and R_{11}.
Transistors Tr_1 to Tr_4 are contained in a single integrated circuit package and are all connected in parallel to act as an equivalent series transistor (emitter follower) which is capable of handling the full-load current, when driven from the output of the error amplifier. Transistor Tr_5 (in the same package) in conjunction with R_4, R_5 and R_6 serves as a current limiting device. If the load current increases the p.d. across R_4+R_5 increases and since the base voltage of Tr_5 is held at approximately 600mV above V_{OUT} the base current to Tr_5 through R_6 increases. Hence the collector current of Tr_5 increases, diverting the base current from the series pass transistors. Thus the collector currents of these transistors, and hence the load current, falls back to its previous value. The value of load current at which the current limit becomes operative is set by R_5, the maximum limited current being determined by R_4, a 3-Ω resistor. Capacitor C_3 provides compensation for the operational amplifier the other capacitors serving to remove residual hum at the input and to control the closed-loop gain of the amplifier at high frequencies.

Modification
Careful layout of the printed circuit is essential otherwise the circuit may oscillate.
This form of circuit may be modified to provide output voltages in the range 100mV to 50V at currents up to 1A with a 55V input by making the following changes. R_1 is increased to 4.3kΩ, 1W and a 1kΩ resistor connected between D_4 anode and Tr_6 base; otherwise the pre-regulator and voltage reference circuits are basically unchanged. The sliding contact of R_8 is connected directly to the inverting input of A_1. R_9 is omitted along with C_4 and the compensation capacitor C_3 is increased to 1nF. R_{10} and R_{11} are changed to 43kΩ and 8.2kΩ respectively, and their junction taken to the non-inverting input of A_1. This inversion of the inputs to A_1 is required because of the addition of an inverting current-boosting stage at the output of A_1 as shown. Darlington-connected series transistors Tr_6 and Tr_7 replace Tr_1 to Tr_4 and Tr_8 provides current limiting by adjustment of R_{15}.

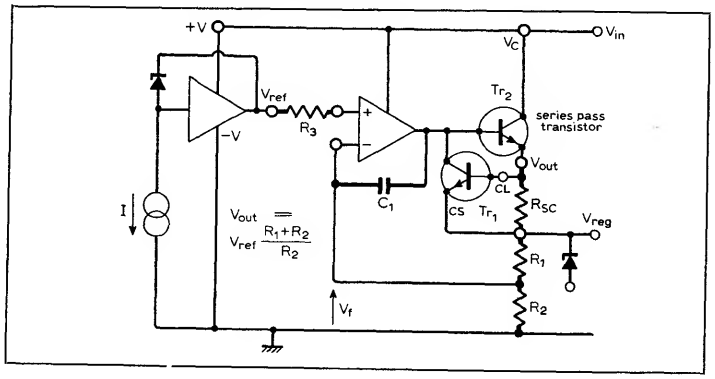


Typical components are
Tr_6 2N3055, Tr_7, Tr_9 2N2102
Tr_8 2N5294, R_{12} 3.3kΩ, 1W
R_{13} 1kΩ, R_{14} 1Ω, R_{15} 10kΩ
C_1, C_5 100μF, C_2 5μF
Full load regulation 0.05%
Line regulation 0.01%/V

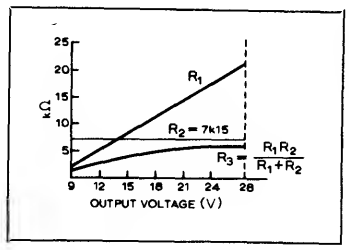
Cross references
Set 24, cards 1, 2, 3, 5, 6.
Set 23, card 3.
Set 20, cards 1, 2.

Further reading
Solid State Datasheet, RCA no. 817 (CA3130), 1974.
Solid State Databook, SSD–201B, RCA, 1974, pp. 183–8.

Monolithic regulators—1



Typical data
IC μA723C or LM723C
Temperature range 0 to 70°C
Line regulation for V_{IN} 12 to 40V 0.1%. For 12-15V, 0.01%
Load regulation 0.03% for 1 to 50mA current range
R_1 7.87kΩ ±5%
R_2 7.15kΩ ±5%
V_{REG} +12V, C_1 100pF
Ripple rejection 74dB
Temp. coeff. of 0.003%/degC
V_{ref} 7.15V
Standby current 2.3mA for V_{IN} 30V
Input voltage range 9.5 to 40V
Output voltage range 7 to 37V



Circuit description
The schematic diagram of this regulator package is shown above, with the external components for a high voltage regulator circuit. The series-pass transistor is connected as an emitter-follower, and the amount of feedback to the internal operational-amplifier is defined by R_1 and R_2. V_f is approximately equal to V_{REF} because the differential input to the op-amp is very small, and hence, as $R_{SC} \ll R_1$ or R_2.
$V_{OUT} = V_{REF}(R_1+R_2)/R_2$
i.e. the emitter of the series-pass transistor is constrained to be a multiple of V_{REF}. Therefore, if the unregulated input V_{IN} increases, this increase must be absorbed by an increase in the collector-emitter voltage of series transistor. Conceptually, if the emitter potential tends to increase, then V_f to the inverting input would increase, which would cause a decrease in potential at the base of the series transistor, and due to emitter-follower action, this opposes the assumed increase.
Load regulation. Percentage change in output voltage for a specified load current change.
Line regulation. Percentage change in output voltage for a defined change in input voltage.
Note—above are defined for a constant junction temp.
Ripple rejection. Ratio of pk-pk input ripple voltage to pk-pk output ripple voltage.
Input-output differential. Working range of regulator based on difference between supply and regulated voltage.
Standby current. Current drain for no load on output or reference.
Note—regulation is sometimes defined on basis of a percentage change in input.
Fig. 1 is a low-voltage arrangement suitable for a 2 to 7V output voltage range
$V_{OUT} = V_{REF}R_2/(R_1+R_2)$
For V_{REG} of +5V, R_1 2.15kΩ, R_2 4.99kΩ, R_3 1.5kΩ.
Fig. 2 provides a negative regulated voltage suitable for a −9V to −28V range.
Typically V_{REG} −15V, R_1 3.65kΩ, R_2 11.5kΩ, R_3 R_4 3kΩ, R_5 2kΩ, Tr_3 2N4898.
An extension to −6V is possible but V^+ must be at +3V minimum.
Fig. 3 is similar to Fig. 1 but permits a remote shutdown facility via a logic source.
Current limiting and sensing depends on the value of R_{SC}. When the load current is large enough to cause the potential between C_L and C_S to turn on the related transistor, this removes drive current from Tr_1 to limit any further increase in output current.
Curves above show typical load regulation and current limiting characteristics for V_{OUT} 5V, R_{SC} 10Ω, V_{IN} +12V.

Further reading
Hinatek, E. R. Users Handbook of Integrated Circuits, Wiley, 1973.
μA723 The Universal Voltage Regulator, Fairchild.

Fig. 1

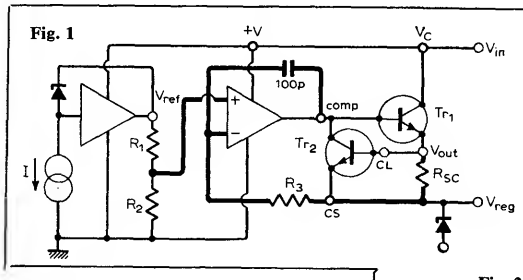
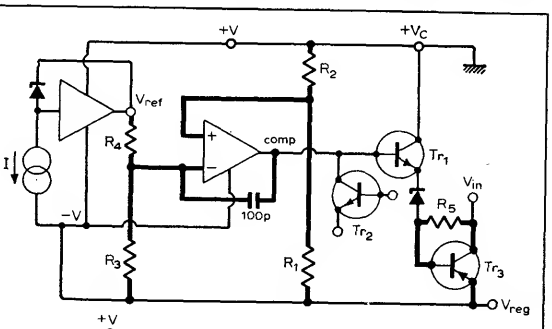


Fig. 2



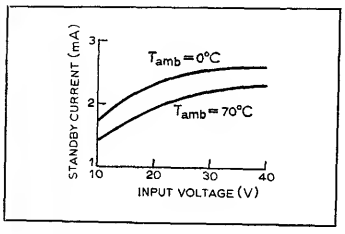
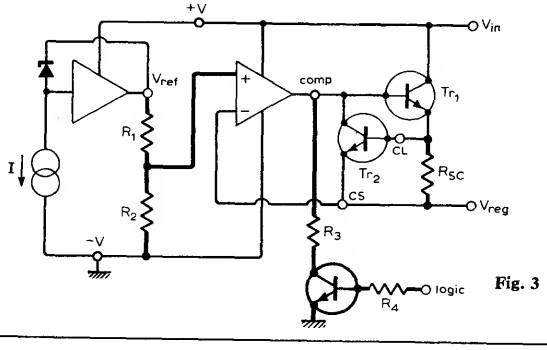
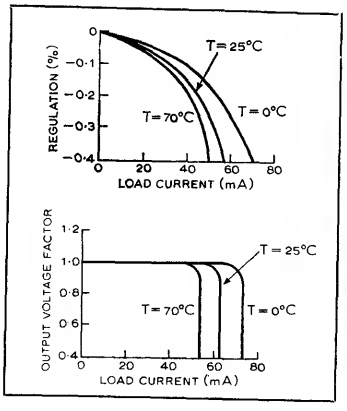


Fig. 3





Monolithic regulators—2

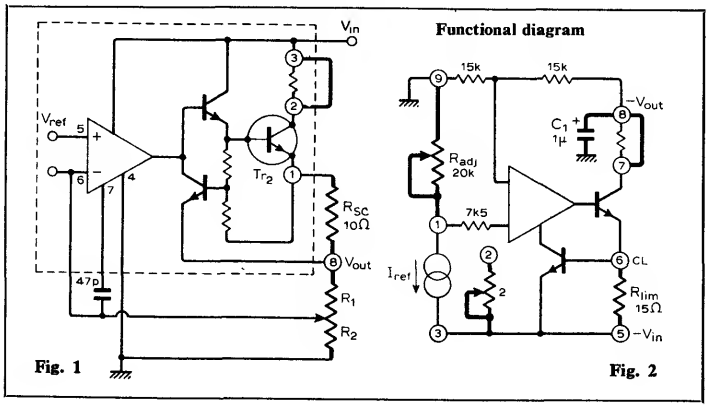
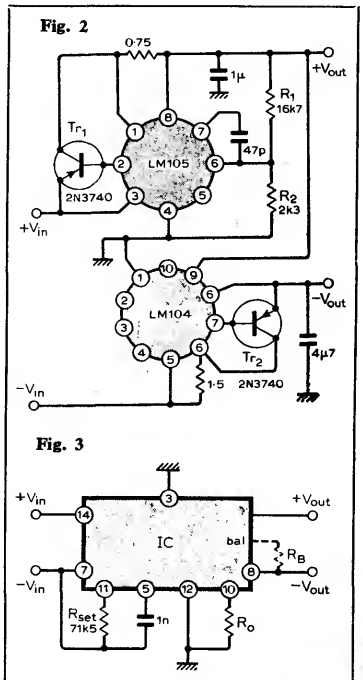


Fig. 1 Fig. 2

The schematic diagram of the LM105/205/305 group is within the dashed box. External components provide a basic low current positive regulator circuit.

LM305, Fig 1.
Temperature range: 0 to 70°C
Input voltage range: 8.5 to 40V
Output voltage range: 4.5 to 30V
Output current: 20mA
Load regulation: 0.03% for load current 0 to 12mA
Line regulation: depends on $V_{IN}-V_{OUT}$ differential 0.025%/V
Parallel combination of R_1 and R_2 should be about 2kΩ
LM305A can provide 45mA.

Negative voltage regulator (LM104, Fig. 2, Current reference is temperature compensated. Output voltage programmed by value of R_{ADJ}. R_{LIM} provides short-circuit protection. C_1 (tantalum) prevents oscillation.
Output current: 25mA
Input range: −50 to− 8V
Output range: −40V to −15mV
Typical load regulation: 0.05% from 0 to 25mA
Typical line regulation: better than 0.2% for ±20% input change
V_{OUT}: R_{ADJ}/500 V
The LM104/LM105 interconnection, Fig. 2, provides a dual polarity tracking regulator.
Using the LM104 as an inverting amplifier i.e. $+V_{OUT}$ at pin 9 appears as $-V_{OUT}$ at pin 8. $V_{IN} \geq \pm 18V$, V_{OUT} ±15V defined by potential divider chain R_1, R_2
Output current: 200mA
The RC4195 or MC1468 in Fig. 3 provide a dual balanced ±15V supply in one package, with current capability of around 100mA.
Input voltage range 18 to 30V.
The RC4194 is a dual tracking voltage regulator in which the positive and negative output voltages are adjustable over the range 0.05 to ±32V by variation of R_7. This should be 2.5kΩ for each volt required.
Input voltage range: 9.5 to 35V
Load regulation (1 to 100mA) 0.001% V_{OUT}/mA
Line regulation: For a 10% change in V_{IN} 0.02% V_{OUT}
Load current: 100mA
An unbalanced output (+12V, −6V) suitable for comparators is obtainable with R_0 of 15kΩ and the addition of R_B of 20kΩ. (LM340) is a three-terminal series positive regulator. It uses an internal temperature independent voltage reference dependent on the predictable gap-energy voltage (card 6, set 23).
Preset output voltages depend on the internal resistor R_1.
LM109/309 are earlier versions on the same principle, but designed specifically for +5V logic levels. Fig. 5 is an adjustable output circuit.
Capacitors are optional depending on transient response requirement and distance from supply.
Another advantage of this i.c. is the internal circuitry which provides shutdown of the regulator if the die temperature reaches 175°C, thus providing virtually absolute protection.



The current capability of most voltage regulators can be boosted with additional external series transistors. A typical configuration extending the LM105 capability to 2A is shown in Fig. 6.
Foldback current limiting allows control of the current when the output is short circuit.
Appro imately, for a short circuit voltage across $R_{SC}=V_{be}-mV_{be}$. At full load, voltage across R_{SC} is $(1-m)V_{be}+k\,V_{out.}$

Hence $\frac{I_{L\,max}}{I_{SC}}=1+\frac{kV_{out.}}{(1-m)V_{be}}$

For a specific V_{out}, the current ratio is controlled by k. The typical V-I curve is given by

$I_L=\frac{(1-m)V_{be}+k\,V_{out.}}{R_{SC}}$

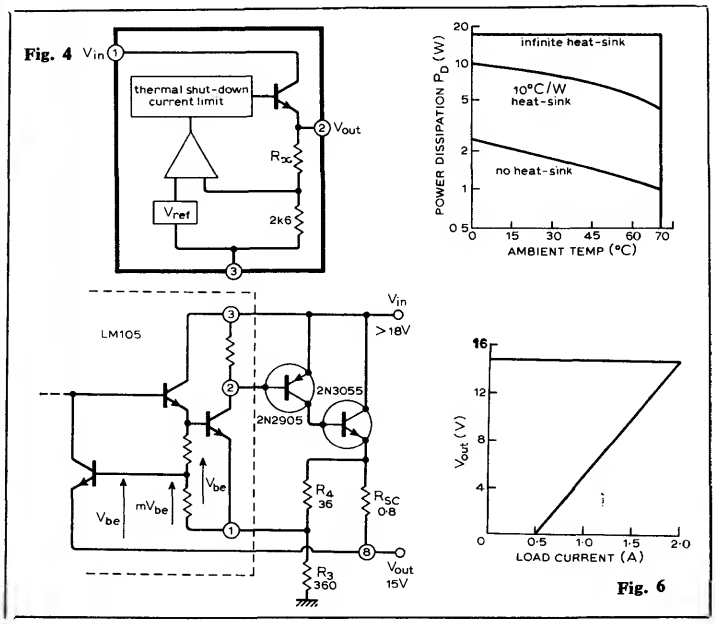
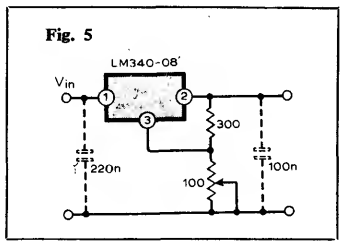


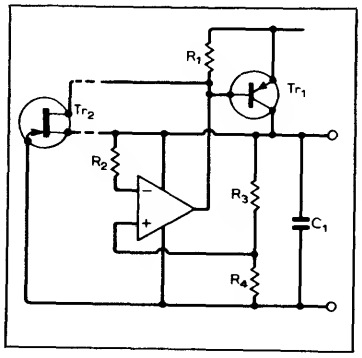
Fig. 6



Further reading
Application notes AN103 (LM340); AN23 (LM105), AN82 (precision tracking regulators), National Semiconductor.
Linear Integrated Circuits Data Book, Motorola, 1972.
Total Linears, Raytheon, 1974.

Cross references
Set 24, cards 8, 3, 4
Set 23, card 6
Set 6, cards 2, 10
Set 7, card 11
Set 20, cards 1, 2, 9.

Voltage regulation using current-differencing amplifiers



Typical performance
R_1 330Ω
R_2 1MΩ
R_3, R_4 10kΩ potentiometer set for V_0 of 5V. Typically R_4=675Ω
Tr_1 BC125
Tr_2 2N5457
C 10μF tantalum
V +7V

Circuit description

The basic voltage regulators described previously using a current-differencing amplifier had two distinct limitations. The obvious one is the very limited output current available, and this can be overcome by adding an emitter follower inside the feedback loop. This actually increases the second problem—that the minimum value of the supply voltage has to be one or more volts above the regulated output. It is possible to solve both problems while simultaneously improving the regulation against supply changes, if the amplifier is supplied from the regulator output (simultaneously regulating the supply to the three other amplifiers in the package). The trick is to make use of the ability of the output stage to sink current safely even when the output potential is greater than that on the amplifier positive supply terminal (provided the difference does not exceed 5V, breakdown in the internal p-n junctions is avoided). The minimum sink current in this mode is 1.3mA and R_1 is chosen so that Tr_1 is kept out of conduction when minimum output current is required. In the simplest form shown 'nV_{be}' biasing is used that fixes the output voltage at $(R_3/R_4+1)V_{be}$ where the V_{be} is that of the internal transistor at the amplifier non-inverting input. R_1 provides a small bias current to the inverting input. (Improved regulation would follow from the replacement of R_3 by a suitable zener diode.) The main problem remaining is that the circuit is not self-starting since with output temporarily at zero no current flows and the state is held permanently. One solution is to add a junction f.e.t. of low pinch-off voltage and on-current sufficient to bring Tr_1 into conduction. Once the output voltage is established, the reverse bias on the f.e.t. gate-source cuts it off and prevents it from disturbing the normal operation.

Component changes

Tr_1: Any silicon p-n-p transistor with suitable current/power rating—circuit can supply up to 200mA but maximum $V_{IN}-V_{OUT}$ rating limited by internal breakdown of amplifier to 5V i.e. 1W dissipation is adequate. BFR81.
Tr_2: Junction f.e.t. n-channel. Pinch-off voltage< regulated output. Zero-bias on-current must be sufficient to drive Tr_1 into conduction—typically >2mA.
R_1: 150 to 390Ω. If resistor is too high the minimum sink current of 1.3mA drives Tr_1 into conduction losing control at light loading. If R_1 is too low, insufficient drive current is available for Tr_1.
R_3, R_4: In this mode of operation, the potential at the non-inverting input is 0.6V and the ratio of R_3: R_4 scales this up to $[(R_3/R_4)+1]$ 0.6V. Stability is considerably increased by replacing R_3 with a zener diode when $V_0=V_Z+0.6V$.
R_2: Not critical. Sets operating currents of input transistors. Suitable values 1 to 10MΩ.

Circuit modifications

- For increased input-output voltage differential the amplifier is supplied directly from V+. To allow the amplier output to be out of saturation the base of Tr_1 is driven through a potential divider. Without this Tr_1 could not be driven off. The upper voltage limit is then the rating of the i.c. (36V for the LM3900). All other amplifiers in the package are subject to the full supply voltage variations.
- To increase the supply voltage rating further while retaining a low ($V_{IN}-V_{OUT}$) a second transistor is added such that all terminals of the amplifier are operated at a low voltage while Tr_1, Tr_2 must be chosen for a suitable voltage rating. An alternative zener circuit is shown in which R_6, R_4 set the output voltage R_4V_Z/R_6 in the absence of R_7. A Resistor to ground from either input causes current flow in either R_4 or R_6, and the resulting contribution to the output voltage has a temperature coefficient which can be used for overall temperature compensation. As shown R_7 contributes $-[1+(R_4/R_7)]V_{be}$ to the output.
- To remove the effect of supply variations via R_1 a diode network is chosen that ensures self-starting but has D_3 dropping out of conduction after starting has been achieved.

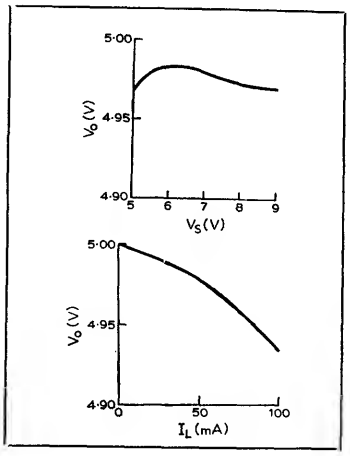
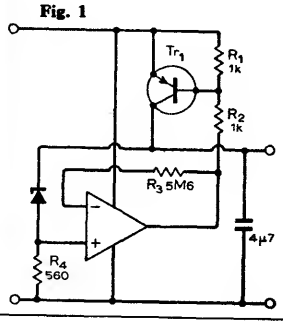


Fig. 1



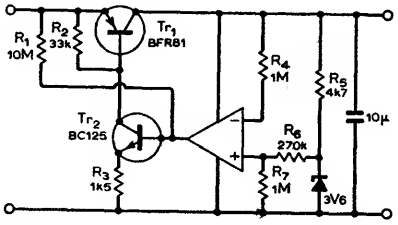


Fig. 2

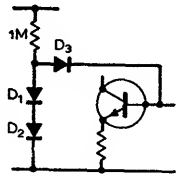
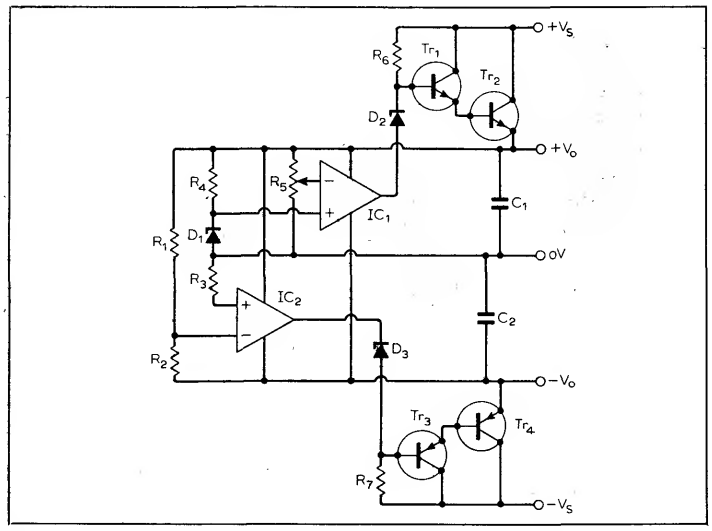


Fig. 3

Further reading

Frederiksen, T. M., Howard, W. M., Sleeth, R. S. The LM3900, A New Current-differencing Quad of ± Input Amplifiers, National Semiconductor application note AN72

Dual-polarity regulator



Typical performance
IC_{1-2} 741
Tr_1 BFR41, Tr_2 2N3055
Tr_3 BFR81, Tr_4 2N2955
D_{1-3} 6.8V zener diodes
R_{1-2} 8.2kΩ, R_3 3.9kΩ
R_4 2.2kΩ; R_5 10kΩ
R_{6-7} 22kΩ, C_{1-2} 47μF
Vs ±15V
Vo ±10V, Io 0-1A

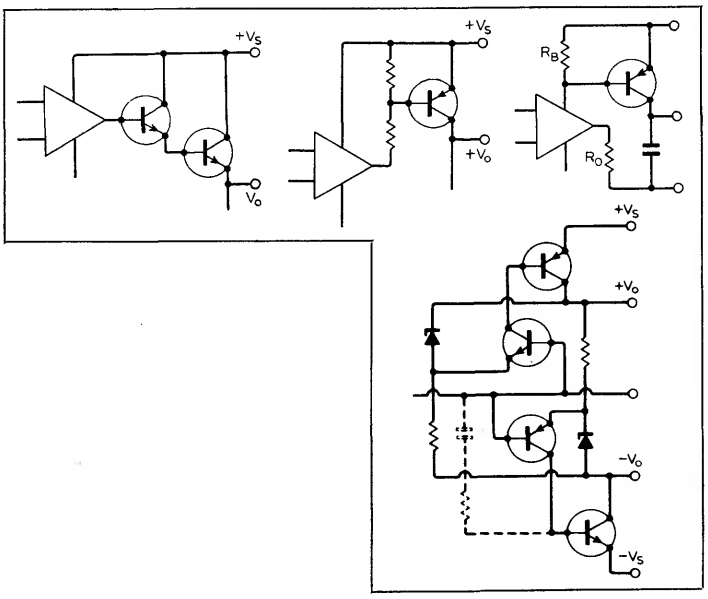
Circuit description
In a dual regulator it can be very important that the outputs track well. This can be achieved by having one section dependent on a particular zener diode or other reference element; the other output uses the output of the first as its own reference. Any variation in the zener voltage whether due to supply or temperature changes affects each equally. To maximize the regulation the zener diode and the error amplifiers should if possible be supplied from the regulated outputs. This can complicate the coupling network between each amplifier and the power output stage. The positive regulator compares a variable portion of the output via R_5 with the constant voltage across D_1. Any difference is amplified by IC_1, whose output is coupled via D_2 to the Darlington pair composed of Tr_1, 2. The negative output is controlled by IC_2 via $Tr_{3,4}$, the amplifier operating in the virtual earth mode with $R_{1,2}$ defining the inverting gain.

For $R_1 = R_2$ the positive and negative output voltages are equal in magnitude. As shown the positive output is restricted to values greater than the zener voltage, but the negative output can take up values from zero to just short of the negative supply.
The outputs are highly stabilized against both supply and load current changes (typically to within 1 or 2mV) and the stability is limited by that of the zener diode D_1.

Component changes
$IC_{1,2}$. Most compensated op-amps may be directly substituted. The output stage contributes no additional voltage gain and hence no change in compensation is warranted. Tr_{1-4}. The drive transistors are standard silicon medium-power devices and a maximum collector current of a few tens of milliamperes is sufficient for output currents beyond 1A. The power devices may then have to dissipate considerable power under short circuit conditions, i.e. current limiting should be added or adequate heat-sinking provided.
D_1: Zener diode with low temperature coefficient for minimum drift.
D_{2-3}: Not critical. Included to allow op-amp outputs to remain in linear region while retaining control of output. Diodes can be replaced by resistors typically of same value as R_{6-7}.
$R_{1,2}$: Equal for precise tracking of outputs. 1 to 100kΩ.
R_3: Minimizes offset if $R_3 = R_1/R_2$. Can be omitted.
R_4: Sets zener diode current to optimum for low drift. 470Ω to 10kΩ.
R_5: May be padded out with series resistors where pot. is to provide trimming action only 1 to 100kΩ. Lower range for least offset/drift though overall drift likely to be dominated by zener anyway.
$R_{6,7}$: Set maximum base drive and hence, give coarse limiting of output 1 to 100kΩ.
$C_{1,2}$: Suppress h.f. oscillation. Not critical but must be close to output or load inductance may initiate instability.
Vs: Because amplifiers powered from regulated outputs, Vs can be high if transistors have appropriate ratings. Increase $D_{1,2}$ voltages to match.

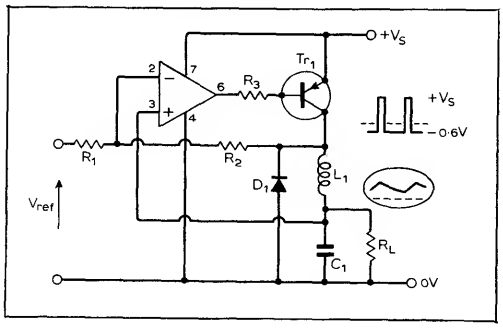
Circuit modifications
- The error amplifier outputs may be coupled to the power stage in several ways. Direct coupling reduces the component count but requires that the op-amp be powered from the supply rail. The input-output differential is increased to >3V in many cases.
- To reduce this, the output stage is operated in common emitter (with or without an intermediate driver). The inversion requires the op-amp inputs to be reversed and the resulting circuits are typically non-self-starting and require additional components for starting.
- As in previous power amplifiers the amplifier may drive a dummy load resistor R_O, the resulting current bringing the output transistor into conduction when the p.d. across R_B exceeds 0.6V.
- A simple discrete form of the circuit has a good performance with few components but requires to be started either by a CR network together with the switch-on transient or by a separate switch.

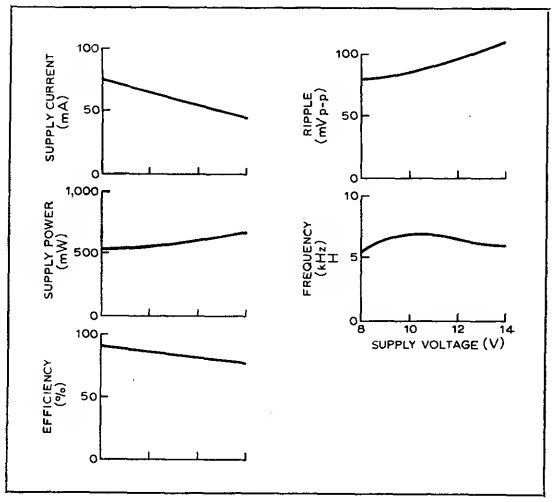
Further reading
Eckhardt, R. Regulator for op-amps practically powers itself, *Electronics*, Oct. 3, 1974, p. 106.
Holmskov, Ole, Voltage stabilizing a symmetrical power supply, *Wireless World*, May 1975, p. 226.



wireless world circard

Switching regulator





Typical performance
IC_1 CA3130 (RCA)
Tr_1 BFR81
D_1 1N4148
L_1 680μH
C_1 15μF
R_1 1kΩ
R_2 470kΩ
R_3 680Ω
V_{REF} 5V
R_L 50Ω
V_S 10V

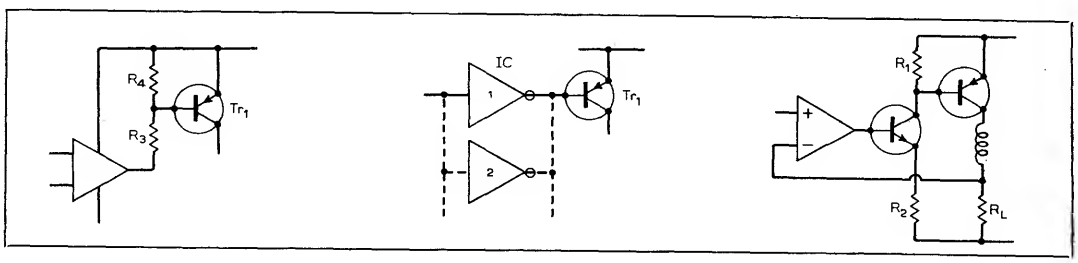
Circuit description
Switching regulators are related to Class-D switching amplifiers. The power stage Tr_1 conducts for a varying portion of the time. If the switching frequency is high, the current in L_1 varies little throughout the cycle, with D_1 sustaining the current in the load when the transistor is off. The inverting gain provided by Tr_1 reverse the effective polarity of gain at the amplifier inputs; 100% negative feedback is applied from the load to one input and with L_1 short circuit, a linear regulator would result were V_{REF} to be fed directly to the other input. A small amount of hysteresis via R_2, R_1, combined with the L_1R_L creates an astable—the LR equivalent of the standard op-amp CR astable. The load voltage has a similar exponential waveform with a ripple of the order $(R_1/R_2)V_S$ and a mean value of V_{REF} when the hysteresis is small. Power losses include those due to the speed of switching including core losses in L_1, and the "d.c." losses such as $V_{ce(sat)}$ for Tr_1 and the on voltage of D_1. For low output voltages the latter limits the efficiency—between 70 and 90% is common even where the output voltage is $< V_S/2$. As the supply voltage varies the mean current changes in the opposite sense because the mark-space ratio is adjusted automatically via the astable action. Hence the mean power drawn from the supply depends mainly on the power required by the load.

Component changes
IC_1: This op-amp is particularly suitable for several reasons (i) high input resistance (m.o.s.) allows high R_2: R_1 ratio without R_1 becoming too low. (ii) input common-mode range includes zero line allowing control of output down to zero. (iii) high slew-rate allows switching speeds to be increased to suit optimum frequency-range of ferrite-cored inductor. (iv) c.m.o.s. output stage allows direct coupling to Tr_1 if needed with rapid switch-off reducing charge-storage problems.

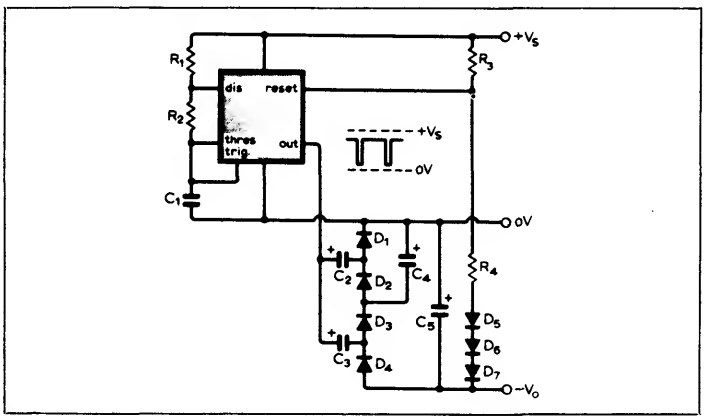
Most other un-compensated op-amps and comparators can be used provided following precautions observed: V_{REF} must lie within input common-mode range; the output may not be able to swing high enough to switch Tr_1 off and a resistive network such as R_3, R_4 may be needed (left); current capability must be sufficient to saturate Tr_1 at max. load current—say $I_L/20$. Tr_1 p-n-p silicon, peak current equal to mean load current; low saturation voltage; switching speed fast enough to make rise/fall times much less than the period of waveform; high frequency minimizes dissipation in transistor if above observed.
D_1: current rating mean output current; peak inverse voltage rating (p.i.v.) V_S; efficiency increased at low output voltages by reducing diode on-voltage (Schottky or germanium diodes if temperature not too high).
L_1: Typically 200μH—10mH depending on current/frequency used. Ferrite cores reduce size provide high Q, low losses; saturation of core at higher currents can inhibit oscillations.
C_1: Modifies frequencies for given L_1 R_L combination. Not essential to operation, but reduces transients in load.
R_1, R_2: Ratio sets hysteresis and hence ripple. As ripple is reduced, so is time taken for completion of cycle i.e. frequency increases. By keeping R_1, R_2 as large as possible injection of switching current into V_{REF} is minimized. Ratio R_2/R_1 typ. 100 to 1,000; high value gives low ripple provided increased frequency does not bring transient problems in.
R_3: Not critical. 100Ω to 1kΩ with this op-amp.
V_{REF}: Equal to required output.
R_L: Load currents up to 200mA+possible
V_S: +5 to +15V.

Circuit modifications
Paralleled c.m.o.s. buffers may be used to boost output drive (centre). See op-amp data sheet. Alternatively use additional transistors (right). Final stage should be common emitter for highest efficiency. R_1, R_2 100 to 470Ω. Outputs to 1A.

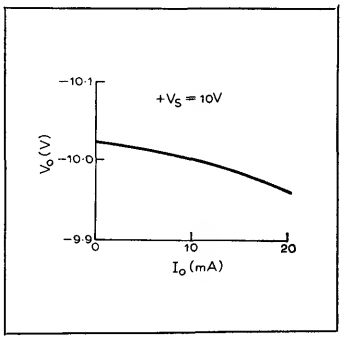
Cross references
Set 6, card 7.
Set 24, card 10.
Set 7, card 12.



Self-regulating d.c.-d.c. converter



Typical performance
IC_1 555 timer
D_{1-7} 1N4148
C_{2-5} 47μF, C_1 0.015μF
R_1 1.2kΩ, R_2 10kΩ,
$R_{3,4}$ 22kΩ
$+V_S$ +10V
V_O −10V
I_O 0 to −20mA
V_O/V_S ±0.5% for V_S 7 to 14V

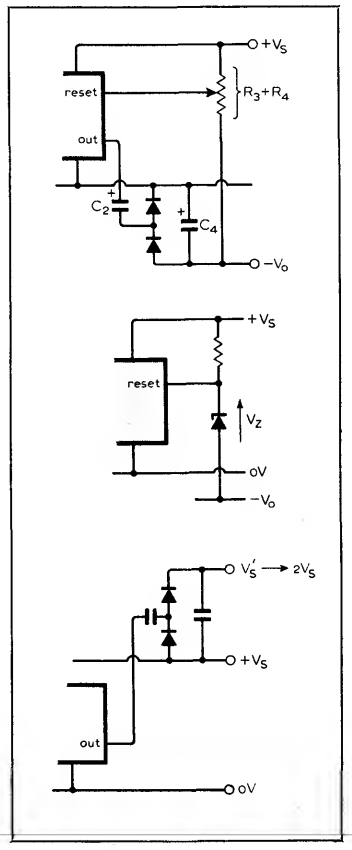


Circuit description
Dual-polarity supplies are needed in many systems where only a single supply is initially available. The circuit shown achieves this by acting as a free-running astable oscillator producing an output voltage just less than the supply. This is applied via a diode-capacitor network D_{1-4}, C_{2-5} to produce a negative output voltage. Assume ideal diodes, D_1 clamps the right hand side of C_2 to zero on positive output swings; similarly D_3 clamps the right hand side of C_3 to C_4.

On negative swings, C_2 transfers charge via D_2 into C_4 as does C_3 through D_4 into C_5. Eventually C_2, C_4 each acquire a p.d. equal to the output swing, while C_3, C_5 achieve double that value. Two factors reduce this output voltage: losses across the diodes drop the maximum output by about 2V. The timer has a reset terminal; when the potential on this approaches ground the oscillations are inhibited.

A potential divider composed of R_3, R_4 and D_{5-7} provides a potential at the RESET terminal such that each time the magnitude of the negative output increases, the oscillation is inhibited and the magnitude decreases. The diodes optimize the tracking for $|V_O| = V_S$.

Component changes
IC_1: The circuit depends on the particular characteristics of the 555 timer available from most i.c. suppliers.
D_{1-7}: Not critical. Any fast silicon diodes.
C_1: 470p to 0.1μF. At low frequencies ripple increases and at high frequencies switching losses.
R_1: 470 to 10kΩ. Too low a value wastes current.
R_2: 2.2k to 22kΩ. Select for frequency of oscillation.
R_3, R_4: can be replaced by potentiometer for variable output. Value not critical.
V_S: +5V to +20V
V_O: Up to 2V_S in magnitude.



Circuit modifications
- For some applications the circuit can be considerably simplified. Where the negative voltage required is less than the positive supply available then the rectifying network can be simplified as shown. If the precise tracking of the two supplies is not important then the compensating diodes D_{5-7} can be omitted. With R_{3-4} replaced by a potentiometer, the result is a convenient circuit for producing, say, −6V from a +12V supply as required by widely used i.c. comparators.
- A second modification allows the negative output to be regulated rather than be proportional to the supply voltage. Replacing R_4 by a zener diode, the oscillator is reset each time the negative output pulls the reset terminal close to zero. The resulting ripple characteristics are comparable to the previous circuits. N.B. the regulation and ripple for a single diode pair is significantly better than for the voltage doubler, loads down to 100Ω being tolerated
- The same oscillator circuit can be used to generate a voltage more positive than the supply as shown. To regulate the output, a separate sensing circuit would be required since the original depended on using the RESET as a virtual earth.

The circuit has affinities with certain re-triggerable monostables, and those based on op-amps in which the switching action is controlled by positive feedback can be adapted.
The two functions performed by the timer can be separated, with a clock generator driving a monostable. The latter is gated off each time the required output voltage is exceeded. Where the output swing of the timer is insufficient any of the usual power output stages may be added—Darlington pairs for increased current, complementary common emitter stages for increased output voltage swing. At low supply voltages conventional i.cs are not applicable, and discrete transistor oscillator-switches are required.

Further reading
Gartner, T. IC timer and voltage doubler form a dc-dc converter, *Electronics*, Aug. 22, 1974.

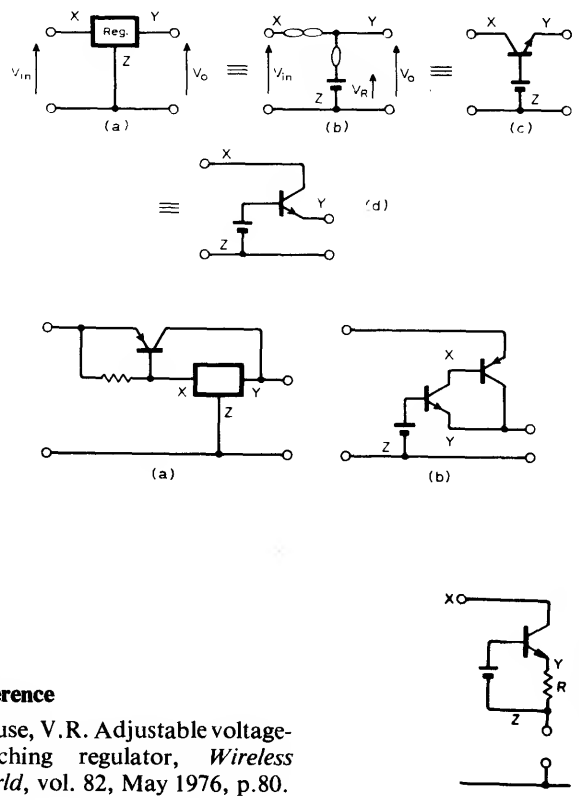
Cross references
Set 21, card 9.
Set 10, card 2.
Set 10, card 10.
Set 24, card 9.

wireless world circard

Set 24: Up-date

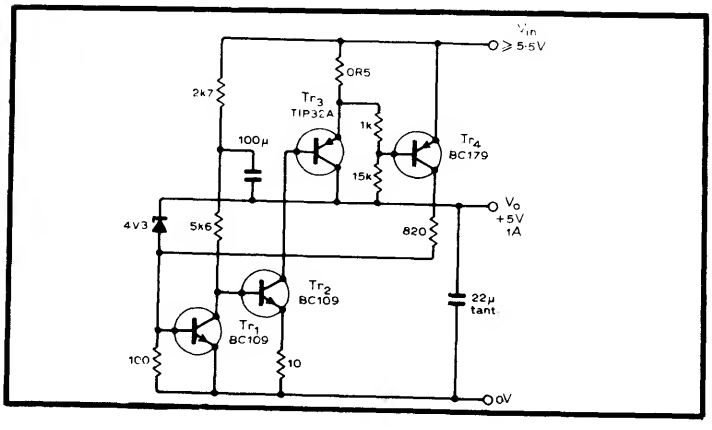
The most significant advance in regulator design is arguably the appearance of the i.c. three-terminal regulator. These are now available in a range of voltage and current ratings, but there are bound to be gaps in this range that can be filled by more conventional variable-voltage multi-terminal devices. Alternatively the three-terminal devices can themselves be adapted if their nature is clearly understood. To find a suitable equivalent circuit compare Figs 1(a)–1(d). A nullor (combined with a voltage reference) equivalent to an ideal transistor with infinite voltage and current gain would provide the same performance as an ideal three-terminal regulator, viz that for all conditions for which $V_{IN} > > V_O$ then $V_O = V_R$. This follows from the nullor/ideal transistor properties that a nullator/base-emitter voltage is always zero and the norator/collector-emitter voltage may have any arbitrary value, with the load and supply currents being equal. Just as practical transistors and reference elements require biasing so practical voltage regulators carry a small but finite current in Z rendering the X and Y currents unequal. This current in Z is much less than typical load current and is also kept moderately constant by careful internal design of the i.c. If the equivalent circuit has a potential-divider of low resistance then $V'_O = (R_2/R_1 + 1)VR$ and the regulator gives a regulated voltage of any required output value $> V_R$ up to the device breakdown limits.

Fig. 3(a) shows a modification that is proposed for increasing the output current. By redrawing as in Fig. 3(b) the circuit is seen to be equivalent to a complementary Darlington pair (again assumed to be ideal) fed from the same voltage reference i.e. the current capability is scaled up by h_{FE} with no change in output voltage. If the load is placed in series with the device as in Fig. 4 but with a dummy resistor R added between Z and Y, then the load current is defined as V_R/R, with the addition of the small current in Z mentioned above.



Reference

Krause, V.R. Adjustable voltage-switching regulator, *Wireless World*, vol. 82, May 1976, p.80.



As the performance/cost ratio of integrated-circuit voltage regulators continues to improve it is tempting to ignore discrete-component designs altogether.

This is dangerous because the constraints of i.c. processing, for example absence of high performance p-n-p transistors, can bring limitations. In particular for highest efficiency the output transistor has to operate in common emitter, and if a separate power device has to be added the advantages of a single-chip solution are abated. The circuit shown is a neat solution in that the input-output voltage differential can fall to ~0.5V or even towards zero if the current limiting network is eliminated (the 0.5Ω resistor Tr_4 etc). The performance claimed for this circuit is particularly good in respect of regulation against supply and load changes, the current-limiting is of the fold-back variety and the transistor types are non-critical.

Mitchell, K.W. High performance voltage regulator, *Wireless World*, vol. 82, May 1976, pp.83/4.

notes

Sets 25 & 26: RC oscillators

One might have expected the introductory article to deal with the point of theory concerning nullors. They are instead introduced in a concise and easily assimilble way on page 67, making any explanation here superfluous. Those unfamiliar with nullors will see from page 00 the usefulness of the concept in rearranging and regrouping circuits to generate new circuits (even though the method gives no phase information). See also Circuit Designs 1, pp.122/3. Circuits covered are obvious from the titles, the first ten or 11 covering Wien circuits, single-component frequency control and amplitude control methods. Set 26 deals mainly with phase shift and T-circuits.

RC oscillators

Amplifiers oscillate; oscillators may not. These guiding principles have been developed and confirmed over many years of patient experimenting, not least during the preparation of Circards. Early versions of operational amplifiers were particularly critical of the source/load/supply impedances and were prone to oscillate at high frequencies unless carefully used. Early transistors had low values of current gain and cut-off frequencies making it difficult to produce controlled oscillations.

These properties point to a dividing line between oscillators and amplifiers with feedback viz that they are of the same kind, differing only in the quantity and nature of the feedback. The point can be illustrated by Fig. 1 in which an amplifier of gain A has a portion of its output volage β subtracted from the signal at the input. The gain of the amplifier with feedback can be greater or less than A, and the output will in general differ in phase. For well-controlled characteristics, the phase-frequency response has to be such that the feedback does not become regenerative until the magnitude of the βA term is below unity.

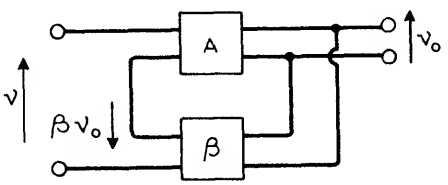
Feedback theory is formally expressed in many different ways, but one graphical approach that is helpful is to consider the root locus (Fig. 2). The graph plots the locus of the system transfer function as the frequency varies. Points on the horizontal axis correspond to phase shifts of zero (to the right of the origin) and 180° (to the left). Points on the vertical axis represent phase shifts of $+90°$ and $-90°$. The distance of a point from the origin represents the magnitude of the transfer function. Thus in many amplifiers the region of the locus near the horizontal axis would represent a very wide range of frequencies since the gain remains constant and the phase-shift is zero or 180° over this range.

An important point on this graph is the point $1 \angle 0°$. A general criterion, due to Barkhausen, suggests that if the locus of the system response does not enclose this point then the loop may be safely closed and the feedback will not cause the amplifier to become unstable. An exceptional state of conditional stability can result where the amplifier/feedback network has multiple reactive elements producing a complex locus which would enclose the point in the event of a fall in the magnitude of the gain.

When the locus passes through the point we have $\beta A = 1 \angle 0°$ commonly called positive feedback and this constitutes an oscillator of constant but undefined amplitude, i.e. the signal feedback is just sufficient to sustain the output unchanged and without the need for an input signal. Alternatively we may view it as an amplifier of infinite gain, the denominator of the expression, $1-\beta A$, having gone to zero.

The inevitable small variations in β and A caused by temperature, supply or load conditions as well as by long term drift in component values, cause the amplitude either to decay away ($\beta A > 1$) or to increase ($\beta A < 1$). The limit is set by non-linearities in the system either inherent to the amplifier or deliberately added externally in the feedback network(s). These reduce βA and the oscillations settle down to a stable situation in which the mean value of βA over the cycle is unity.

For good frequency stability a number of precautions have to be observed (1) the amplifier should have negligible or very closely controlled phase-shift at the frequency of oscillation. (2) Amplitude of oscillation should be controlled to minimize distortion, since harmonics are fed back to the



$$(v + \beta v_0)\, A = v_0$$

$$v_0 (1 - \beta A) = A v$$

$$T_v = \frac{v_0}{v} = \frac{A}{1-\beta A}$$

Fig. 1. A fraction of the output is added to the source at the input in deriving a standard form of the basic feedback equation. Positive feedback occurs when βA is positive.

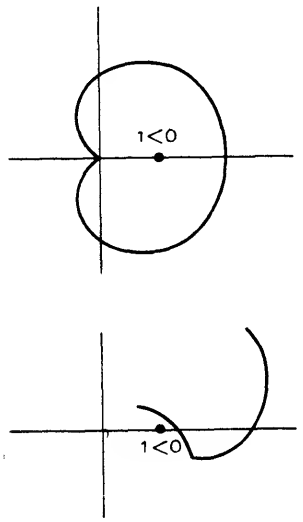
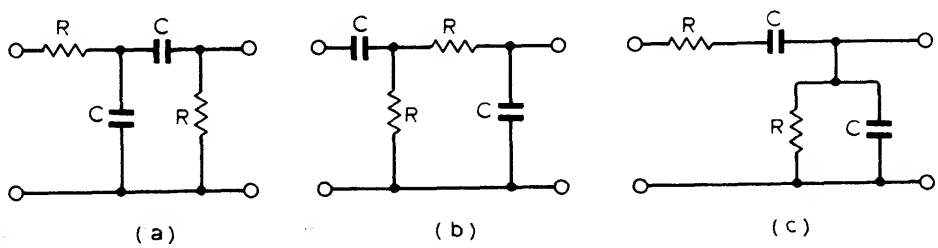


Fig. 2. If the in-phase and quadrature components of the overall loop gain are used as axes, the locus as the frequency is varied indicates the stability of the system.

Fig 3. These three networks have an identical transfer function and can be used interchangeably in oscillators.



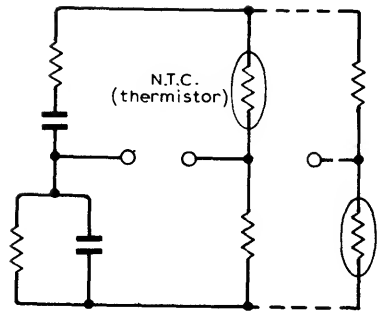


Fig. 4. Some oscillators use temperature-dependent resistors heated by the amplitude of the oscillation.

input and the resulting intermodulation reduces the frequency of oscillation below that predicted from the simple theory. (3) Input and output impedances of the amplifier must not load the RC networks significantly.

A major class of oscillators which includes the Wien bridge circuits, uses networks as in Fig. 3. Using equal values of R, C throughout, the transfer function of each of these circuits is the same, with the output reaching a maximum of one third of the input when the phase shift is zero. Frequency is $1/2\pi RC$. Each can be used with an amplifier of gain +3 to produce sustained oscillation. Many other combinations of these networks and amplifiers can be devised, by using current, transconductance and transresistance amplifiers.

Amplitude control may be via a gain-controlled amplifier whose gain is reduced as the output exceeds a given value, usually via a peak- or mean-rectifier and f.e.t. or similar controlled resistor. The classical solution is to use the RC network as part of a bridge configuration with a high-gain amplifier monitoring the bridge unbalance. One of the bridge resistors is made amplitude sensitive, e.g. a filament lamp or thermistor arranged so that increasing amplitude of oscillation increases the amount of negative feedback thus stabilizing the oscillation amplitude Fig. 4.

These oscillators are controlled in frequency over a very wide range commonly by switching in pairs of capacitors as the coarse control or range-setting, with ganged resistors for fine control. The reverse is possible with high input-impedance amplifiers where high resistances allow the use of ganged tuning capacitors. Single-element control has obvious advantages of simplicity and economy, as well as the possibility of remote control via light dependent resistors and the like. Most solutions to this problem require a larger number of amplifiers to provide separate feedback paths by splitting the

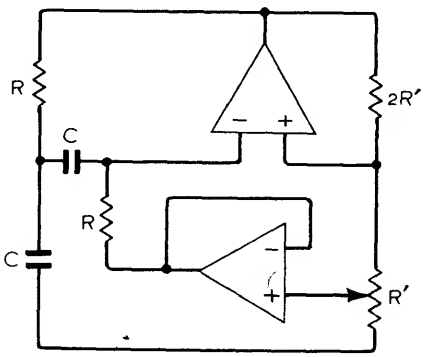
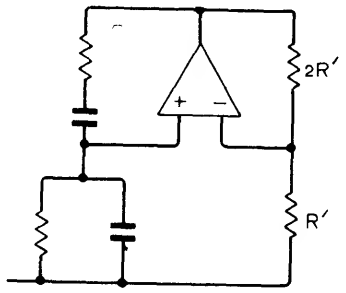
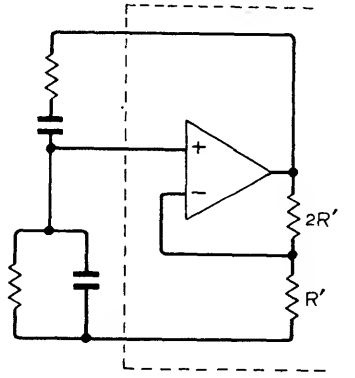


Fig. 6. Adding another amplifier at appropriate points in various oscillators allows a single control to change the frequency without varying loop gain.





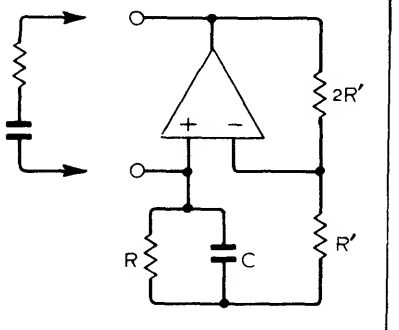


Fig 5 (a). A standard configuration uses an operational amplifier to activate the bridge. (b) Circuit partitioned to show an amplifier of gain +3 with the frequency-dependent network providing positive feedback. (c) Removing one section of the network, the impedance across the port is found to be negative, leading to Negative Impedance Converter interpretations.

passive network in some way, and in addition there is an effective loss in Q of the system that results in increased distortion. One example out of many that have been designed is shown in Fig. 6. Frequency ranges of up to three decades have been reported, while the amplitude control mechanisms are similar to those above.

T, phase-shift, and two integrators

Since both inverting and non-inverting amplifiers are obtainable, circuits can be designed in which the phase-shifts in the external networks are 180° and zero (or 360°) respectively. An example of the former is the classical three section phase-shift circuit shown in Fig. 7. Using equal values of resistors and capacitors the network attenuation is rather large, the output being 1/29th of the input at the frequency where the overall phase-shift is 180° . It is usually preferred to the alternative form using interchanged Rs and Cs, because the increased attenuation at high frequencies reduces the harmonic distortion and with it the corresponding shift in frequency.

If the RC values are scaled, then with n large each section can be analysed separately since the loading effects of the following section can be ignored. The phase shift of each section is then close to 60° at the critical frequency with a halving of the signal level. The amplifier then needs a voltage gain of −8 but the demands on input and output impedances are more severe (the current that can be drawn from the network without loading it becomes very small while the current needed to supply it increases). Alternative methods are to separate the phase-shift networks, using one amplifier of gain −2 between each section. Fig. 8 shows a related circuit that combines the gain and phase-shifting sections. Variants such as this are convenient for three-phase oscillators particularly as gain required from each stage is minimal.

A separate class of oscillators is based on null/notch/band-stop RC networks in which the signal transfer function tends to zero or a low value at a particular frequency (Fig. 9). These can give improved sharpness of tuning with lowered distortion, but interaction between the impedances can make them less tolerant of component drift. More important is the difficulty of tuning such circuits since several components need to be changed simultaneously. Separating the paths through these networks and driving them with individual amplifiers can allow control of the frequency without change in the amplitude condition.

There is a very close relationship between active filters and oscillators. They share common passive networks and in many cases one can be converted simply into the other by adjusting the damping factor (sharpness of tuning). A very important configuration which has wide application in both fields is the

two-integrator loop (Fig. 10). Well-known in analogue computing, it and its near relatives appear under a number of names including 'bi-quad,' 'triple,' 'state-space,' 'gyrator' etc. For ideal amplifiers the circuit Q is infinite without the need for positive feedback and it is particularly suited to the design of high-Q active filters by the addition of a small amount of negative feedback. In practice the net feedback will depend on internal phase-shifts as well as finite-amplifier gains, and both positive and negative feedback may be used to produce controlled oscillations.

If a single resistor or capacitor is varied then with ideal amplifiers, the circuit is still on the edge of oscillation, but the frequency at which oscillation can be sustained is varied. Single-element control of frequency is of considerable advantage in simplifying the construction of oscillators, since dual-gang controls are difficult to keep in a well-matched condition over a wide range. The feedback needed remains small under these conditions, being sufficient only to overcome amplifier imperfections and the finite Q of the capacitors.

Because the amount of feedback required is small it can be introduced via a clipping network that comes into action sharply at a particular amplitude without bringing in significant distortion. This gives instantaneous control of amplitude without the time delay due to heating effects with thermal control. In addition there are three separate outputs with 90° phase differences and the addition of another inverting amplifier gives the fourth phase if required. Again there are a number of combinations of amplifiers and network which share these desirable properties as in Fig. 11. In all of them there is a tendency to instability at high frequencies where the slew-rate limiting of the amplifiers produces a jump phenomenon that locks the oscillator into an output oscillation of higher frequency and uncontrolled amplitude.

Some of these networks are more usually interpreted as forms of impedance inverters/converters, in particular the gyrator, *viz*, a circuit that with a capacitor across one port synthesizes a purely inductive reactance across a second port. If that port has a second capacitor placed across it, a resonant circuit is established which sustains oscillation if a small amount of positive feedback is introduced. It is instructive to draw out the passive networks in such circuits since this clarifies the interrelationships between the various forms of oscillator and filter (Fig. 12).

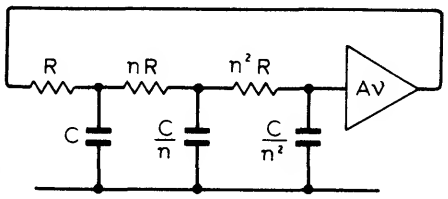
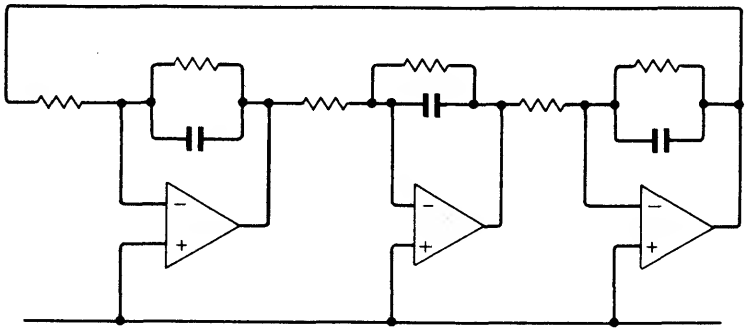


Fig. 7. If the impedances are graded to minimize loading of each section on the preceding one, each contributes 60° to the overall phase-shift at the frequency of oscillation.

$n = 1 :- A_v \longrightarrow -29$

$n \longrightarrow \infty :- A_v \longrightarrow -8$

Fig. 8. Three amplifier stages with defined gain/phase characteristics comprise a three-phase oscillator.



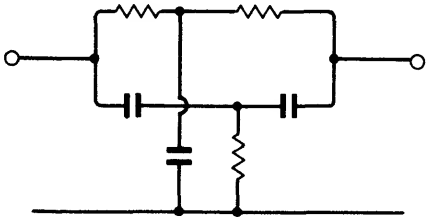
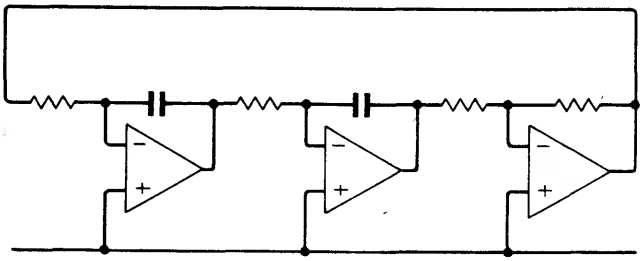


Fig. 9. T-networks can have zero-transmission at a particular frequency. Oscillators utilize positive feedback with the T-network in a negative feedback path.

Fig. 10. Two integrators plus an inverter form the nucleus of a number of oscillators and filters.



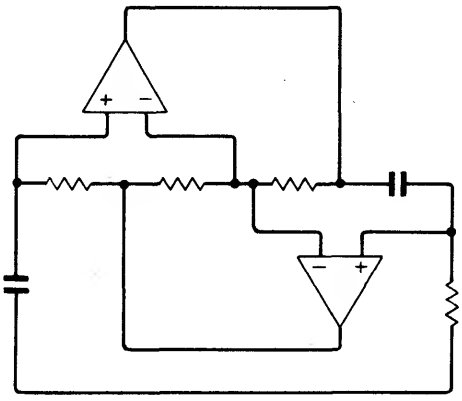
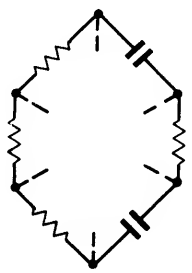


Fig. 11. Gyrators are a class of circuits that synthesize an inductive reactance from a capacitor. An oscillator results from resonating the reactance with a second capacitor.

Fig. 12. The previous two oscillators share a common passive network and can be shown to be functionally identical.



wireless world circard

Nullors, networks and n.i.cs

Two circuit elements were devised to complement the short-circuit (zero p.d. at any current) and the open-circuit (zero current at any p.d.). They are the nullator (zero V, I) and norator (arbitrary V, I). Neither has a separate real existence but a high-gain amplifier embedded in a feedback network approximates to the combination. Such an amplifier can be replaced in circuits by a nullor, the name given to the combination, and this can simplify drawings by allowing the separation of input and output networks.

An op-amp has the constraint that one end of the norator is grounded, a transistor that of a common point between nullator and norator. An f.e.t. has a lower gain and requires an additional resistor to simulate it. With multi-amplifier systems if several points are equipotential because of nullator action there are multiple ways of achieving this effect.

To illustrate this consider the differentiator circuit. Feedback theory indicates the alternative of placing an integrator in the feedback path of an amplifier, and this solution can be convenient in analogue computing.

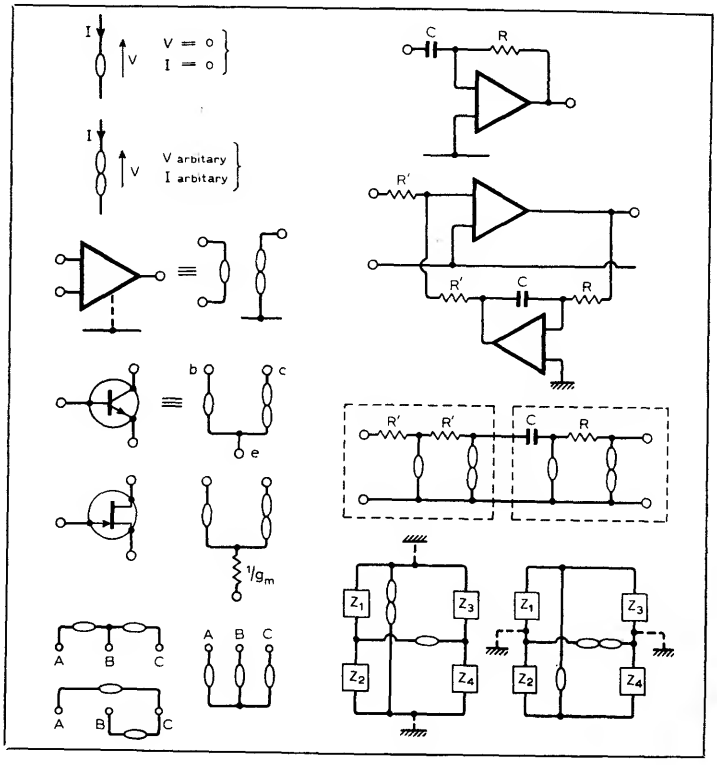
Re-drawing in nullor form, and combining the nullators and norators, shows that the system is equivalent to an amplifier followed by a differentiator. It suggests that drawing in nullor form and then re-pairing is another method of generating new circuits. Yet another method is that of interchanging the positions of a nullator and a norator in changing the source and load in bridge measurements. This lead to four forms of oscillator derived from a common passive network.

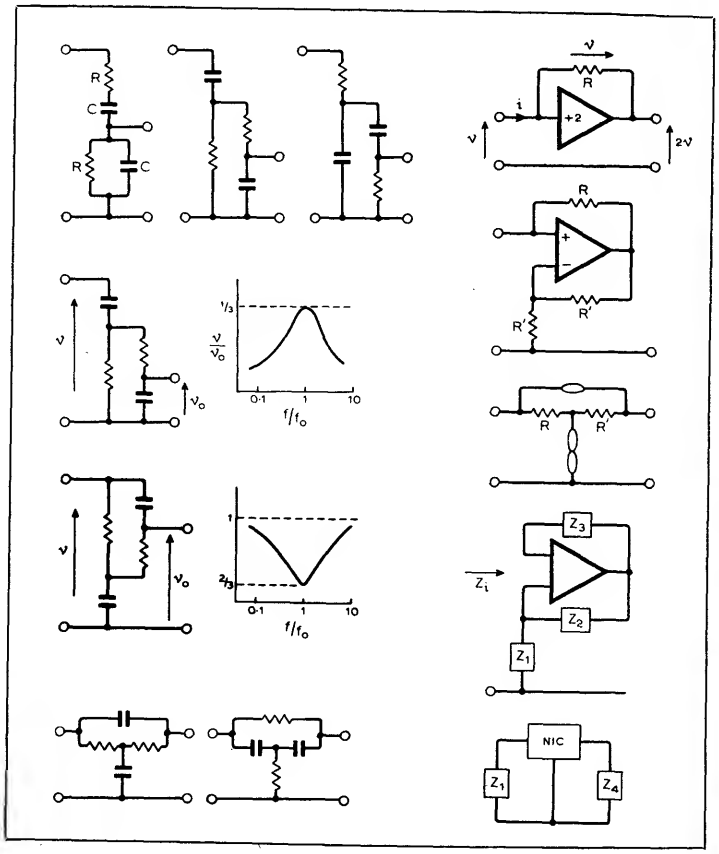
A standard network in RC oscillator design is that due to Wien, having a transfer function

$$v/v_o = T_v = \frac{1}{3+j(f/f_o - f_o/f)}$$

where $f_o = 1/2\pi CR$. Two other networks of cascaded lead and lag sections have identical transfer functions for identical R, C values. The response is a maximum of 1/3 with zero phase shift at $f = f_o$, falling at both high and low frequencies. If the network is inverted (taking the lead-lag as an example) the response has a minimum value at $f = f_o$. The former network can be used as a feedback path, balanced against resistive negative feedback to inhibit oscillation except at the peak of the response; the inverted network is balanced against positive feedback, the latter dominating only at the trough in the network's response.

Re-drawing this inverted network gives the bridged-T. The nullor gives no information on the phasing of input-output to be used in practical amplifiers that implement it. A class of circuits called negative impedance convertors (n.i.cs) show the advantages and snags. Resistive feedback across an amplifier with positive voltage gain leads to a negative input resistance $R_i = v/i = v/-(v/R) = -R$. If the input phasing is reversed the input impedance is still found to be $-R$, but is now stable only for source resistances $> R$ instead of $< R$. Extracting the amplifier and feedback resistances leads to a form of n.i.c. which can be generalized to the form shown, where $Z_i = -Z_1 Z_3 / Z_2$. This allows negative resistances, capacitances and inductances to be synthesized using only Rs and Cs. If a n.i.c. is combined with parallel and series RC networks which cancel at a single frequency, oscillations result.





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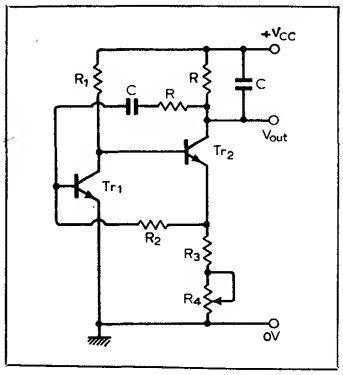
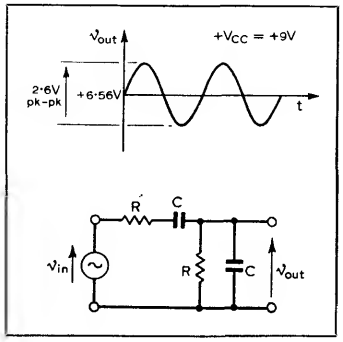
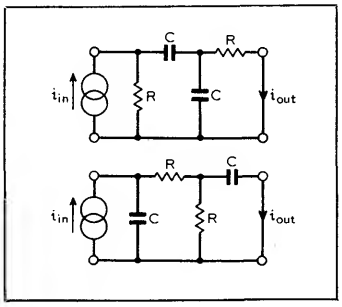
Current-driven Wien oscillator

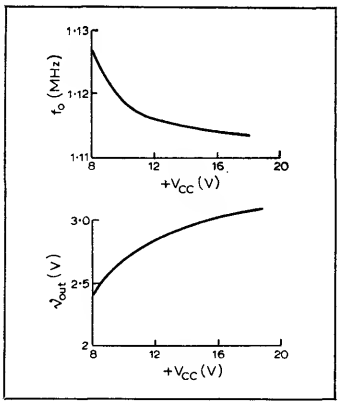


Typical performance
+Vcc +9V, 2.7mA
R 2.2kΩ, C 56pF
R_1 4.7kΩ, R_2 1.5kΩ
R_3 470Ω, R_4 470Ω
Tr_1, Tr_2 1/5×CA3086
(Note: Tr_1 emitter is pin 13)



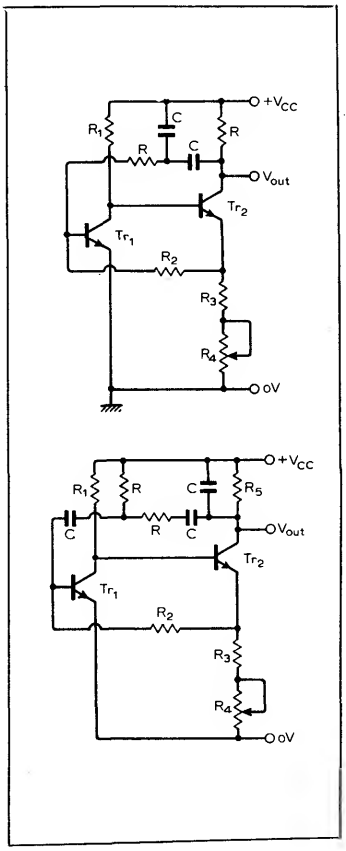
Circuit description
Many RC oscillators use a Wien network as the frequency-determining part of the closed loop and very often the Wien network is used where it may be driven from a low-impedance source and loaded by a high-impedance load as shown right.
However, in many applications it is more convenient to use the current dual of the above network which is driven from a current source and ideally is loaded by a short circuit. The reciprocity principle requires that this network has the same transfer function as the voltage-driven form, which is $V_{out}=V_{in}Z_2/(Z_1+Z_2)$ where Z_1 is the impedance of the series-connected RC pair and Z_2 is the impedance of the shunt-connected RC pair. The resulting dual network is then as shown top right.
The transfer function of this network is given by $i_{out}=i_{in}Z_2/(Z_1+Z_2)$.
The circuit shown above left is an RC oscillator employing the current-dual network to close the loop of a bipolar transistor amplifier which is in the form of a d.c. feedback pair. The Wien network is supplied from the collector of Tr_2 which serves as a reasonably good current source due to the increase in output impedance provided by the feedback network. The output of the Wien network is loaded by the d.c. feedback network in shunt with the input impedance at the base Tr_1. Whilst not an ideal load negative feedback through R_2 provides a sufficient approximation to the desired low value.
In order to provide sustained oscillations the closed-loop phase-shift must be zero and the amplifier must provide sufficient gain to overcome the losses in the Wien network. For the usual case of equal Rs and equal Cs in the series and shunt parts of the Wien network the frequency of zero phase shift occurs at $f_o=1/2\pi CR$ and at this frequency $i_{out}=i_{in}/3$. Hence, the minimum gain required from the amplifier is 3. In the d.c. feedback pair shown this current gain is given approximately by $A_i=1+R_2/(R_3+R_4)$. Resistor R_4 is provided in the form of a variable to allow convenient adjustment of the loop gain to provide a reasonably-sinusoidal

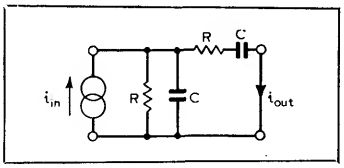




output waveform. The more the gain exceeds the critical value the more distorted will the output waveform become and the lower will be the frequency of oscillation. (See graphs for effect of increasing supply voltage, for example, after setting the critical condition at a lower value of +Vcc.)

Component changes
Useful range of Vcc +4 to +20V. Scale RC values for





lower-frequency operation. For higher oscillation frequencies, f_o will become less-accurately predictable due to presence of internal transistor capacitance and any shunt capacitance of load. R_4 will need re-adjustment if operating frequency is changed.
Separate transistors may be used or the whole circuit excluding capacitors and R_4 integrated on a single monolithic chip.

Circuit modifications
- Any other frequency-determining network which operates with an optimum source impedance tending to infinity (a current source) and an optimum load impedance tending to zero can be used in place of that shown.

Two examples are given.
- D.c. feedback pair forms of these networks are shown below.

C, R and R_1 to R_4 same values as original circuit. X_{C1} tends to zero at f_o and R_5 is large, say 10kΩ.

Further reading
Williams, P. Wien Oscillators, *Wireless World*, November 1971, pp. 541-6.
Stott, C. Transistor RC Oscillator, *Wireless World*, February 1962, pp. 91-4.

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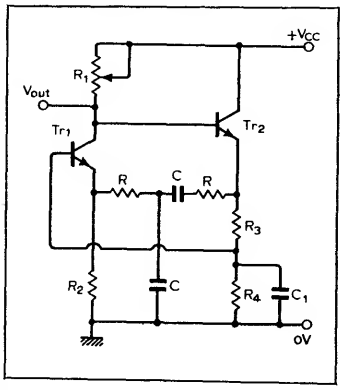
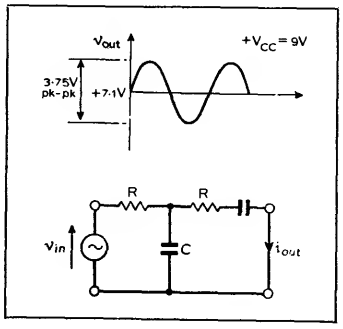
RC oscillators



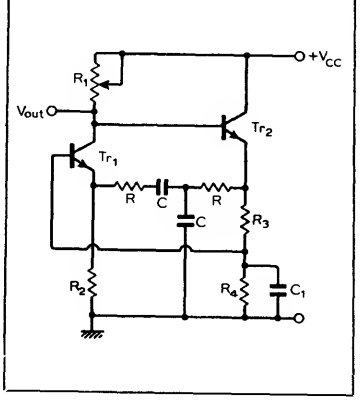
Typical performance
$+V_{cc}$ +9V
R 4.7kΩ, C 4.7nF
R_1 50kΩ var. (typically 15kΩ)
R_2 22kΩ, R_4, R_3 2.7kΩ
C_1 2.2μF
Tr_1, Tr_2 1/5×CA3086
(Note Tr_1 emitter is pin 13)

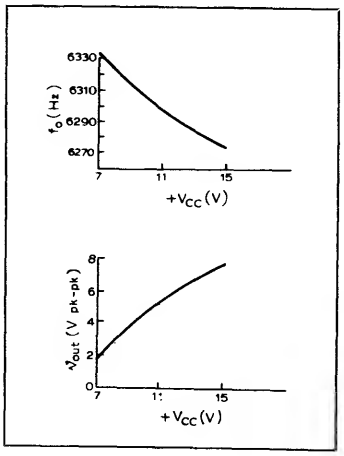


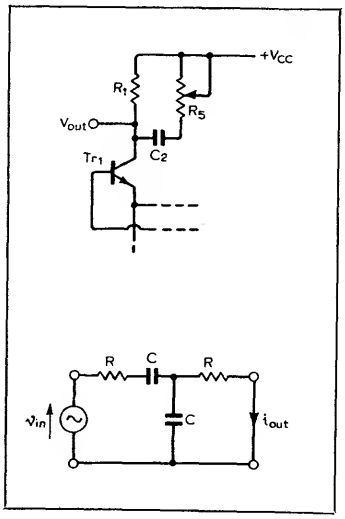
Circuit description
The above oscillator circuit uses a Wien-network which is fed from an emitter-follower Tr_2 and is loaded by a common-base Tr_1. This realization is an example of an RC oscillator which has the Wien-network ideally fed from a voltage source and loaded by a short-circuit as shown below. At the frequency of oscillation $f_o=1/2\pi CR$ Hz, the loop phase shift is zero and the trans-admittance of this frequency-determining network is $(1/3R)$ siemens. Hence, to sustain impedance of the common-base stage only an approximation to a short-circuit load on the network. However, as R_2 is much greater than the common-base stage input impedance, virtually all of the output current from the RC network enters the emitter of Tr_1. If Tr_1 has a reasonably large current gain the base current be neglected to a first approximation, so that the collector current in R_1 is virtually equal to the output current from the RC network. Thus, assuming that the voltage gain of the emitter follower is only slightly less than unity, the amplifier gain $A_z=V_{out}/i_{in}$ is essentially equal to R_1. The circuit will oscillate, theoretically, provided that R_1 is made three times the value of R with C chosen to determine the frequency of oscillation.

In the above circuit, for example, where R was selected oscillations the amplifier must provide a current-to-voltage gain (A_z) of $3R$ ohms to make the closed-loop gain unity i.e. $\beta_y.A_z=1$.
In the circuit arrangement the emitter follower is only an approximation to the ideal voltage source to feed the RC network and the input as 4.7kΩ, R_1 should be $3\times4.7k\Omega=14.1k\Omega$ and in practice, using 5% tolerance resistors, the circuit just oscillated with $R_1\approx15k\Omega$.

Component changes
The useful range of supply voltage is approximately +4 to +20V, but note that changing the supply will change the operating currents and hence







the overall gain of the amplifier. Hence, large changes in supply voltage will change the loop gain sufficiently to either prevent oscillation or to severely distort the output waveform. For example, in the above circuit the oscillations cease at V_{cc} of +6V (having adjusted R_1 with V_{cc} of +9V) and the output waveform becomes clipped on positive peaks when V_{cc} exceeds about +11V. Thus, change of V_{cc} will normally require a readjustment of R_1 for a reasonable sinewave output waveform.
Scale RC values for different oscillation frequencies but note that C scaling only allows R_1: R ratio to be maintained without changing R_1 significantly.

Circuit modifications
- If it is desired to change the frequency of oscillation by changing both the R and C values, but without changing the d.c. operating conditions, then R_1 can be fixed and the a.c. closed-loop gain adjusted by the arrangement shown.

From an a.c. viewpoint R_5 is in shunt with R_1 provided $X_{c_2}<<R_5$ at the frequency of oscillation.
- Another network having the same transfer function as that shown already at the frequency of oscillation is shown on the left.

Again the frequency of oscillation is given by $f_o=1/2\pi CR$ Hz and the required amplifier gain is again $A_z=R_1$ in the ideal case. A practical realization is shown bottom again using an emitter follower and a common-base stage.
The same component values may be used for the same frequency of oscillation.

Further reading
Williams, P. Wien oscillators, *Wireless World*, November 1971, pp. 541-6.
Industrial Circuit Handbook, SGS-Fairchild 1967, pp. 42/3.

Op-amp Wien oscillator

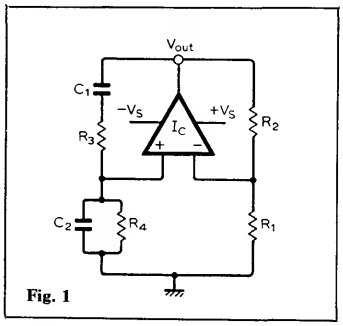
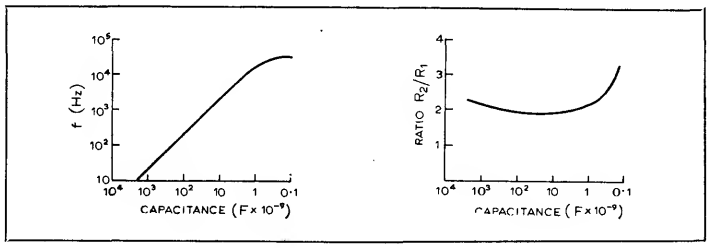


Fig. 1

Typical data
$\pm V_S$ $\pm 15V$
IC 741
R_3, R_4 4.7kΩ $\pm 5\%$
C_1, C_2 0.1μF
Frequency 355Hz
R_1 3.4kΩ, R_2 6.6kΩ
Harmonic distortion 0.4%
Output 26V pk-pk up to 14kHz
Drops to 16V pk-pk at 27kHz



Circuit description
This is a single-frequency oscillator circuit which may be envisaged as a bridge network, where oscillation will occur when the bridge is balanced and the differential input to the amplifier is near zero. Positive feedback is applied via two reactive arms, and negative feedback via the resistor potential divider R_1, R_2. The gain of this loop is $(R_2+R_1)/R_1$. The gain of the positive feedback loop is real at a positive loop frequency that makes $A_+=1+R_3/R_4+C_2/C_1$ and if $R_3=R_4$, $C_2=C_1$, then $A_+=3$. Oscillation then occurs when $A_-=3$, or when $R_2 \approx 2R_1$. This oscillatory condition will require a minimum distortion to maintain a stable output. However, if the A_+ gain falls below this value, oscillation will stop due to the negative feedback being more than the positive feedback, and if the gain increases, the output amplitude will increase until it is limited by non-linear distortion. This could be the power supply limitations or additional network limiting. In general the frequency of oscillation is given by $f=1/2\pi\sqrt{C_1C_2R_3R_4}$ Hz for C in farads, and R in ohms.

Component changes
- Varying $C_1(=C_2)$ over the range of 4.7μF to 220pF provides frequency range above. (Slew rate-limiting of the op-amp causes fall-off at lower C values.)

- Simpler technique maintains C constant, but demands ganged potentiometer for R_3 and R_4 for frequency adjustment with single control, i.e. ratio R_3: R_4 is maintained constant.

- Amplitude limiting is available using either of the additions shown in Fig. 2.

- Nominally R_5 should be much greater than R_2, and R_5 in parallel with R_2 should be less than $2R_1$ when the diodes are conducting (see Fig. 2).
R_1 3.3kΩ, R_2 8.62kΩ
R_5 22kΩ, frequency 354±1Hz
Vs ±12V
Amplitude is stable then for power supply increases up to ±18V. With diode or zener diode limiting, the frequency is more independent of the power supply, but is more dependent on the break level of the limiting network. Another advantage is that instantaneous oscillation is available at low frequencies. With no limiting, time for build up of amplitude is frequency dependent.
- Note that at high frequencies, since gain of amplifier is finite, it is more noticeable that a small differential input must exist, which demands an adjustment of the R_2: R_1 ratio (see second graph).

Circuit modifications
Circuits above, Figs. 3 to 5, provide exactly the same performance as the basic circuit. Notice that the output and ground terminals are shifted depending on op-amp connection (see Nullors, card 1).

With limiting network, typical performance given below.
Diode limiting for circuits 1, 3, 4, 5.
Outputs: 16.8, 16.8, 16, 15.6V pk-pk, harmonic distortion: 0.95%, 0.95%, 0.9%, 0.89%, respectively.
R_2 6.39kΩ, R_1 3.61kΩ for R_5 22kΩ.
Zener limiting for circuits 1, 3, 4, 5.
Outputs: 21.5, 26.5, 26.5, 19V pk-pk, frequency: 350, 352, 352, 352Hz, harmonic distortion 5, 5.9, 5.9, 5.1%, respectively.
R_2 6.9kΩ, R_1
In general, a trade can be made between distortion and amplitude stability.

Further reading
Williams, P. Wien Oscillators, *Wireless World*, Nov. 1971, pp. 541-6.

Cross references
Set 25, cards 6, 5.
Set 21, card 4.

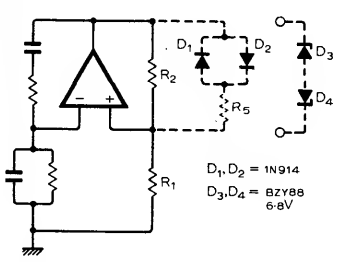


Fig. 2

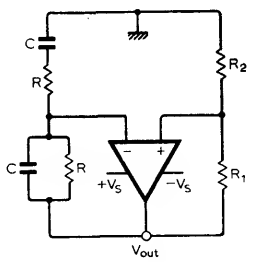


Fig. 3

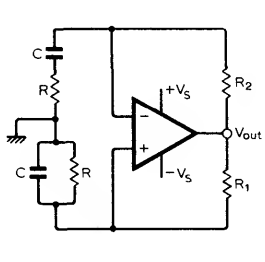


Fig. 4

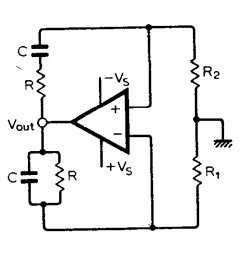


Fig. 5

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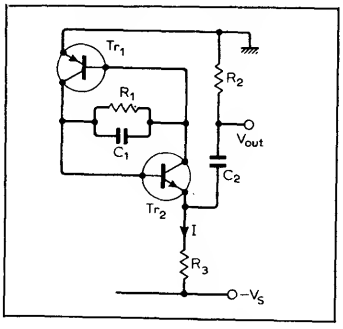
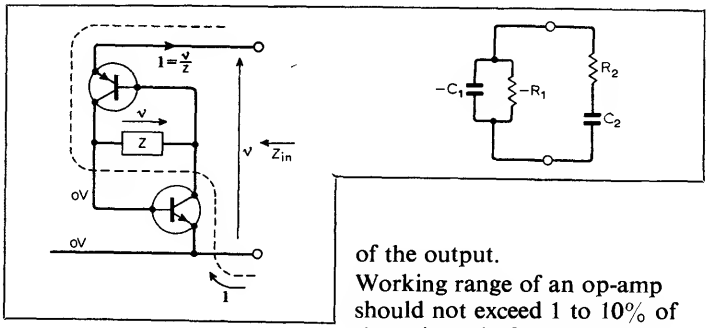
Micropower oscillator



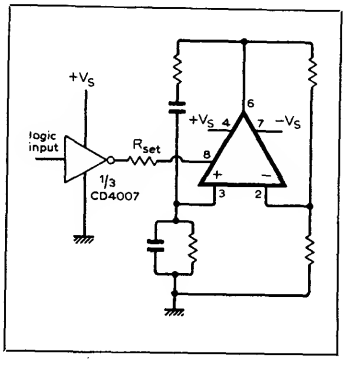
Typical data
$-V_s$ -20V, R_3 220k
This combination approximates a constant current source
I 86μA
R_1 3.85kΩ, R_2 1.5k $\pm$5%
C_1 100nF, C_2 220nF
V_{out}: 54mV pk-pk
frequency 436Hz
Tr_1 BC126, Tr_2 BC125



Circuit description
This is one form of a negative impedance converter circuit. It may be considered as a two terminal device, and be inserted in a constant current path that may already exist in a circuit. The circuit will provide a low voltage amplitude sinusoidal oscillation (but not necessary low distortion) with a minimum of components, no biasing being necessary but the choice of components is critical. Provided the appropriate gain and phase shift are possible, transient analysis shows that oscillations will build up exponentially in such a network after shock excitation, if the circuit losses are negligible. This is achieved by presenting a negative resistance across an existing circuit resistance. Oscillations are sustained when the average value of the negative resistance provides the correct ratio for the frequency chosen.
In the above circuit, V_{be} of the transistor is neglected, and hence the direction of current through the impedance Z must be as shown: through the collectors. The impedance presented at the input terminals, then is $Z_{in}=v/(-v/Z)=-Z$. The loop impedance for the given network is:

$$R_2+\frac{1}{j\omega C_2}+\frac{-R_1/j\omega C_1}{-R_1-1/j\omega C_1}$$

The numerator reduces to $1-\omega^2C_1R_1C_2R_2+j(\omega C_1R_1+\omega C_2R_2-\omega C_2R_1)$. For oscillation, the loop impedance should be zero giving $C_1/C_2+R_2/R_1=1$ or $R_1=2R_2$, $C_1=C_2/2$ and $f=1/2\pi\sqrt{C_1R_1C_2R_2}$.



Component changes
Minimum value of R_1 2.73kΩ
Frequency 320Hz
Variation of output with R_1 shown over.
R_1 maximum 2.9kΩ before resistors for optimum performance.

Circuit modification
- Micropower operation with the classical Wien network (this series, card 4) is possible with the LM4250 programmable operational amplifier. For a fixed dual polarity supply, one external resistor determines the quiescent current and consequently the slew rate and gain-bandwidth product. Voltage range is $\pm$1 to $\pm$18V. Care is necessary in the choice of frequency in relation to the programmed set-current because of the slew-rate and gain-bandwidth dependence. For a cisoidal waveform

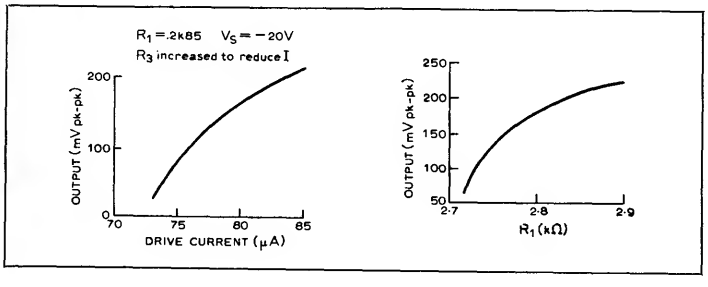
$$\text{frequency (Hz)}=\frac{\text{slew rate}}{2\pi V_{max}}\text{(V/s)}$$

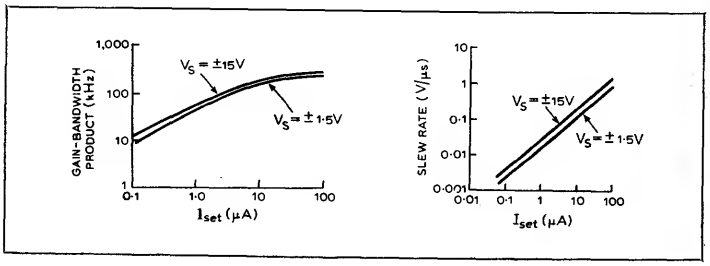
where V_{max} is the peak value of the output.
Working range of an op-amp should not exceed 1 to 10% of the unity gain frequency to avoid severe unbalance at the bridge input, i.e. at $I_{set}=1\mu$A, gain-bandwidth product is 70kHz. If oscillator frequency is 700Hz, amplifier gain is 100, and hence input required is 1% of output. If set current is reduced to 0.1μA, then for same frequency gain is only 10. Hence for the same output greater unbalance required at the input.
- Normal diode limiting possible at much lower currents.
- High values of resistance usable to minimize power drain, however stray-capacitance effects may then be significant for designed frequency. High input impedance of op-amp will not load bridge arms.

Oscillator may be gated using a c.m.o.s. inverter to sink the programmed set-current, shown left.

Further reading
Braun, J. Equivalent n.i.c. networks, nullators and norators, *IEEE Trans.* vol. CT-14, 1967.
Linear Integrated Circuits, LM4250, National Semiconductor.

Cross references
Set 10, card 8.
Set 25, cards 8, 1, 4.





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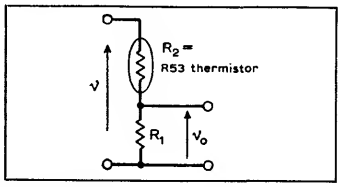
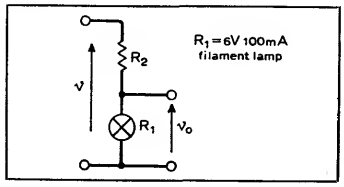
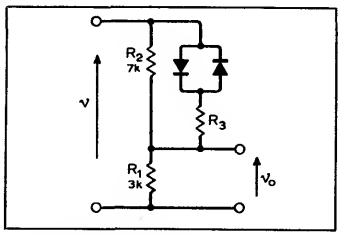
Amplitude-control methods



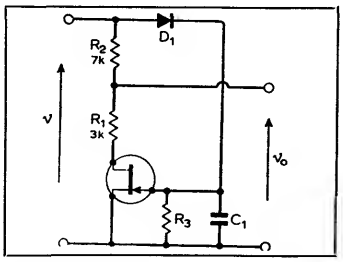
Thermistor
A bulk semiconducting resistor with negative temperature coefficient. Placed in series with a resistor, and with an increasing voltage applied, the thermistor is heated by the resulting flow of current; its resistance falls and the attenuation of the network decreases. There will be a single amplitude at which a desired attenuation is achieved. If the network is incorporated into an oscillator, where the frequency-determining network has zero phase shift together with the same attenuation (at a particular frequency) then oscillations will be sustained.



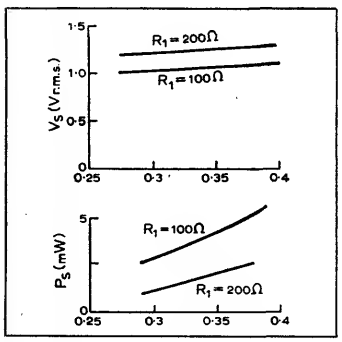
Lamp
Place in series with a resistor which is low enough to permit sufficient current to heat the lamp. As the voltage increases, the lamp resistance rises and again the attenuation decreases. The lamp can operate at a higher temperature than the thermistor and is less sensitive to ambient temperature changes. Its power consumption is considerably higher and the sensitivity to amplitude changes markedly less (dissipation for significant temperature rise >50mW for most lamps—as little as 3mW for thermistors designed for this application).



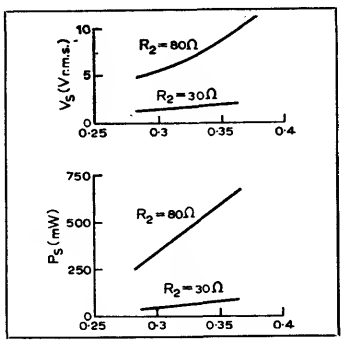
Non-linear network
Self-sustaining oscillation can also be achieved by passing the feedback through a non-linear network. At low amplitudes the diodes are non-conducting and the attenuation is determined by R_1 and R_2. For larger peaks, the diodes conduct and R_3 appears in parallel with R_3 increasing the attenuation. There will be a single amplitude of input at which the average value of the output meets the condition. There is a compromise between distortion and sensitivity of the amplitude to small changes in the resistor values.



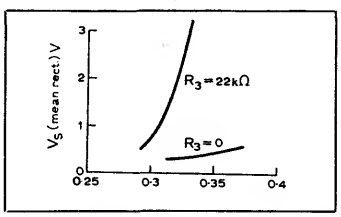
Peak rectifier
A field-effect transistor has an output slope resistance that is moderately linear and is controlled by the gate-source voltage. If the amplitude of the input increases, the peak rectifier has an increased output. It is applied to the gate of a p-channel junction f.e.t. reverse biasing it and increasing its resistance. This decreases the a.c. attenuation of the network. The range is small as the f.e.t. cannot accept a large drain-source voltage in this mode without increasing the distortion.



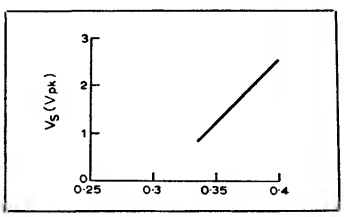
Thermistor
Maximum device dissipation of 3mW for the quoted device changes its resistance by two orders of magnitude. The rise in temperature is relatively small and the final amplitude when used in an oscillator is slightly temperature dependent. A 25% change in the transfer function of the oscillator (due to either passive components or fall in amplifier gain at high frequencies) would be accommodated by an amplitude change of as little as 2% when oscillations re-stabilize.



Lamp
For the same change in the oscillator network (25%) the amplitude using a lamp might only be stabilized to within 20-40%. The power consumption is 10-100 times greater making it more difficult to choose a suitable amplifier. The lamp costs less and, operating at a higher temperature, is less affected by ambient changes. To extend the lamp life it is advisable to limit the power input which brings its performance somewhat nearer to that of a thermistor.



Non-linear network
The ratio R_2: R_1 is set to give an attenuation less than that needed to inhibit oscillation. The diodes begin to conduct when the peak voltage across R_2 exceeds 0.6V. At some higher voltage the attenuation exceeds the critical value. With R_3=0 this state is rapidly reached and the amplitude is controlled within reasonable limits— 50% change for a change in the oscillator network of 15%. With R_3 of 22kΩ the amplitude has to change by a much larger amount to cope with a corresponding change in the network—in this example a greater than 5: 1 range. In return the resulting distortion is much lower.



Peak-rectifier/f.e.t.
The network consisting of D_1, C_1, R_3 feeds the gate of the f.e.t. with a voltage equal to the peak input less the diode forward drop. For input amplitudes above 0.6V peak the f.e.t. becomes reverse-biased with a drain-source resistance increasing from about 500Ω to many times that value. At high values of reverse bias, the range of drain-source voltages for low distortion is reduced. This conflicts with the increased p.ds across the network that cause the bias and limits the range attenuations that can be achieved—a range of about 12% in this case which is sufficient to cope with the usual spreads.

wireless world circard

Baxandall RC oscillator

Circuit description

The circuit below is a bipolar transistor version of a Wien network oscillator due to Baxandall. In comparison with its more common operational amplifier form it has the merit of simplicity. The usual negative supply rail for the operational amplifiers may be dispensed with, and only two resistors (R_1 and R_2) are required in addition to the Wien bridge resistors (R_3 and R_4) and frequency-determining components (R and C). Also, the Wien network resistors are arranged so that the circuit is self-biasing. This circuit simplicity is achieved at the expense of departure of the frequency of oscillation from the ideal value of $f_o = 1/2\pi RC$ Hz.

In the ideal case, the circuit would just oscillate when $R_4/R_3 = 2$ but the finite gains in the transistors cause the critical condition to be achieved with an R_4/R_3 ratio somewhat in excess of this value. Also, as the supply voltage is varied the operating conditions of the transistors, and hence their gains, change which will require readjustment of the R_4: R_3 ratio either to sustain oscillation or to restore the output waveforms to reasonably undistorted sinusoids. Although, with the component values shown, the output waveforms from Tr_1 and Tr_2 collectors are of different magnitudes, they have the useful feature of being in antiphase.

Component changes

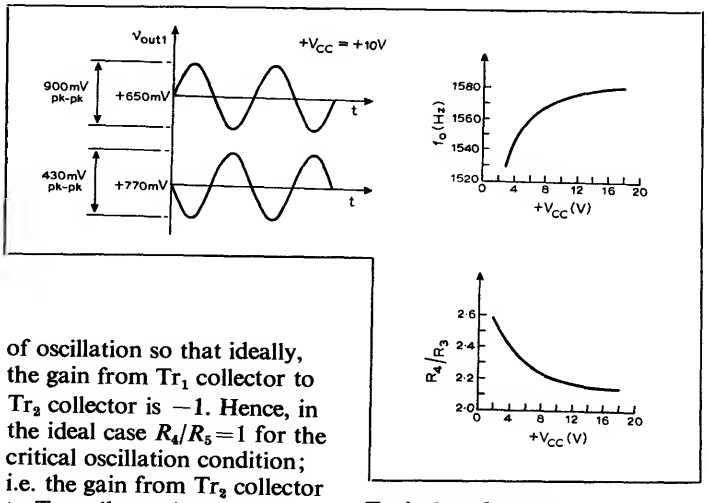
Useful supply range +3 to +20V
Useful range of R 100 to 100kΩ
Useful range of C 1n to 10μF
With given R values the frequency of oscillation can be changed without changing the d.c. conditions by changing the capacitor values only.

Circuit modifications

The output waveforms from Tr_1 and Tr_2 collectors can be made of equal amplitude as well as being in antiphase, without changing the frequency of oscillation, by scaling the frequency-determining RC components of the Wien network as shown below. With this arrangement the impedances of the series and parallel RC components are the same (R_2) at the frequency of oscillation so that ideally, the gain from Tr_1 collector to Tr_2 collector is −1. Hence, in the ideal case $R_4/R_5 = 1$ for the critical oscillation condition; i.e. the gain from Tr_2 collector to Tr_1 collector is also −1 giving a closed-loop gain of +1. In practice, with the circuit values R 10kΩ, C 10nF the frequency of oscillation was virtually unchanged, and R_4/R_3 was typically 1.1 to sustain oscillations with V_{out_1} and V_{out_2} typically 1 volt pk-pk and 980mV pk-pk respectively. A closer approach to the ideal state can be obtained by using two inverting operational amplifiers in place of Tr_1 and Tr_2 as shown below.

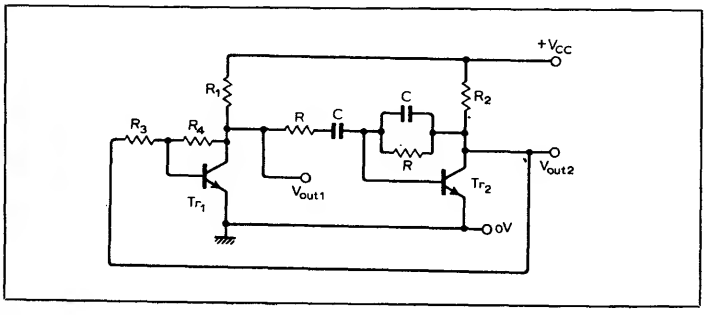
R, C, R_3 and R_4 are direct replacements from the bipolar transistor version and A1 and A2, which could be 741s, replace Tr_1 and Tr_2 respectively. The same scaling of the R and C values to provide equal-amplitude outputs may be used as before. These outputs are now available from low output impedance points.

As with other oscillator circuits, a bandpass filter may be obtained by setting the gain (by adjusting the ratio R_4: R_3) just below the value needed to produce oscillation and injecting the signal through a reasonably high resistance at the inverting input to A_1. This can also be achieved with the bipolar transistor version by injecting the signal at Tr_1 base, where the need for a high impedance source is more stringent since this point is an imperfect virtual earth.



Typical performance

+Vcc+10V, 2mA
R_1, R_2, R 10kΩ, C 10nF
R_3+R_4 10kΩ (realized with 10kΩ potentiometer to adjust loop gain)
Tr_1, Tr_2 1/5×CA3086
(Note Tr_1 or Tr_2 emitter is pin 13)

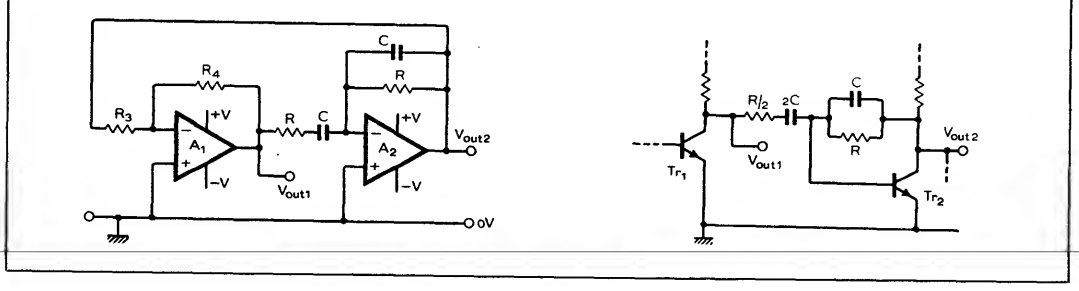


Further reading

Williams, P. Wien Oscillators, *Wireless World*, Nov. 1971, pp. 541-7.

Cross references

Set 1, card 3.
Set 10, card 8.



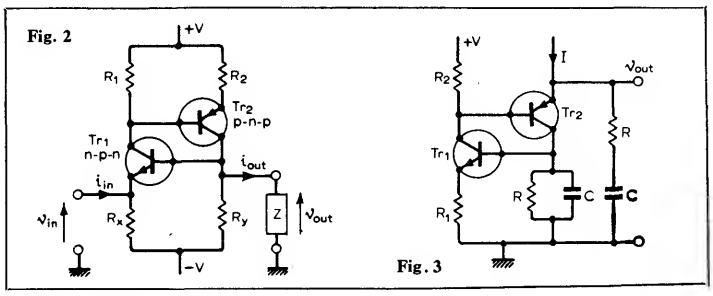
N.I.C. oscillators

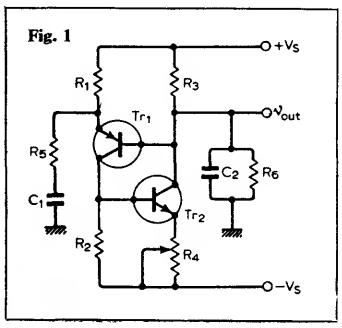
Circuit description

A negative impedance converter is a two-port active device which if loaded at one port with an impedance Z, can provide an impedance $-nZ$ at the other port. If the impedances are frequency dependent, then a frequency constraint exists, for at only one single frequency the serial and parallel RC networks have equivalent magnitudes and the

Typical data

Tr_1 BC126, Tr_2 BC125
R_1, R_2 10kΩ, R_3 5kΩ
R_4 4.66kΩ R_5, R_6 4.7kΩ
C_1, C_2 0.1μF
V_S $\pm$5V
Ratio required of R_2: R_4 slightly greater than two to allow for component tolerances
Frequency 373Hz (maximum 20kHz)
v_{out} 1.55V pk-pk, 0.3V offset





appropriate phase angle to the make the loop phase shift zero. The Fig. 1 circuit is of similar form to Fig. 2 for which an approximate analysis is given. Assume the base-emitter voltages are negligible. Then the signal v_{in} will appear as v_{out}. The input signal current i_{in} comprises v_{in}/R_1 and $i_{in}-v_{in}/R_1$ up through Tr_1. The voltage across R_1 is then $i_{in}R_1-v_{in}$ which must be that across R_2. Therefore the emitter, thus collector, current of Tr_2 upwards is $i_{in}R_1/R_2 - v_{in}/R_2$. Thus i_{out} is $-(v_{in}/R_2+i_{in}R_1/R_2 - v_{in}/R_2)=-i_{in}R_1/R_2$. If an impedance Z is across the V_{out} terminals, then

$$Z_{in}=v_{in}/i_{in}=v_{out}/i_{in}$$
$$=-\frac{v_{out}}{i_{out}R_2/R_1}=-\frac{R_1Z}{R_2}$$

If $R_1=R_2$, $Z_{in}=-Z$.

Component changes

Another oscillator using a different n.i.c. is shown above. Separate voltage and current supplies are necessary, but low level operation is possible. Typically, for V of 1V, I of 70μA, circuit will oscillate ($f=1/2\pi RC$) to provide a peak output of about 1.2V. An advantage of these circuits is that the frequency-tuning networks have a common ground point, and a minimum of components is used. When these circuits are analysed using nullor concepts (card 7), the similarity is more obvious. The equivalent representations are given in the circuits showing nullator, norator interchange. Bridge oscillators using operational amplifiers (card 4) can also be considered as a form of n.i.c. oscillator. For the above general case

$v_{Z3}=v_oZ_3/(Z_3+Z_4)=v_{Z2}$
$i_2=v_{Z2}/Z_2=v_oZ_3/(Z_3+Z_1)Z_2-i_1$

From Millman's theorem,

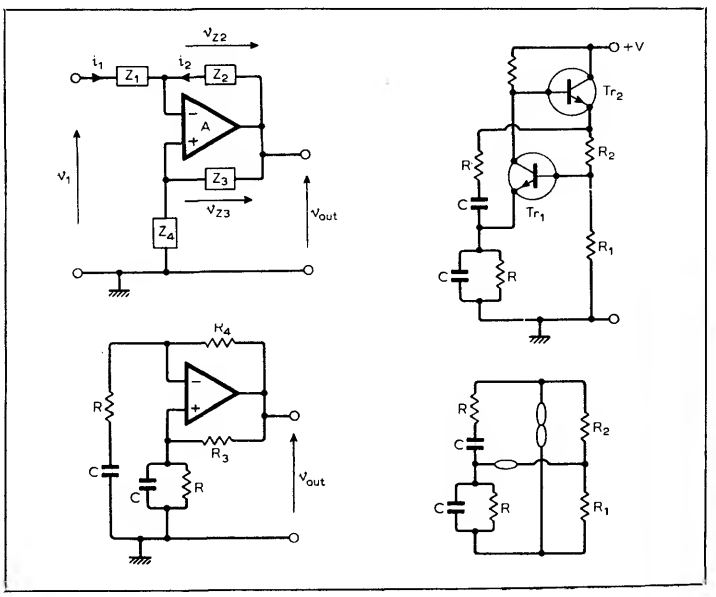
$v_-=v_1y_1+v_0y_2/(y_1+y_2)$
$v_+=v_0y_3/(y_3+y_3)$

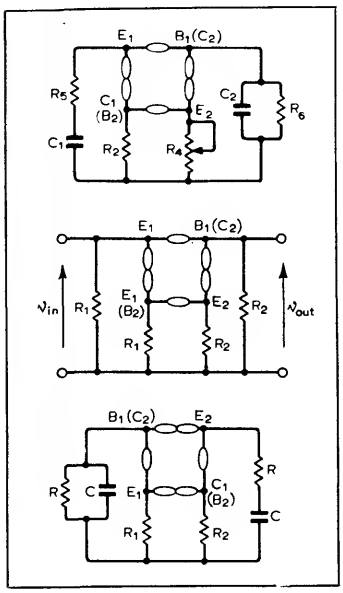
For high A, $v_-=v_+$ and

$$\frac{v_1}{v_o}=\left(\frac{y_1+y_2}{y_3+y_4}\right)\frac{y_3}{y_1}-\frac{y_2}{y_1}$$

Also $Z_{in}=v_1/i_1=$

$$\frac{-v}{v_o}\left(\frac{Z_3+Z_4}{Z_3}\right)Z_2$$





If $Y_2=Y_3$, then $Z_{in}=Z_1-Z_4$
If $Z_1=0$ $Z_{in}=-Z_4$

A parallel tuned circuit of dynamic impedance L/Cr connected across the input terminals would be the basis for an oscillator, if the magnitude of Z_4 is made equal to r. Specifically, $Z_{in}=-Z_4.Z_2/Z_3$. Hence if Z_4 is a parallel RC network, then a series RC network across the input, with an appropriate ratio of R_4: R_3 provides one form of Wien bridge oscillator. The nullor concept allows certain nullor/norator interchanges which provide an alternative Wien shown below, which again can be analysed from a n.i.c. concept. A discrete version is shown above, where if the transistors gains are high, the ratio R_2:R_1 approaches two.

Further reading

Pasupathy, S. Transistor RC oscillator using negative impedances, *Electronic Engineering*, December 1966.
Newcomb, R. W. Active integrated circuit analysis, Prentice-Hall, 1968.
Pasupathy, S. Equivalence of LC and RC oscillators, *Int. J. Electronics*, vol. 34, no. 6, pp. 855-7.
William, P. Wien oscillators, *Wireless World*, Nov. 1971, pp. 541-6.

Cross references

Set 25, cards 1, 5.

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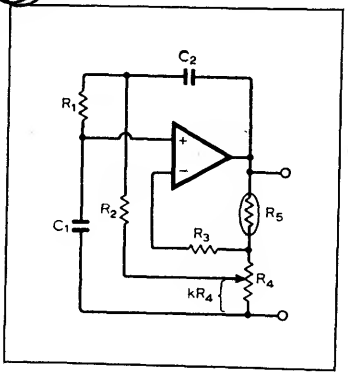
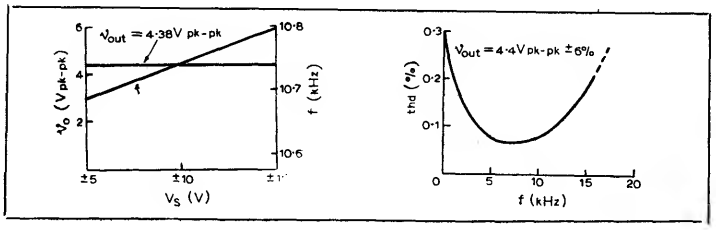
Single-element-control oscillators—1



Typical performance
IC 741
Supplies ±15V
R_1, R_2 (=R) 10kΩ
R_3 15kΩ, R_4 1kΩ log
R_5 ITT thermistor R24
C_1, C_2 (=C) 1nF
f 1.5kHz to 20kHz

$$f=\frac{\sqrt{1-k}}{2\pi CR}$$

provided $R_2 \gg R_4$



Circuit description
As described earlier the lead/lag network, C_2R_2 followed by C_1R_1, is an alternative to the Wien network. If the network is driven by two amplifiers (see ref.) then it is possible to vary the frequency of oscillation by changing the gain of one amplifier, without changing the condition for sustaining the oscillations. This simplifies the amplitude control circuitry but still requires two amplifiers, one with variable gain. If instead the impedance level of the frequency dependent network is much greater than the resistance of the amplitude-controlling network, one amplifier can be eliminated. Resistor R_2 is tapped onto R_4. As k is reduced to zero the frequency of oscillation reverts to that of the basic Wien bridge/lead-lag oscillator viz. $1/2\pi RC$. As $k \rightarrow 1$ the frequency $\rightarrow 0$. This leads to a practical range of frequencies in excess of 10: 1 on a single control without any serious increase in distortion. The component count is comparable to that with conventional oscillators, but the need for a twin-gang control which normally requires a good match is avoided. A further advantage of this circuit is that low frequencies are obtained without using large values of capacitance. Provided the thermistor has a long enough thermal time constant, frequencies down to 10Hz are possible with capacitances of 0.1μF.

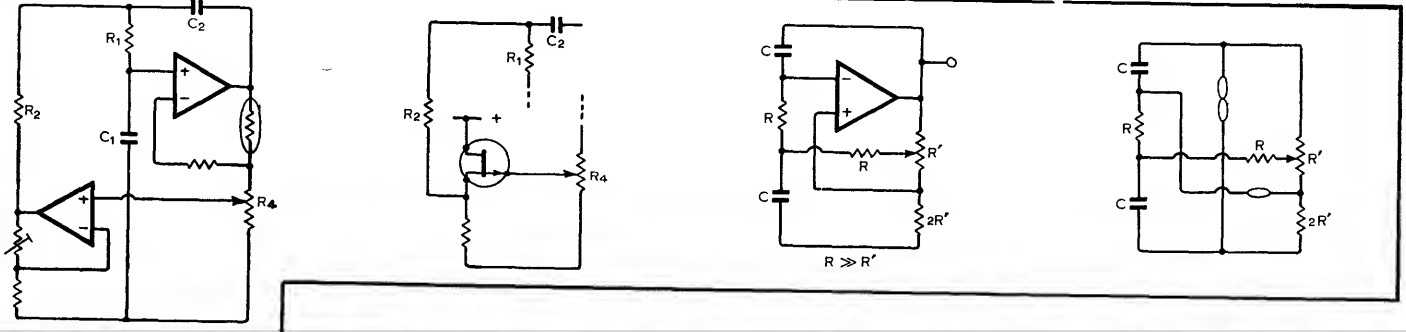
Component changes
IC: any general-purpose compensated op-amp. For lower frequencies, f.e.t. input op-amps allow the use of larger resistors. This also minimizes the loading on the potentiometer and widens the range that can be covered by variation of k alone.
Supplies: not critical. Should be appreciably greater than required peak-peak output if rapid thermal stability of thermistor to be achieved. Typically ±6 to ±15V.
C_1C_2: to suit frequency range, but 220pF to 1μF possible. Normally $C_1=C_2=C$.
R_1, R_2: 1k to 1MΩ. High values only possible if f.e.t. op-amp available, e.g. CA3130. Allows very low frequency with suitable amplitude control mechanism. Normally $R_1=R_2=R$.
R_4: selected to suit thermistor. $R_4 \ll R$, typically 100 to 470Ω.
R_3: not critical. Minimizes offset due to unbalanced input currents. Excessive offset disturbs amplitude control by permanently heating thermistor.

Circuit modifications
- Adding a unity gain buffer amplifier between R_4 and R_2 removes interaction permitting wider range for fixed Cs. End-resistance effects on R_4 prevent $k \rightarrow 1$ and a voltage gain >1 in the buffer stage corrects for this. Some versions of this circuit can achieve a range in excess of 100: 1 on a single potentiometer.
- A simpler buffer may suffice in some applications where only the impedance levels are critical. A source follower removes the loading on R_4 though the maximum buffer gain is unlikely to exceed 0.9, i.e. range of frequencies is restricted.
- The original circuit again has a related form in which output and ground on the bridge are interchanged as are the inverting and non-inverting inputs. This is in line with the results on the basic Wien bridge oscillator (cards 2, 3, 4). Performance is basically similar to the original. The advantages of alternative configurations are that different components are grounded which can simplify frequency and amplitude control.
The nullor form is shown. It gives no information on phasing can make it easier to generate new versions. An alternative viewpoint is that of shifting the groundpoint in the system.
- Further oscillators (not shown) interchange the locations of the Cs and Rs to make lag-lead oscillators. These can be used with inverting buffer amplifiers where it is required to reduce the frequency of oscillation below the basic value $1/2\pi CR$.

Further reading
Sun, Y. Generation of sinusoidal voltage (current) controlled oscillators for integrated circuits, *IEEE Trans.* 1972, CT-19, pp. 322-8.

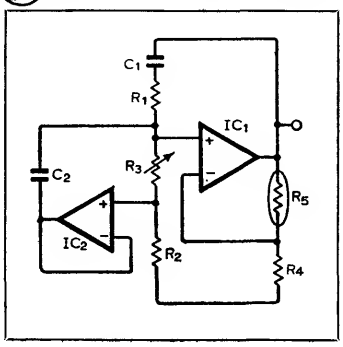
Cross reference
Set 25, card 10.

Circuit modifications



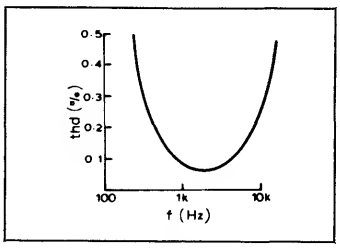
wireless world circard

Single-element-control oscillators—2



Typical performance
$IC_{1,2}$ 741
Supplies ±15V
R_1, R_2 2.2kΩ
C_1, C_2 0.047μF
R_3 2MΩ log
R_4 470Ω
R_5 ITT thermistor R54
At f 1kHz, v_o 6.4V pk-pk
T.h.d. 0.1%
f_{max} >18kHz as $R_3 \rightarrow 0$
f_{min} <120Hz as $R_3 \rightarrow 2M\Omega$

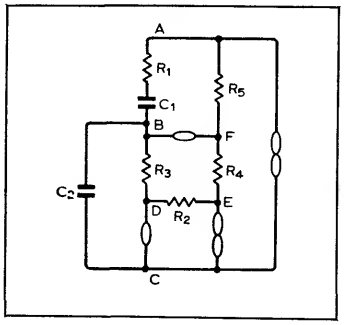
Circuit description
A circuit given by Brokaw (see ref.) used a modified form of Wien bridge oscillator. In it, one of the frequency determining resistors is varied, while a second amplifier has a variable gain controlled by that same resistor. The form of circuit used (see over) gave a wide range of frequencies on a single control with no change in the amplitude control condition. By drawing the nullor equivalent circuit the alternative form was found in which one of the amplifiers was used as a voltage follower. This allows the substitution of specially optimized voltage followers such as the LM310 to minimize errors in this stage. For even simpler circuits less demanding of performance



emitter or source-followers can be used. The frequency of oscillation is $1/2\pi\sqrt{R_1R_3C_1C_2}$ provided that $R_2=R_1$ and the amplitude-maintaining condition $R_5=R_4$ is maintained.

N.B. R_3 can be replaced by any other element or device that behaves as a linear resistor. If a photo-conductive cell is used the frequency becomes light sensitive and a wide range of light intensities can be covered. Oscillator amplitude stability ±1% from 120Hz to 15kHz, V_s ±10 to ±15V.

Component changes
IC_1: any compensated op-amp. For low frequency operations, the increase in R_3 results in greater errors due to op-amp input currents, and f.e.t. input stages would be better. As indicated above, 100 : 1 range is readily obtained with general purpose units.
IC_2 can be replaced by a voltage follower, source follower, Darlington-connected emitter-follower etc. A useful feature is that d.c. offset in this stage has no effect.
Supplies: Not critical. Usual range 5V to ±15V for op-amps. Restriction mainly placed by choice of amplitude control devices/circuits.
C_1, C_2 to suit frequency range but typically 1nF to 1μF.
$C_1=C_2$.
R_1 1k to 100kΩ.
R_3 Range should be wide if frequency range is to be great



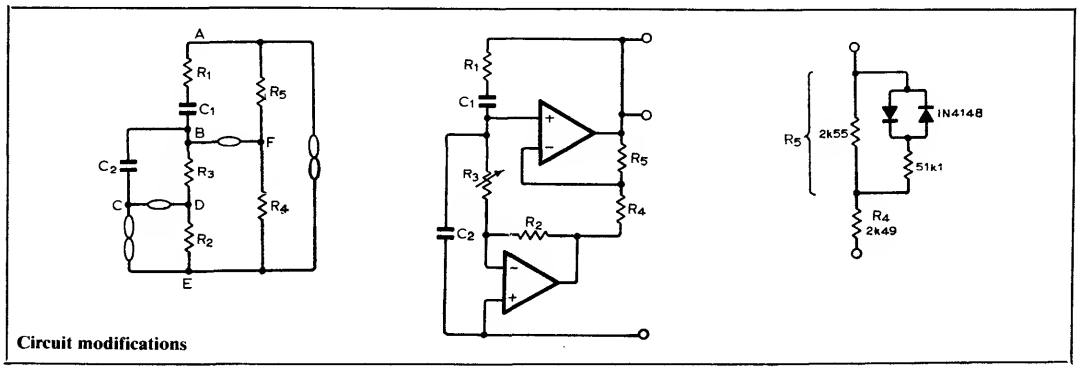
since $f \propto 1/\sqrt{R_3}$. Typically R_3 may range from 100Ω to >1MΩ.
R_2 For $C_1=C_2$, $R_4=R_5$ for amplitude control and $R_2=R_1$ is the remaining condition.
R_4 chosen to suit the particular thermistor used—see manufacturer's data.

Circuit modifications
● The input of each amplifier is replaced by a nullator, the output-ground port by a norator and the circuit is redrawn in this nullor form in Fig. 1. Points C, E and A may be at arbitrary relative potentials because of these norators. One alternative configuration having the same property is Fig. 2. This can also be interpreted as a shift of ground point from E to C. Re-pairing of these nullators and norators leads to the practical circuit of Fig. 3 given in a recent reference. It is a high performance oscillator with a frequency range 200: 1 but again uses f.e.t. input amplifiers. A number of other oscillators can be similarly developed by moving the norators to change their common point, and then cross-pairing the nullators and norators in different ways. The disadvantage of the nullor approach is that it gives no information as to the phasing of the amplifiers. This has to be deduced once the format of the circuit has been established by considering the feedback paths. The advantage is that by generating fresh circuits, particular units will have the merit of having anti-phase outputs, grounding of more convenient components or will suggest simplifications not apparent in the original.

● A suitable amplitude-control network for the circuit of Fig. 3 is suggested in ref. 1 and is shown below As the amplitude increases the diodes conduct and the average value of R_5 is reduced until it equals R_4—the condition for stable oscillations.

Further reading
Brokaw, P. FET op-amp adds new twist to an old circuit, *EDN*, June 3, 1974, pp. 75-7.

Cross reference
Set 25, card 9.



Circuit modifications

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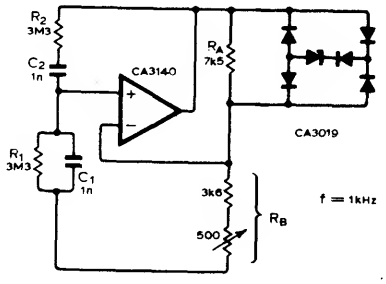
Set 25: Up-date

The reference quoted brings out two points worth noting. Amplitude control by non-linear feedback is a known method of rapidly stabilizing an oscillator. The disadvantage is that it can be difficult to combine stable amplitude and low distortion, the degree of non-linearity for the first inhibiting the second. One cause of distortion is unequal clipping because of unmatched zeners. By placing a zener inside a full-wave bridge of matched diodes the clipping is identical for both polarities minimizing distortion. The diodes are part of an array and the temperature coefficients of zener and diodes are said to achieve good temperature compensation. The amplifier has p-m.o.s. input devices allowing large resistors and hence small capacitances for low-frequency oscillations. The high slew-rate allows full-output (~16V pk-pk, quoted) up to 180kHz. Better use of the high gain-bandwidth follows from scaling the series impedances down and reducing the minimum gain for oscillation. The modified relationships are $f = 1/2\pi\sqrt{R_1R_2C_1C_2}$ and $\frac{R_A}{R_B} = \frac{C_1}{C_2} + \frac{R_2}{R_1}$.



References

Bailey, M. Op-amp Wien bridge oscillator, *Wireless World*, vol. 83, Jan. 1977, p.77. Application Note CA3140, RCA.

Voltage control can be applied to lead-lag and Wien oscillators in various ways. One approach is via the Blumlein-Miller effect of Fig. 1 where the input resistance is reduced to very small values as $A > -\infty$. This requires grounded resistances and to modify the passive network to permit this the sustaining amplifier requires a controlled gain and differential inputs (Fig. 2). The resistors R′ then represent a pair of circuits as in Fig. 1 with voltage-controlled amplifiers providing the variable gain to set R′. Such an amplifier (Fig. 3), similar to Set 22, card 8, can also be used as the sustaining amplifier of Fig. 2 with the control voltage pre-set or driven from a peak or mean-sensing circuit for amplitude control. The number of amplifiers can be reduced to two in a circuit related to that of card 9. The low-gain needed for sustaining oscillations (~3) is defined by the resistor R_F between the emitters while the variable gain amplifier setting the frequency can be as in Fig. 4. By extension the Blumlein-Miller effect can be applied to LC oscillators to replace a capacitor that normally appears in a feedback path by either a grounded capacitor or one connected across a separate amplifier. If A_1 is fixed to sustain oscillations, then A_2 varies the effective capacitance and hence the frequency without disturbing the amplitude condition.

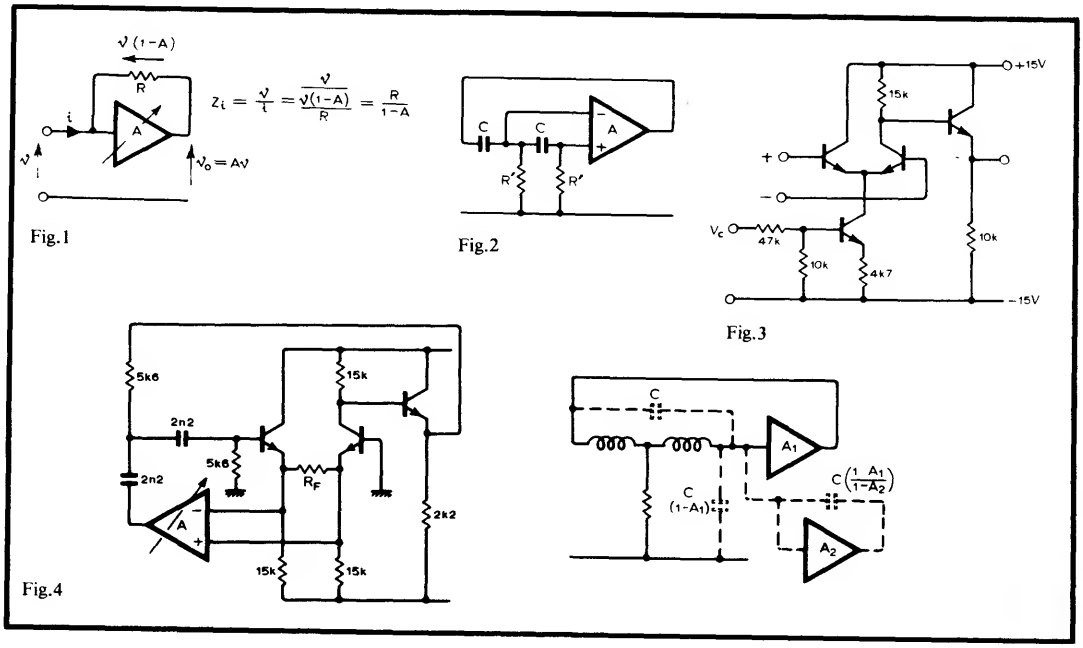


Fig.1

Fig.2

Fig.3

Fig.4

Saha, S. K. Electronically tunable RC sinusoidal oscillator, *IEEE Trans. Instrum. & Meas.*, vol. 24, June 1975, pp. 156/9.

Sun, Y. Generation of sinusoidal voltage (current) — controlled oscillators for integrated circuits, *IEEE Trans. Circuit Theory*, vol. CT-19, March 1972, pp. 137-41.

Passive and active networks

T-networks. The parallel or twin-T network is widely used to obtain a sharp null at a given frequency. By combining this with a small amount of positive feedback oscillations may be sustained at the null frequency if the network is in a negative feedback path i.e. inhibiting oscillation at all other frequencies. For other ratios of parallel and series arm impedances, an inverted output of reduced magnitude is obtained, and this can be applied directly to the inverting input of an amplifier. An apparently new oscillator follows from a change in ground point on the T-network or by redrawing the circuit in nullor form. The output is still applied between A and C and the amplifier is driven by the resulting p.d. between B and C. The network now has an in phase output slightly greater than its input. If the original transfer function T_1 is negative then the new transfer function becomes $T_2 = 1 - T_1$ i.e. $> +1$. A second network has a minimum response at a given frequency and can also be used as negative feedback combined with resistive positive feedback to initiate oscillations. The network is the Bridged T, Fig. 2. Inverting it yields a network with a peak in its response if the output is taken between B and A, and this is the previously described lag-lead network. The response is identical to that of corresponding lead-lag and Wien networks.

The oscillators may be interpreted as (i) frequency dependent n.f.b. with a minimum value at a given frequency just insufficient to neutralize the fixed positive feedback. (ii) frequency-dependent positive feedback just large enough at the same frequency to overcome the fixed negative feedback. Alternatively they may be recognized as particular forms of the bridge oscillators described in the previous set of Circards.

Phase-shift networks. Cascaded RC networks produce a lagging phase-shift while attenuating the signal. A minimum of three sections is needed if the phase-shift is to reach 180° at a finite frequency. With three identical sections the attenuation for this condition is large requiring an amplifier with a gain of -29 to sustain oscillation. The amplifier may be an ideal voltage-amplifier (low output-impedance high input-impedance). Thus networks I or II (Fig. 4) may be used with an amplifier of voltage gain A_v with signal flow as in Fig. 6(a) or with an amplifier of current-gain A_i with signal flow as in Fig. 6(b). Network II can be adapted to provide a current output into a short-circuit, having the same phase relationship to the input, as does the voltage output in II. Thus network III should be fed from a voltage source, should feed into a low impedance input and requires the amplifier to have a defined transimpedance. For the example shown this could be achieved using a standard shunt-feedback amplifier where $A_z = v/i = -R_f$. If $R_f = 29R$ the condition for sustained oscillation is met. Where this level of voltage-current gain cannot be obtained, the impedance levels can be graded reducing the interaction between the sections. This reduces the voltage gain requirements to around -8 if n is large (Fig. 5).

Cross references
Set 25, cards 1, 4
Set 26, cards 2, 3, 4
Set 17, card 1

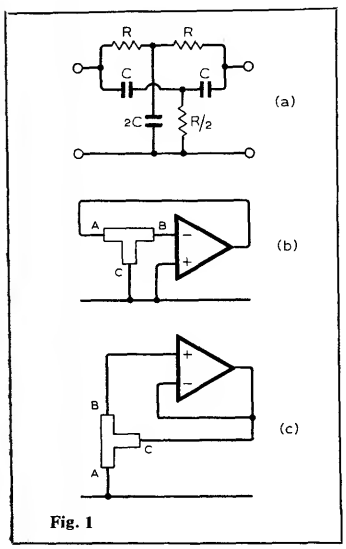


Fig. 1

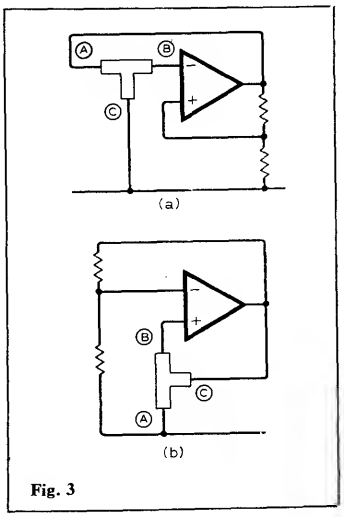


Fig. 3

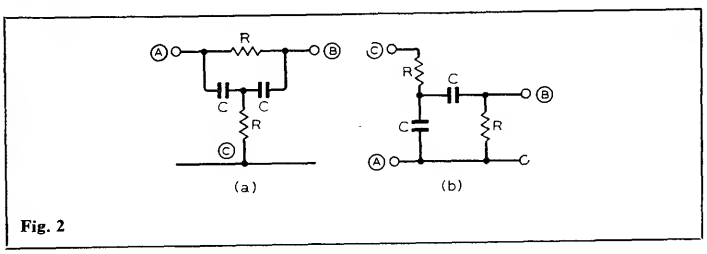


Fig. 2

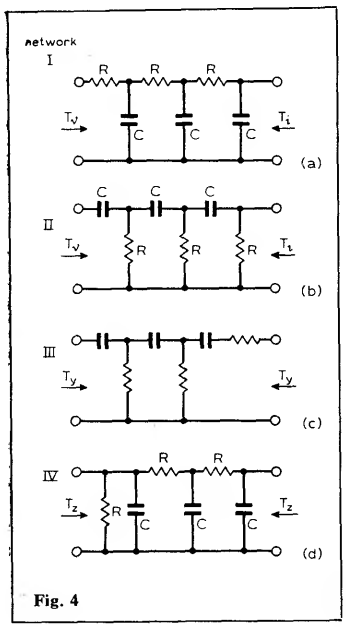


Fig. 4

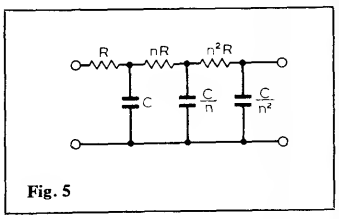


Fig. 5

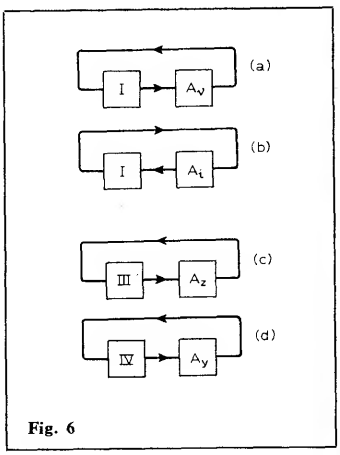


Fig. 6

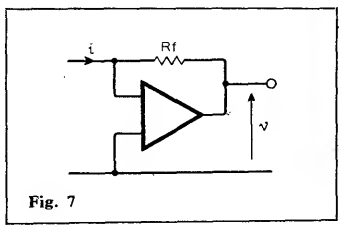


Fig. 7

wireless world circard

Parallel-T oscillators

Circuit description

It is often assumed that RC networks must attenuate any voltage signal applied to them, and that the voltage gain of the associated amplifier must exceed unity to sustain oscillations. Certain networks have a voltage output that slightly exceeds the input at a particular frequency (see Card 1). They can be derived from networks having phase inversion, and the parallel-T network is one such. The op-amp has a voltage gain very close to unity and with the components chosen there is a "voltage gain" due to the passive network of 1.09. This is sufficient to produce overdriven output with clipping. Adding R_4 to attenuate feedback allows the level of oscillation to be set for minimum distortion. The amplitude control methods shown on Set 25, card 6 are applicable, provided the value of R_4 is kept very much higher than R_1, R_2.

Let $R_1 = R_2 = R$
$C_1 = C_2 = C$
$R_3 = nR$
$C_3 = C/n$

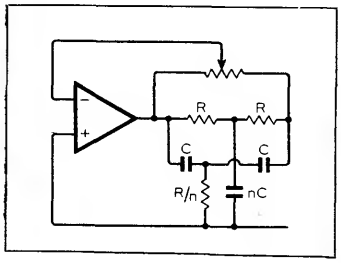
The passive network transfer function is then given by

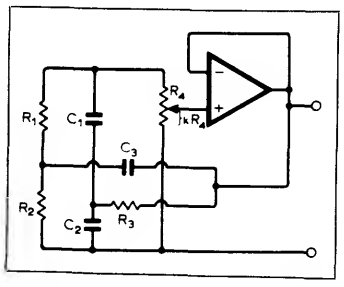
$$T_v = \frac{(f_o/f - f/f_o) + j(2n-1)}{(f_o/f - f/f_o) + j(2n+1+1/n)}$$

where $f_o = 1/2\pi RC$. For $n = 1/5$ the response for zero phase-shift when $f = f_o$ is $T_v(f=f_o) \approx 1.094$.

Similarly for $n = 1/3$, $T_v(f=f_o) \approx 1.073$.

This suggests that the amplifier gain must not fall more than 5% or so below unity if oscillations are to be maintained.





Component changes

IC not critical. Any op-amp capable of accepting 100% negative feedback, or an i.c. voltage follower.

Supply voltage: Normal range of op-amp supplies e.g. ±5 to ±15V.

R_1, R_2 1k to 100kΩ.

R_3. Can range from $R_1/2$ downward. As $R_3 \rightarrow R_1/2$ the response at zero phase-shift→ null. When $R_3 \ll R_1$, R_2 loading of the output or by the input becomes more critical. $R_4 \gg R_1$, R_2. If the ratio is not 10× or more, significant departure from predicted frequency occurs.

C_1, C_2 1n to 1μF, select from frequency equation, when resistors have been chosen from loading requirements.

C_3. C_1/n.

n typically 1/3 to 1/8.

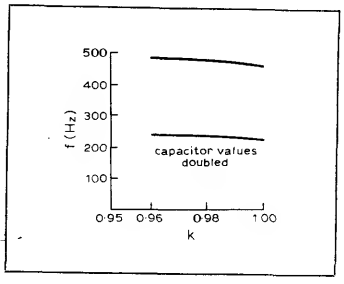
Frequency change in graphed results because increasing feedback brings increased distortion.

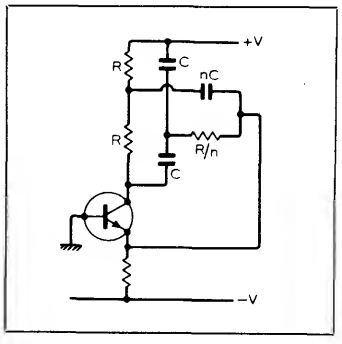
Circuit modifications

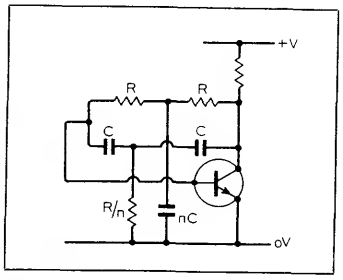
- The first circuit can be derived from that overleaf either by shifting the ground-point on the passive network and determining the sign of the amplifier gain required or by drawing the nullor circuit and shifting the ground point on that. Re-drawing in op-amp form then leaves the gain sign to be deduced. Again the loop gain is greater than is needed to sustain oscillation, and the feedback is attenuated to produce minimum distortion. The same constraints on impedance levels apply, and the performance is very similar to the original.
- A transistor has sufficient gain to be used with this network and in one form sometimes referred to as current-driven, the resistors of the T-network also provide the d.c. collector load. The circuit may use either a centre-tapped supply or the base may be fed from a decoupled potential divider across the single-supply. If the transistor is replaced by a nullor and/or the bias components omitted, with the supplies replaced by short-circuits, other forms of the circuit can be visualized. There are three in total, corresponding to which of the three device electrodes is grounded. Note that it is not correct to speak of "common-emitter" etc. since an oscillator has no input and there can be no "common" point.
- If the emitter is grounded then the resistors of the T-network provide d.c. negative feedback to the base. The collector load resistance loads the output circuit and can with advantage be replaced by a constant-current stage. The transistor needs to be operated at a low current to raise its input impedance so that the passive network is loaded as little as possible.
- The third transistor configuration corresponds to the op-amp circuit on the front of the card viz it is an emitter follower with a voltage gain slightly less than unity. Though not approaching the ideal as closely as an op-amp the gain in each of these configurations is sufficient for oscillation if biased carefully. The frequency response of a transistor can be so much higher than for a compensated op-amp that oscillation up to the MHz region could be possible.

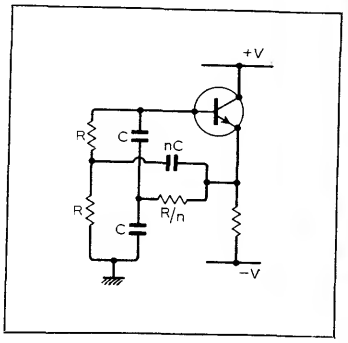
Typical performance

IC_1 741
Supplies ±15V
R_1, R_2 12kΩ
R_3 2.2kΩ
R_4 100kΩ
C_1, C_2 33nF
C_3 150nF
f 475Hz
Oscillation commencing with R_4 set to ≈ 0.965 of maximum









Phase-shift oscillators

Circuit description

The conventional phase shift oscillator uses a cascade of three RC or CR networks giving an output with 180° of phase shift at a particular frequency. It is fed into an inverting amplifier with sufficient gain to overcome the network losses, and oscillation is achieved. An op-amp has an excess of voltage gain and could use a separate passive feedback network to control the gain to the precise level required. Alternatively the final resistor in the chain could be removed from ground and used to drive the virtual ground point of the amplifier as shown, with no change in loading on the passive network. The gain is then defined by R_4/R_3.

The nullor form of the circuit is shown and indicates another viewpoint—summing two signals, one in phase and one inverted, both derived from the output. When these are equal in magnitude oscillations are maintained at the frequency of zero phase-shift.

By changing the ground point an apparently new circuit is obtained as in Fig. 2 where the amplifier is used as a voltage follower. The frequency of oscillation and the gain condition are not identical for the two circuits since neither can be an exact realization of the nullor version. They will differ amongst other reasons because of input common-mode effects with circuit 2 not present in circuit 1. A disadvantage of the CR-sections is that harmonics are progressively less attenuated. When oscillations are vigorous, and distortion ensues, these harmonics are fed back introducing intermodulation distortion and shifting the frequency of oscillation away from the 180° phase-shift frequency of the network.

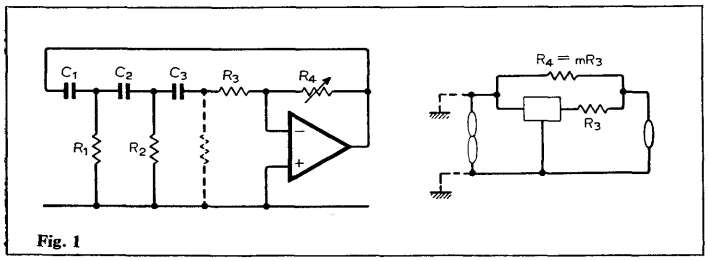


Fig. 1

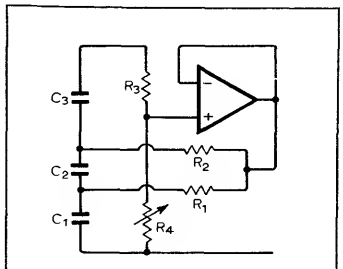


Fig. 2

Component changes

IC: general purpose op-amp—high input impedance advantageous.
R_1, R_2, R_3 1k to 33kΩ
C_1, C_2, C_3 1n to 1μF
$R_4 \approx 29R_1$ if $R_1=R_2=R_3$.
Larger values needed to overcome losses in most circuits. If the network is graded with the impedances progressively increasing, then the voltage attenuation is reduced e.g. if succeeding resistors are increased by a factor of 2 and capacitances reduced by the same factor the gain required is changed from −29 to −16. In the limit as $n\to\infty$ the gain requirement is relaxed to −8. This raises the network output impedance to such a level as to place excessive demands on the input characteristics of the op-amp and ratios from 3 to 5 are more realistic.

Circuit modifications

- The principle of the voltage follower circuit is illustrated above. The gain requirement of the amplifier ranges from 0.97 for the original network down to 0.90 for one with graded components as described above.
- In the original circuit the action could be viewed as summing in phase and inverted currents, derived from the input and output voltages of the phase-shift network. A dual form can be constructed in which the input and output currents generate voltages which are summed to zero at the amplifier input. It is shown in summary form in Fig. 4. Re-drawing in nullor form and shifting the ground point to alternate sides of the norator leads to different practical versions.
- The first employs a voltage follower, and the resistor R/n is used to set the condition for oscillation. For equal Rs and Cs in the remainder of the circuit $n\to 29$ is the appropriate condition. For R 10kΩ, C 33nF, and $R/n=330$, oscillations were sustained at a frequency of ≈1.18kHz.
- The second form has an op-amp with non-inverting input grounded and uses comparable component values to achieve the same frequency. Increasing the capacitance values to 0.1μF reduced the frequency to 375Hz. The components can again be graded to change the voltage- and current-gain requirements of the amplifier.

Theory. The transfer function of the CR network shown leads to a frequency of 180° phase-shift given by

$$\omega_0^2=\frac{1}{C^2R^2}\cdot\frac{1}{(3+2/n+1/n^2)}$$

and a gain condition.
$A_0=1-(3+2/n+1/n^2)(3+2/n)$.
For $n=1$, $\omega_0=1/CR\sqrt{6}$,
$A_0=-29$
For $n\to\infty$, $\omega_0\to 1/CR\sqrt{3}$,
$A_0\to -8$.

Typical performance

IC 741
Supplies ±15V
R_1, R_2, R_3 12kΩ
C_1, C_2, C_3 33nF
R_4 360kΩ
f 161Hz for circuit 1
156Hz for circuit 2
N.B. Normal attenuation of equal-valued 3-section phase-shift network is 1/29, indicating $R_4\approx 29\times 12k\Omega$.
For the voltage follower version, R_4 had to be increased to >500kΩ suggesting loading effect of op-amp input impedance.

Cross references

Set 26, cards 1, 2, 4

Fig. 3

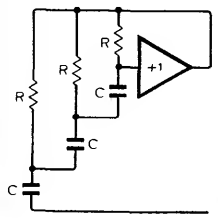


Fig. 4

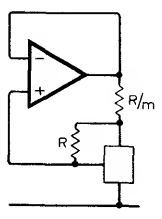
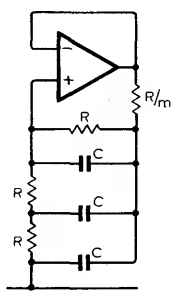


Fig. 5



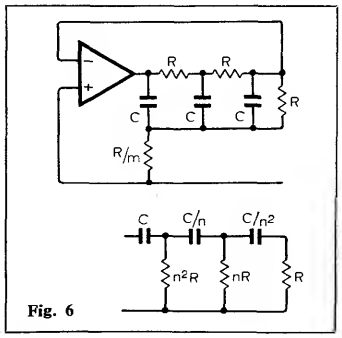
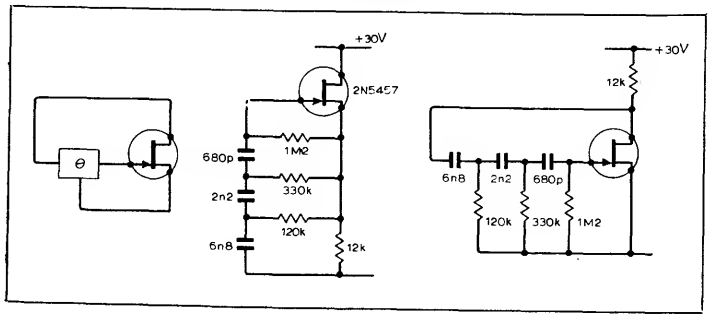


Fig. 6

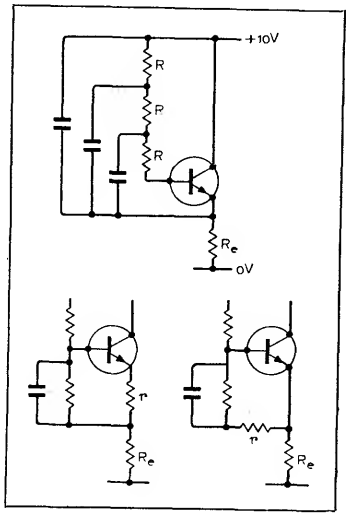
F.e.t. phase shift oscillators



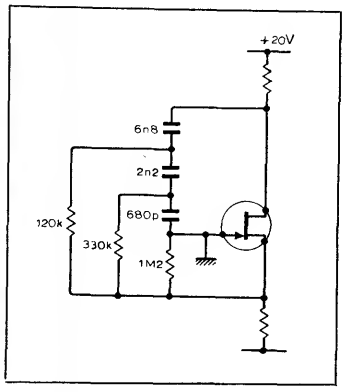
Circuit description

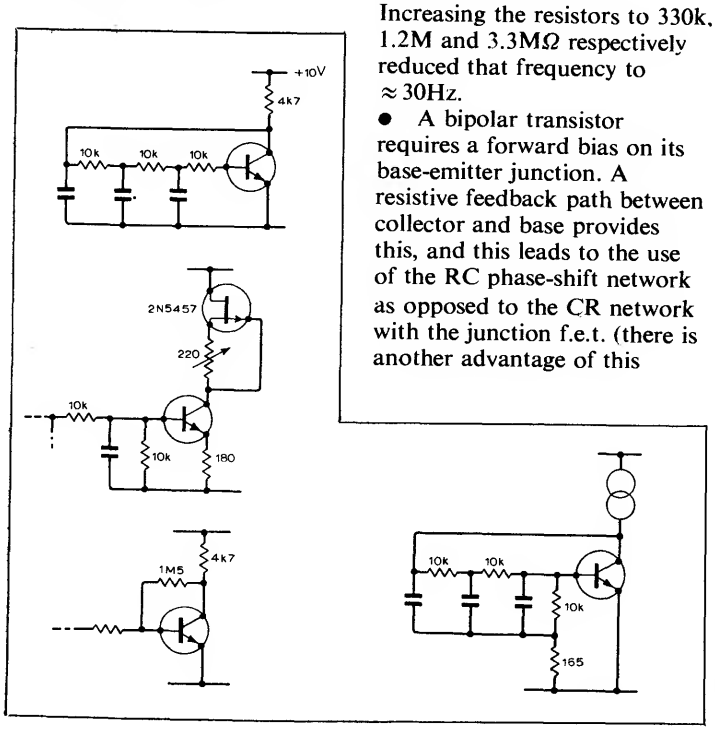
The basic principle is that of a passive network which has a frequency dependent transfer function such that in one configuration the output is 180° out of phase with the input at a particular frequency. The network contains a cascade of RC or CR sections and by grading the component values, the loading effects of successive sections is reduced. In the limit each section attenuates by $\frac{1}{2}$ with a 60° lag leading to a gain requirement of −8. Practical ratios raise the magnitude of this figure to 10 or 12, within the range of a f.e.t., while the high f.e.t. input impedance prevents loading problems from being significant. The f.e.t., if a junction device, needs either a zero gate/source p.d. or a reverse-biased gate for correct operation.

- This is achieved in the first circuit by allowing the final resistor of the phase-shift network to be connected directly between gate and source. The f.e.t. then has zero gate-source p.d. and operates at its maximum g_m. This is not the condition for maximum voltage gain unless the load resistance can be replaced by a constant current load. This circuit corresponds directly to that of card 3, circuit 2, with the reduced gain of the f.e.t. just sustaining oscillation.
- Corresponding to card 3, circuit 1, the phase-shift network can be interposed between drain and gate with source grounded. Again the restricted voltage gain of the f.e.t. means that in the absence of a constant-current load, the supply voltage has to be raised to maximize the load resistance for a given operating current and g_m. In general a junction f.e.t. has a greater voltage gain for a given supply voltage when operated at a lower current. This is because as the current falls, the g_m falls more slowly while the load resistance increases directly in proportion to the reduction in current. Hence the voltage gain ($-g_m R_L$) increases in magnitude. The limit is set when the passive network exerts significant loading on the output.



- The third form (over) of the oscillator is that of grounded gate in which both source and drain loads have to be present. One method of increasing the voltage gain in each of these circuits is to include a decoupled resistor in the source lead. This lowers the current allowing the load resistors to be increased as indicated above.
- With the component values as indicated, the frequency of oscillation was ≈75Hz. Increasing the resistors to 330k, 1.2M and 3.3MΩ respectively reduced that frequency to ≈30Hz.
- A bipolar transistor requires a forward bias on its base-emitter junction. A resistive feedback path between collector and base provides this, and this leads to the use of the RC phase-shift network as opposed to the CR network with the junction f.e.t. (there is another advantage of this network, in that harmonics are attenuated reducing the shift in frequency due to intermodulation effects when the output distorts). The network is used in its reversed mode ideally requiring current drive and a low impedance load. By using a f.e.t. or other constant current load, the output impedance approaches the ideal while series feedback can increase the input impedance. The final network resistor is then grounded and the p.d. across it used as the feedback, more nearly satisfying the impedance conditions. Shunt feedback would improve the input matching but would drive the network more nearly from a voltage source. Any mismatch shifts the frequency of oscillation. A better solution is to combine the high output impedance arrangement of the amplifier with the network arrangement of card 3, circuit 6.
- Grounded-collector and grounded-base versions of the oscillator follow in the same way as for the f.e.t. oscillators and, feedback arrangements to control the amplitude of oscillation are indicated.





Cross references

Set 1, card 9
Set 26, cards 1, 3
Set 25, card 1

C.d.a. oscillator

Circuit description

This circuit* takes advantage of the quad current-differencing amplifier package and is in the form of a two-integrator loop (IC_4, IC_2) plus inverter (IC_3), which does not contribute to the loop gain, but provides a 180° phase shift between v_{out1} and v_{out2}. For $R_3 = R_4$, frequency of oscillation is given by $\omega = 1/C_1R_1C_2R_5$. Resistor R_2 acts as a damping resistor IC_1 acts as a comparator and supplies the input square wave fed back to IC_2 to keep "ringing" the circuit. IC_2, IC_3, IC_4 is a bandpass filter with a Q defined by R_2C_1. To initiate oscillation with the loop closed, the differential input to IC_1, (C_4 charge initially zero) causes IC_1 to rise initially to positive saturation, but rapidly changes to 0V when C_4 charges. This shock-excites the loop (overall phase shift zero), amplitude of oscillation builds up until a balanced condition is reached, where the output across R_{15} is just sufficient to maintain a steady oscillation, approximately 220mV square waves.

Component changes

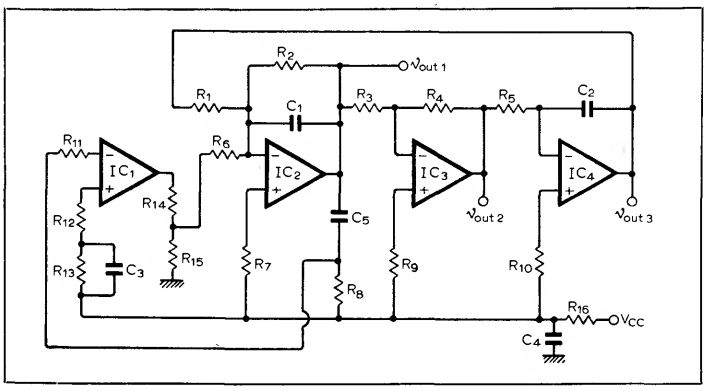
R_{15} 680Ω, V_{out} 4.2V pk-pk, t.h.d. 0.35%. For 1500Ω, V_{out} 8.6V pk-pk, t.h.d. 0.5%. R_{14} 39kΩ, V_{out} 8.6V pk-pk, t.h.d. 0.4%. For 56kΩ, V_{out} 5.6V pk-pk, t.h.d. 0.25%. R_6 220kΩ, V_{out} 8.8V pk-pk, t.h.d. 1.2%. For 470kΩ, V_{out} 4.4V pk-pk, t.h.d. 0.3%. R_2 7.8MΩ V_{out} 6.8V pk-pk, t.h.d. 0.6%. For 4.7MΩ, V_{out} 4.1V pk-pk, t.h.d. 0.2%. For all above alterations, frequency does not change more than 0.2%. Variation with supply C_1, C_2 shown on graphs.

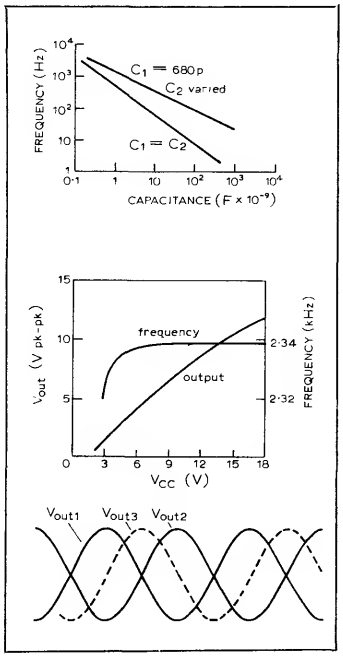
Typical data

IC_1 to IC_4 $\frac{1}{4}\times$ LM3900N or MC3401
R_1, R_3, R_4, R_5, R_9 100kΩ
R_2 6.8MΩ, R_6 330kΩ
R_7, R_{10}, R_{12} 220kΩ, R_8 470kΩ
R_{11} 22kΩ, R_{13} 270kΩ
R_{14} 47kΩ, R_{15} 1kΩ, R_{16} 4.7kΩ
C_1, C_2 680pF, C_3 2.2μF
C_4 10μF

V_{CC} +10V
v_{out1} v_{out2} v_{out3} 6.9V pk-pk

Oscillation frequency 2338Hz
Phase difference between outputs 90° as shown in waveform diagram.
Total harmonic distortion: 0.55%.



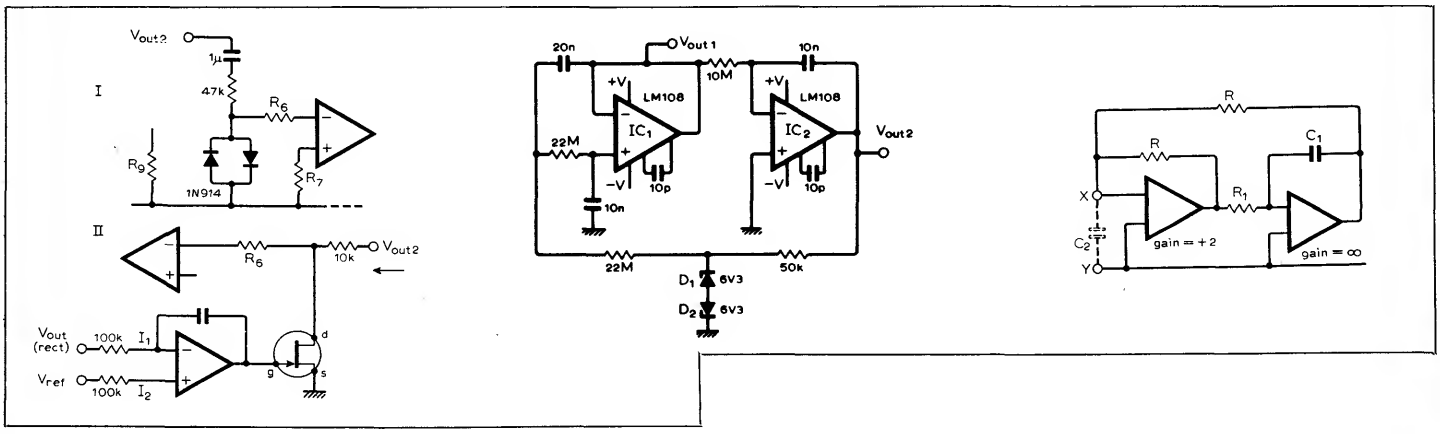


Circuit modifications

- Comparator can be replaced by diode limiter of I above. Control is less precise because square wave is not available across diode.
- More precise limiting achieved from II. V_{out2} is half-wave rectified, capacitor current is $(I_1 - I_2)$. If output increases, the p-type junction f.e.t. gate is driven negative to increase f.e.t. conduction, and v_{out2} is attenuated to decrease overall positive feedback and thus reduce output.
- Alternative integrator-based oscillators. IC_1 is connected as a low pass filter and IC_2 as an integrator. Diode limiters D_1, D_2 introduce distortion. The symmetrical clipping minimizes even harmonics, and the predominant third harmonic is attenuated by about 40dB by low-pass filter action. Temperature compensation to stabilize amplitude is obtained if n-p-n transistors connected as diodes (base-emitter breakdown 6.3V) are used as limiters. Circuit between X and Y is a simulated inductor. C_2 induces oscillation if amplifier gain is +2.

Cross references

Set 26, cards 6, 7 Set 17, card 2
*Rossiter, T. J. M. Sine oscillator uses c.d.a. *Wireless World*, April 1975.



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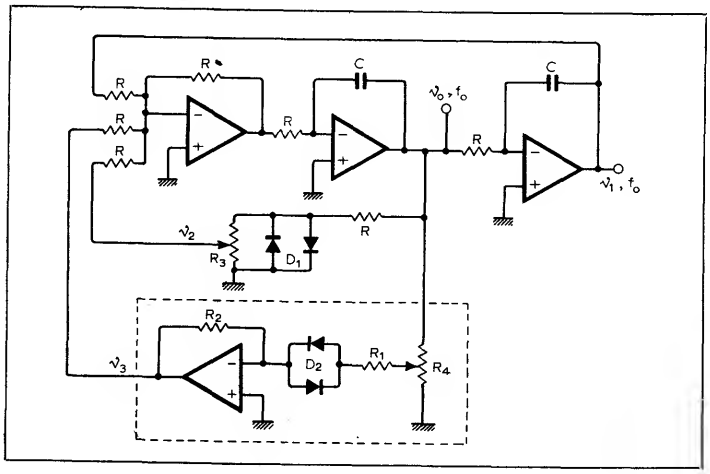
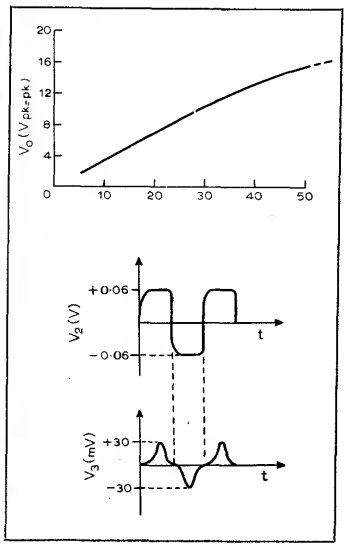
Set 26: RC oscillators II—6



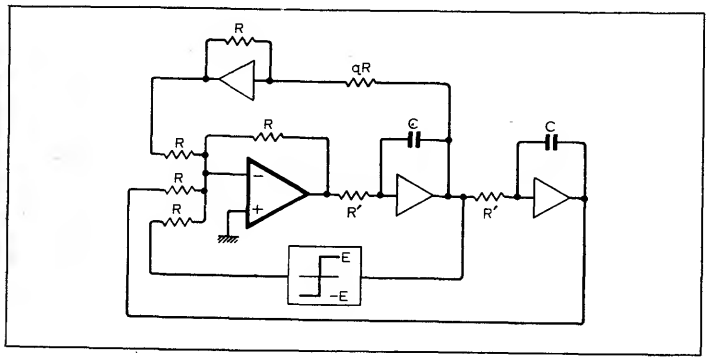
Two-integrator loop oscillator

Components
Supply ±15V
IC 741 op-amps
R 10k ±5%
R_1 22k ±5%
R_2 220k ±5%
R_3 100kΩ, R_4 1kΩ
C 0.1μF ±5% polyester
D_1, D_2 1N914



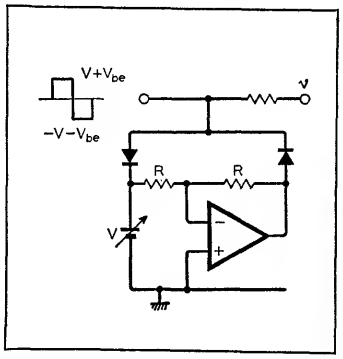
Performance
With R_3 set at 0.1, a value which caused the circuit to oscillate with slight clipping when R_4 was at zero, variation of v_o plotted against the inverse of R_4 setting is shown. Total harmonic distortion throughout this range lay between 0.96% and 0.86% and the frequency f_o was 159.35 ±10Hz. With perfect op-amps, identical R and lossless capacitors, the theoretical f_o is $1/2\pi CR$. Typical traces for v_2 and v_3 are shown.

Circuit description
The circuit is a straightforward two-integrator oscillator[1] with v_2 providing sufficient positive feedback to overcome the damping inherent in the imperfect capacitors and op-amps thus ensuring oscillation. This positive feedback is of a constant nature in that once oscillation has reached a level to ensure conduction of the diodes D_1 then v_2 is approximately a square wave whose magnitude does not depend on v_o. Potentiometer R_3 can provide a measure of amplitude control[1] with the positive feedback always balancing out the inherent damping. However, although the circuit is invariably used as a low frequency oscillator (< 1kHz) problems of amplitude control do arise at high frequencies when phase shifts in the imperfect components reduce the inherent damping[2]. Under these conditions the basic oscillator tends to go into oscillation limited only by saturation of the op-amps. To prevent such oscillation the dead zone limiter (the dotted section) is added. This section produces an output only when v_o is sufficient to cause the diodes D_2 to conduct; when this happens a large amount of negative feedback is applied, thereby damping out any tendency to oscillate with too large a magnitude. One therefore has a section comprising D_1 etc forcing oscillation and another section comprising the dead zone limiter holding down the oscillation, giving good overall control[2].
Distortion content in the output v_o (or v_1 which is 90° out of phase with v_o) depends on circuit Q. With good quality passive components Q is approximately $K/2$ where K is the op-amp open-loop gain.
should not be so low as to cause damage to the diodes D_2.



Component changes
Polycarbonate capacitors up to 10μF and higher values of R can reduce the operating frequency to a fraction of one hertz. Amplifiers of greater gain than that of the 741 would be necessary to increase the operating frequency much beyond 1kHz (for which Wien type oscillators are available, Set 25). The ratio R_2:R_1 should be kept large to give heavy negative feedback when necessary. At the same time R_1 should not be so low as to cause damage to the diodes D_2.

Circuit modifications
- Because the negative feedback section prevents oscillations from growing without bound there is no need to include the limiter in the positive feedback path. The positive feedback can therefore be directly from the output of first integrator back to the summing inverter, and might be expected to produce lower distortion figures.
- Amplitude control with



sinusoidal negative feedback and limited positive feedback can be obtained as shown above. It can be shown[1] that for this circuit the output is given by $2qE\sqrt{2}/\pi$ volts r.m.s. A possible voltage-controlled limiter is shown above

References
1. Girling, F. E. J. and Good, E. F. Active filters—8. *Wireless World*, March 1970.
2. Foord, A. Two-phase low-frequency oscillator, *Electronic Engineering*, Dec. 1974.

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Set 26: RC oscillators II—7

Four phase oscillator

Components

R_1 to R_7, R_{12}, R_{22} 10kΩ
R_8 to R_{11} 47kΩ
R_{13} 220kΩ, R_{14} 330kΩ
R_{15}, R_{16} 100Ω
R_{17} 100kΩ, R_{18} 2.7kΩ
R_{19}, R_{20} 2.2MΩ, R_{21} 22kΩ
R_{23}, R_{24} 47kΩ twin gang
R_{25} 10kΩ, R_{26} 50kΩ
R_{27} 220kΩ
C_1, C_2 22nF
D_1 to D_4 1N914
D_5 6V zener, F.e.t. BF244
IC_1 to IC_6 741 op-amps with ±15V supplies

Performance

This circuit provides four outputs, at points A, B, C and D. If A is taken as the reference then B, C and D are 180°, −90° and +90° out of phase with A respectively. The output signal magnitude was set at 15V peak-to-peak by suitable setting of R_{25} and the graphs shown indicate the total harmonic distortion at various frequencies, obtained by varying R_{23} and R_{24}. The scales chosen are not ideal but the graphs all show the same general shape as that for B which is shown in full. In relation to one another they are as one might expect with the exception that one would anticipate B to be better than C since harmonics are reduced by an integrator. The difference is slight and could be accounted for by imperfections in the op-amps.

Description

This oscillator is closely related to the two-integrator loop oscillator[1].
It has one extra inverter (IC_4) which enables one to produce four outputs all 90° apart. This allows the use of a four-phase rectifier (D_1 to D_4) which requires little smoothing to produce a direct voltage proportional to the output magnitude.
The oscillator works on the basis of fixed negative feedback (from D via R_{13} to IC_1) being balanced by a variable amount of positive feedback. The amount of positive feedback is dependent on the discrepancy between the desired output voltage (set by D_5 and R_{25}) and the actual output as sensed by D_1 to D_4. The positive feedback path is from the output of IC_2 via IC_6 and R_{14} to IC_1. IC_2 and its associated circuitry provide a path of positive gain, the magnitude of which gain is set by the resistance of the f.e.t. (n-channel). The output of IC_2 is

$$v_p \frac{R_{12}}{R_{12}+R_{27}} \cdot \frac{R_{21}+R_F}{R_F}$$

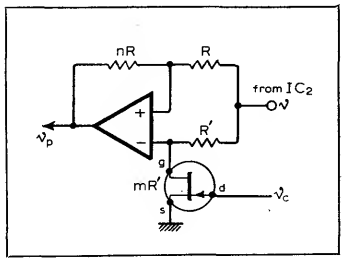
where R_F is the f.e.t. resistance. R_{20} and R_{19} serve to linearize the f.e.t. resistance and it is possible to omit R_{20} and replace R_{19} by a short for the purpose of explanation.
Bearing in mind the f.e.t. characteristics note that a positive increment in v_c (corresponding to a reduction in output voltage) gives a lower value of R_F and a larger positive feedback voltage, v_p, which will increase the magnitude of the oscillation.
A similar balancing effect occurs if the oscillations increase in magnitude. Note that the d.c. value of v_c must be slightly negative for correct f.e.t. operation and that this is ensured by the integrator action of IC_5 and its associated circuitry.
A four-phase oscillator allows rapid amplitude stabilization since any change in amplitude is quickly sensed; this is of importance in low frequency oscillators[2].

Circuit modifications

- Use of fixed positive feedback and variable negative feedback requires care with polarities of most of the items in the amplitude control loop.
- It is possible to remove the positive feedback link altogether and obtain either positive or negative feedback, depending on whether the output is low or high, by using the circuit above right to generate the feedback signal. For this circuit

$$v_p = v(1+n)\left(\frac{m}{m+1} - \frac{n}{n+1}\right)$$

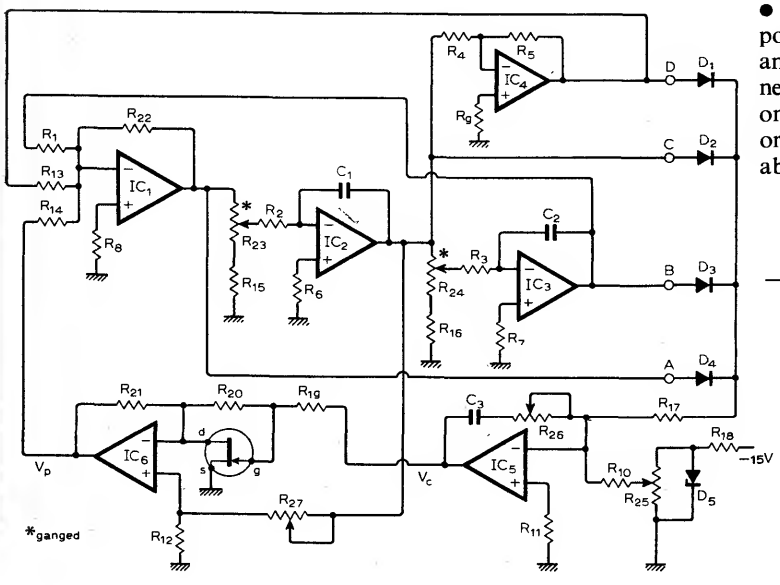
Since m can be controlled by v_c, positive and negative values of v_p can be obtained giving positive and negative feedback respectively.

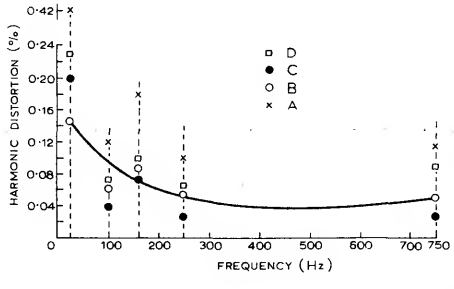


- An alternative, though more expensive scheme, to provide the same function of positive and negative feedback control on the same path is to use a multiplier, one input of which is the output of IC_2 and the other is v_c. The magnitude and sign of v_c control the amount and nature of the feedback[2].

References

1 Circards this set, card 6.
2 Fast amplitude stabilisation of an R-C oscillator, Vannerson and Smith, *IEEE Journal of Solid State Circuits*, vol. SC9, no. 4, Aug. 1974.
3 Circards, this set, cards 9, 10.





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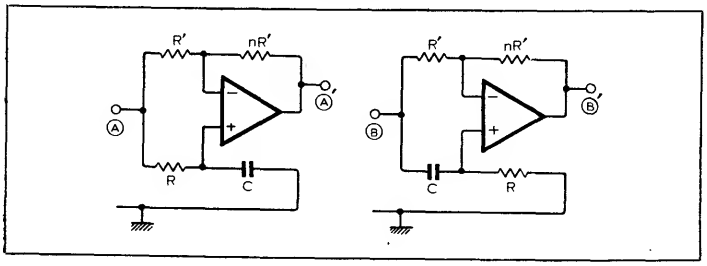
All-pass network oscillator



Typical performance
IC_1, IC_2 741
Supplies ±15V
R, R′ 10kΩ
C 15nF
$n \approx 1$
f 1065Hz
Connect A′ to B, B′ to A.
Oscillation commences for loop gain >1 at zero phase-shift. Set either value of $n > 1$.

Circuit description
Most oscillators have a peak in their loop amplitude response at the frequency of zero loop-phase-shift. This stems from the band-pass nature of their transfer function. The Barkhausen criterion demands only that the loop-gain exceeds unity at this frequency and it is not necessary for the amplitude response to be frequency dependent—though it may assist in reducing the effect of distortion on frequency. If circuits having frequency dependent phase-shifts are combined such that the overall phase-shift is zero at a single frequency then oscillations can occur at that frequency. These circuits are called all-pass (non-minimal phase-shift circuits) and can be made with one op-amp three resistors and one capacitor. The gain can be trimmed about unity. The outputs are 90° out of phase and the frequency of oscillation is the same as for Wien, two-integrator and gyrator oscillators using the same components.
Transfer function of A to A′.
T_{vA} given by equating potentials at inputs

$$\frac{v_o/n+v}{n+1}=\frac{v}{1+sCR}$$

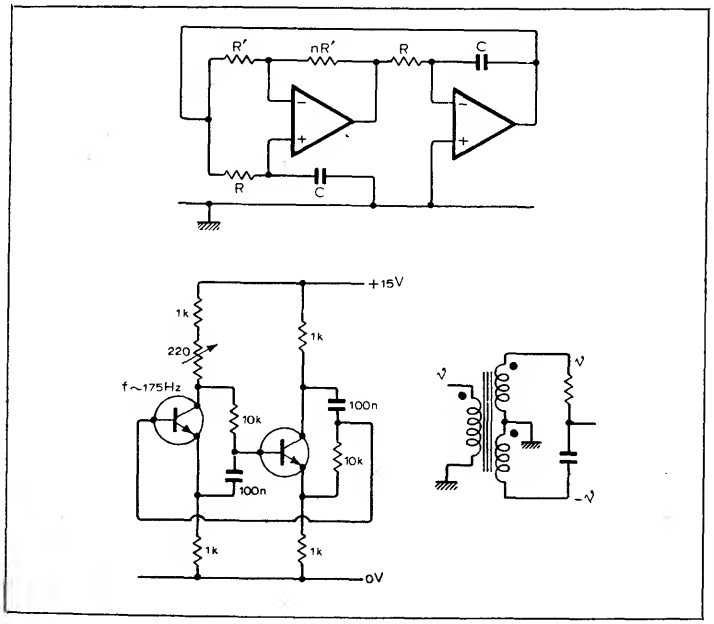
$$\therefore T_{vA}=\frac{v_o}{v}=\frac{n-sCR}{1+sCR}$$

For $n=1$, magnitude of transfer function is unity at all frequencies with the phase shift varying from zero as $f \to 0$ to $-\pi$ as $f \to \infty$. The phase shift is $\pi/2$ lagging at $\omega = 1/CR$.

Similarly $T_{vB}=\dfrac{sCR-n}{1+sCR}$

with unity gain for $n=1$ and a $\pi/2$ phase-lead at $\omega = 1/CR$.

Component changes
IC_1, IC_2: compensated op-amps not critical except where high frequency operation required.
R′: 1k to 100kΩ
nR′: Replace one of the resistors by a thermistor or other amplitude sensitive network for amplitude control. This may necessitate reducing R′ to suit the operating resistance of the thermistor.
C: 1n to 1μF
R: The capacitors can be switched to change ranges as in Wien etc. oscillators and the resistors R replaced by a twin-gang potentiometer for continuous frequency control.
N.B. In the majority of oscillators of this kind the frequency of oscillation is of the form $f = 1/2\pi RC$ where all Rs and Cs are equal.



Circuit modifications
The transfer function of an integrator is given by $T_v = -1/sCR$ Combining this with the first all-pass circuit overleaf gives an overall transfer function.

$$T_v=\left(\frac{n-sCR}{1+sCR}\right)\left(\frac{-1}{sCR}\right)$$

For $n=1$ this reduces to unity when $(sCR)^2=-1$, i.e. at $f=1/2\pi CR$ the same frequency as in the previous circuit. The outputs differ in phase by 90° and amplitude control can be achieved by replacing nR' by a low-power thermistor, and R' by a low value resistor to match e.g. R54 (ITT) and a 1kΩ resistor.
Many other oscillators have been designed using various combinations of lead, lag, all-pass and integrator networks and some examples are quoted in the references. In all cases some non-linearity is required to control and limit the amplitude of oscillation—these include diode clipping/limiting saturating high-gain amplifiers, thermistors lamps etc.
A very simple form of oscillator based on the all-pass network idea can be implemented using only two transistors. The all-pass networks load the transistor outputs causing departures from the theoretical performance, but this can be allowed for by increasing one of the collector resistors as shown. The voltage swing is limited because the self-biasing action of the circuit leaves a relatively small collector-emitter p.d. for each transistor. The outputs should not be heavily loaded or the frequency/amplitude will be disturbed but the circuit gives roughly quadrature outputs with a low component count. The transistors are general purpose silicon planar. The all-pass network behaves similarly to that using a transformer with a centre-tapped secondary as indicated.

Further reading
Yewen, J. Two-phase sinewave oscillator, *New Electronics* 1974, vol. 7, no. 6, p. 25.
Das, S. K. & Das G. Amplitude stabilized low frequency oscillator. *Int. J. Electron.*, 1972, vol. 33, pp. 371-5.
Hanna, N. N. and Kamel, S. A. A low frequency sine-wave oscillator, *Int. J. Electron.*, 1973, vol. 35, pp. 685-90.
Baril, M. Three-mode network is filter or oscillator, *Electronics*, Apr. 12, 1973, pp. 105/6.

Gyrator oscillators

Circuit description

A gyrator is a circuit that synthesizes an impedance at one port that is related to the physical impedance presented at a second by the relationship

$$Z_1 = R^2/Z_2.$$

If one impedance is capacitive e.g. $Z_2 = 1/j\omega C$ then $Z_1 = j\omega CR^2$ equivalent to a pure inductor having $L = CR^2$. Such a circuit can be constructed using two ideal op-amps, four resistors and one capacitor. The circuit is widely used in active filters but can be used to make oscillators. Many variants are possible. First the passive network can be changed so that the locations of the capacitors vary. Two capacitors are used occupying any pair of the starred locations—circuit 2 is an example. Then the amplifier inputs may be moved so long as they maintain the circled junctions at equal potentials—circuit 3 is derived from circuit 2. An additional feedback path labelled R_{f1} or R_{f2} initiates oscillation.

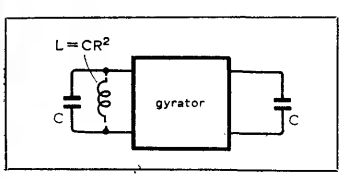
Typical values

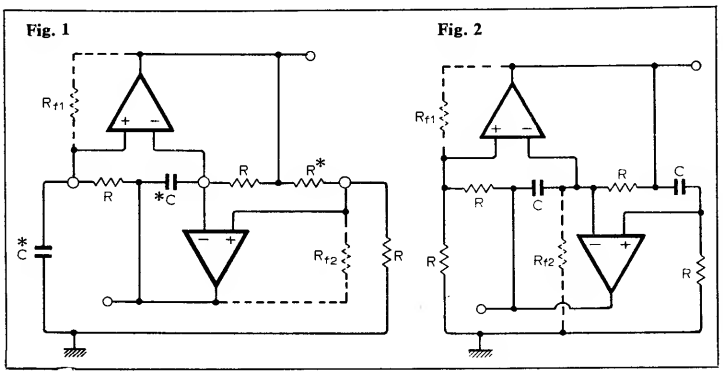
R 10kΩ, C 15nF, R_{f1} 680kΩ, f 1055Hz.

The p.ds across Z_2 and Z_3, Z_4 and Z_5 are equal as are the currents in Z_1 and Z_2, Z_3 and Z_4, Z_5 and the source. Thus the input current is given by

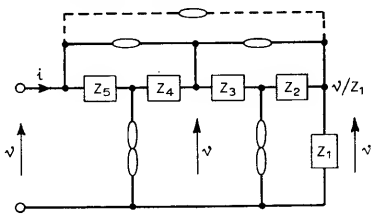
$$\frac{v}{Z_1} \times Z_2 \times \frac{1}{Z_3} \times Z_4 \times \frac{1}{Z_5}$$

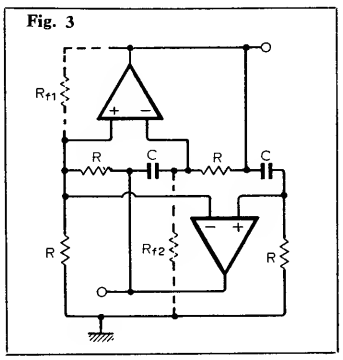
Input impedance of the circuit is $v/i = Z_1Z_3Z_5/Z_2Z_4$. If a capacitor replaces Z_2 or Z_4 and the other elements are resistive, the input impedance becomes inductive. If a capacitor is placed across the input port, it resonates with this synthesized inductor, and only a small amount of positive feedback is needed to overcome losses due to finite amplifier gain etc. and





Equivalent circuit





produce sustained oscillation. For $Z_1 = Z_2 = Z_3 = Z_5 = R$ and $Z_2 = 1/j\omega C$, $Z_i = j\omega CR^2$.

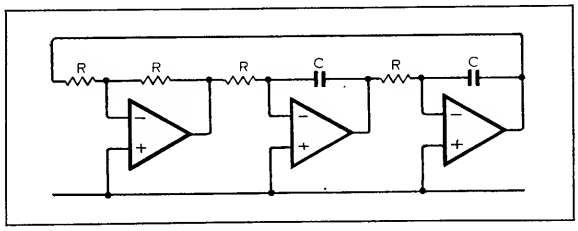
The combination of a capacitor C and a synthesized inductor, $L = CR^2$, formed by gyrating the other capacitor produces an equivalent parallel tuned circuit. The self resonant frequency is

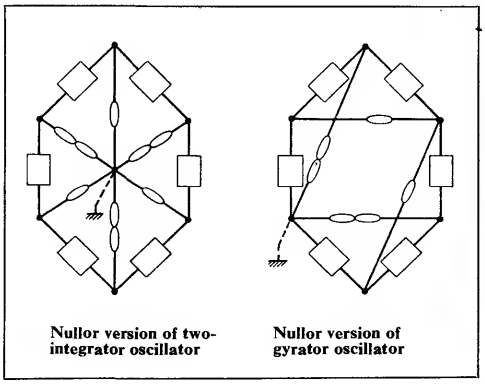
$$f_o = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{CR^2C}} = \frac{1}{2\pi CR}$$

This is the same frequency as occurs in a Wien oscillator using the same component values in the frequency dependent network. Tuning of the oscillator frequency is obtained by varying any of the component values either singly or in pairs. For ideal op-amps there is no damping and the circuit is continuously on the point of oscillation regardless of component values. In practice an external component or network may be added to initiate and sustain oscillation.

Two-integrator loop

This circuit, described on cards 6, 7, uses the same passive components and has the same frequency of oscillation. Though developed separately these two are different forms of the same basic circuit. This can be seen by re-drawing the passive networks in a similar format (where the impedances in practice are composed of four resistors and two capacitors). Then replacing the input of each amplifier by a nullator and the output/ground port by a norator the identity can be seen. Of the six vertices, three are equipotential points with no current being fed into or taken out of the vertices (the properties of the nullators). The other three points are at arbitrary potentials, regardless of loading effects at these points. Provided the passive networks are chosen correctly there can be only one frequency at which these constraints are met; oscillation occurs at that frequency but with undefined amplitude. An external network must be added to limit the amplitude e.g. by using a f.e.t. to place controlled variable damping across a grounded capacitor with positive feedback to initiate the oscillations.





Cross references

Set 26, cards 6, 7, 10
Set 25, cards 9, 10
Set 1, cards 6, 7

Further reading

Pauker, V. M. Equivalent networks with nullors for positive immitance converters, *IEEE Trans. Circuit Theory*, Nov. 1970, pp. 642-4.

Antoniou, A. New gyrator circuits obtained by using nullors, *Electronics Letters*, Mar. 1968, pp. 87/8.

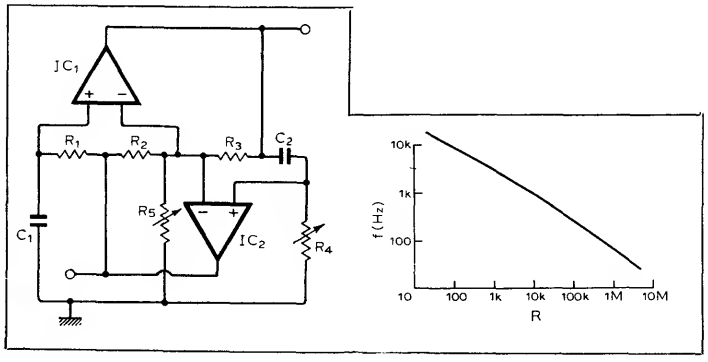
Wide-range gyrator oscillator

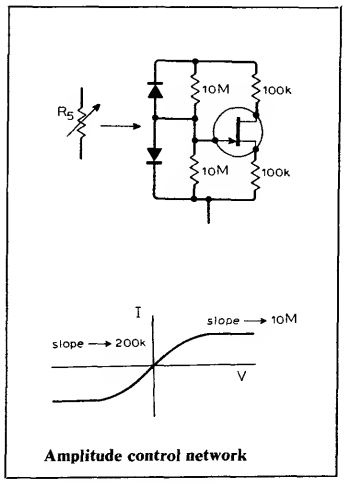
Circuit description

Another version of the gyrator oscillator, this one uses a single variable resistor, R_4, to control the frequency of oscillation. For ideal active and passive elements only the smallest amount of positive feedback would ensure that the amplitude builds up until peak clipping restores the loop gain condition. Losses including those due to capacitor loss factors, require the presence of R_5 or other path to initiate the oscillations. As R_4 is varied, the value of R_5 at which oscillations just start also varies. Though much greater than R_1, R_2, R_3 at all settings of R_4, either R_5 has to be re-adjusted manually/automatically or set to a low enough value to ensure oscillation over the whole range. This brings increased clipping at high values of R_4. The circuit is of considerable interest because it illustrates the way in which gyrator oscillators can achieve a very wide range of frequencies using a single variable resistor —greater than 200:1 in this example. Amplitude control methods could include replacing R_5 by a network incorporating a f.e.t. whose on-resistance is varied via a peak-rectifier; or by replacing it by a non-linear network adjusted so that it has a low resistance at low amplitudes to excite the circuit, rising at higher amplitudes to levels where the loop gain is insufficient. A possible example for such a network is shown opposite.

It is equally possible to change the frequency by varying both capacitors and/or a pair of resistors, making the components switched or continuously variable. This reduces the variation needed in R_5 but does not eliminate it. In the original circuit, for capacitor to produce the effect of a self-resonant LC circuit. The example shown is best considered in two parts. First an integrator with overall resistive feedback from input to output via R′ simulates a parallel LR circuit. This is then combined with a negative resistance circuit (also viewable as a n.i.c. acting on R_1). If the integrator is fed from the output of the first amplifier, less compensation is required for the positive resistances in the system by this negative resistance circuit. For oscillation $R_2 = R_1$ with ideal amplifiers.

- R_2 or R_1 may be made variables using thermistors, lamps etc, or the first amplifier can be replaced by any other variable gain amplifier capable of being remotely controlled e.g. multiplier, a.g.c. amplifier etc.
- Because of the integrator, the two outputs are in quadrature throughout while control of frequency via a single component is again possible.





Amplitude control network

$$R_1 = R_2 = R_3 = R,\ C_1 = C_2 = C$$

$$f = \frac{1}{2\pi CR}\sqrt{\frac{R}{R_4}}$$

Component changes

The component values will be comparable to those used in the two integrator oscillators (cards 6 and 7). At high frequencies, cumulative phase-shifts can raise the effective Q of the circuit, while slew-rate limiting can lead to unpredictable jumps in the amplitude of oscillation.

$IC_{1,2}$: Compensated op-amp. High input impedance necessary if R_4 is to be made very large.

R_1, R_2, R_3: 1k to 100kΩ

C_1, C_2: In to 1μF

R_4: 47 to 4.7MΩ

R_5: Typically 220k to 2.2MΩ. Low resistance needed at high frequencies.

Supplies: ±5 to ±15V.

Circuit modifications

- Any other circuit that synthesizes a pure inductor can be combined with a

Typical performance

$IC_{1,2}$ 741
Supplies ±15V
R_1, R_2, R_3 10kΩ
C_1, C_2 15nF
R_4 10kΩ
R_5 470kΩ
f 1.05kHz

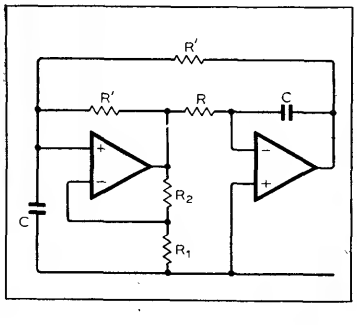
Further reading

Ford, R. L. and Girling, F. E. J. Active filters and oscillators using simulated inductances, *Electron. Lett*, vol. 2, 1966, p. 52.

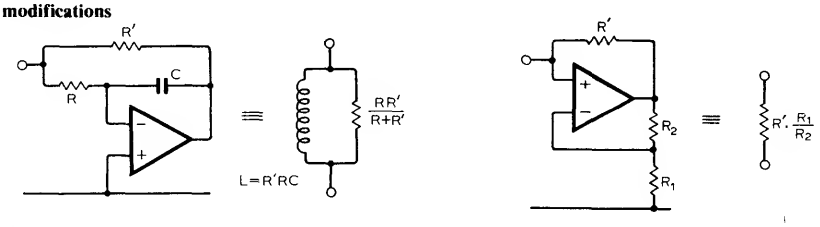
Harris, R. W. Two-op-amp RC resonator with low sensitivities, Proc. 16th Mid West Symposium on Circuit Theory, 1973, vol. 1.

Cross references

Set 26, cards 6, 7, 9, 10
Set 25



Circuit modifications



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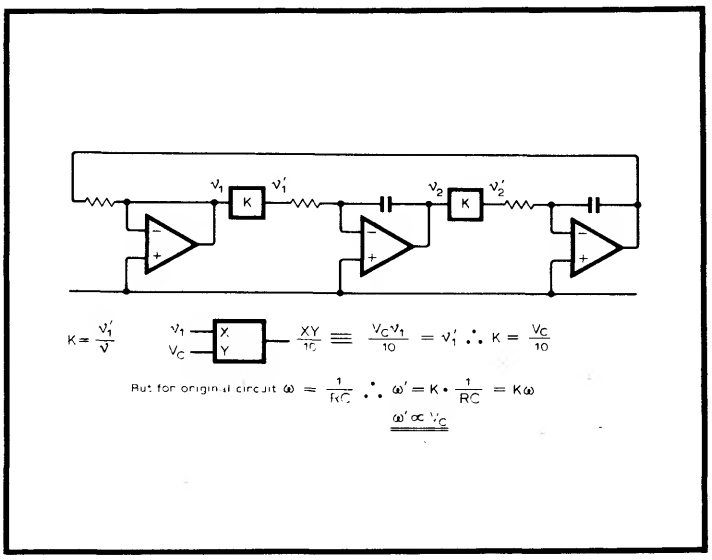
Set 26: Up-date

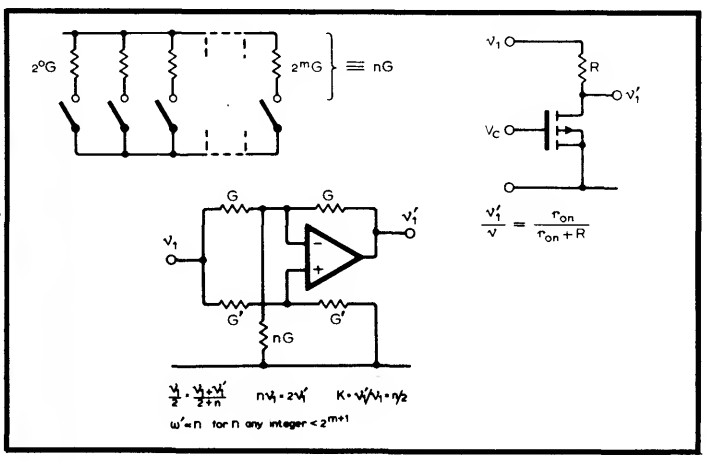
Control of oscillator frequency from an external signal is of increasing importance in such diverse applications as computer-controlled test systems, electronic musical instruments and communication receivers. Rather than giving detailed information on one or two circuits this update surveys the novel and ingenious methods proposed in recent publications. To aid comparison they are shown applied to a two-integrator loop, the principles then serving for both oscillatory and filtering functions. The same methods can be applied to most other RC oscillators.

Consider a pair of identical blocks K which change the voltage transferred from one stage to the next. Increasing the voltage by a factor K increases the current fed to the capacitor by K charging it more rapidly. It is equivalent to reducing the resistor by a factor K i.e. the frequency of oscillation is increased K times. (N.B. No amplitude control etc indicated; see details on preceding cards.) The block K can be provided by an analogue multiplier in which K becomes proportional to the control voltage V_c fed to one of the multiplier inputs.

Reference

Sparkes, R. G. and Sedra, A. S. Programmable active filters, *IEEE J. Solid State Circuits*, Feb. 1973, pp. 93-5.





Any other amplifier or attenuator can be substituted including a simple field-effect transistor, for example, a n-channel m.o.s.-f.e.t. from the CD 4007 package as shown. The control is then non-linear and to avoid distortion the signal levels must be low. A second remote-control method is via a digitally-controlled amplifier or attenuator. An *R*/2*R* ladder network may be used directly if it can handle bipolar signals. A neat alternative is the balanced amplifier shown in which any additional conductance to ground produces a proportional output. The switches control a binary-weighted resistor network, and because the switches are grounded might be t.t.l. open-collector outputs or multiple m.o.s. devices from certain c.m.o.s. packages (Set 27 card 7), again provided the signal level is restricted. Any other electronic switches including analogue gates can be substituted.

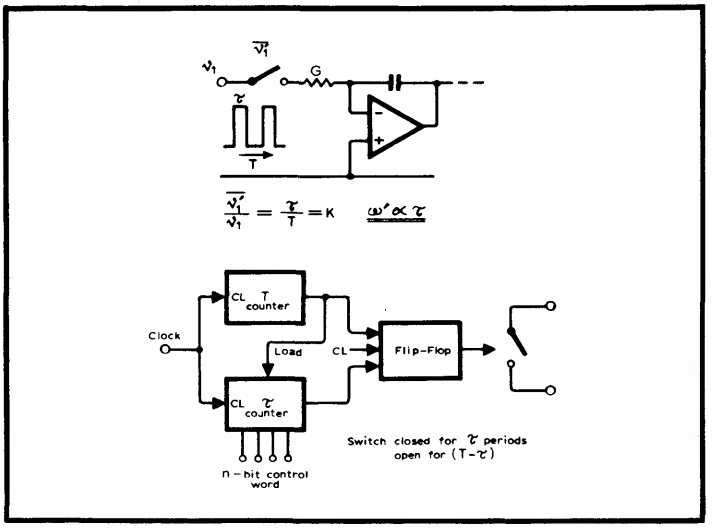
Reference

Hamilton, T. A. Stable digitally-programmable active filters, *IEEE J. Solid-State Circuits*, Feb. 1974, pp. 27-9.

To summarize the methods so far: in place of direct variation of the resistances necessitating a twin-gang potentiometer we have substituted (i) voltage-controlled amplifiers or attenuators (ii) digitally-controled amplifiers that can be programmed in discrete, binary steps. A third principle that has been in use for more than twenty years is regularly re-invented. An electronic switch periodically opened and closed replaces the multiplier attenuator or amplifier. If the switching rate is high compared with the signal frequency the effect is to make the average current proportional to τ, the on-period of the switch. A pair of switches inserted at locations K (above) results in $\omega' \propto \tau$. If switching and signal frequencies are widely separated, simple passive filtering serves to remove the output transients. This is a form of p.w.m. control and can be implemented via a voltage-controlled monostable or by a member of digital techniques including the counter-based idea indicated or binary rate multipliers and dividers.

Reference

Harris, R. W. and Lee, H. T. Digitally controlled, conductance tunable active filters, *IEEE J. Solid State Circuits*, June 1975, pp. 182-5.



Sets 27 & 28: Complementary m.o.s.

The first few cards of set 27 form a useful potted summary of the properties of complementary f.e.ts for readers not wholly familiar with c.m.o.s. devices. Properties that characterize these devices—high input impedance, low quiescent consumption, relatively wide supply range, large output swing—are dealt with first, page 92, followed by dynamic considerations and device equations on page 93, and then modes of connection on page 94. Another characteristic feature is the very wide variation in dissipation with supply voltage, page 93, and the pronounced sensitivity of c.m.o.s. devices to voltage is more fully illustrated by the curves of page 96.
Many circuits based on op-amps can be constructed using c.m.o.s. inverters and gates. Examples included are the rectangular-to-triangle wave converter of page 101, the two- and three-phase oscillators of pages 108 & 109, and the filters of pages 104 & 105. Eight sensing and detection applications are given in pages 106 & 107, using the D-type flip flop.
(Typographical slips on card 6 have been corrected on page 108—they involved incorrect inequality signs in the first and last few lines.)

Linear c.m.o.s. circuits

By considering the various families of logic circuits one can deduce what parameters, designed-in to optimize digital operation, result in adverse performance if the circuits are used in the analogue mode. The most interesting family that is available at a low cost is complementary symmetry metal oxide semiconductor logic or c.m.o.s. By adding an extra diffusion to the processing steps needed for a single type of device, Fig. 1, the complementary type can be produced. Thus the p-channel device is obtained by diffusing p^+ source and drain into the n-type substrate; a deeper p-type well is diffused to contain the n-channel device.

In addition to the conducting channels between the respective sources and drains, there are a number of p-n junctions. Though these are normally reverse-biased by the selected operating mode, their parasitic effects cannot always be ignored. Other p-n junctions are deliberately introduced at the inputs to prevent damage to the thin oxide films by high voltages that might be produced electrostatically or due to external transients.

The conductivity of the channels is increased by a forward bias on the gates. For an n-channel device this corresponds to a gate voltage positive with respect to the source. The conductivity tends to zero for zero gate-source voltage because the doping of the channel is such that there are virtually zero current carriers available. At a particular value of gate voltage, called the threshold voltage, charges induced in the channel by the resulting field allow conduction to commence. No gate current flows because of the insulation provided by the oxide layer. Drain-source conductivity continues to increase with rising gate-source voltage, while the current flow depends on both V_{gs} and V_{ds}. At low values of V_{ds}, the slope resistance is reasonably linear and is controlled by V_{gs}. Ultimately, the output current reaches a limiting value again set by V_{gs} i.e. the output slope resistance becomes very high making the device suitable for various forms of constant-current circuits.

The basic inverter stage is shown in Fig. 2 and the transfer function in Fig. 3. When the input voltage is low, there is insufficient forward bias on the n-channel device to bring it above the threshold of conduction. The reverse is true for the p-channel device which has a high conductivity i.e. the output is virtually equal to $+V_s$. Conversely a very positive input voltage pushes the output close to zero. When lightly loaded the output swings to within 1% of the supply voltage. At voltages in the region of $+V_s/2$ both transistors are conducting. This region is traversed rapidly when the inverter is used as a

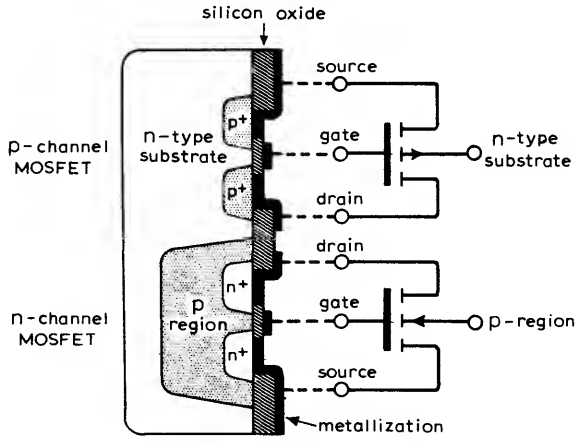


Fig. 1. Structure of c.m.o.s. inverter.

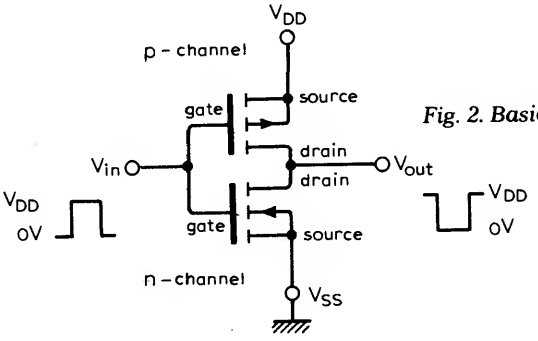


Fig. 2. Basic c.m.o.s. inverter.

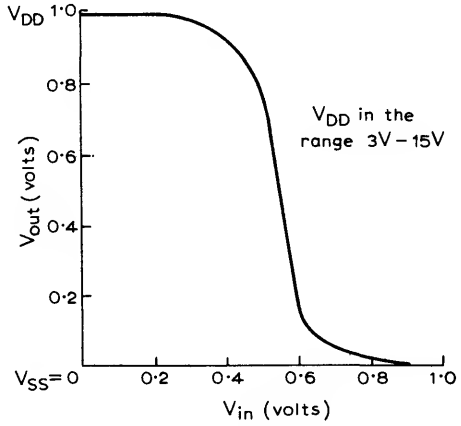


Fig. 3. Transfer function of c.m.o.s. inverter.

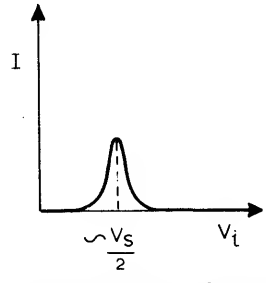


Fig. 4. Variation of inverter current with input voltage.

logic level inverter, but the transient current pulse as shown in Fig. 4 is then the only significant contribution to current drain, as one or other of the transistors is non-conducting in each of the logic states. (At high pulse rates power consumption is associated with the multiple charge/discharge of internal and load capacitances.)

For analogue systems this central region of the characteristic is of great interest. The slope is moderately high, corresponding to a voltage gain of the order −10 to −100 with the unusual property that the gain is greater at lower values of supply voltage (both transconductance and output conductance fall, the last-mentioned more rapidly than the first).

Although not designed for high d.c. stability, temperature dependence of the transfer function is small. Recently c.m.o.s. i.cs have been produced designed specifically for analogue applications; though the configurations may be identical to particular logic circuits, the processing is optimized for linear operation.

Because each m.o.s. transistor can be used as a voltage-controlled resistor, packages containing several devices offer interesting possibilities. The drain-source resistance characteristic remains approximately linear for small values of reverse voltage and current, making a.c. operation feasible. The devices on a common chip will be similar and will be subject to the same temperature variations. Thus, operated from a common gate-source voltage supply, they offer closely-matched resistance characteristics for use in amplifiers etc.

An interesting extension of this technique is possible even where single devices are not accessible separately. By grounding the positive supply line of a package containing multiple inverters, the p-channel devices are kept out of conduction provided the p.d. applied between output and ground of each device is small. Thus a hex buffer inverter i.c. can be used as a set of six matched n-channel f.e.t.s.

Any inverting amplifier can be used with n.f.b. to give a see-saw amplifier of reduced but well-defined voltage gain. As only a single gain-stage is involved external compensation against high-frequency stability is not required even with 100% negative feedback. The bandwidth is not particularly high though well above the audio-frequency range, with some gain to beyond 1MHz. High values of resistors may be used without loading effects due to amplifier input impedance, though the resulting RC time constants due to strays can further reduce the bandwidth.

A recent example of the way in which device technologies change forces a warning note at this point. To improve the performance of gates/inverters for their main functions in purely digital applications, some manufacturers produce "fully-buffered" versions. These might contain three inverters in cascade to perform the function previously using a single inverter. The improved response is welcome to users with critical requirements in the digital field; those wishing to adapt them for analogue circuits, as decribed in Circards Set 27, would find high-frequency instability resulting from the much-increased loop gain and multiple phase-shifts. Remember to check the characteristics of any device or circuit rather than assume that similar titles guarantee identical performance.

If logic circuits could be adapted only for amplifying functions, the exercise would still be worthwhile — it would avoid having to add separate operational amplifiers on those occasions when only simple signal processing is needed. In fact most other electronic circuits can be designed if care is taken to work with the characteristics of c.m.o.s. rather against them. A restriction is that only inverting stages can be used with negative feedback, there being no equivalent to the series-applied feedback circuits (e.g. voltage followers) common in operational amplifier designs. Non-inverting buffers or cascaded inverters lend themselves to positive feedback functions such as Schmitt trigger circuits. Variety can be introduced by using individual devices from certain c.m.o.s. i.cs in combination with inverters and gates.

As a general rule it is simpler to adapt those familiar circuits that use inverting amplifiers, unless the function required cannot be performed in this way.

Circuits that can be designed using inverting amplifiers include active filters such as the two-integrator loop, three-stage phase-shift oscillators, and the like. There is no need to restrict ourselves to simple buffers and inverters; other i.cs can be readily applied in analogue circuits of various kinds. For the more complex i.cs, the degree of internal interconnection reduces flexibility and it is less easy to see ways in which non-logic functions can be performed.

One form of flip-flop, the D-type, has a pair of outputs Q and $\overline{Q}$. When fed with a positive-going pulse on the clock input C, the output Q is forced to take up the logic state on the data input D at the instant of clocking. This state at the output is retained regardless of any variation at D until the next clock pulse. Such a flip-flop finds application in the processing of analogue signals, as in some forms of analogue to digital converters and phase-locked loops. In a particular application, the delta-sigma modulator, the integrator receives a current from the input voltage, which causes its output to change until the comparator output swings through zero. On the succeeding clock pulse the Q-output must change, since the D value has changed, and this changes the f.e.t. between its conducting and non-conducting states. The polarity of input and reference voltage must be opposite so that the fed-back reference can reverse the direction of integration. Combining the clock pulse with Q (or $\overline{Q}$) in a suitable logic gate gives a pulse train in which the average number of pulses is proportional to input voltage.

The above appears to be a complex system, but two properties of c.m.o.s. allow efficient use of the flip-flop. The sharpness of the transfer-function means that the region of doubt at the D input is very small i.e. that even voltages close to $V_s/2$ are clearly distinguished as either logic 0 or logic 1. Hence the comparator can be dispensed with, the flip-flop acting as its own comparator. Similarly the output of the flip-flop is well-defined, and for a stable supply voltage the f.e.t. and separate voltage reference can also be eliminated reducing the system to one op-amp and a flip-flop.

Similar considerations lead to economical circuits for Schmitt trigger, astable and monostable circuits, by making use of the S and R or set and reset inputs, also available in D-type flip-flops. It must be remembered that such circuits may depend on properties which may not be covered directly by manufacturer's data, although the experimental evidence for their satisfactory behaviour is clear.

A semi-digital mode of operation is where inverters are used to drive power transistors. Output stages for class-D power amplifiers are examples where this technique is of use, the c.m.o.s. drivers also helping to switch the transistors off rapidly, though delays may be needed at the inverter inputs to avoid the possibility of simultaneous conduction of both transistors.

There is one family of c.m.o.s. circuits designed specifically for use in linear and non-linear analogue circuits viz the analogue gate/bilateral switch. By driving a parallel complementary pair of m.o.s. transistors with anti-phase logic level signals their conduction can be linearized so that the transfer of voltage is near unity when lightly loaded. This extends over the whole supply range and these gates can be used to switch components in and out of circuit as well as for direct gating of signals. Applications include d. to a. conversion, waveform synthesis and switched filters.

The technology developed for logic applications in c.m.o.s. has proved to have many characteristics that can be pressed into the service of linear circuit designers. The very low cost of these i.cs must commend them, and with care their limitations can be overcome or side-stepped in a wide variety of applications.

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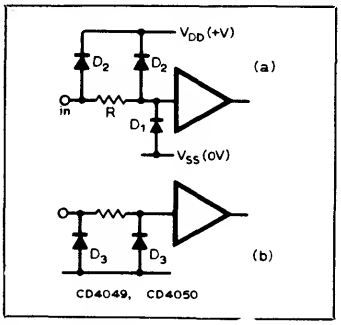
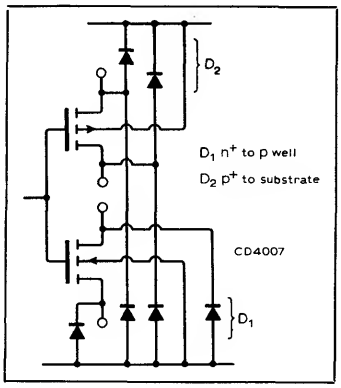
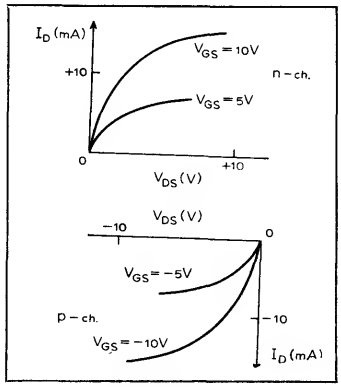
Devices and characteristics



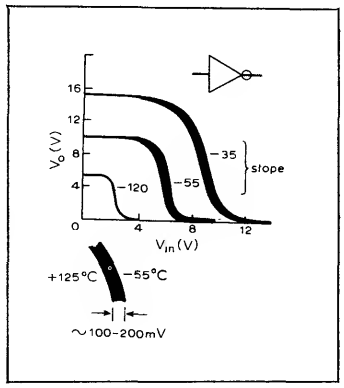
Input protection
A network of diodes at the input of each gate/inverter protects against transients. In linear applications they limit the range of input voltages that can be applied, in particular when the designer seeks access to individual devices, using a non-standard supply voltage to disable unwanted devices. Most packages conform to Fig. 1(a)—certain buffers to Fig. 1(b).



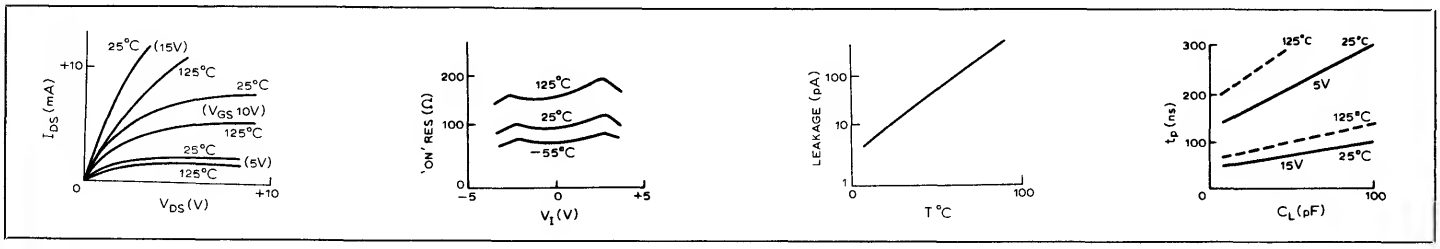
Output diodes
The processing steps needed to produce complementary devices leave a number of p-n junctions between source and drain and the supply terminals. In most devices the sources are already directly connected, but the junctions become apparent in certain i.cs with access to individual devices.



Device characteristics
Each device has a current that is a function of both gate and drain potentials. Above a critical voltage on the drain, which varies with V_{GS}, the drain current becomes largely constant i.e. the slope resistance is large and the device is in a constant-current mode, and said to be saturated. Below this voltage the output resistance is lower, non-linear and is varied by the gate-source voltage.



Transfer function
The output voltage changes sharply with input voltage at a particular input that is remarkably stable against temperature, has a broad tolerance from device to device but is at a roughly fixed percentage of supply for a given device.



Device temperature drift
The drift in characteristics for individual f.e.ts, is much larger than for a complete inverter, verifying the matching characteristics of p-channel and n-channel devices. The resistance increases by about 0.3%/degC. The current for any combination of V_{DS} and V_{GS} falls by around 30% for the temperature range indicated. The current depends on a square-law relationship involving V_{GS} and V_{DS}, except in saturation when V_{DS} has little further effect.

Analogue gate : on-resistance
One class of c.m.o.s. i.cs uses complementary pairs in parallel with the gates driven in antiphase, so that either they are conducting or non-conducting simultaneously. The result is an analogue gate or switch with a very high off-resistance and a low but non-linear on-resistance. Again the resistance is temperature dependent, with a comparable temperature coefficient (caused by the same change in mobility of the current carriers). The pattern repeats itself at all voltages and currents.

Gate input leakage
The input resistance of a f.e.t. is exceedingly high—in practice swamped by external leakage effects due to package pins or p.c. boards. The protective diodes at the input of c.m.o.s. circuits, provide leakage paths which leave the input current either positive or negative depending on the input voltage. Though still very small the current varies exponentially with temperature. A leakage current of 10pA at room temperature could increase a hundredfold at the device maximum temperature. It is generally safe to assume an input resistance in excess of 10MΩ.

Propagation delay
The self-capacitance of a device is a function of its geometry, and is not affected by temperature changes. The increase in resistance increases all the time-constants and, for example, the propagation delay increases at about 0.3%/degC. Similar figures apply to most pulse characteristics, the speed at higher voltages being markedly improved. This is because the sharp fall in resistance allows the larger voltage swing to be achieved in a much shorter time. For linear operation, the bandwidth is much increased at higher voltages, and somewhat decreased at higher temperatures.

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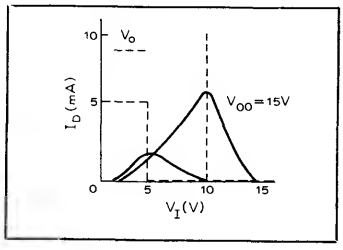
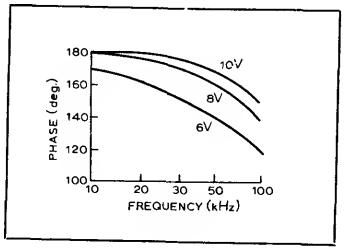
Set 27: C.m.o.s.—2

Linear circuit characteristics

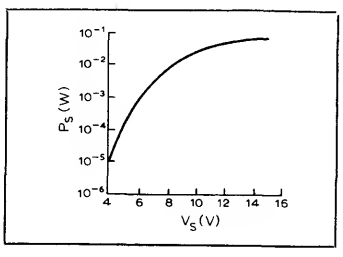


Current variations
When the input voltage to an inverter is varied, it is no longer true that the current remains at zero as in logic applications. For $V_I \approx V_{DD}/2$ the inverter output is in its linear region, both devices are forward-biased and the current rises to a maximum. At high supply voltages the current can be >20mA for high-current buffers. At low supply voltages the current is so low that the operation approximates to class B.

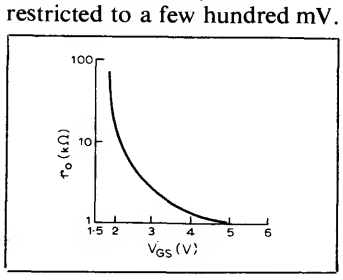
Phase/frequency variation
The change in characteristics with supply, extends to the phase shift at high frequencies. In a multi-stage amplifier this could bring the frequency at which instability might occur to below 100kHz (60° phase lag per stage at 6V supply would give a total phase shift of 180° in a three stage feedback amplifier). This together with the drastically increased output resistance makes it difficult to design linear amplifiers at supply voltages of 5V and below.

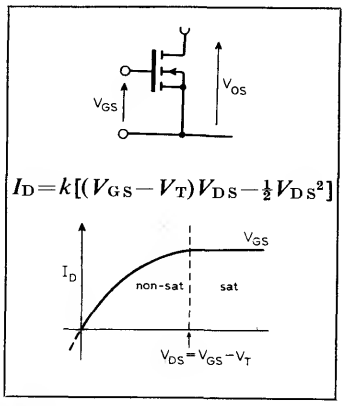


Power dissipation
As an example a NOR gate was biased for $V_O = V_I$ and the supply voltage varied from 4 to 15V. At the low end the current fell to 2μA with a dissipation below 10μW. At the supply maximum the dissipation approached 100mW—the limit suggested for any single gate or buffer with a package limit of 200mW. Thus it would not be safe to operate all four gates in the linear mode at the otherwise safe supply voltage of 15V.



Output resistance
The slope-resistance of a m.o.s.f.e.t. is moderately linear close to the origin, and can be varied over a very wide range. At high values of V_{GS} the resistance can fall well below 1kΩ. As V_{GS} approaches the threshold voltage, the device is cut off and the slope resistance tends to infinity. In practice a controlled resistance of order 100kΩ is possible. In all cases the polarity of V_{DS} may be reversed, and the V/I characteristic is continuous though the voltage swing for reasonable linearity is restricted to a few hundred mV.





Basic device equations
The equation gives the drain current as a function of the p.ds between gate and source, and drain and source in the unsaturated region. As V_{DS} is increased to the point where $V_{DS} = V_{GS} - V_T$ (*) the current becomes substantially constant. Alternatively when V_{GD} exceeds the threshold V_T, the channel is pinched-off to an extent that inhibits any further increase. Both regions of operation are of interest for different applications.

Below saturation
Both drain and gate potentials have an effect, but if V_{DS} is small then the equation approximates to a linear one—it extends below the origin but there is an additional constraint imposed by protective diodes.
$I_D \approx k(V_{GS} - V_T)V_{DS}$
Thus the slope resistance at low voltages becomes
$dV_{DS}/dI_D \approx 1/k(V_{GS} - V_T)$
This is a voltage-controlled resistance though it is neither a linear resistor nor a linear function of the controlling voltage. The departure from linearity is small enough for $V_{DS} < 100$mV to use the resistor in feedback networks etc to control gain, but distortion prevents its use at higher voltages than a few hundred millivolts.

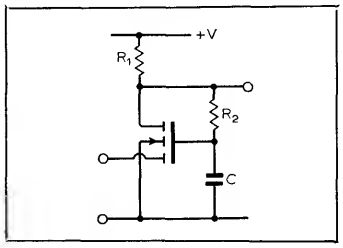
Above saturation
The current is assumed to be constant at the value it has for the condition given by *.
Hence $I_D = k(V_{GS} - V_T)^2/2$
This is a square-law function requiring the elimination of V_T by some compensating circuit if a square law relationship is to be obtained between input and output voltages.
Transconductance can be obtained by differentiating I_D with respect to V_{GS}
$g_m = dI_D/dV_{GS} = k(V_{GS} - V_T)$
i.e. $g_m \propto \sqrt{I_D}$. As the drain current is increased by increasing the forward bias on the gate, the g_m increases, but more slowly than the fall in load resistance that would be needed in a resistively loaded stage to allow that current to flow. Since the voltage gain depends on the product of g_m and R_L, higher voltage gains can be obtained by operating at the smallest possible current, increasing R_L accordingly. This information does not apply directly to c.m.o.s. inverters where the load of one m.o.s. device is the output of the other; it indicates a different pattern for f.e.ts from that familiar in bipolar designs where comparable voltage gains are available at all current levels.

Assuming that the device is operated with the lowest possible V_{DS} to maximize R_L i.e. just at pinch-off, voltage gain becomes
$-2[(V_{DD} - V_{GS} + V_T)/(V_{GS} - V_T)]$
This is the maximum possible voltage gain for a m.o.s.f.e.t. with threshold voltage V_T operated with a gate-source voltage V_{GS} and with a supply voltage V_{DD}. In practice the voltage gain will be smaller in magnitude because of finite output resistance etc.
N.B. The basic form of these equations applies to all m.o.s.f.e.ts; the coefficients of practical devices differ from those given and account has to be taken of this—see card 7.

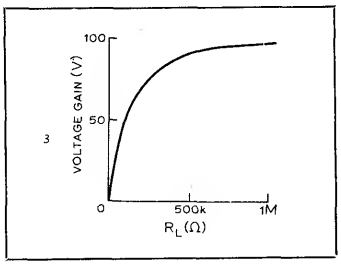
Further reading
Motorola, McMOS Handbook, 2nd edition 1974, pp. 1-7 to 1-18 and 3-1 to 3-7.
Santoni, A. & Trolese, G. Design ideas with COS/MOS, *New Electronics*, April 30, 1974, pp. 27-34.

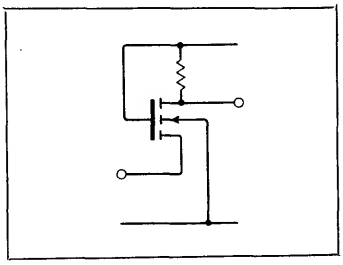
wireless world circard

Device configurations



Typical performance
IC CD4007AE
n-channel device
Supply +10V
R_1 100kΩ
R_2 10MΩ
C 100nF
Voltage gain +50



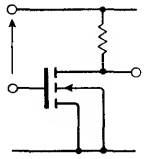


Circuit description
In certain c.m.o.s. i.cs, access may be gained to the sources/drains of individual f.e.ts (CD4007, CD3600 and similar). Where this is so, circuits may be constructed that are the counterparts of the more familiar common-base common-collector etc. Consider the common-gate amplifier shown above. The gate is grounded for a.c. purposes by the capacitor. The gate current is negligible and the p.d. across R_2 may be assumed to be zero. The d.c. operating conditions for the amplifier are thus $V_{GD}=0$ and R_1 defines the direct current flow. The alternating voltage gain depends on the parallel value of R_1, R_2. The input impedance is low, and to a good approximation is $1/g_m$ where g_m is the transconductance of the device as usually defined. This varies with the operating current being proportional to $\sqrt{I_D}$. Since $I_D \propto 1/R_1$ if the p.d. across R_1 is constant (a reasonable approximation when the supply voltage is well above the device threshold voltage) then the voltage gain ($\approx g_m R_1$) is proportional to $\sqrt{R_1}$. The approximation is not valid at very low currents and the voltage gain is limited to about +100. The voltage gain for a given value of R_1 is roughly proportional to the square root of the supply voltage by the same reasoning, falling more rapidly as this approaches the threshold values. The amplifier has a high non-inverting voltage gain, a low input-impedance and a high output-impedance.

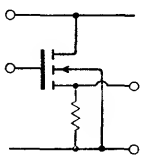
Component changes
IC: must be package with separate access to drain. Any discrete m.o.s. device (enhancement mode can be used in these circuits—the aim here being to indicate where c.m.o.s. packages can be adapted to provide functions that would otherwise require separate discrete components).
Supply: +5 to +15V.
Some gain available at lower supply voltages.
R_1: sets the quiescent levels and the output impedance. Can be replaced by current source for increased voltage gain.
10k to 1MΩ.
R_2, C: provide decoupling and the time-constant must be long compared with period of lowest frequency. R_2 1M to 22MΩ.

Circuit modifications
- The gate can be connected directly to the positive supply, which reduces the component count, but removes the stabilizing action of the d.c. negative feedback. Otherwise, the a.c. properties are comparable.
- Each of the other device configurations is possible, the common-source version simply disregarding the presence of the p-channel device by ensuring that its source and/or drain is open circuit. The voltage gain is comparable to that for the common-gate stage but the input current is now zero, and the output is inverted.
- A common-drain or source-follower configuration can often be provided while using the other transistor of the complementary pair in some other circuit, e.g. astable oscillator. Whatever waveform appears at the common gate is transferred to the source with some attenuation but without loading the waveform. Since source and drain currents are equal an antiphase output can be obtained at the drain.
A novel arrangement joins the gate to the drain for 100% negative feedback. The device is now apparently a two-terminal device and might be expected to behave as a non-linear resistor. In fact it acts as a non-inverting voltage amplifier with a low voltage gain. This is because the substrate connection acts as a subsidiary gate and the operation is that of a grounded-gate amplifier with the gain much reduced by the feedback to the main gate.
Any of the multi-transistor circuits can be implemented using several devices from a package and the example illustrated is the cascode circuit useful for high voltage gains where input-output isolation is important.

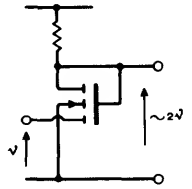
Cross references
Set 27, card 2.
Set 20, card 8.



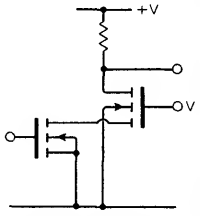
common source



common drain

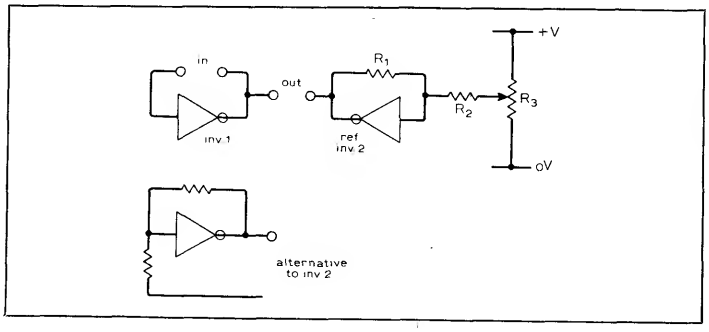


two-terminal amplifier

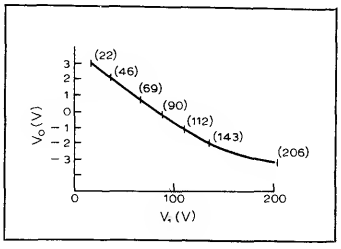


cascade amplifier

D C amplifiers



Typical performance
IC CD4001AE NOR gates with 2 inputs active
Supply +10V
R_1 27kΩ
R_2 1MΩ
R_3 100kΩ



Circuit description
C.m.o.s. inverters are not suited to the amplification of small d.c. voltages. They have a threshold voltage range below and above which the output is saturated. The simplest way of biasing an inverter/gate into its linear region is via direct or resistive feedback from output to input. This ensures $V_{out} = V_{in}$ which is near the middle of its linear region, the voltage gain lying between −10 and −100. Although there is a measure of matching between devices on the same chip, the tolerances are much relaxed for digital circuits. The output voltage under these conditions may have a total spread of up to 40%, with the difference between gates from a given chip reduced to the order of 100mV. This allows the use of a pair of gates, one as the amplifier and the other to act as an artificial ground point. The offset voltage can be ruled out by injecting a portion of the supply via R_3 and R_2 as shown, while the offset itself has a relatively small temperature dependence. There remains one major advantage of these devices as d.c. amplifiers, viz their very high input impedance. If feedback is to be used to define the voltage gain while exploiting this high input impedance as fully as possible, the source can be connected between the input and output of the inverter. For a voltage gain of −100, 99% of the source voltage appears at the output terminal and 1% at the input i.e. the accuracy with which an input signal is transmitted to the load can be well within the tolerance of moving-coil meters. The current drawn from the source is not specified in the data sheets as these devices are intended for digital functions, but is basically due to the minute leakage currents of the reverse biased protective diodes. With some sample gates, the output changed by <1% for a change in source resistance of 4.7MΩ. The configuration is clearly restricted to a floating source (high impedance transducer such as piezo-electric devices) or would require a floating power supply. The second inverter compensates for most of the quiescent output by its matched characteristics, the remainder being cancelled by injecting a variable current via R_2, R_3.

Component changes
● The only changes in the resistors are to vary this offset compensation. The values are not critical, but $R_2 \gg R_3$ and R_1/R_2 = offset voltage/supply voltage, indicate the values.

The inverters can be buffers, NOR and NAND gates or the inverters constructed from CD4007 or CD3600 packages. None of these compete in performance with op-amps constructed from the appropriate m.o.s. and bipolar transistors. They are intended only to extend the applications of inverters/gates to simple d.c. applications where the signal voltages are large enough that significant offset can be tolerated.

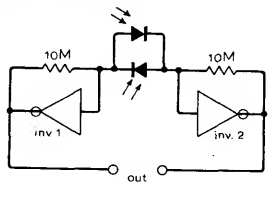
Circuit modifications
● A possible application is in the amplification of small currents from photo-diodes used in their photo-voltaic mode. For matched diodes exposed to different light intensities, there will be a current of given polarity representing the difference between the light intensities. This will drive the outputs of the inverters in anti-phase, and currents well into the sub-microampere range could be detected. $V_0 \approx 20M\Omega \times I_{diff}$. The inverter can be used in the see-saw mode with resistor values of megohms if required.

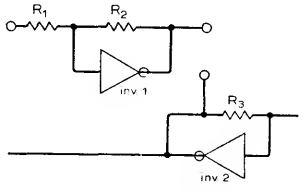
The voltage gain can be set to between −1 and −10 with good accuracy, with a second inverter to provide an artificial ground point. Both input and output voltages are then referred to this point. For constant supply voltages, the inverter can also be used as a comparator since its input threshold voltage varies little with temperature (<1mV K^{-1} for some gates i.e. <0.01% of the supply voltage at V_s = 10V). A zener diode placed in the feedback has a current forced in it of $\approx V_s/2R_1$ and the gate output voltage is raised by V_z over its normal threshold. This can be used to define the compensation current fed into other stages used as d.c. amplifiers etc.

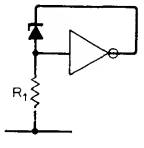
Further reading
McMOS Handbook, Motorola 2nd edition 1974, p. 8-15.

Cross references
Set 27, card 1.
Set 11, cards 5, 6.
Set 20, card 8.
Set 9, card 11.

Circuit modifications

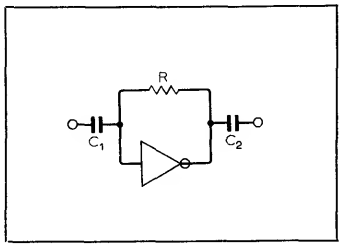


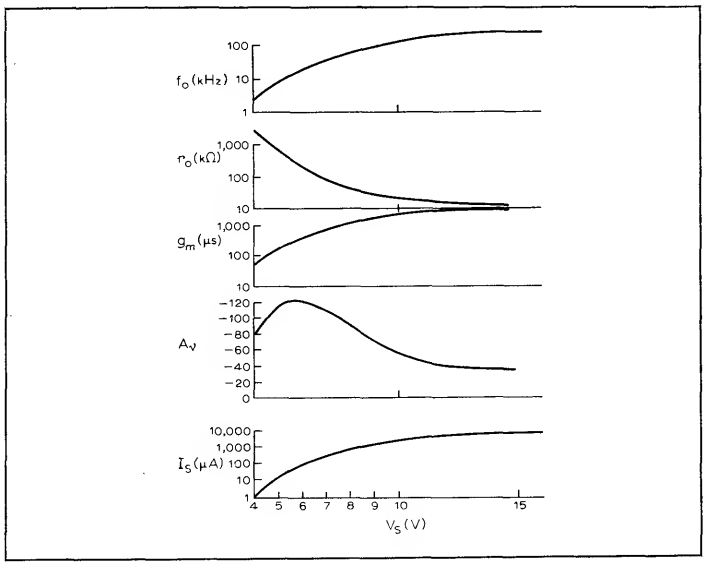




A C amplifiers

Typical performance
IC ¼×CD7001AE
Supply +10V
Quiescent current 1.9mA
Output resistance 25kΩ
Voltage gain −53
Transconductance 2.1mS
Upper cut-off frequency 130kHz
R 6.8MΩ
C_1, C_2 100nF



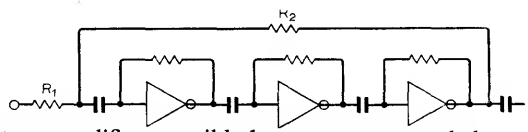


Circuit description
The basic open-loop behaviour of an amplifier can be predicted from its internal structure fairly readily in cases as simple as a c.m.o.s. inverter. For the resistive feedback bias as shown, the input and output potentials are equal. Hence each device operates with equal gate and drain potentials. This introduces opposing effects on the voltage gain as the supply voltage increases. First the increase in operating current which is very marked leads to an increase in the transconductance (g_m). At the same time the output resistance is markedly reduced because each device is operated on or below the knee of its output characteristic. The net effect is that the overall voltage gain is relatively constant varying by only 10dB over a 1,000:1 range in currents. The measurements were all made with a probe having an input resistance of 10MΩ and with a total input capacitance and strays of about 18pF. The high voltage gain at the lower supply voltages is hard to make use of, since even the high feedback resistance contributes to the loading effect. The increase in cut-off frequency as the current rises, can be explained if we assume a total output capacitance which is constant. If the output resistance is r_o, the cut-off frequency f_o and the shunt capacitance C, then $f_0 = 1/2\pi R_0 C$ would be the appropriate relationship if the transconductance is assumed to contribute nothing to the frequency dependence. This implies $f_0 R_0$ should be a constant. Comparison of the data shows a variation of around 2:1 over a 1000:1 range of currents. On these figures, the output capacitance would be around 20pF.

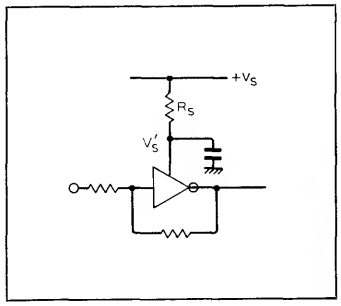
Circuit modifications
- Multi-stage amplifiers are possible, but since c.m.o.s. stages give sufficient gain/accuracy for routine functions, the additional complexity of the compensation networks would appear to be a bad bargain. With d.c. coupling, the low-frequency time constants are eliminated and over-all feedback can hold all three stages within their linear range.
- An inverter can be operated at low current from a high-voltage supply by adding a series resistor in the supply line and decoupling the inverter supply pin. N.B. The supply rejection ratio is only 6dB since the output of a device with feedback biasing is always of order $V_s/2$. If the series resistor is chosen so that the quiescent current is only a few microamperes, the devices must settle at V_{GS} values close to the device thresholds. This sets the effective supply voltage V_s to about the sum of the threshold voltages i.e. 3.6V.
- In devices with access to the sources (CD4007, CD3600 etc) resistors may be added as shown to define and reduce the g_m values while increasing the output impedance.

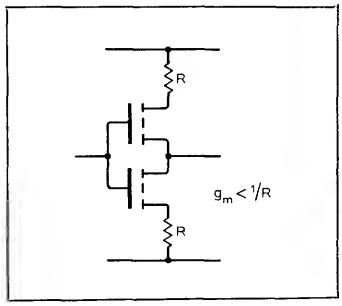
Further reading
McMOS Handbook, Motorola pp. 8.3-8.15, 3.13-3.18, 2nd Edition, 1974.
Fitchen, F. C. and Ellerbruch, V. G., Linear operation of the m.o.s.f.e.t. complementary pair, *IEEE J. Solid State Circuits*, SC-6, 1971, Dec. pp. 422-423.
Santoni, A. & Trolese, G. Design ideas with COS/MOS, *New Electronics*, April 30, 1974, pp. 27-34.

Cross references
Set 27, cards 1, 4, 6.
Set 27, cards 4, 6, 8.
Set 12, card 1.

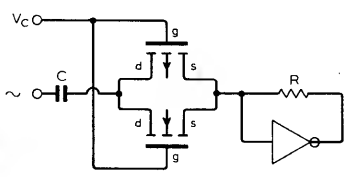


Multistage amplifier: possible but not recommended as accumulated phase shifts make it difficult to apply sufficient feedback without oscillation and input stage noise can saturate the output stage.



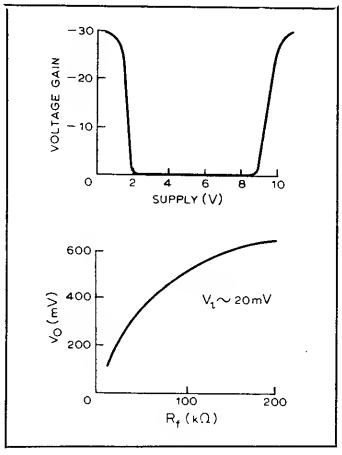


Gain-controlled amplifiers

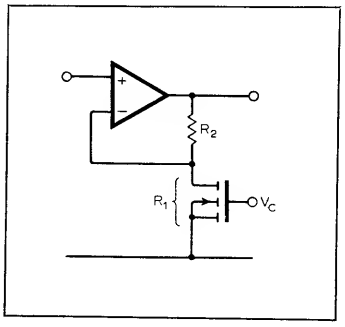


Typical performance
IC 2/3×CD4007
Supply 10V
R 220kΩ
C 1μF
Control V_c 0 to 10V voltage

Circuit description
A more familiar method of using a m.o.s.f.e.t. as part of a gain-controlled amplifier is to use it as the lower section of a potential-divider in either the forward or feedback paths of an amplifier. This allows the m.o.s.f.e.t. to operate with source grounded and makes it easier to apply a control voltage to the gate. If the source is connected to any other point at a constant potential then a control signal may be applied, but it must be sufficient to take V_{GS} above its threshold value V_T. In the circuit shown, either or both of a complementary pair can be used with gates, sources and drains commoned, provided these are not already grounded internally. If the control voltage V_c is in the mid-range of the supply there is insufficient V_{GS} to bring either device into conduction and the voltage gain→0. When the control voltage is very low, the p-channel device is brought into its conducting state and the gain sharply increases. For $V_c \rightarrow V$, the n-channel device has a low slope resistance and the gain increases. The graph shows that either characteristic can give a voltage gain which can be controlled from zero up to −30. At the low values of gain the control action is rather sharp. The amplifier is another c.m.o.s. pair used as an inverter with R providing shunt feedback defining the input potential by the virtual earth action.

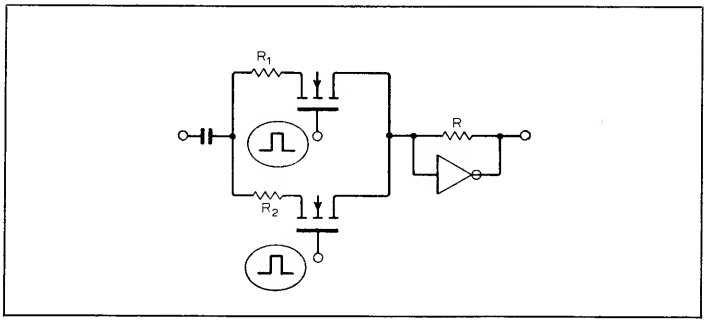


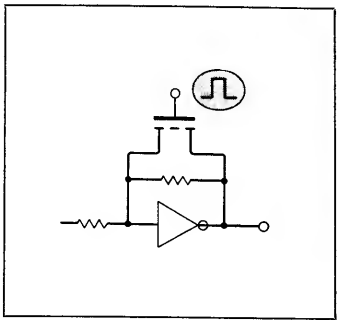
Component changes
IC: Any single m.o.s.f.e.t. either p- or n-channel may be used.
Supply voltage: since each f.e.t. receives a gate-source voltage which is $< V/2$ the supply voltage has to be $> 8V$ in this circuit.
R_f: 10k to 1MΩ
C: not critical. Determines l.f. response. 0.1 to 10μF.



Circuit modifications
- A conventional op-amp circuit can be used as a virtual earth amplifier with the f.e.t. in the forward or reverse paths. Because the f.e.t. has a variable resistance, this complicates the design of the system unless the source has a very low internal resistance By placing the f.e.t. in the series feedback path, the loading affects the output of the amplifier which can tolerate it.
- If two or more f.e.ts are placed in parallel paths they may be gated on or off. This offers a simple alternative to a separate analogue gate i.c. if the performance requirements are not too critical. Both the gates and the inverting amplifier can be derived from a single low cost CD4007 or similar. If the gates of the m.o.s.f.e.ts are paralleled the gain is switched between $-R/R_1$ and $-R/R_2$ provided the on-resistances are low compared with R_1, R_2. It is suitable for gains in the region −1 to −25.
- The f.e.t. can also be placed across the feedback path provided the voltage swing is small enough to prevent non-linearity from producing excessive distortion. One or more devices can be used across both input and feedback paths. Non-linear elements or reactive components can also be placed in series with the f.e.ts. The on-resistance is high compared with devices designed specially as analogue gates.

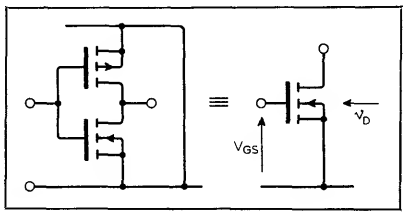
Cross references
Set 27, cards 1, 5, 7.
Set 20, card 8.
Set 21, card 4.
Set 22, card 7.
Set 16, card 10.



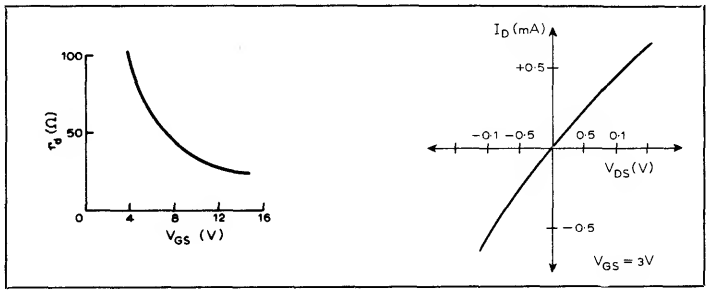


wireless world circard

Controlled resistances



Typical performance
IC CD4049
V_D 50Ω at V_{GS} of 7V for n-channel device



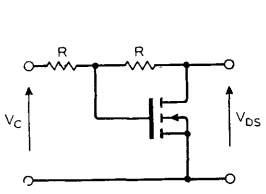
Circuit description
Some i.cs contain multiple inverters e.g. CD4049 hex buffer. Consideration of their internal structure shows that if the V_{DD} line is shorted to the V_{SS} and then used as the common line, then a positive control voltage on any input varies the slope resistance of that output as if it were a single n-channel f.e.t. If the p.d. across the drain source path is less than 0.5V the internal diodes are not brought into conduction. Hence the package is equivalent to six independent well-matched n-channel enhancement mode f.e.ts. These can be used separately or in combinations in any circuits where voltage-controlled resistors are required. The slope resistance at the origin is controllable over a 10:1 range though the resistance becomes non-linear at a progressively lower drain-source voltage as the gate voltage approaches the threshold value. The non-linearity is indicated for V_{GS} of 3V. The devices match to within 5% with the samples tried but this is not covered by the package specifications since these were designed for digital applications. The resistance is non-linear. As the forward voltage drop across the drain-source path is increased, the value of V_{GD} is reduced, this reduces the forward bias and decreases the channel conductivity. Conversely, a negative current in the drain increases V_{GD} and increases the channel conductivity. When V_{GS} is large the contribution due to the small values of V_{DS} (0 to 200mV) is negligible and the on-resistance can be assumed linear for most applications. The example shown represents the lower limit of V_{GS} at which use as a controlled resistance might be acceptable. The non-linearity is predictable from the basic device equation (Set 27, card 2) $I_D=k[(V_{GS}-V_T)V_{DS}-nV_{DS}^2]$ This theoretical equation represents a wide variety of devices over a range of currents and voltages, and it is common to assume $n=\frac{1}{2}$. Where this is true it leads to a particularly simple technique for removing the non-linearity from the on-resistance.

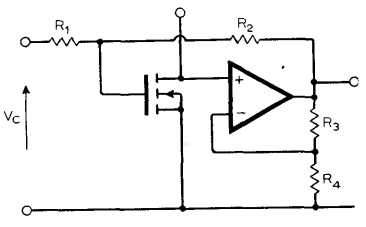
Circuit modifications
- Assume equation to be valid for $n=\frac{1}{2}$. If $V_{GS}=(V_C+V_{DS})/2$ achieved by using equal value resistors as shown, then substituting into the first equation gives $I_D=k[(V_C/2+V_{DS}/2-V_T)V_{DS}-\frac{1}{2}V_{DS}^2]=k(V_C/2-V_T)V_{DS}$ i.e. V_{DS} is a linear function of I_D for all values of I_D within the device limits, but the slope is controlled by the direct voltage V_C. The resistors attenuate the control action and V_C has to have twice the value it had in the simple circuit overleaf. Tests with devices from c.m.o.s. packages suggest that in this application considerably more feedback is needed to linearize the characteristic, though some improvement is offered. To test the principle the drain-source voltage has to be amplified before deriving the feedback.
- If the gain is made > minimum required to achieve compensation (e.g. $R_3=9R_4$ giving a gain of +10) then compensation is achieved with $R_1 \ll R_4$ i.e. the control voltage reaches the gate with little attenuation. With $R_2=7R_1$ and the above ratio for R_3/R_4 the on-resistance of a CD4049 n-channel device was controllable from 25 to 200Ω with characteristics matched in the positive and negative quadrants to better than 0.5% and a non-linearity of less than 1.5% (less than 0.5% up to 100Ω). The range of control voltages required was from 3.4V (200Ω) to 16.5V (25Ω). These resistor values feed back a portion of V_{DS} to the gate given by $[V_{DS}R_1/(R_1+R_2)][(R_3+R_4)/R_4]=1.25V_{DS}$. This suggests using $n=1.25$ for these devices to determine the necessary compensation. Unless $n<1$ it would seem to be necessary to use an amplifier with each device to obtain accurate linearization.
- An alternative circuit combines the resistive networks to apply a voltage to the gate of $V_C/4+1.25V_{DS}$. Though simpler, this version requires a larger range for V_C.

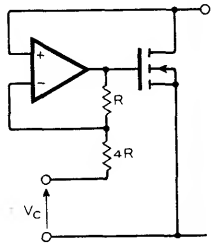
Further reading
Santoni, A. & Trolese, G. Design ideas with COS/MOS, *New Electronics*, April 30, 1974, pp. 27-34.

Cross references
Set 27, cards 1, 6.
Set 22, card 7.

Circuit modifications







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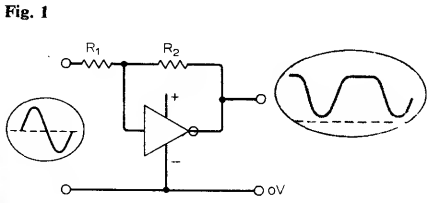
Set 27: C.m.o.s.—8

Non-linear circuits I

Fig. 1



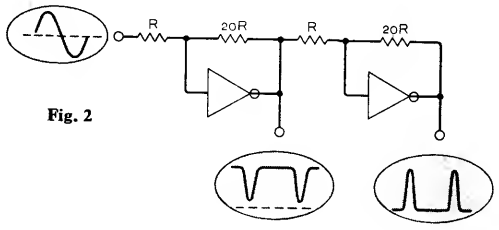


Fig. 2

Circuit description 1
The inverter transfer function is such that the output changes rapidly only when the input is close to a threshold voltage of about 45% to 55% of the supply. If the circuit is fed from ground-referred sine-wave with no d.c. blocking capacitor then the output will be severely distorted in most cases. As an example consider a device with threshold 50% of supply and with $R_1 = R_2$. When the input is at zero, the output must be at +V since there will be equal p.ds across R_1, R_2. For all negative inputs the output holds constant at +V. For all positive inputs the change in the output is equal and opposite i.e. the positive half-cycle of input is reproduced as a negative half-cycle with respect to the positive line. The amplifier gain falls as the swing approaches the supply lines so that perfect half-wave rectification is not possible.

If the circuit is followed by an identical second stage, the output is inverted and approximates to a non-inverted half-wave rectified version of the input. In each case the peak input has to approximately equal the supply for the output to swing through the whole supply range.

Circuit description 2
The resistors are made unequal to give an inverting gain to −10 to −20 depending on the open-loop gain. In this case the output remains at +V until the input approaches very closely to the inverter threshold voltage. It is only the positive peaks of the input signal that cause any change in the output. The output then consists of short-duration negative going swings coinciding with the positive peaks of the input. If a second identical stage follows it, the peaks are further sharpened up and inverted. The result is a highly amplified version of the extreme positive peaks of the input. The threshold voltage of a given device is a well defined fraction of the supply and varies little with temperature. Thus each device would respond to a particular peak input but once adjusted the response could be maintained.

Circuit description 3
If the original waveform is unimportant, negative-feedback need not be used. The input is biased up to the supply rail and the output consists of negative-going pulses coinciding with the positive peaks of the input (the pulse width increases as the input-amplitude increases since the waveform lies above the threshold for a longer fraction of the cycle). If the output is applied directly to a second inverter the output is re-inverted and is sharpened into an almost rectangular pulse equal in height to the supply.

Circuit description 4
The output pulse from such a system can also be sharpened by introducing non-linear elements into the forward or feedback paths. As an example, a pair of parallel-connected back to back diodes limit the output swing to 1V peak to peak since the currents are small. Further, this swing is centred on the threshold voltage which can assist in direct coupling to other stages.

Circuit description 5
A simple frequency-doubler uses a NOR gate together with a peak-selector circuit. If either of the NOR gate inputs goes above its threshold, the output goes to logic 0. This happens on positive peaks of the input via R (which serves to limit any input current for negative inputs). On negative peaks, the input of the inverter is pulled below its threshold and its output goes high. This again drives the NOR gate output to logic 0. Thus there are two negative peaks to the output during one cycle of the input, representing frequency doubling. In principle the circuit could be followed by an active filter to retrieve a sine-wave which would be available for further frequency doubling.

Further reading
Dean, J. A. & Rupley, J. P., Astable and monostable oscillators using RCA COS/MOS digital integrated circuits, RCA app. note ICAN-6267.

Cross references
Set 27, card 9.

Fig. 3

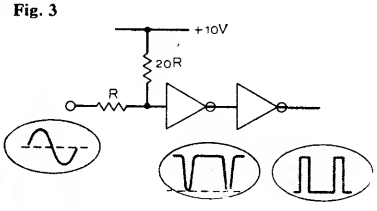


Fig. 4

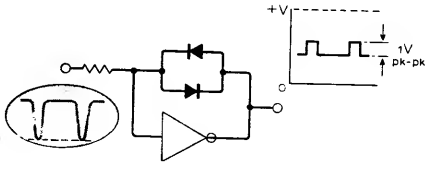
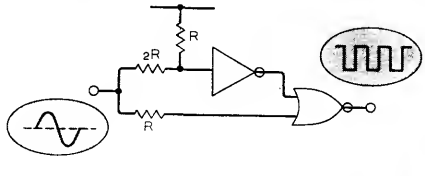


Fig. 5



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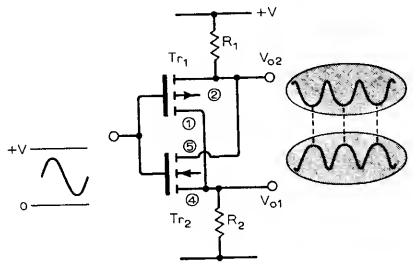
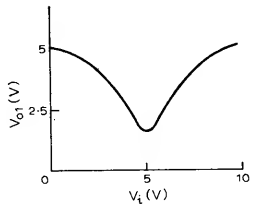
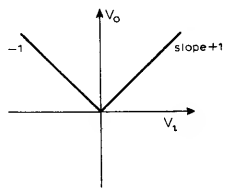
Non-linear circuits II



Typical data
IC 1/3×CD4007AE
Supply +10V
R_1 10kΩ
R_2 10kΩ
Output ≈ $V/2$ at $V_i=0, V$ and $V/4$ at $V_i=V/2$.





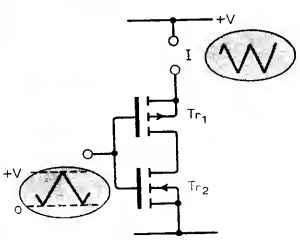
Circuit description
The circuit exploits the non-linear characteristics of c.m.o.s. pairs by cross-coupling sources and drains of a single pair having a common gate. This produces the novel transfer function shown. When the input voltage is high, the p-channel device Tr_1 is non-conducting and the output voltages are determined only by the current in Tr_2. This has resistor R_2 in its source making the transfer function somewhat less than unity but with a linear slope. At all times the currents in R_1, R_2 are equal making the slopes inverse. As the input is low the reverse occurs with Tr_1 conducting, Tr_2 off. If the devices are truly complementary the output voltage would be the same at two values of input voltage, V_i and $V-V_i$. The minimum current and hence the minimum value of V_{01} occurs for $V_i \sim V/2$. If the input is biased to this value and a sine-wave superimposed then the circuit behaves as a full-wave rectifier. This can be seen from the transfer function of an ideal full-wave rectifier in which $V_o = |V_i|$. Any other waveform can be applied, with bias offset if desired to further modify the output waveform. The output for a triangular wave input is a triangular wave of twice the fundamental frequency. In principle the process can be repeated by a.c. coupling into an identical second stage but waveform deterioration limits it to two or three stages at most.

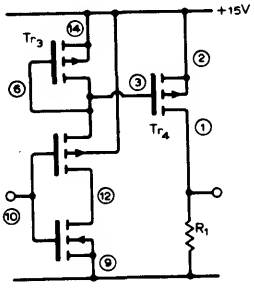
Component changes
For anti-phase outputs $R_1=R_2$. Values not critical and similar shape of transfer function obtained for R_1 1k to 100kΩ. Supply voltage: 5 to 15V. IC: the circuit depends on having access to both sources and drains of a complementary pair and can only be implemented with CD4007 and similar devices.

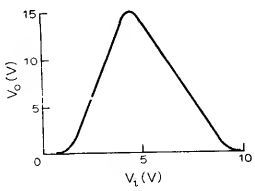
Circuit modifications
- If the current in a c.m.o.s. pair is monitored, it is found to pass through a maximum value at $V_i \approx V/2$ i.e. when both devices are about equally forward biased. At the two extremes $V_i \to 0$, $V_i \to V$ the current falls to zero. This gives a similar non-linear relationship to the previous circuit. To exploit this shape, the current can be fed to a current mirror composed of Tr_3, Tr_4. Output current flowing in R_1 passes through a peak on each excursion of V_i through the supply mid-point (with considerable variation from device to device in the actual values but all with a similar shape of transfer function). The value of R_1 depends on the supply as well as the devices but is typically 1k to 10kΩ.
- A triangular wave input gives a somewhat rounded wave output, there being no negative feedback in this circuit to linearize the transfer function.
- In addition to the above, there are a number of circuits that use the characteristics of the individual m.o.s. devices. By cancelling the threshold voltage, a close approximation to a square-law can be obtained. These will be covered in a later series of Circards.

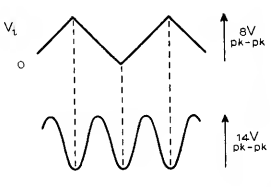
Cross references
Set 27, cards 2, 8.

Circuit modifications









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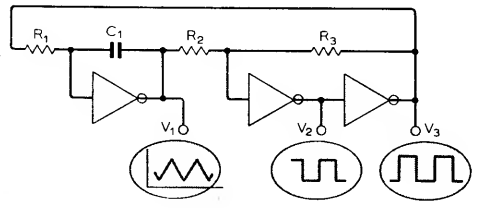
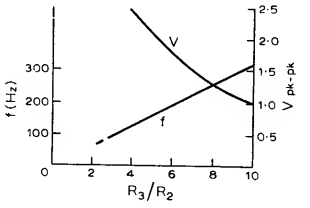
Square-triangle generator



Typical performance
IC CD4007AE
Supply +10V
R_1 100kΩ
R_2, R_3 50kΩ
C_1 3.3nF



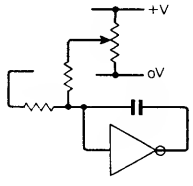
Circuit description
Since a c.m.o.s. inverter has a voltage gain of between −20 and −100 it can be employed for many of the functions usually associated with op-amps. An integrator fed with a constant direct voltage delivers a constant current to the capacitor. The output is then a linear ramp. When the gain of the amplifier is finite, the current changes with output amplitude leading to non-linearity. Even the limited gain of these inverters is sufficient to hold the non-linearity to within one or two per cent. A second limitation, that of finite input current, is not a problem with c.m.o.s. devices and the resistor values are limited only by the effects of stray capacitance on the waveforms. To make a free-running generator the ramp waveform is applied to an amplitude sensing switch—a pair of inverters with overall positive feedback suffices. The output of this switching circuit is a square-wave whose transitions coincide with the peaks of the triangular wave. Because the threshold voltage is not precisely 50% of the supply the positive and negative slopes are unequal as are the on-and-off periods of the square wave. This can be corrected as shown overleaf. There is a second square-wave in antiphase to the main output, while the frequency can be controlled without change in triangular wave amplitude by varying R_1 or C_1. Changing the ratio R_3/R_2 changes the amplitude of the triangular wave as well as the frequency. Since the slope remains the same under this change, the frequency is inverse to the amplitude.

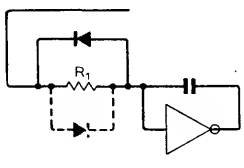
Component changes
IC: any set of three inverters (or a single non-inverting buffer may replace the switch pair if available). NAND or NOR gates may be used with inputs paralleled.
Supply: +5 to +15V. At low voltages the rise in output impedance restricts the resistances to high values.
R_1: 10k to 10MΩ.
R_2, R_3: 10k to 10MΩ.
Triangular wave output should not exceed say 50% of the supply if waveform distortion is to be minimized. Hence $R_3/R_2 > 2$ is required. If the ratio is too large, the triangular wave amplitude may be too small for convenience, and switching transients more troublesome.
C_1: as low as 100pF with high values of resistance but generally 1n to 1μF. Very low-frequency triangular waves possible with this circuit.

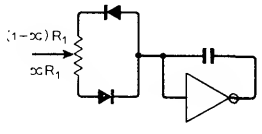
Circuit modifications
- Many op-amp techniques can be adapted to improve or modify the output waveforms. N.B. The triangular wave has a large d.c. content being roughly centred on $V_S/2$. To change the slope a single fixed resistor may be taken from the integrator input to zero or $+V_S$. For controlled compensation, a potentiometer across the supply can be used.
- A good approximation to a sawtooth waveform follows, when R_1 is shunted by a diode. With the cathode driven by the trigger circuit, the output positive ramp is greatly speeded up while the negative ramp remains under the control of R_1. Reversing the diode gives a sharp negative edge followed by a controlled positive ramp.
- Replacing R_1 by a potentiometer and a pair of diodes, the charge and discharge cycles are varied. For equal voltage swings, one part of the cycle is proportional to xR_1 and the next to $(1-x)R_1$. The total period remains broadly constant though there are second-order effects that prevent this from being completely achieved. It gives a variable mark-space ratio to the square-wave with a reasonably constant frequency.
- The triangular wave can be shaped into an approximate sine wave in a number of ways. An amplifier can be added with non-linear elements in the forward or feedback paths. An alternative is to use a second integrator with decoupled d.c. feedback. This converts the ramps into parabolic sections which match a sine-wave reasonably well (as little as 4% t.h.d.).

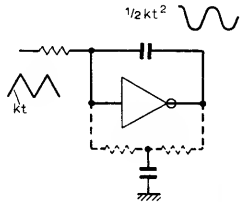
Further reading
Santoni, A. & Trolese, G. Design ideas with COS/MOS, *New Electronics*, April 30, 1974, pp. 27-34.

Circuit modifications









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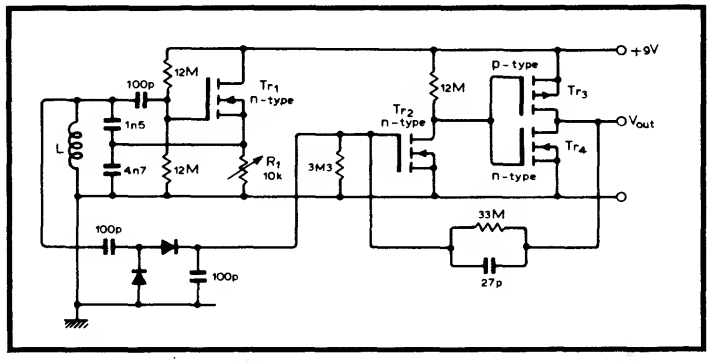
Set 27: Up-date

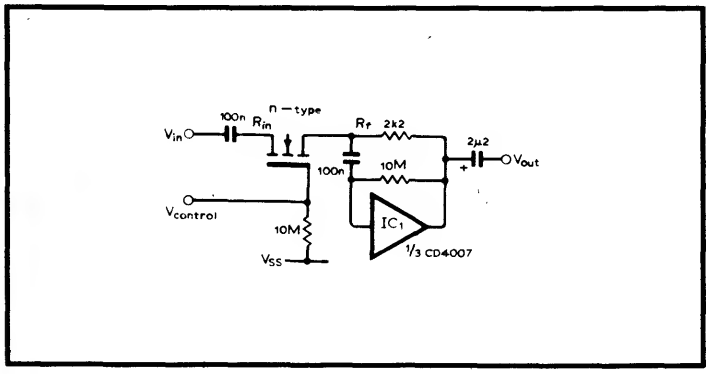
Inductive proximity detector

This employs a CD4007 package to provide an oscillator and Schmitt trigger circuit. The inductor L comprises 150 turns 34 gauge (USA) enamelled wire within half of a Ferroxcube 1811-P LOO-3B7 pot core set, giving around 2mH. The oscillator, operating normally with its high-Q coil at a frequency around 100kHz, drive circuit which maintains transistor Tr_2 on, the input to inverter Tr_3, Tr_4 is low and hence the output high. When a metallic object is close to L, the Q of the coil drops, the oscillator output falls, causing the Schmitt circuit to go off and hence the output rises. Sensitivity is controllable via resistor R_1.

Reference

Fichtenbaum, M. L. *Electronics*, January 22, 1976, p. 112.





This voltage controlled amplifier is derived from a CD4007 package. IC_1 inverter is biased into its linear region by the 10MΩ resistor, and one of the n-type f.e.t. is used as a voltage variable resistor. Control voltage range is dependent on $|V_{DD} - V_{SS}|$. With above network gain is claimed variable from zero to just over unity.

Reference

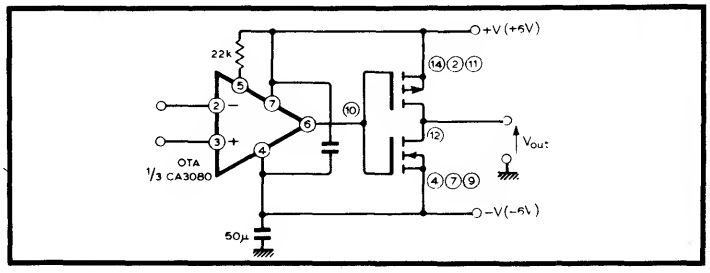
Electronics Today International, October 1976.

CA3600E: This is a m.o.s. transistor-array package configured like the CD4007, but characterized for linear operation.

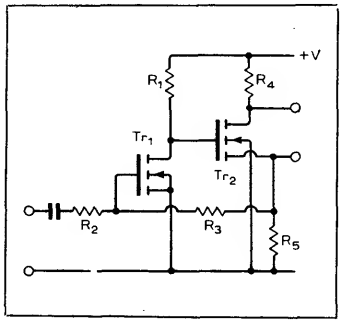
A typical application is a post-amplifier for op-amps, where the high input impedance of an inverter-pair means that the op-amp is buffered from finite loads. This is shown for a CA3080 transconductance amplifier, where the overall gain is 130dB (30dB for the transistor-pair). Each transistor-pair can sink or source 10mA, but for greater current output, the two remaining pairs can be connected in parallel with the output stage.

Reference

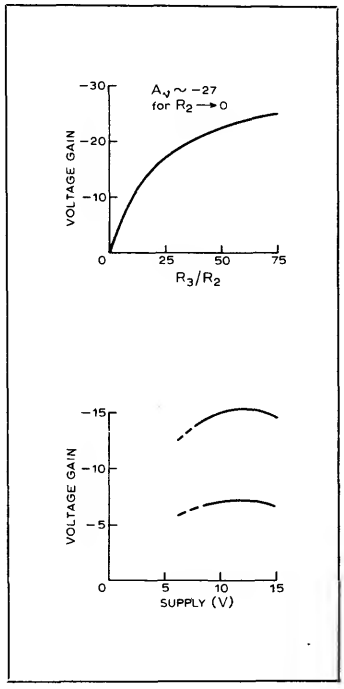
RCA Integrated Circuit Data Book, 1976.



D.C. feedback pair



Typical performance
IC CD4007AE
2 n-channel devices
Supply +10V
R_1 1.2MΩ
R_2 470kΩ
R_3 5.6MΩ
R_4 10kΩ
R_5 4.7kΩ
C 100nF
Voltage gain output 1 −10.7
output 2 −21.8



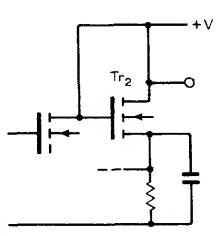
Circuit description
This classic form of circuit has proved so flexible in bipolar designs that it is worthwhile to consider its behaviour in m.o.s. form. It can be constructed using either n-channel or p-channel devices, and complementary forms are also possible. If R_1 is large, the current in Tr_1 is low and it will require a V_{GS} little more than its threshold voltage i.e. around 2V. Input current is negligible and hence the p.d. across R_3 is zero. This defines the p.d. across R_5 and the corresponding current in Tr_2 and R_4. This in turn fixes the V_{GS} of Tr_2 and the drain potential of Tr_1 ($V_{GS1}+V_{GS2}$). Provided the supply voltage is much greater than this value the current in R_1 is well-defined. For a.c. signals the gate of Tr_1 is an imperfect virtual earth—the open-loop voltage gain is around −20 to −40 and so closed-loop gains of −5 to −10 can be defined with moderate accuracy. The input impedance is then $\sim R_2$ and as R_3 and R_2 can be very large, loading of any preceding stage is small. Outputs from source and drain of Tr_2 are anti-phase and can be equal in magnitude or in any desired ratio, since the currents in R_4, R_5 are almost identical (differing only due to the small current in R_3). The frequency response is controlled by shunt capacitance across R_1 (internal plus strays).

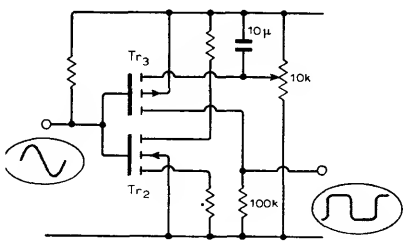
Component changes
IC: Access needed to individual devices—hence CD4007, CD3600 or equivalents.
Supply: +5V to +15V. Gain and output swing fall sharply below 7.5V.
R_4, R_5: 1k to 100kΩ. Compromise between output capability and quiescent current.
R_2, R_3: Ratio sets gain, R_2 defines input impedance. Typically 100k to 10MΩ.
R_1: sets current in Tr_1. If R_1 is too high voltage gain increases but at expense of bandwidth. 10k to 1MΩ.

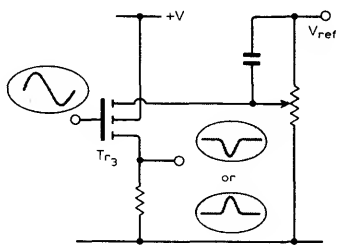
Circuit modifications
- To increase the voltage gain, the source of Tr_2 may be decoupled to ground, removing the a.c. negative feedback. Stray coupling between output and input can cause instability because of the high input impedance. Frequency dependent networks may be used in parallel with or replace resistors in the system to produce a controlled frequency response provided d.c. feedback path remains.
- If the complementary transistor to Tr_2 has its source taken to a decoupled potential divider across the supply, then its output current changes sharply at a particular level of the a.c. signal. Biasing it as shown can produce an approximate square wave without disturbing the normal operation of the amplifier or requiring an extra stage. Because the gate voltage of Tr_2 is defined in potential with respect to the ground line, the squaring action can be made almost independent of supply by deriving the voltage from (or replacing it by a separate stabilized reference voltage). Care is needed to minimize overall feedback when switching stages are operated close to a.c. amplifiers. If the reference voltage is raised or lowered the output transitions occur near to the negative or positive peaks of the input giving pulsed outputs as shown.

Cross references
Set 27, cards 3, 4, 5, 6
Set 20, card 10
Set 12, cards 7, 9

Circuit modifications







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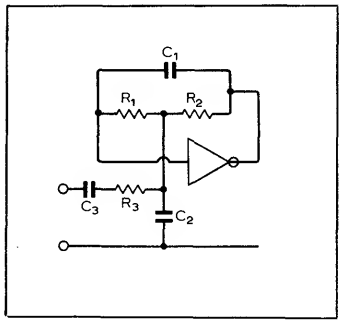
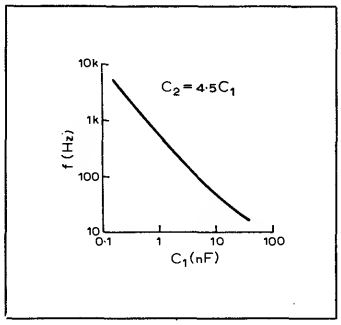
Set 28: C.M.O.S.-II—2

Low-pass/high-pass filters



Typical performance
IC $\frac{1}{4}\times$CD4001AE
Quad NOR gates
Supply +10V
C_1 1nF
C_2 4.7nF
C_3 100nF
R_1, R_2, R_3 100kΩ
Cut off frequency $\approx$750Hz
$Q\approx 0.7$
i.e. Butterworth response low-pass filter.



Theoretical relationships
$f_0=1/2\pi\sqrt{C_1C_2R^2}$
where $R_1=R_2=R_3=R$ and f_0 is the cut-off frequency of the resulting low-pass characteristic. Damping factor ζ is related to Q by $Q=1/2\zeta$ and Q is controlled by the ratio of C_2 to C_1. Accurate control is not possible because of low amplifier gain but $C_2=C_1\times 9Q^2$ i.e. for $Q\sim 1/\sqrt{2}$, $C_2\sim 4.5C_1$.

Circuit description
Low-pass filters normally have a flat response up to a given frequency, a rapid fall-off at much higher frequencies, and very little if any increase in amplitude during the transition from the pass-band to the stop-band. This corresponds to damping-factors of the order of unity and Q-factors which are normally equal to or less than one ($Q=1/\sqrt{2}$ is the condition for one standard filter the Butterworth type). Such a characteristic places no great demands on the amplifier used to implement it unless the accuracy required is high as in multi-order filters. For routine attenuation of hum, noise, and other unwanted signals a voltage gain of -20 to -100 is more than adequate, and c.m.o.s. inverters can be used. In the circuit shown, C_3 is a large value coupling capacitor that allows the d.c. feedback via R_1, R_2 to provide self-bias for the inverter. It rolls off the response at low frequencies but can easily be set to a value that does not affect the normal pass-band. By keeping the resistors constant, the cut-off frequency is inverse to the product C_1C_2, while the Q is controlled by the ratio C_2/C_1. The very high impedance of the c.m.o.s. input makes it possible to use very large values for R_1, R_2 and hence drop the cut-off frequency below, say, 50Hz while using small capacitors. The output has a d.c. content that would make a coupling capacitor necessary in most cases.

Component changes
C_1: 47p to 10μF
C_2: Typically 4 to 5$\times C_1$ or can be varied to change the Q.
R_1, R_2, R_3: 10k to 10MΩ.
C_3: Must be large enough to avoid attenuating lowest frequency signal. 100n to 10μF.
IC: Any c.m.o.s. inverter, gate.
Supply: +5V to +15V

Circuit modifications
- By transposing all the capacitors into resistors and vice versa, the circuit is converted into a high-pass filter. The input capacitor C_3 automatically blocks d.c. and this reduced the component count by one. If a high Q is required, then the ratio R_1/R_2 has to be increased. For $C_1=C_2=C_3=C$, the cut-off frequency is $f=1/2\pi\sqrt{R_1R_2C^2}=1/2\pi C\sqrt{R_1R_2}$ The value of Q is given by $R_1/R_2=4Q^2$ for an amplifier with infinite gain. In practice it would be difficult to obtain a Q of more than 5 while the usual range of Q-values needed in high-pass filters (say 0.5 to 1) is achieved with reasonable accuracy. Higher order filters can be constructed by cascading individual second-order filters. The presence of C_3 at the input simplifies the coupling because each inverter is then self-biasing. It is unlikely that high-order filters would be sufficiently accurate and independent of supply etc to be worth designing by this technique.

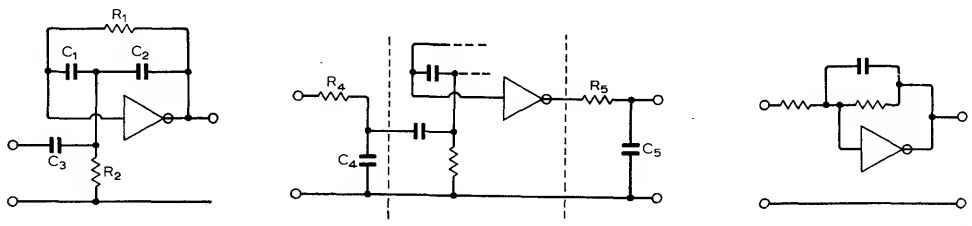
- If precise control of the form of filter characteristics is not needed (i.e. Butterworth, Bessel etc) the order of the filter can be increased by adding separate RC sections at input and/or output.

- Any separate inverter in a system may have a lag introduced into its response by the addition of a capacitor or a series CR network across the feedback resistor. The noise characteristics of c.m.o.s. gates are poor compared with those of low-noise bipolar or f.e.t. discrete circuits, but acceptable results are obtainable for signals well above the millivolt level.

Further reading
Sedra, A. S., Generation and classification of single amplifier filters, *Circuit Theory and Applications*, vol. 2, 1974, pp. 51-67.

Cross references
Set 1, cards 4, 5
Set 16, card 9

Circuit modifications



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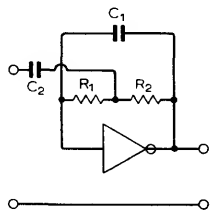
Set 28: C.M.O.S.-II—3

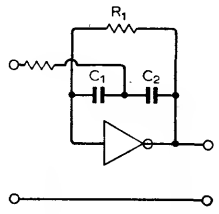
Band-pass/notch filters

Band pass 1



Typical performance
IC ¼×CD4001
(quad NOR gates)
Supply +10V
C_1 100pF
C_2 10nF
R_1 R_2, 100kΩ
f_0 1490Hz
Q 2.5
(For an ideal inverter, $C_2/C_1=4Q^2$ but with the very limited gain the theoretical Q of 5 is reduced to 2.5, see Ref. 1.)

Band pass 2



Typical performance
IC ¼×CD4001
(quad NOR gates)
Supply +10V
R_1 220kΩ
R_2 2.2kΩ
C_1 15nF
C_2 15nF
f_0 460Hz
Q 2.1
$f=1/2\pi\sqrt{R_1R_2C_1C_2}$
& $4Q^2=R_1/R_2$.
In practice $Q>5$ difficult to achieve.

Circuit description
Band-pass filters commonly require differential input amplifiers or multiple amplifiers. This remains true if high Q is needed, particularly if sensitivity to gain and passive component changes is to be minimized. Where a low value of Q is sufficient then simple band-pass filters can be based on single inverting amplifiers. At very low frequencies, the impedance of $C_2\rightarrow\infty$ and the gain $\rightarrow 0$. At very high frequencies the impedance of $C_1\rightarrow 0$ and the gain$\rightarrow$0. At some intermediate frequency, the gain has a maximum value. The theoretical centre-frequency is $1/2\pi\sqrt{R_1R_2C_1C_2}$ and commonly, $R_1=R_2=R$ giving $f=1/2\pi R\sqrt{C_1C_2}$. Considerable departures from the predicted Q-values occur because of the low gain of the amplifier. The centre frequency lay within the tolerance range of the passive components in the samples tested. At the centre frequency, the output is anti-phase to the input. This leads to a simple means of obtaining a notch-characteristic as indicated over. The high values of resistors that can be used make it easy to obtain a very low-frequency band-pass characteristic, while on the high-frequency side operation to beyond 100kHz is possible.

Alternative circuit
The second form of the band-pass filter has comparable performance, and no significant differences were observed. The input impedance will presumably differ from the first circuit, but both impedances can be made high enough for differences to be unimportant.

Component changes
IC: Any c.m.o.s. inverter, buffer, gate.
Supply: +5 to +15V. At low voltages the available voltage gain is too far reduced by loading effects.
R_1, R_2: 10k to 10MΩ. Lower values possible if source impedance is low.

Circuit modifications
The third band-pass filter is based on that of Sallen & Key and the equations given in Ref. 1 are =(4.41 Q^2-1).

$$T_v=\frac{sb\omega_0/2\cdot 2Q}{s^2+s\omega_0/Q+\omega_0^2}$$

where $s=j\omega$

Notch filters are often based on band pass networks, in which a bridge or other balancing system is arranged such that the output tends to zero at the centre-frequency of the band pass. In this case, taking the first circuit overleaf, the input and inverted output are applied to the ends of a potentiometer. As the potentiometer setting is varied, a point is reached where the two signals exactly cancel at the original centre frequency. The principle can be extended to obtain a low impedance output by applying the signals via two resistors to the summing junction of a second inverter as shown. The overall transfer function is then of the form

$$T_v=\frac{H_2s}{s^2+s(\omega_0/Q)+\omega_0^2}-H_1$$

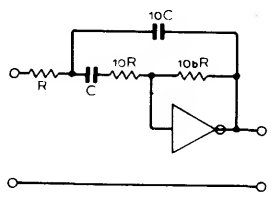
allowing for the inversion due to the second amplifier. ($H_1\propto 1/R_4$, $H_2\propto 1/R_5$)

$$T_v=\frac{H_2s-H_1[s^2+s(\omega_0/Q)+\omega_0^2]}{s^2+s(\omega_0/Q)+\omega_0^2}$$

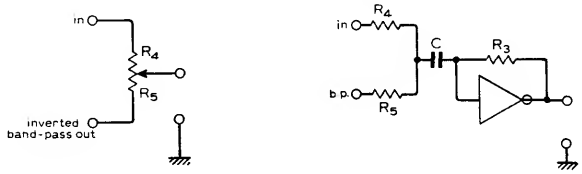
$$=-H_1\left[\frac{s^2+s\left(\frac{\omega_0}{Q}-\frac{H_2}{H_1}\right)+\omega_0^2}{s^2+s(\omega_0/Q)+\omega_0^2}\right]$$

For a notch characteristic, there must be a frequency at which the output goes to zero. This is achieved for $H_2/H_1=\omega_0/Q$ at $s^2+\omega_0^2=0$ i.e. at the same frequency as the peak of the original bandpass function.
For C_2 47nF, C_1 100pF the notch was obtained at $R_5/R_4\sim 33$.
An all pass filter (constant amplitude varying phase shift) follows when the coefficients of in numerator and denominator are equal and opposite. This implies $2\omega_0/Q=H_2/H_1$ and corresponds to $R_5/R_4\sim 16$.

Band pass 3



Notch/All pass filters



Further reading
Sedra, A. S. Generation and classification of single amplifier filters, *Circuit Theory and Applications*, vol. 2, 1974, pp. 51-67.

Cross references
Set 1, card 8
Set 16, cards 7, 8

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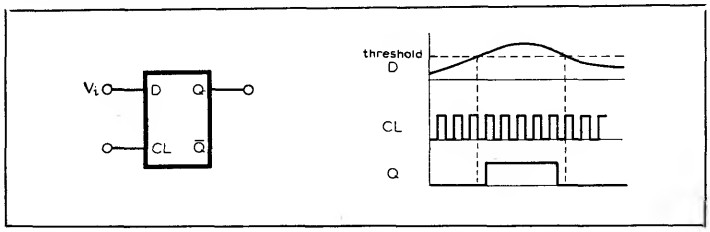
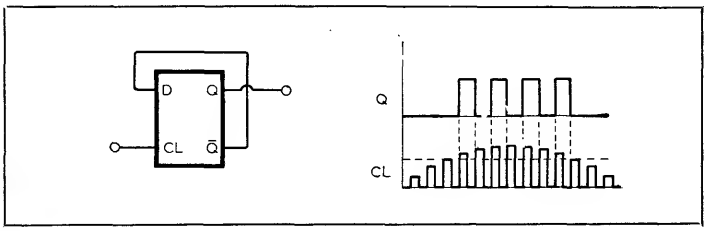
Set 28: C.M.O.S.-II—4

D-type analogue circuits-1





D.C. level sensing
The D-type flip-flop has a data input which responds to a 0 or 1 input by transferring these to the Q output when the device is clocked. The threshold between these two regions varies from device to device, but varies little with temperature. For moderate variations in supply voltage it is also a fixed fraction of that voltage and the transition between regions is sharp. If a varying d.c. voltage is applied to the data input, and the flip-flop is continually clocked, then each time the voltage passes through this threshold region, the output changes state on the next clock-pulse. The threshold remained between 44.7% and 45.0% of the supply voltage for V_s 4 to 7V and the effect of temperature was of the order 1mV K^{-1}. If the unknown voltage is derived from a common supply rail regulation would not be required since both it and the device threshold would vary together. The output is 1 for $V_D > V_T$ and 0 for $V_D < V_T$.

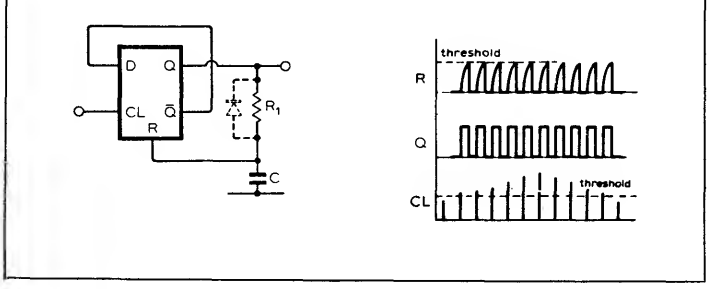
Pulse height detector
The flip-flop is set up as a $\div 2$ circuit by returning the data input to the $\overline{Q}$ output. For each normal clock pulse the Q output is thus set to the previous state held on the $\bar{Q}$ output i.e. the state of Q (and hence of $\bar{Q}$) is reversed. If the clock pulses fall below the threshold value of the C_L input they are ignored and the output retains its previous state. This threshold level is controlled by gates similar to those at the D input and hence the threshold level is of the same order —45/55% of the supply, but with the same well-defined characteristics for any given device. The output is a square wave of half the input frequency for $V_{CL} > V_T$ and either 0 or 1 for $V_{CL} < V_T$. A small amount of inherent hysteresis appears to exist in such applications as these. The input amplitude has to reverse itself by up to about 1% after effecting a change in the output in order to reverse that change.

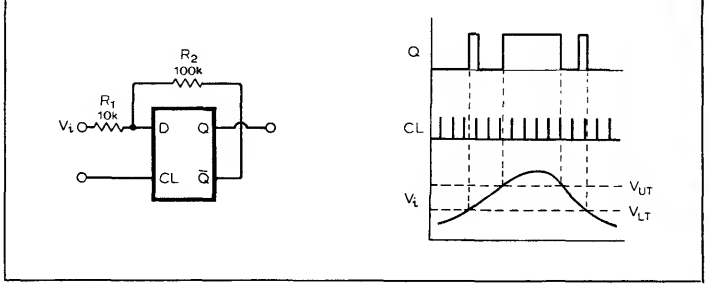
Pulse-height-sensing monostable
The Q output is returned by a short time-constant circuit composed of R_1C_1 to the re-set input. If the input pulse rate becomes too rapid, an additional diode across R_1 shortens the recovery time of the monostable and allows the output pulse-width to remain independent of pulse-rate. Provided the input pulses, applied to the clock input exceed the threshold then the circuit attempts to toggle. The rest state of the system must be $Q=0$, since for $Q=1$ the reset input would be activated after a short charging period and Q would return to 0. Every time a clock-pulse sets Q to 1, this is what happens, and Q remains on for the time it takes the reset input to reach its threshold value via the charging of C_1 through R_1.

There is one output pulse of defined height and width for every input pulse exceeding the threshold voltage. If a further clock pulse is received during the on-period, the output pulse is terminated. If this is not desired, the D input can be returned directly to logic 1 when such pulses are ignored.

Window comparator
Assume the input voltage is low and that $R_2 \gg R_1$. The D input is below its threshold, and on the next clock pulse, Q is driven to (or held at) 0, and $\bar{Q}$ to 1. This change is insufficient to shift the D input above its threshold and Q stays permanently at 0. Conversely if V_i is high, Q is held permanently at 1. When V_i is close to the threshold, each transition of $\bar{Q}$ shifts the D input across the threshold and the circuit toggles. There are now two effective threshold points V_{LT} and V_{UT}, the lower and upper thresholds, separated by $V_S R_1/(R_1+R_2)$.
For $V_i < V_{LT}$ Q is 0.
For $V_i > V_{UT}$ Q is 1, and for $V_{UT} > V_i > V_{LT}$, Q toggles at $f/2$. For a steady clock rate (f constant) the output mark-space ratio is unity.

A moving-coil indicator at the Q output would read zero, $V_s/2$ and V_s respectively for V_i below between and above the thresholds. Alternatively a l.e.d. would be off, flashing at $f/2$ or permanently on for these three ranges of input volts (this would require a slow-speed clock if the flash rate is to be visible).





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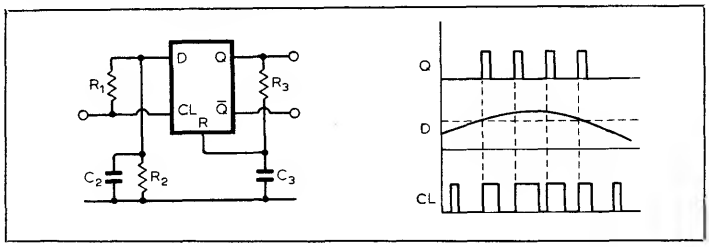
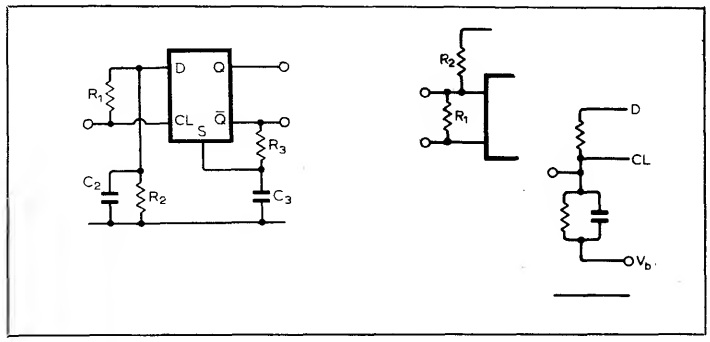
Set 28: C.M.O.S.-II—5

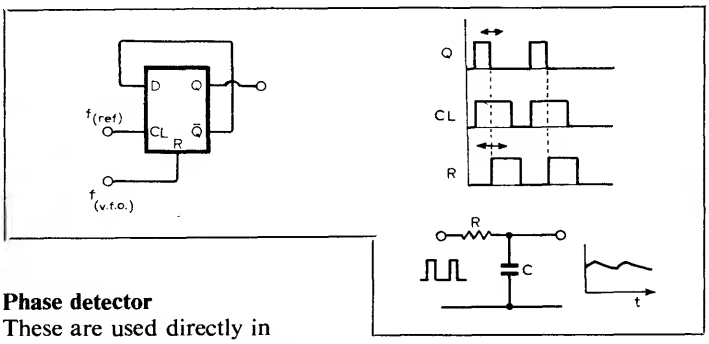
D-type analogue circuits-2



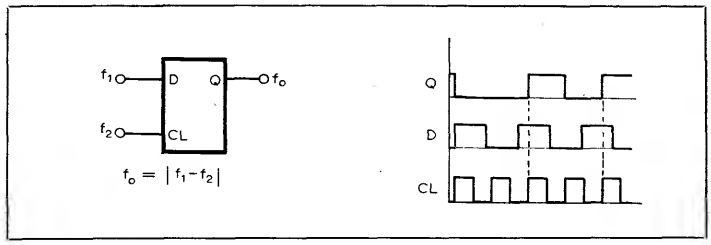
Marks-pace detector
If the input pulse-train has a large mark-space ratio, its mean value may be > 50% of V_S, provided the input pulse height is equal to V_S. If the voltage at D is smoothed by C_2 across the potential-divider formed by R_1, R_2, the threshold will be exceeded and an output pulse-train is obtained. When the mark-space ratio falls below the critical level, the monostable relaxes into its quiescent state with $Q=0$. The circuit basically detects the mean level of the input pulse train and can be used to detect any of the separate variables that affect the area provided that all the others remain constant. Thus for height and frequency constant the circuit detects pulse-width, for height and pulse-width constant it detects a rise in frequency and so on. The pulse-height is well-defined if the previous stage is a c.m.o.s. gate/inverter.



Space-mark detector
The complementary nature of the circuit allows the reversal of the outputs, letting $\bar{Q}$ activate the set input. In each of these circuits the monostable period has to be less than the period of the incoming pulses. As shown, the output at $\bar{Q}$ remains low until the mean value on the D input falls below its threshold, when the $\bar{Q}$ output becomes a pulse train. To adjust the range of mark-space ratios that can be dealt with, a bias current can be provided from the supply or the CR network can be returned to a variable bias voltage. This would need to be supply proportional is using an unregulated supply for all other functions.



Phase detector
These are used directly in determining the phase difference between two signals of the same frequency. The signals are converted into pulses/square waves and the zero-crossings activate a switching circuit such that an output is on only for the interval between the zero-crossings of the two signals. If the output is filtered by an RC circuit the resulting direct voltage is a measure of the phase difference. Assume that the D-type flip-flop is clocked at an instant when $Q=0$. This causes Q to go to 1, a state it retains until the reset goes to 1. The following clock pulse again drives Q to 1 with the period that Q remains at 1 varying as the positive going input at R varies in the delay with respect to the C_L input i.e. according to their phase-difference. The unit is one example of phase-detectors used in phase-locked loops. As the variable frequency oscillator drifts it causes a progressive change in the phase difference between it and the reference oscillator. The resulting change in the mean output is used to control the v.f.o. returning it into synchronism with the reference oscillator.



Frequency differencer
Two signals at different frequencies are fed into the D and C_L inputs of a D-type flip-flop. At each clock instant the D input may have either 0 or 1 and hence the output state may or may not change depending on its previous state. When the frequencies are very close it takes a large number of cycles, before a clocking instant coincides with a different value on the D input, i.e. the output rarely changes. When the frequencies are identical the D input always has the same value at the clocking instant and the output never changes. These results are consistent with the claim that the output pulse train has a frequency equal to the difference in the input frequencies. This can be very convenient in measuring small changes in a high frequency signal. It is compared by such a flip-flop with a stable frequency close to its value, and the result can be monitored on simple counters, or analogue frequency meters, on audio frequency amplifiers or displayed on an oscilloscope.

Cross references
Set 28, card 4
Set 19, card 8
Set 21, card 7

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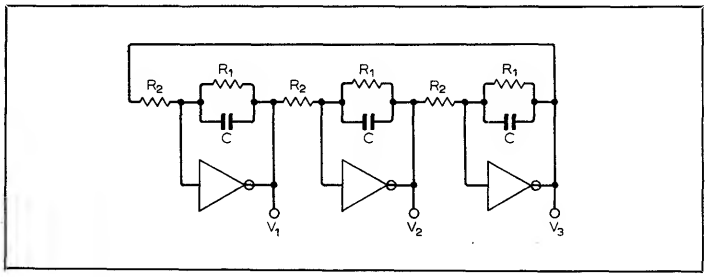
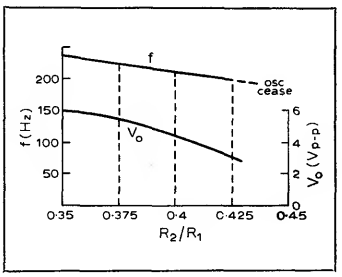
Set 28: C.M.O.S.-II—6

Three-phase oscillator



Typical performance
IC $\frac{3}{4}\times$CD4001AE
quad 2-input NOR gates
Supply +10V
R_1 100kΩ
R_2 40kΩ
C 15nF
f 213Hz
Amplitudes 3.6, 3.4, 3.5V pk-pk
Distortion 2.2%, 0.4%, 1.1%



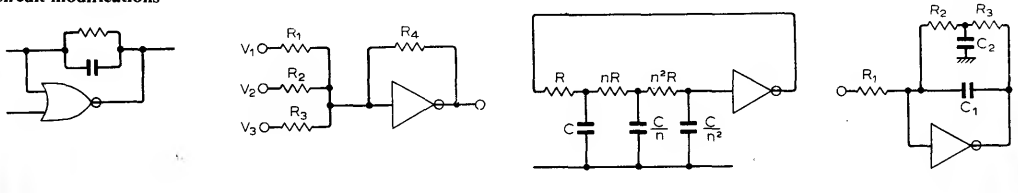
Circuit description
Each inverter has a high input impedance and an inverting voltage gain of magnitude $\gg 1$. The CR network in the feedback path introduces a lagging response. If the system is to oscillate, the loop phase shift must be zero while the overall gain should just exceed unity. If the system is to be symmetrical then each stage must contribute the same phase shift and must separately have unity gain. If the inverter gain is large then with the three inversions, the sum of three equal phase shifts must equal 180° to meet the overall phase condition. This requires a 60° lag from each of the sections. To maintain the magnitude condition at unity, the magnitude of the impedance of R_1 in parallel with C must equal the resistance of R_2. This gives $R_2 = R_1/2$ as the maintaining condition with $f = \sqrt{3}/2\pi CR_1$.
In the practical case the amplifiers have gains ranging from 10 to 50, inverting and with little phase-shift in the audio band. The inherent matching of these inverters because they are formed on a common chip means that provided the resistors R_2 are reduced by the same amount to accommodate this finite gain, then the phase relationships between the outputs are maintained. Non-linearity of the gain provides a coarse form of amplitude limiting. Two effects stem from any change in supply voltage, each controlling the voltage gain of an inverter. The trans-conductance of each device increases as the current increases, while its output slope resistance falls. The voltage gain into open-circuit is higher at low supply voltages making it easier to define the required ratio of resistances; the increased output impedance makes it necessary to use higher value resistors to prevent loss of voltage gain under these circumstances. The output voltage and frequency are also supply dependent but oscillations can be sustained over the range 5V-12V with a broad peak in the output in the 7 to 10V region with the samples used. The phase differences are held to 120° with a deviation of only one or two degrees except where distortion is severe. With R_2 increased to 42.5kΩ, the point at which oscillations are just sustained, one output had a t.h.d. of 0.18%.

Component changes
IC: Any set of three matched inverters: CD4007, $\frac{1}{2}\times$CD4049, $\frac{3}{4}\times$CD4001 with unused inputs taken to '0', $\frac{3}{4}\times$CD4011 with unused inputs taken to '1'.
Supply: In theory any supply voltage within device rating. In practice, at high voltages the open-circuit voltage gain falls; at low voltages the output impedance becomes too high. Best range 5 to 10V.
R_1: Circuit requires relatively high resistance values to reduce loading on output—typically 10k to 10MΩ.
R_2: $R_1/2$
C: can be relatively small even for low frequencies since R large—100p to 1μF.

Circuit modifications
- If the inverters are replaced by logic gates using one input for feedback, then the other input can be used to gate the oscillator. Using NOR gates, a logic '0' leaves the oscillator running, logic '1' drives the output of that gate low i.e. to logic '0'. This via the inverting action of the following stages drives their outputs to '1' and '0' respectively. If all free inputs are taken to '1' all outputs are driven to 0. The converse is true when using NAND gates.
- Most see-saw amplifier circuits can be implemented though at reduced performance because of the low open-loop gain. The outputs of the three-phase oscillator can be summed in any desired proportion by scaling R_1, R_2, R_3, R_4 to give an output at any other phase angle. Note that all outputs are at the same d.c. potential, which will vary from device to device but will be about 50% of the supply.
- A single-stage phase-shift oscillator requires a gain of -8 if the components are graded as shown and n is large. Restricting n to 10, and operating the inverter in the range 6 to 10V comfortably exceeds the condition for sustained oscillation, allowing non-linearity to limit the amplitude. Other combinations of networks and inverting stages can be used (see Set 26).
- An approximately 90° phase-shift can be introduced by passing the signal through the circuit shown. Provided $R_2, R_3 \gg R_1$ and $R_3C_2 \gg R_1C_1$, the circuit approximates to an integrator. If all the inverters are well matched, R_2, R_3, C_2 can be omitted.

Cross references
Set 26, cards 3, 4
Set 21, card 5

Circuit modifications



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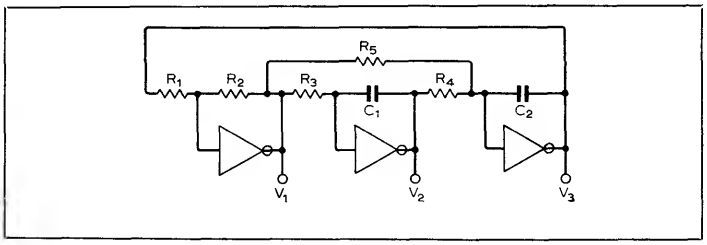
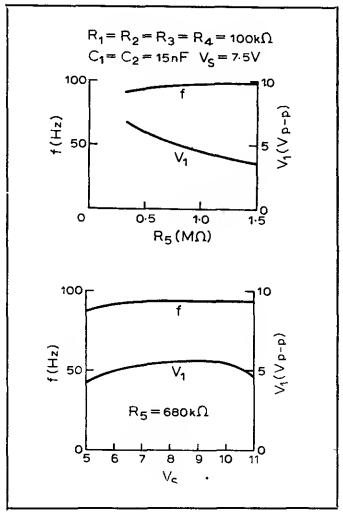
Set 28: C.M.O.S.-II—7

Two-integrator oscillator



Typical performance
IC ¾ × CD4001AE
NOR gates
Supply +7.5V
R_1, R_2, R_3, R_4 100kΩ
C_1, C_2 15nF
R_5 1.5MΩ
Amplitudes
V_1 3.5V pk-pk 1.1% t.h.d.
V_2 3.6V pk-pk 0.6% t.h.d.
V_3 3.9V pk-pk 0.75% t.h.d.



Circuit description
Assume initially that the inverters have a high voltage gain and that the network impedances are high enough to avoid significant loading of the inverter outputs. The system is then a two-integrator oscillator (as described in Set 26). The integrators produce a total phase shift of −180° which combined with three inversions gives an overall phase shift of zero. The finite gains and output impedances of the inverters reduce the effective Q of the system, and a separate positive feedback path is introduced via R_5 to initiate oscillation. Amplitude control is via the non-linearity of the inverters—as R_5 is reduced in value, the amplitude increases until distortion reduces the average loop gain over the cycle to accommodate the increased feedback. An alternative method of controlling the oscillation is to increase the ratio of R_2: R_1 while maintaining R_5 constant (or omitted in some cases). The three outputs are of different phase and somewhat different amplitude. The phase differences are of the order of ±90° with V_1 lagging and V_3 leading on V_2 (strictly these voltages lead and lag but with an additional inversion in each case). The resistor values may be large without the inverter inputs loading the network; the values should be large to minimize loading on the amplifier outputs. N.B. The low distortion obtained above is because only a small amount of positive feedback was used i.e. the output was not driven into its very non-linear region. For guaranteed oscillation more distortion would have to be accepted.

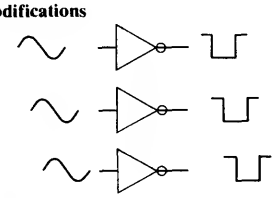
Component changes
IC: Any c.m.o.s. device containing at least three inverters, NAND or NOR gates.
Supply: Will not oscillate satisfactorily at either very high or very low voltages unless excessive feedback used. 5 to 10V is suitable range for most i.cs.
R_1 to R_4: Normally equal; variation of any one changes f with relationship $f \propto 1/\sqrt{R}$. For continuous variation in frequency with less change in amplitude, replace R_3 and R_4 by a twin-gang pot. Range of values for R_1 to R_4 typically 10k to 10MΩ. With high values it is more difficult to provide controlled positive feedback.
$R_5 \gg R_1$ etc typically $R_5/R_4 \approx 5$ to 20.
C_1, C_2: 1n to 10μF.
(To obtain very low frequencies use large capacitors but not polarized units. The leakage currents may restrict the Q and inhibit oscillation.)

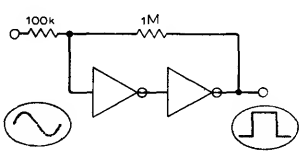
Circuit modifications
● Spare gates/inverters can be used to provide anti-phase outputs. If used with a pair of resistors as in the first amplifier overleaf an inverted sine wave output can be obtained from any of the three outputs. If the outputs are fed directly to the gates of three inverters, then three square-waves are obtained with 120° phase differences. The rise and fall times are not very fast and Schmitt triggers using two inverters with overall positive feedback give a sharp switching action. All of these outputs are compatible with normal c.m.o.s. logic circuits operated from the same supplies.

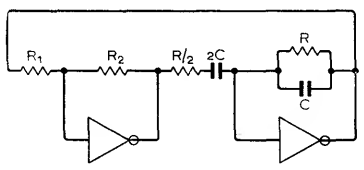
● Most other RC oscillators based on inverting amplifiers, op-amp see-saw circuits etc can be constructed using c.m.o.s. gates/inverters. Because the gain is already low any further losses at high frequency worsens the performance, increasing the distortion to unacceptable levels. Nonetheless oscillation to beyond the audio band is possible. As an example consider the Baxandall version of the Wien-bridge oscillator. As with the previous circuit, using more than one amplifier helps to offset the limited gain of each stage. The RC values are scaled so that the outputs are antiphase and approximately equal in value. The maximum gain of the frequency-dependent stage is a little less than unity. Hence $R_2 > R_1$ is needed.

Further reading
Good, E. F. Two-phase low-frequency oscillator, *Electronic Engineering*, vol. 29, 1957, pp. 164-9 and 210-3.

Circuit modifications







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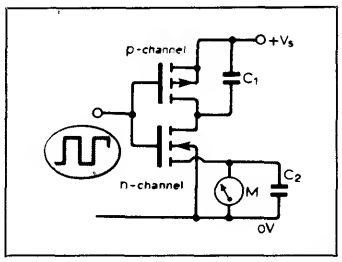
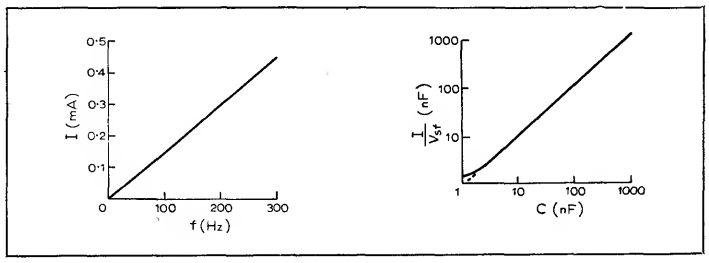
Set 28: C.M.O.S.-II—8

Frequency-voltage converter

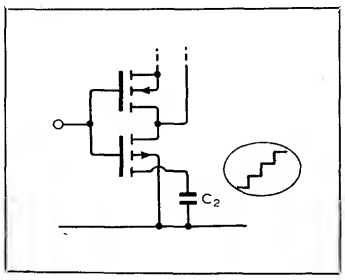


Typical performance
IC $\frac{1}{3} \times$ CD4007AE
Supply +10V
C_1 0.1μF
Meter 500μA, 200Ω
Input Logic level pulse train
0 to 300Hz
C_2 100μF
I fC_1V_s

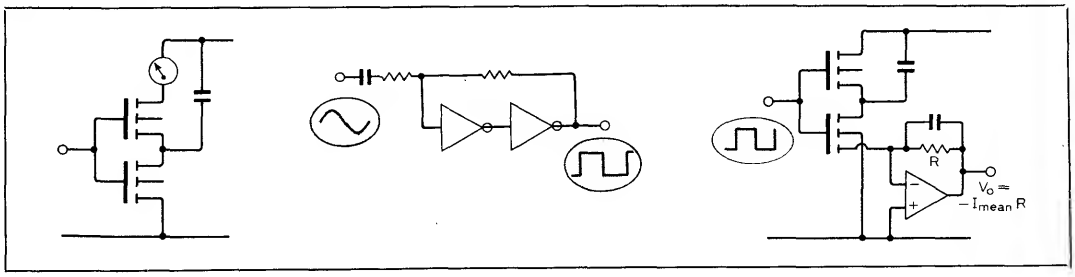


Circuit description
The circuit is simple in concept and exploits the characteristics of c.m.o.s. very well. The two devices are switched alternately in and out of conduction. When the p-channel device conducts it completely discharges the capacitor provided that it is left in conduction for a long enough period. When the n-channel device conducts, it charges the capacitor fully to the supply voltage. The current flows through the meter with the shunt capacitor limiting transient effects due to meter inductance. The total charge flow per pulse is C_1V and if this occurs at a frequency f, the charge per second is fC_1V. This is by definition the mean current flow, the parameter to which the moving-coil meter responds. A small non-linearity occurs when the meter p.d. increases, since this reduces the p.d. to which the capacitor charges on the following pulses. The effect at these levels is to reduce the full scale value by less than 1%. In addition to the external physical capacitance, various strays internal and external to the circuit add to the meter reading. For a 15V supply and a meter full-scale sensitivity of 1.5mA, the meter reading was 9% high at 100kHz with a 1nF capacitor. Removal of that capacitor confirmed the presence of strays by leaving a meter reading of just over 9% of full-scale at the same frequency. The full-scale frequency range is then inverse to the value of capacitance used. This is verified up to 1μF, where the full-scale reading corresponds to 100Hz. Using a 10V supply, a 1mA movement gives the same overall sensitivity.

Component changes
IC: Any pair of complementary enhancement mode m.o.s.f.e.ts. Other manufacturers equivalents of this i.c. may vary in respect of minimim/maximum supply voltage, frequency range cost etc but the same principles apply.
Supply: 3 to 15V. At low voltages meter sensitivity needs to be increased to 100μA. At high voltages a limiting resistor in series with the capacitor minimizes the peak current.
C_1: 1n to 10μF. For low values, a smaller capacitance than indicated in simple theory will be needed to allow for strays. At very low frequencies additional smoothing of the output is needed to reduce meter fluctuations.
C_2: Used to suppress transients and/or reduce meter fluctuations at low frequencies. Not critical —may be omitted.
Meter: 50μA to 5mA depending on supply voltage and range required.



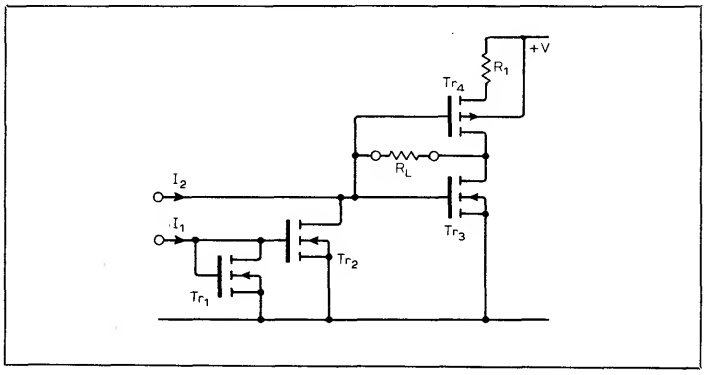
Circuit modifications



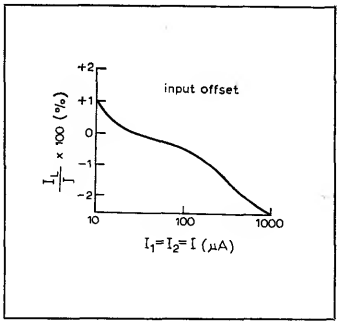
Circuit modifications
Omitting the meter and any other resistive load, produces a simple staircase generator. The output becomes non-linear as it becomes a significant fraction of the supply. A simple threshold detector using a D-type flip flop (see card 4) operated from a lower supply voltage, could be used to discharge the capacitor and restart the cycle after the end of the monostable period. The high impedances would allow a simple pulse-counting approach to be implemented at low frequencies since there would be negligible capacitor discharge. The locations of meter and capacitor can each be altered to either of the supply lines i.e. the meter can be used to measure the mean current of either charge of discharge cycles. The mark-space ratio of the input should not deviate too far from unity since the charge and discharge times of the capacitor should each be long enough for the action to be effectively completed before the changeover.
The i.c. contains two other complementary pairs that can be used as a Schmitt trigger for converting smaller sinusoidal or other inputs into a logic-level output. Alternatively if the input pulses are very narrow, they could be used as a monostable or triggered astable. If the frequency range becomes too great, this creates problems with the mark-space ratio.
The output can be converted, into a large linear voltage swing by feeding the current pulses into the virtual earth of an op-amp. Smoothing is eased by virtue of the high feedback resistor e.g. 100kΩ if a 10V output is required from an input averaging 100μA.

Further reading
Johnson, P. A. Complementary MOS Integrated Circuits, *Wireless World*, 1973, pp. 395-400.

Current-differencing amplifier



Typical performance
IC CD4007 (Tr_{1-4})
Supply +15V
R_1 100kΩ
R_L 1kΩ
I_1, I_2 100μA
I_L ±1μA
$I_L = I_1 - I_2$
Output resistance > 100MΩ
at $I_L = 10\mu A$
Max. $R_L \approx 0.5M\Omega$
at $I_L = 10\mu A$ for good linearity



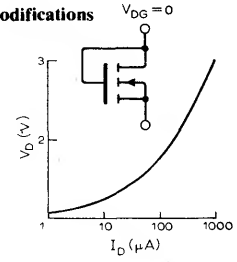
Circuit description
It is possible to duplicate bipolar circuits in m.o.s. form, but a flexible approach is needed if existing c.m.o.s. packages are to be adapted. As an example, consider the current-differencing amplifier (c.d.a., or Norton amplifier). In bipolar form this uses a current-mirror at the input such that the first transistor of the amplifier proper is fed with a current equal to the difference between the input currents. Substituting a pair of n-channel transistors the current-differencing action is still obtained but the p.d. is larger. Assuming the drain-source voltage on Tr_2 is above the pinch-off level, its drain current is comparable with I_1 (net current in R_L is then $I_1 - I_2$). If R_L becomes too large, the output stage saturates and a large voltage change at the gate of Tr_3 disturbs the relationship. The inverting amplifier, Tr_3 has a constant-current load provided by Tr_4 and R_1, since the small voltage swing at the commoned gates of $Tr_{3,4}$ produces a very small fractional change in the p.d. across R_1. Thus R_1 reduces the quiescent level of current and makes the system operate as a defined transconductance (Tr_3) operating into the feedback resistor R_L. This gives the very high output resistance indicated above. The current transfer-ratio of the current mirror remains close to unity over a wide range of currents—a total change in the imbalance of 3% over a 1000:1 range. The absolute accuracy cannot be expected to be better than one or two percent even under favourable circumstances, but the circuit is capable of resolving minute changes in current i.e. with I_2 as the unknown current, I_1 is adjusted until the output voltage is at some reference level. Any change in I_2 produces an output voltage swing $\Delta I_2 R_L$. Alternatively R_L may be a meter, reading the current difference directly.
The p.d. across Tr_1 is more strongly dependent on current than the V_{be} of a bipolar transistor, but at low currents the rate of change for a given fractional change in current is low enough to allow the assumption of a constant p.d. ($\Delta V \approx 80$mV for a 2:1 range of currents). Hence the current can either be derived from a true current source or from a voltage source and a high series resistance.

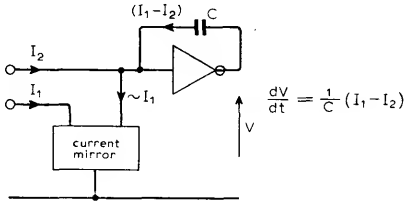
Component changes
IC: Requires access to individual devices
Supply: +10 to +15V
R_1: 10k to 220kΩ

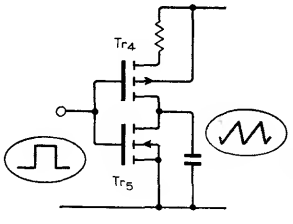
Circuit modifications
- The circuit can be used with any feedback element to define its overall transfer function. For example, with capacitive feedback an integrator results. If either or both of I_1, I_2 are switched in value then the magnitude or direction of the slope of the output waveform can be changed. This allows various triangular and ramp waveforms to be generated. When $I_1 = I_2$ the net current is zero and the output voltage holds its last value.
- Because the currents can be extremely small, long integrating periods can be controlled and it could be the basis of a simple long-period timer. Tr_3 can conduct heavily if overdriven so the output can be rapidly reset to a low value.
- The output stage alone can be gated by a logic level pulse, such that when the input is low Tr_4 conducts as a low-current source and produces a linear ramp (Tr_3 is off). When the input goes high Tr_4 is cut-off and Tr_3 rapidly discharges the capacitor to ground. A source-follower could be used to buffer the resulting triggered ramp.

Cross references
Sets 16, 17, 18

Circuit modifications







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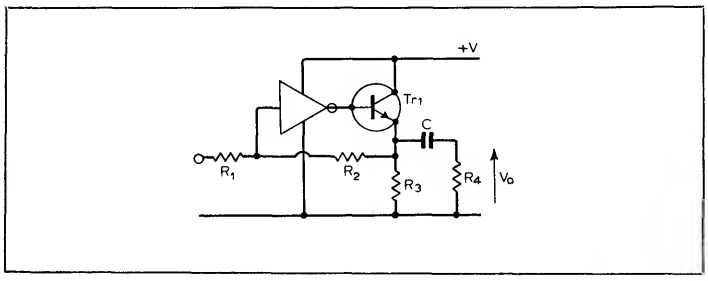
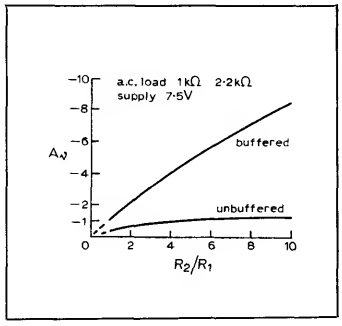
Transistor outputs



Typical performance
IC ¼ CD4001AE
(quad NOR gates)
Supply +5V
R_1, R_2 100kΩ
R_3 100Ω
R_4 100Ω
C 100μF
V_0 2V pk-pk without heavy distortion
Tr_1 BFR41
Supply current 20mA



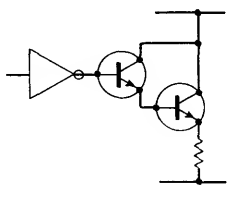
Circuit description
At low supply voltages the c.m.o.s. inverter carries a low current and has a high output resistance. Each of these facts restricts operation to high load resistances. By adding an emitter follower, the effective output impedance can be reduced and the output current increased, both by a factor of 100 or more with a suitable transistor. In the example shown, a peak current of up to 10mA was available for the load while the normal inverter quiescent current under these conditions would be ≪ 1mA. To demonstrate the effect the resistor ratio defining the gain was varied from 1:1 to 10:1 with the c.m.o.s. device driving a 1kΩ load (i) with d.c. coupling to the load i.e. unbuffered (ii) with a transistor having R_3=2.2kΩ, circuit diagram as above. In the unbuffered case, the maximum value of voltage gain obtained was almost independent of the feedback values. This showed that the 1kΩ load was an effective short circuit i.e. that the gain without feedback would have been restricted to −1.3. This corresponds to a g_m of 1.3mS, while the presence of the transistor would increase this to 130mS assuming a current gain of 100. This is enough to allow a practical gain of −8.3 for a resistive ratio of 10:1 even with the a.c. load being represented by R_3 in parallel with R_4.
Another advantage is that the c.m.o.s. output is buffered from the shunt-capacitance of the load plus strays, and the gain-bandwidth product is increased.

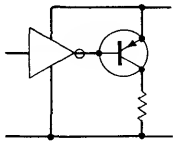
Component changes
IC: Any c.m.o.s. inverter, gate
Supply: +5 to +15V
Because of the current boosting of the output transistor, the c.m.o.s. stage can be operated at lower voltages than is usual for linear operation.
R_1, R_2: Not critical as R_2 no longer loads the output.
R_3, R_4: For class A operation, R_3 has to carry a quiescent current equal to or greater than the peak current required by R_4. This may be up to 100mA with a power transistor.
Tr_1: Current/power rating to suit load. Not critical.

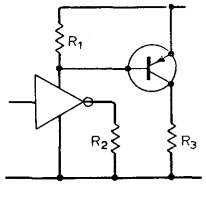
Circuit modifications
As usual, any compound pair of transistors may be added to increase gain-complementary versions if load is to be referred to positive supply rail.
An alternative configuration is to drive the base of a common emitter amplifier (a base limiting resistor may be added at higher voltages). The output is now in phase with the input and the combination is not suitable for the direct application of overall negative feedback. Shunt feedback over the inverter together with series feedback in the transistor (emitter resistor) would be another possibility with overall feedback from the emitter to the input—a form of d.c. feedback pair.
If the inverter supply current is monitored it can be used to switch an output stage; R_2 limits the peak current in the c.m.o.s. stage while R_1 holds the transistor off at lower inverter quiescent currents. In addition to the load current, the c.m.o.s. pair pass through a peak of current as the output swings through its linear region and this complicates the calculations.
Over a large part of the range, the n-channel device can be assumed to be non-conducting particularly when R_2 is low. This leads to the simplified form of circuit shown, where the circuit may be seen as a form of Darlington pair with a p.m.o.s. input stage. Overall negative feedback is possible as shown since the complete stage remains an inverter albeit with a higher output current.

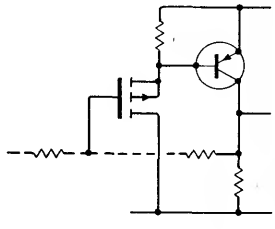
Cross reference
Set 27, card 5

Circuit modifications









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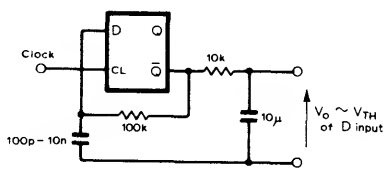
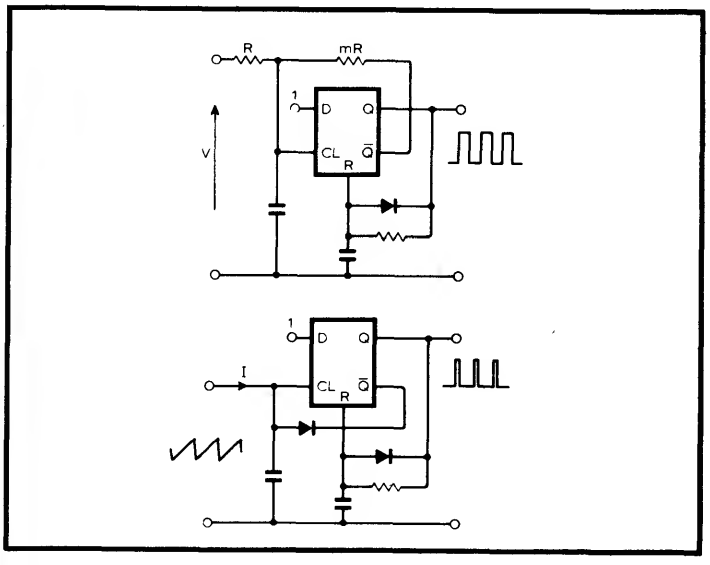
Set 28: Up-date

These notes offer some novel applications of D-type flip-flops within analogue systems. Where a number of c.m.o.s. devices are to be used for sensing, amplifying etc it can be very convenient to have a reference voltage close to the threshold values of these devices. Such a voltage automatically tracking with any supply or temperature changes by using one D-type flip flop as shown. When it is clocked the Q output switches either to 1 or 0 depending whether the D-input is above or below its sharply defined threshold. The inverted Q output attempts to return the D-input to the opposite state. By choosing the capacitor value in conjunction with the clock frequency, the ripple at the D-input is small and centred about its threshold. The almost-zero input current ensures that the *mean* voltage at Q equals that at D. If the output is smoothed a low-ripple direct voltage results with $V_O \sim V_{TH}$ of the D-input.

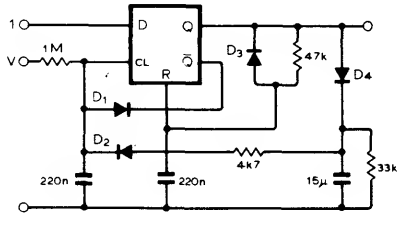




By using the other terminals that may be available such as the R and S inputs novel functions are possible. Monostable action has been noted in previous sets, and it can be combined with feedback to the D-input as above. For a low input voltage, then at switch on either Q or Q may go to 1. Assume the former: at some later instant R is driven high driving Q high until the CL input is raised above its threshold and Q goes high again. A pulse train is developed in which the mean value at Q is a function of V. If the monostable action ensures pulses of constant height and width then the pulses rate is a linear function of V. If the output is taken from Q then by adjusting the value of m about unity it is possible to obtain a pulse rate that tends to zero for V = O and to some full-scale value as V approaches V_s.

A ramp generator results if a current is fed to the capacitor at the clock input with a periodic discharge via the diode from Q. Resetting is again a function of the monostable that determines the output pulse width.

Several of these actions can be combined to provide complex functions using the bare minimum number of active devices. The circuit shown is a level-sensing, latching audible alarm. It is easiest to follow by assuming that at some point the input V has exceeded the CL threshold and that the alarm has been initiated. Diode D_4 acts as a half-wave rectifier charging the 15µF capacitor almost to supply level. This constant voltage attempts to raise CL input via D_2. Each time it does so, triggering the flip flop, Q goes high and Q low. The CL input is rapidly returned to zero via D_1 while the monostable action via the R input defined the output pulse width. After resetting D_1 is reverse-biased and the cycle restarts. The Q output is an audio-frequency pulse train whose frequency is only marginally affected by any further changes in V. Until V first exceeds the CL threshold, the circuit remains in a quiescent state with Q low Q high.



notes

Set 29 : Analogue multipliers

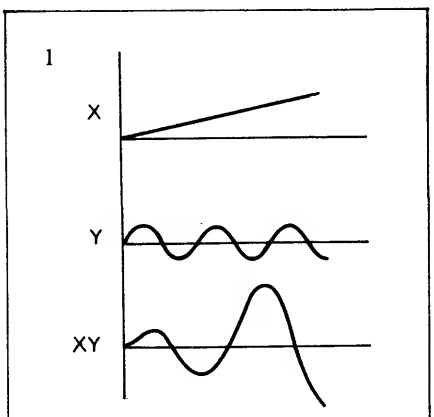
A most versatile i.c. appears in this set, incorporating four-quadrant multiplier, op-amp and buffer on the same chip, page 123, with an h.f. capability up to the order of MHz (higher in some applications). Squaring, suppressed carrier a.m., and demodulation of a.m. are uses of it shown on page 124 and page 000 (set 30) includes some further applications.
This is one of these subjects where it's difficult to avoid ending each card heading with the name of the circuit type! It is also a set containing an important class of circuit, card 8, that didn't quite do justice to its originator—Barrie Gilbert of Analog Devices. In the original card for the translinear multiplier R_8 was shown wired to the wrong end of R_6. And a missing minus sign, between I_A and I_B in circuit modifications and now corrected, made nonsense of the analysis.
The circuit of card 5 was originally incorrectly drawn too; inputs to R_{111} and R_{12} come from the series diode-resisfor junction in the precision rectifier circuits. (Omission of R_2 occurred on card 4 and, on the same card, the lower-case abbreviation i should have been shown as I to correspond with the diagrams.)

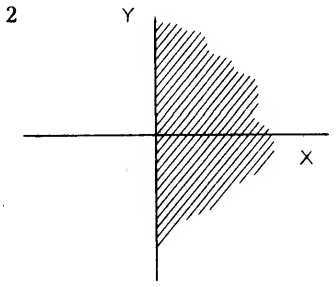
Introducing analogue multipliers

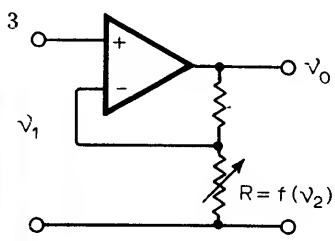
In the processing of electrical signals there is a need for circuits that can perform all the standard arithmetical processes – addition, subtraction, multiplication and division. The first two fall into the domain of linear amplifiers and present no great difficulty; the last-mentioned pair provide a real challenge to the ingenuity of circuit designers. Fig. 1 shows the waveforms of a particular example where an input signal Y is to be under the control of a second input X, the output being of the form XY. This is a gain-controlled amplifier and is one of the simpler forms of multiplier since usually the gain is required to be either positive or negative and not both. Hence X takes up only one polarity, and Fig. 2 shows the multiplier as needing to operate in only two of the four quadrants viz X positive, Y positive and X positive, Y negative. Such a system can be realized as in Fig. 3 where v_1 corresponds to Y and v_2 to X. In many such circuits it is not even essential that the gain be a linear function of v_2, in which case the circuit ceases to be a multiplier. A problem with circuits based on this idea is that of finding a resistor having negligible non-linearity over a suitable range of currents and voltages, while being controllable by an external signal.

While true and direct multiplication would be ideal, and can be obtained by using suitable transducers such as Hall-effect devices (see card 9), the designer often has to resort to devices and circuits obeying other laws. These are then manipulated until some combination of them yields a term which is proportional to the product of two signals.

It can be very difficult to eliminate all unwanted terms consistently and over a wide range of temperatures and supply voltages. One well-established technique is to use a circuit with a square-law voltage transfer function. This can be synthesized by a "piece-wise linear" technique, where a network of diodes, resistors and reference voltages, provides a slope that changes progressively as the input increases (see card 1). With a large enough number of segments, a power law can be approached to any desired degree of accuracy. For economy the number of segments has to be restricted particularly if both polarities of input have to be accommodated – twenty or so might be needed in such a case.



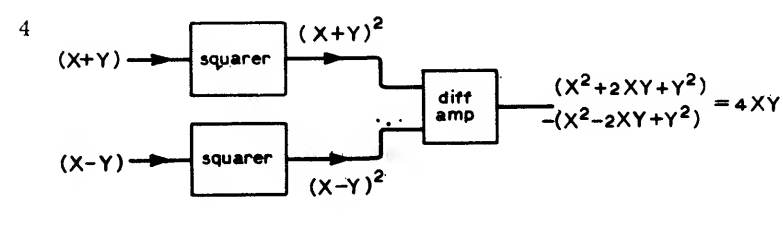




The quarter-squares multiplier applied in analogue computing uses two such squaring circuits as shown in Fig. 4. The sum of the two input signals is fed to one squarer, and the difference to a second. Each output contains a product term but also the square of each input signal. By subtracting the two outputs, these square terms cancel leaving only the product term, in this case $4XY$ i.e. a quarter of the output giving the desired multiplication of X by Y (card 1).

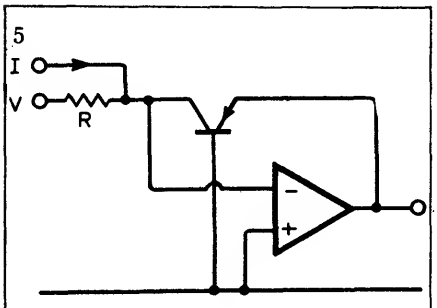
Of considerable interest in this respect are the characteristics of field-effect transistors. Both junction and m.o.s. devices have an on-resistance below pinch-off that is controlled by the gate-source voltage. The resistance is non-linear but can be linearized with feedback, while the control-law contains a square-law term (card 10).

Although bipolar transistors have output current/input voltage transfer characteristics which include square-law terms, their true nature is exponential with all their higher-order terms. It would be pointless to try to manipulate these transfer functions in the same way as above. Instead the exponential function is exploited directly in various ways. The exponential equation is reasonably accurate for p-n junctions over a few decades of currents. To ensure that the current in the diode/transistor is well-controlled the device can be placed in the feedback path of an operational amplifier, Fig. 5.



One problem introduced by the use of a transistor is that of the increased loop gain, the transistor operating effectively in common-base with a voltage gain dependent on the input voltage. This leads to h.f. oscillation unless the amplitude-frequency response is carefully controlled by means of external compensation – one possibility being capacitive feedback from output to inverting input, by-passing the transistor at high frequencies. To use this logarithmic function for multiplication (as in card 4) the system shown in block diagram form in Fig. 6 may be used. The antilog circuit is simply a log circuit with input (resistor) and feedback (diode/transistor) elements interchanged. Similar systems can be devised to provide other power law and ratio circuits by expressing the desired function in log/antilog forms first.

5



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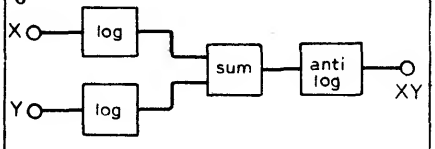

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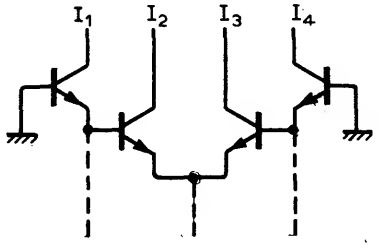
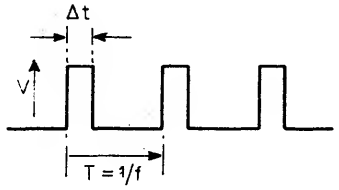


$V_{be1} + V_{be2} = V_{be3} + V_{be4}$

ie: $\log_e I_1 + \log_e I_2 = \log_e I_3 + \log_e I_4$

$I_1 I_2 = I_3 I_4$

8



$V_{mean} = f.V.\Delta t$

A related technique uses multiple transistors (card 8), shown in a general configuration in Fig. 7. It is assumed that the currents are controlled by external generators and/or feedback with one of them, or the difference between two of them, as the output. In the example shown, for I_2 maintained constant, $I_1 \propto I_3 I_4$ i.e. a multiplier. As shown, operation would be restricted to a single quadrant, but a large number of circuits have been published both to extend the operation into all four quadrants and to produce a range of interrelationships such as those based on the log approach.

A totally different approach yielded many ingenious and effective multipliers, prior to the ready availability of matched transistors. It stems from the concept that the terms to be multiplied need not remain in the same physical domain while being processed e.g. the variables of interest may both be voltages and the output may also be required as a voltage but each input may be used separately to control a different parameter of an output waveform, while a third property might be proportional to the product of the other two.

Consider the pulse waveform shown in Fig. 8. The pulse height is V, the repetition frequency $f = 1/T$ and the pulse width of Δt. The mean output voltage as would be indicated on a moving coil meter is given by the product of these three variables, increases in each individually producing a proportional change in that mean value. Thus if any pair of these variables (f, V), (f, Δt) or (V, Δt) is brought under the separate and linear control of two input voltages, then the mean output voltage is a measure of the input product (card 2). There is a close relationship between these circuits and various forms of pulse modulators in the same way that the analogue multipliers described earlier are related to amplitude modulators.

There are purely digital methods of multiplication, but an intermediate solution is offered by the multiplying d.-to-a. converter. For a given binary input the converter has a number of output switches activated. If these operate on an external reference voltage the final output depends on the product of that reference voltage and the binary number. A class of digital circuits called binary-rate-multipliers is used to operate on a pulse train, producing a second train of pulses at a slower rate, card 3. At first sight this must cast doubts on the terminology since we associate multiplication with outputs greater than the inputs. The property of the circuit is however to multiply the input pulse rate by a factor such as $n/100$ where $n < 100$ and n can take up any value between 1 and 100, i.e. it is equivalent to multiplying by n but shifting the decimal point by two places.

The variety of methods available for achieving the multiplication of two variables electronically is growing, and modules are readily available to a high degree of accuracy. As the methods vary widely in both properties and in the physical processes involved it is important to consider the options carefully – it is a field where the opportunities to place one's foot firmly in it (unspecified) are remarkably high.

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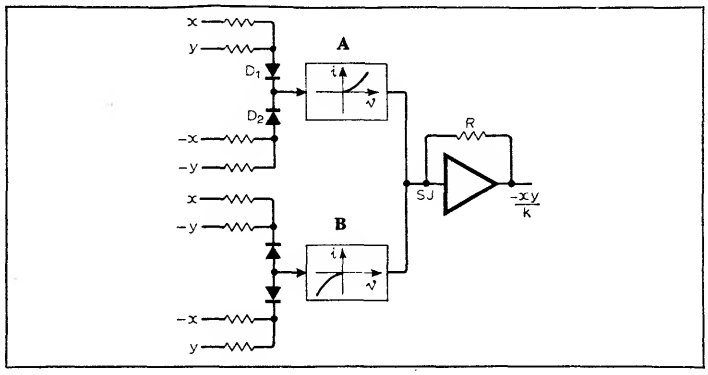
Quarter-squares multiplier



Description

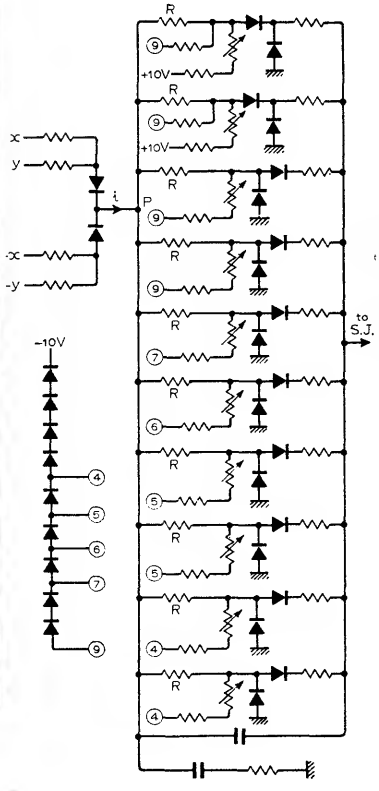
Quarter square multipliers are found frequently in analogue/hybrid computers in which their high accuracy (0.05% of half scale) is required and their limited bandwidth (less than 10kHz) is no disadvantage. They implement the relationship $xy=\frac{1}{4}[(x+y)^2-(x-y)^2]$ i.e. multiplication based on a square law device—this is usually a diode function generator permanently set to provide a square law action. Such generators are usually single quadrant devices, e.g. A (above) requires a positive input and this necessitates the use of an absolute value circuit prior to it. If, for instance, $(x+y)$ is positive then D_1 conducts (and D_2 does not) and a positive voltage is applied to A. Likewise if $(x+y)$ is negative D_2 conducts (and D_1 does not) but again it is a positive voltage that is applied to A. Hence the output of A is proportional to $|(x+y)|^2$, which is the same as $(x+y)^2$. A similar argument applies to the other absolute value circuit, B; being a 3rd quadrant device, it produces a current proportional to $-(x-y)^2$.

The constant k appearing in the output expression depends on R and on the output characteristics of A and B. Generally, if the maximum value of X and Y is say P volts, then k is set to P.

If an absolute value circuit does not precede the squaring section then a total of four squaring sections are necessary. Despite the apparent increased complexity this is still sometimes done to avoid errors due to the diodes D_1 and D_2 and to provide further functions.

An example of a square law generator circuit is shown (ref. 1). The current i has a total of 10 possible paths between P and the summing junction (SJ). Depending on the voltage at P, however, not all of these paths are open. If the voltage is very small, only one path, via the top R is open. With increasing voltage more paths become open so that the resistance between P and SJ decreases thus increasing the gain between P and the amplifier output in steps. The points at which these step changes in gain occur are termed breakpoints and are usually equally spaced as the figure above shows. Uniform breakpoint spacing allows identical slope increments and equal positive and negative errors. For this situation errors can be kept within $x\%$ of half scale with $10/\sqrt{x}$ segments. Unequal spacing of the break-points makes no significant difference to the overall accuracy although it is common to have one or two extra breakpoints near zero for improved accuracy.

The use of the diode string to provide some of the biasing functions provides temperature compensation as well. The capacitors shown increase the frequency response.



Related circuits

If bandwidth is not essential but increased accuracy is, then use can be made of the relationship $m^2=\frac{1}{4}(1+2u+u^2)$ where $u=2|m|-1$.

The right hand side of this equation is not totally dependent on u^2 so that errors produced by a squaring circuit producing u^2 have a reduced effect on the errors in m^2. One can, of course, invert the situation and say that, for the same accuracy, fewer breakpoints are necessary and a less expensive squarer is produced. A "card" mechanising the right hand side of the equation is simply inserted as the A card in the circuit overleaf and with minor modifications a B card is produced.

If we now examine

$$xy=\frac{x+y^2}{2}-\frac{x-y^2}{2}=m_1^2-m_2^2$$

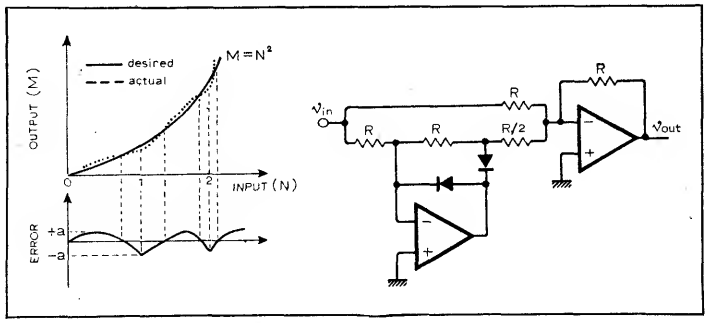
and apply the above equation for m we obtain

$$xy=\tfrac{1}{4}[2(u_1-u_2)+(u_1^2-u_2^2)]$$
$$=\tfrac{1}{2}(|x+y|-|x-y|)+\tfrac{1}{4}(u_1^2-u_2^2)$$

Reapplying the formula on the second bracketed term $(u_1^2-u_2^2)$ and truncating the series which will result from repeated application gives

$$xy\approx\tfrac{1}{2}(|x+y|-|x-y|)+\tfrac{1}{4}\{||x+y|-1|-||x-y|-1|\}$$

This does not require a squaring circuit and can be based on precision absolute value circuits such as those given in ref. 2



References

1. Whigham, R. H. Fast 10-V quarter-square multiplier. Simulation 1965.
2. Set 4, card 3.
Korn and Korn. Electronic Analog and Hybrid Computers, 2nd edition, McGraw-Hill.

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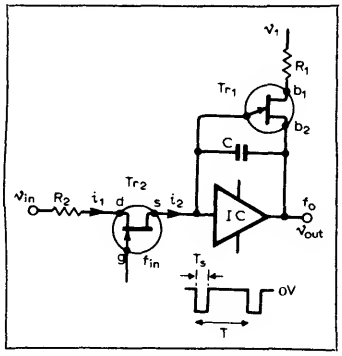
V-f converter multiplier



Typical performance
IC 741, ±15V supplies
Tr_1 2N2646 u.j.t.
Tr_2 2N5486 f.e.t. (n-channel)
R_1 100Ω
R_2 1kΩ
C 47nF
T_s 100μs
Pulse height −5V

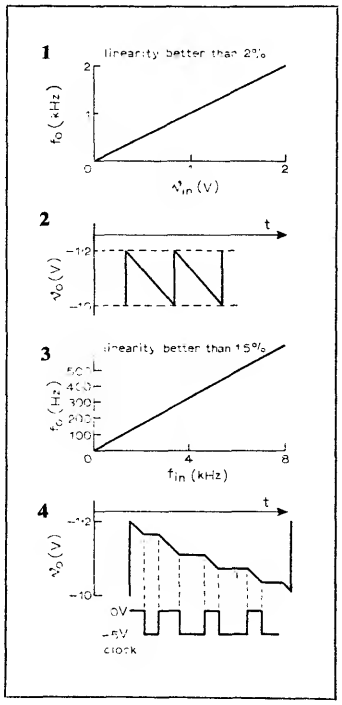
Circuit description
The circuit is a modification of the v-f converter described in ref. 1. The f.e.t. Tr_2 is the only addition. Graph 1 was obtained with f.e.t. permanently conducting, i.e. $V_{gs}=0(f_{in}=0)$, and shows f_o to be proportional to v_{in}. This graph was obtained with v_1 set to 3.3V which setting gave an f_o of 2kHz with $v_{in}=2$V. Control of the relationship between f_o and v_{in} depends on the u.j.t. breakdown voltage and this is variable from device to device. The v-f conversion can be described as a conversion first from v_{in} to i_1 and secondly from i_1 to f_o. The greater i_1 the more rapidly does the capacitor charge and the more rapidly is the breakdown condition of the u.j.t. met. The downwards ramp of graph 2 shows this charging. On breakdown the u.j.t. shorts the capacitor so the output voltage rises towards zero until the u.j.t. assumes its normal non-conducting role.
If now pulses are fed to the f.e.t. gate as shown, i_1 will become a train of current pulses i_2. f_o then depends on i_2.

$$f_o=k\,i_2=k\,i_1\cdot\frac{T_s}{T}=k\frac{v_{in}}{R_2}T_s\cdot f_{in}$$
$$=k_1\,v_{in}f_{in}$$

Graph 3 shows that f_o is indeed proportional to f_{in}, the proportionality between f_o and v_{in} being shown in graph 1. The multiplying action is thus experimentally verified.
If f_{in} is derived from another v-f converter we have $f_{in}=k_2v'_{in}$ and then $f_o=k''\,v_{in}\cdot v'_{in}$ so that f_o is proportional to the product of two voltages.

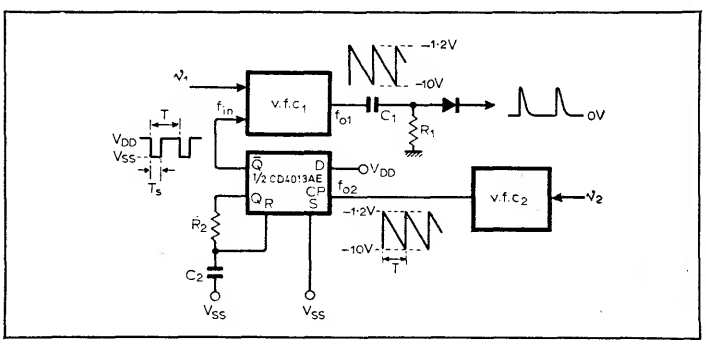
Component changes. The value of R_2 quoted i.e. 1kΩ is the absolute minimum usable. R_2 should be much larger than the f.e.t. "on" resistance (≈200Ω). Max. $R_2\approx100$kΩ; beyond this op-amp input currents become significant. The value of C is related to that for R_2 as the ramp slope is $1/R_2C$. With $C=4.7$nF (and $T_s=10\mu$s) we achieved a maximum f_o of 10kHz. Higher values of f_o are difficult to achieve because of charge-storage effects in the u.j.t. affecting the discharge time. Pulse height must be sufficient to cause pinch-off of f.e.t. but not so high as to cause breakdown. −1 to −10V with this device was satisfactory.

Circuit modifications
The circuit above shows a complete circuit whose output frequency, f_{o1}, is proportional to the product of the voltages v_1 and v_2. The second voltage to frequency converter, VFC_2, is assumed to be identical to that shown in the main diagram overleaf with the omission of the f.e.t. gate; it will therefore produce an output as shown in graph 2. This output is fed to the c.m.o.s. monostable shown (ref. 2) in which $V_{DD}=0$V and $V_{SS}=-10$V (−15V would also be acceptable). This monostable is triggered when the c.p. voltage is about 50% of $[V_{DD}-V_{SS}]$, the rising edge being the only one which is effective. The output pulse width is controlled by the R_2C_2 time constant, resetting occurring when the voltage at R is approximately 50% of



$[V_{DD}-V_{SS}]$. Taking the output from $\bar{Q}$ gives trigger pulses of the correct polarity to gate the f.e.t. in the input path of VFC_1 which is identical to that shown . The output f_{o1} will then be as shown in graph 4.
The network comprising C_1, R_1 and D_1 is simply a differentiating network to produce a somewhat more normal type of pulse train. Note that f_{in} is equal to f_{o2} and that f_{o1} must be less than f_{in}. In fact consideration of the operation of the system overleaf shows that f_{in} should be of the order of ten times the desired f_{o1}. Hence VFC_2 must operate at a much higher frequency than VFC_1 and consequently the input resistors and feedback capacitors will be different. Voltages v_1 and v_2 also affect the frequencies of operation. As the maximum frequency attainable from a unijunction type of v-f converter is of the order of 10kHz it may be necessary to use different types for a particular application. There is certainly no need for VFC_1 and VFC_2 to be of the same type. V-f converters have been considered in ref. 3. If different v-f converters are used different gating arrangements may well be required and in particular different monostables may be needed ref. 4.
A multiplier using two identical (in form) v-f converters designed for long term stability and able to accommodate floating inputs is described in detail in ref. 5.

Related circuits
1 Set 21, V-f converters, card 1
2 Set 19, Monostables, card 8
3 Set 21, V-f converters
4 Set 19, Monostables
5 Versatile integrator-multiplier, E. Ljung and S. Berglund, *Electronic Engineering*, Aug. 1974, pp. 38-40.



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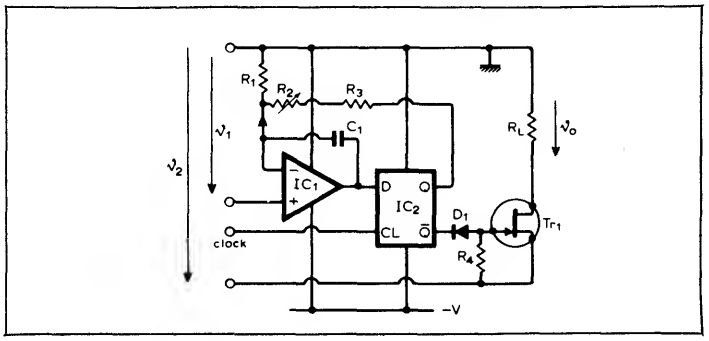
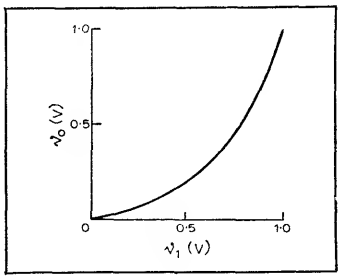
Delta-sigma modulator/multiplier



Typical performance
IC_1 N5741V (Signetics)
IC_2 ½CD4013
D_1 1N4148
Tr_1 2N5457
R_1 4.7kΩ
R_2 100kΩ pot.
R_3 100kΩ
R_4 15kΩ
R_L 15kΩ
Supply −10V
v_1, v_2 0→ −1V
v_o 0→ −1V
$|v_o| = v_1 v_2$



Circuit description
If an output waveform has a constant pulse height and width but the pulse-rate is proportional to an input voltage, then the mean value of the output is also proportional to that voltage. If the pulse height is made proportional to a second voltage the mean output becomes proportional to the product of the two voltages. A delta-sigma modulator converts a pulse-train into one with a smaller number of pulses, using an integrator to control the voltage on the D input of a flip-flop. As the mean voltage at the inverting and non-inverting inputs are the same and the mean current in the capacitor is zero, the fraction of the time for which Q is high is controlled by the input voltage v_1. The circuit configuration has a negative input voltage and supply because it was desired to use the simplest arrangement, and certain op-amps (e.g. Signetics 741) have an input common-mode range that includes the positive supply rail. The circuit can be adapted for any other op-amp by providing a separate positive bias. With dual supplies the system may equally be used with positive inputs and outputs if the flip-flop is powered from the positive rail.

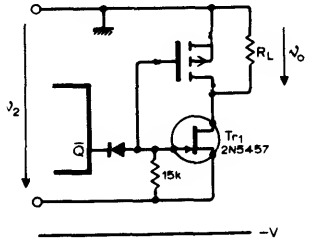
The $\bar{Q}$ output is used to gate a junction f.e.t. on and off. With $\bar{Q}$ high (zero volts), the diode is non-conducting and R_4 establishes zero gate-source bias. With $\bar{Q}$ low (−V) the f.e.t. is off. This is true provided the second input voltage v_2 is small so that the reverse gate-source voltage is in excess of the pinch-off voltage. The load receives voltage pulses of duration equal to the inter pulse period and just less than v_2 in magnitude. The number of pulses in a given time is proportional to v_1. Hence the mean load voltage is $\propto v_1 v_2$. This can be read directly on a moving-coil meter, or filtered and fed to a d.v.m.

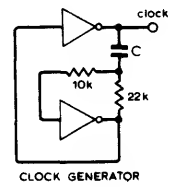
Component changes
IC_1: Any op-amp if supply requirements observed. Output is always close to the flip-flop threshold voltage i.e. does not approach either supply line. Supplies can be single-ended negative or positive depending on op-amp. Must be large enough to gate f.e.t. 6 to 15V.
Tr_1: Any n-channel junction f.e.t. with pinch-off below, say, 5V. Low on-resistance preferred.
D_1: General purpose switching diode.
IC_2: Any c.m.o.s. D-type flip-flop (set and reset grounded).
R_1, R_2, R_3: Ratio sets 'gain' i.e. usual potential divider relationship defines ratio of mean output at Q to v_1. Total resistance 10k to 10MΩ. Suggested ratios 5: 1 to 20: 1.
R_4: If too high, results in slow switching of f.e.t. from off-on state with reduced overall accuracy. If too low, additional current places unwanted extra load on v_2 source.
v_1, v_2: Typically 0→ −1V. v_1 feeds into very high impedance, v_2 has to supply load current via Tr_1.
R_L: Compromise between sensitivity of meter and loading of v_2 5k to 50kΩ.

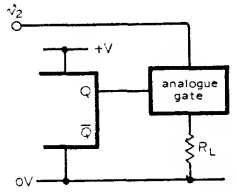
Circuit modifications
- To improve switching times without adding an extra i.c., it is possible to use a p.m.o.s. transistor from a CD4007 package. If the remainder of the package is connected as in the circuit shown, a clock generator results. Frequencies from 10kHz to >100kHz have been tested with this system. In general clock rates of several MHz are feasible but would make heavy demands on the analogue switches. The p.m.o.s. device prevents charge storage across the load resistance in the off-state, and allows the high load resistance represented by a d.v.m. to be used. This makes the input impedance at the v_2 input high, without restricting the switching rate.
- If positive input voltages are used, and standard analogue gates are available, then a series switch arrangement as shown may be driven from the Q output. Then when v_1 is at its maximum value, Q is almost permanently at logic 1 and v_2 is gated through to the load for almost 100% of the time. A shunt gate driven from $\bar{Q}$ completes the configuration for higher switching speeds or where R_L is to be raised.
- In principle this can be interpreted as a combined V_1-f and V_2-amplitude converter system.

Related circuits
Set 15, card 9

Circuit modifications







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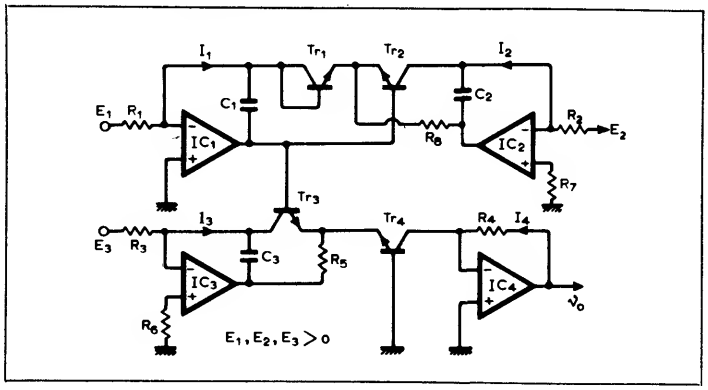
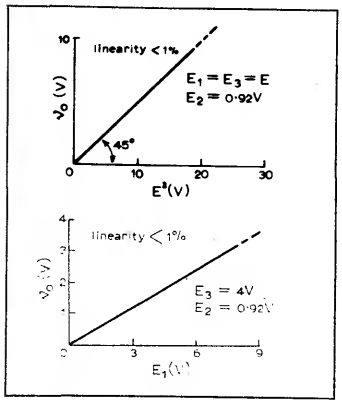
Log-antilog multiplier



Components
IC_{1-4} 741 (e.g. RC4136 quad package)
Tr_1 to Tr_4 1/5 CA3086
R_1, R_2, R_3, R_6, R_7 100kΩ
R_4 10kΩ, R_5 2.2kΩ
C_1 300pF, C_2 200pF
C_3 22pF
All passive components ±5%
Supply voltage ±7.5V

Performance
It can be shown (see text) that $v_o = E_1E_3R_2R_4/E_2R_1R_3$. With the resistor values chosen, assuming perfect components, $v_o = E_1E_3/10E_2$ and so the circuit can be used as a squarer ($E_1 = E_3$ and E_2 constant), as a multiplier (E_2 constant E_1 and E_3 variable), as a divider (E_2 as divisor E_1 or E_3 as dividend, the other fixed) or as a device for obtaining the reciprocal of E_2 (E_1 and E_3 fixed). Results as a squarer are shown in graph 1 from which it will be noted that E_2 was set at 0.92 rather than 1V to achieve the slope of 45°



(making up for component inaccuracy) and that the maximum v_o obtainable is less than 4V. Saturation of the transistors occurs at higher voltages. Graph 2 shows similar linearity for operation as a multiplier, multiplying the variable E_1 by the constant E_3. Identical results were obtained when the roles of E_1 and E_3 were reversed. Similar linearity was obtained with the device operated as an arithmetic inverter (reciprocal).

Circuit description
Analysis of the circuit is as follows:

$$I_1 = E_1/R_1 \text{ and } V_{be1} = \frac{kT}{q}\log_e I_1$$

$$I_2 = E_2/R_2 \text{ and } V_{be2} = \frac{kT}{q}\log_e I_2$$

$$V' = V_{be2} - V_{be1} = \frac{kT}{q}\log_e \frac{E_2R_1}{E_1R_2}$$

$$V_{be4} = -V' + V_{be3} = -\frac{kT}{q}\log_e \frac{E_1E_3R_2}{E_2R_1R_3} \quad (1)$$

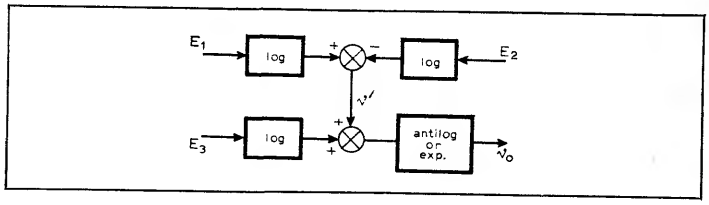
as $V_{be3} = \frac{kT}{q}\log_e I_3$ and $I_3 = E_3/R_3$.

But $\log_e I_4 = qV_{be4}/kT$ and $I_4 = V_o/R_4$
Combining this last pair of equations with equation 1 gives

$$V_o = \frac{E_1}{E_2}E_3\frac{R_4}{R_3}\frac{R_2}{R_1}$$

A functional block diagram following from these equations is shown, right. The antilog function is performed by Tr_4 and IC_4. Principally it is Tr_4 which performs the antilog function in converting its base-emitter voltage to a current: IC_4 and R_4 convert this current to a voltage, viz V_o.
The above analysis concerned d.c. conditions only, so all capacitors were ignored. Likewise R_5 and R_8 were ignored. The function of all of these components is to stabilize the loops in which they are contained. To see this, consider the simplest case viz. IC_3 and its associated circuitry. The loop gain of this circuit is the open-loop gain of IC_3 together with the gain of Tr_3 which is in common base mode and has a voltage gain given approximately by $g_m \times$ the load on Tr_3. The load on Tr_3 is R_3 (by superposition the E_3 input end of R_3 is at ground). This voltage gain g_mR_3 is large and the overall loop gain is, therefore, considerably enhanced and instability is a considerable problem. The inclusion of R_5 reduces the feedback path gain as only a portion of the i.c. output voltage is applied to the base-emitter junction. For high frequency effects C_3 completely shorts out this feedback path amplifier, again improving stability. Note that g_m depends on the operating conditions i.e., in this case, on E_3 so that the problem is complex indeed. Note that all the input voltages must be positive to maintain correct transistor biasing. If a sinusoid is to be used it must be suitably biased to prevent negative going inputs and the output circuitry must be considerably rearranged to remove the effect of the biasing term on the output.

Component changes
This circuit was built from the cheapest possible components and no effort was made to null the i.cs. Considerable improvement in accuracy is obtainable if the resistors $R_1R_2R_3$ and R_4 are chosen to a much tighter tolerance. Nulling of i.cs will improve performance as will the use of i.cs with facility for feedforward compensation e.g. LM301 etc. The use of i.cs with very low input currents e.g. LM108 or f.e.t. input i.cs such as CA3130 will improve the lower end of the input range. These comments do not apply strictly to IC_4 which simply converts the current through Tr_4 to a voltage. Indeed, an appropriate moving coil meter connected between the collector of Tr_4 and ground will suffice to give a reading of the output.

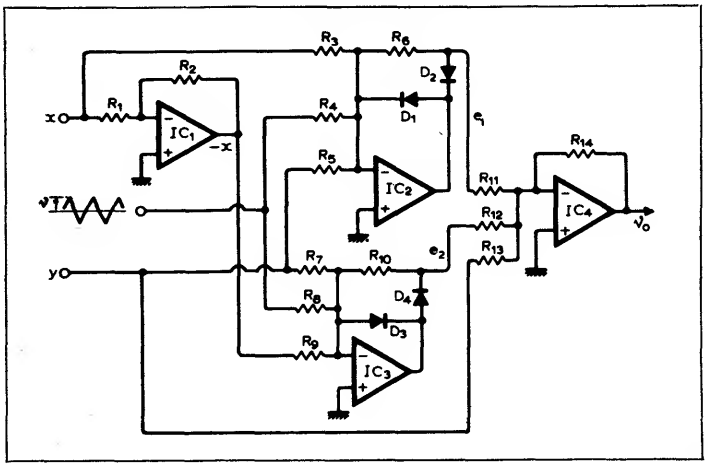


Further reading
National Semiconductor application notes AN-30.

Related circuits
Set 4, card 11

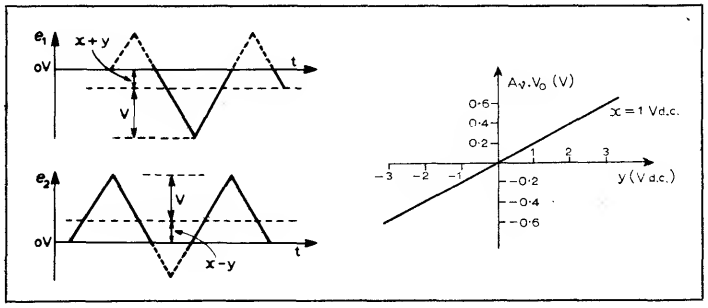
wireless world circard

Triangle-wave averaging multiplier

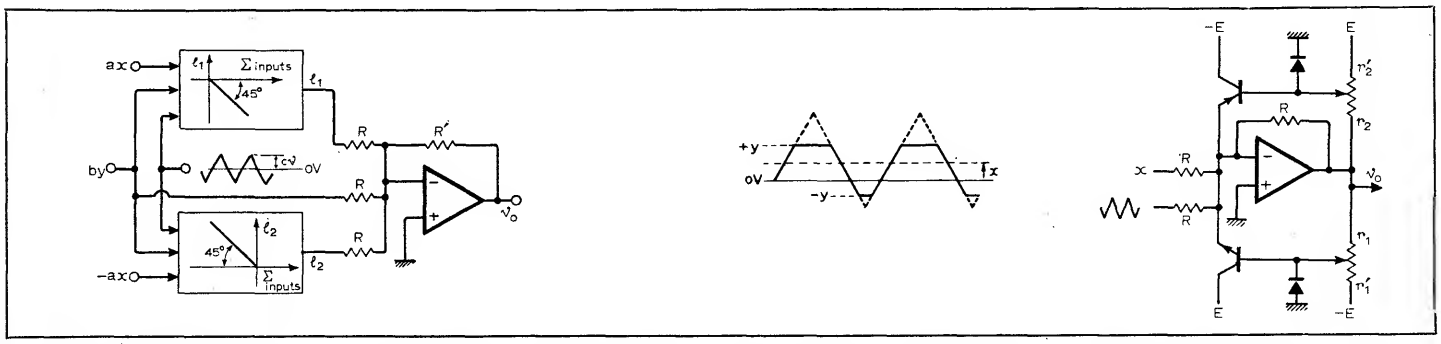


Components
R_1 to R_{14} 120kΩ
IC_1 741
D_1 1N914
Supplies ±15V

Performance
With v set at 4V and the frequency of the triangular waveform set at 1kHz graphs 1 and 2 were obtained. Linearity shown in graph 2 is better than 1%. Note that x and y are direct voltages and v_o is the average voltage at the output of IC_4. v_o is, of course, the inverted sum of e_1, e_2 and y. With x and y both at 1V and varying the frequency of the triangular wave the output accuracy was maintained within 1% up to 6kHz. The device is a 4-quadrant multiplier.



Description
The block comprising IC_2, R_3, R_4, R_5, R_6, D_1 and D_2 is a precision half-wave rectifier producing a negative output equal in magnitude to the sum of the input voltages when that sum is positive. The block producing e_2 can likewise be described. The sum of e_2, e_1 and y produces the output and at first sight the multiplier appears related to time-division (a.m./p.w.m.) multipliers. Analysis shows however that this multiplier is more closely related to the quarter-square multiplier, the reason being that the height of e_2 is closely related to the base of hatched triangle in graph 1 so that the area of the triangle becomes a square function.



A more general diagram is shown above: for this system it can be shown that the average value of V_o is:

$$-\frac{R'}{R}(\text{average of } e_1+\text{average of } e_2+by)$$

$$=-\frac{R'}{R}\left[\frac{-1}{4cV}(cV+ax+by)^2+\frac{1}{4cV}(cV+ax-by)^2+by\right]$$

If $R'=\alpha R$, then this expression simplifies to

$$V_{oav}=\alpha\, xy\,\frac{ab}{cV}$$

Comparing this with the circuit overleaf we see that we have $\alpha=a=b=1$ and $cV=4$.

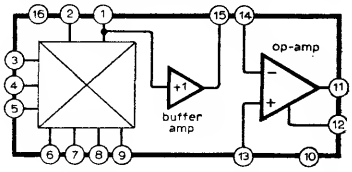
Returning now to the original circuit one can observe that the somewhat restricted input range is due to the fact that at no point should the bias voltage exceed the peak of the triangular wave. Clearly the input signal size can be increased by increasing the carrier magnitude and also by introducing factors a and b, reducing the effective input. The effect of these changes can be then cancelled by setting $R'=\alpha\, cV/ab$.
The circuit is sensitive to d.c. components in the carrier and also to the carrier magnitude. The effect of a d.c. component is particularly noticeable at low signal levels.

Circuit modifications
Resistor values are not critical but lower values than those shown may be preferable to improve the bandwidth by reducing the time constants of stray and other capacitive paths. Resistor R′ may be replaced by a filter to remove the a.c. components of V_o. The d.c. impedance of such a filter should still equal R'.
The system bandwidth can be increased by using a faster version of half-wave rectifiers[1].

- An alternative scheme is shown above; this arises from the fact that the product xy is obtained by biasing a triangular wave by x and limiting the resultant at $\pm y$. A suitable high speed limiter is shown above. The output is limited at r_1E/r' for negative inputs and at $-r_2E/r_2'$ for positive inputs. These would be set to $\pm y$ respectively. Note that $r_{1\ 2} \ll R$ for good limiting.

References
1 Set 22, card 3
2 Korn & Korn, Electronic Analog and Hybrid Computers, 2nd edition McGraw-Hill.

Four-quadrant multiplier—characteristics



Pin designation

1, 2 multiplier outputs
3 x input 4 common
5 y input 6 and 7 y gain
8 and 9 x gain
10 negative supply
11 op-amp output
12 compensation
13 non-inverting op-amp input
14 inverting op-amp input
15 high-frequency output
16 positive supply

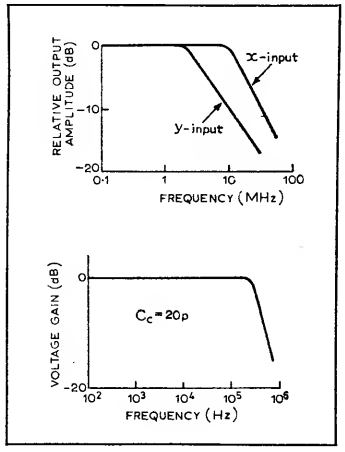
Description

The XR-2208/2308 is an op-amp combining a four-quadrant analogue multiplier, a high-frequency buffer amplifier and a differential-input op-amp on the same monolithic integrated circuit. The package is suitable for arithmetic operations and communication signal processing, maximum versatility being achieved by internally separating the amplifier and the multiplier-buffer section; suitable interconnections being made externally with passive components. The op-amp can be used as a post-detection amplifier in coherent detector applications or as a preamplifier for low-level input signals.

The output from the buffer amplifier can be used for high-frequency signal processing, the multiplier-buffer section having a small-signal 3dB bandwidth of 8MHz and a transconductance bandwidth of 100MHz.

The package can be operated from symmetrical supply rails in the range ± 4.5 to ± 16V. Very good power supply rejection and temperature stability are achieved by internally-regulating current and voltage levels.

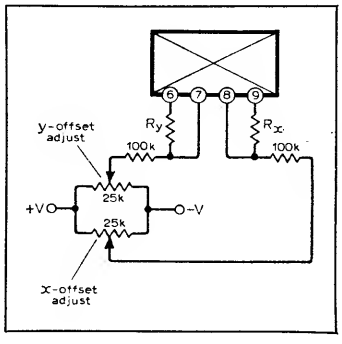
The multiplier inputs x and y are applied to pins 3 and 5 respectively, with pin 4 common—normally the reference or ground terminal. However, in some applications x and y inputs are strapped together and pin 4 used as an



input terminal. The d.c. bias currents at pins 3 and 5 are typically 3μA and at pin 4 typically 6μA. The differential output voltage (v_o) between pins 1 and 2 is often connected directly to the op-amp (pins 13 and 14), the final output (v_z) being obtained from pin 11.

$$v_o \approx \frac{25}{R_X \,.\, R_Y} v_X \,.\, v_Y$$

where all voltages are in volts and the gain control resistances



(R_X and R_Y) for the x and y sections of the multiplier are in kΩ. Conversion gain of the multiplier is

$$K_M \approx \frac{25}{R_X \,.\, R_Y} (V^{-1})$$

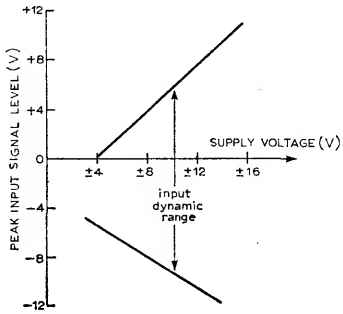
resistors R_X and R_Y being connected as below, where the arrangement for adjusting the x and y offsets at pins 7 and 8 is also shown.

The operational amplifier is internally protected against short-circuit load conditions and can sink or source a current of 10mA into a resistive load. This amplifier can be compensated for unconditional stability by connecting a capacitor (C_C) of 20pF across pins 11 and 12. For higher voltage gains than unity, C_C is reduced to increase small-signal bandwidth and to improve slew-rate.

The unity-gain buffer amplifier if brought into use by connecting a resistor from pin 15 to ground and provides a low-impedance output for the multiplier section when the latter is used at high frequencies, in order to minimize capacitive loading of the multiplier output proper. The buffer output is not short-circuit protected and typically has a direct voltage of $V^+ - 4.5$ volts. The maximum direct current extracted from pin 15 should not exceed 10mA.

NOTE: When only the multiplier section or op-amp section is being used the input terminals of the unused section must be connected to ground.

The maximum peak x or y input signal that can be used for a given supply voltage without significant improvement of the linearity of the multiplier is shown.



Further reading

XR-2208/2308 Operational multiplier data sheet, EXAR, 1972.

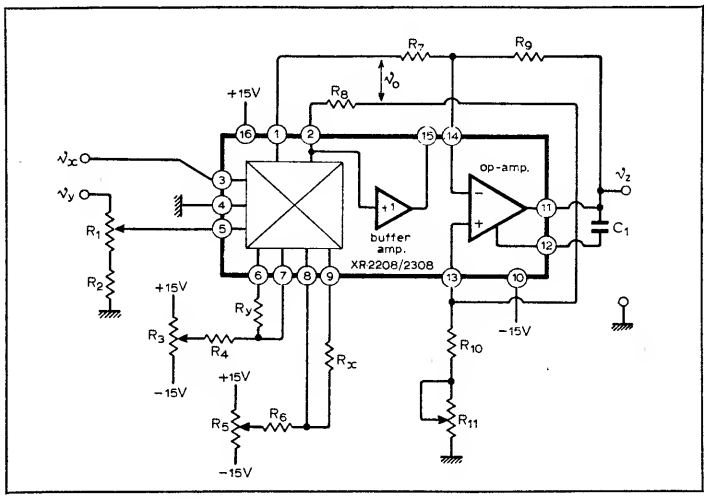
XR-2208 Operational Multiplier, *New Electronics*, 1 April 1975, pp. 27-31.

Related circuits

Set 29, card 7

wireless world circard

Four-quadrant multiplier—applications



4-quadrant multiplier—applications

In most multiplication applications the operational amplifier and multiplier sections are interconnected as shown left providing a single-ended output signal and having a wide dynamic range. With the values shown below, the linear output swing is typically 10V for maximum input signals of 10V with a scale factor $K=0.1$.

Setting-up procedure

1 With 0V applied to both inputs the output offset is adjusted to be 0V with R_{11}.
2 With a 20V pk-pk, 50Hz signal applied to the x-input and 0V to the y-input, R_3 is adjusted to provide minimum output voltage.
3 With a 20V pk-pk 50Hz signal applied to the y-input and 0V to the x-input, R_5 is adjusted to provide minimum output voltage.
4 Repeat step 1.
5 With +10V applied to both inputs, R_1 is adjusted to provide an output of +10V.
6 Step 5 may be repeated with different input voltages and different polarities to obtain best accuracy either over the whole input range or over some specific part of it.

Squaring circuit

As shown over, the circuit used for squaring is essentially that used for multiplication except that the input signal is applied simultaneously to the x and y input terminals and only one input offset adjustment is required.
Adjustment procedure is:

1. With 0V applied to the input the output offset is adjusted to be 0V using R_{11}.
2. With +1V applied to the input R_3 is adjusted to make v_o 0.1V.
3. With +10V applied to the input the output is adjusted to be +10V using R_1.
4. With −10V applied to the input check that the output is +10V, if this is not so repeat steps 1 to 3.

A.m. generator

The circuit (middle) is that recommended for generating double sideband signals or for suppressed-carrier a.m. generation. Modulation and carrier are applied to the x and y inputs respectively with a carrier level of 1V (r.m.s.). The level of the carrier appearing at the output is adjusted by means of the 25kΩ potentiometer which sets the d.c. level at pin 3. In suppressed-carrier applications, the carrier level at the output can be further reduced by means of the x and y offset adjustment controls. The buffer amplifier provides a unity gain low-impedance output, but if not required pin 15 should be open circuited to reduce power dissipation. Carrier suppression of 40dB up to 1MHz and 30dB up to 10MHz is obtainable without the use of the x and y offset adjustments.

Component values

Supplies ±15V
$v_{x(max)}$, $v_{y(max)}$ 10V
R_1, R_2 5kΩ
R_3, R_4, R_5, R_6, R_{11} 100kΩ
R_7, R_8 24kΩ, R_9 300kΩ
R_{10} 240kΩ, R_x 30kΩ
R_y 62kΩ, C_1 20pF
$V_z=V_x\ V_y/10$
R_1 scale factor
R_3 y-offset
R_5 x-offset
R_{11} output offset

Synchronous a.m. detector

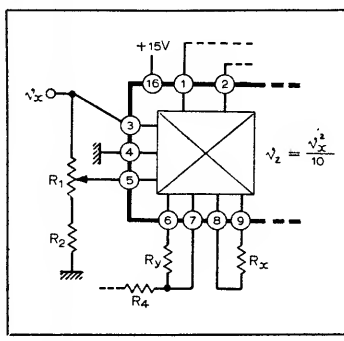
The circuit (right) is suitable for demodulation of a.m. signals with carrier frequencies up to 100MHz, with an input signal of at least 25mV r.m.s. The a.m. input is applied to the common terminal of the multiplier, the y-gain terminals are strapped allowing this section to act as a limiter for inputs greater than about 50mV r.m.s. and the x-section acts in its linear mode. Capacitors C_1 at pins 1 and 2 in the low-pass filter serve to reduce the carrier feedthrough to the output.

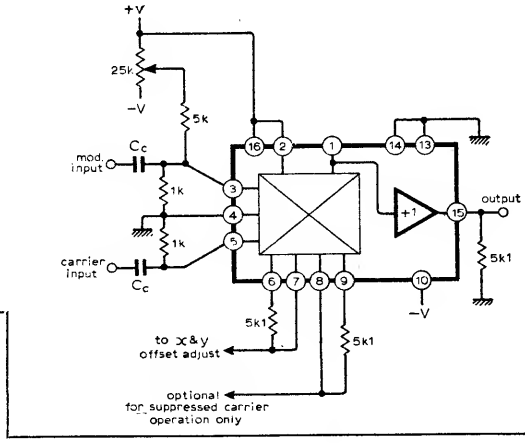
Further reading

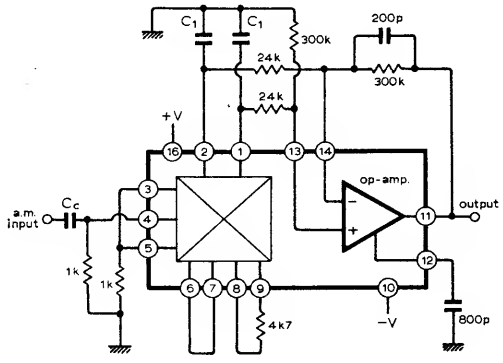
XR-2208/2308 Operational multiplier data sheet, EXAR, 1972.

Related circuits

Set 29, card 6







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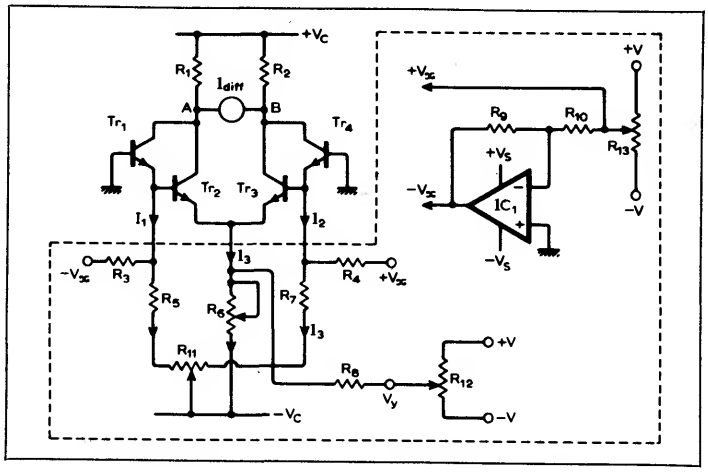
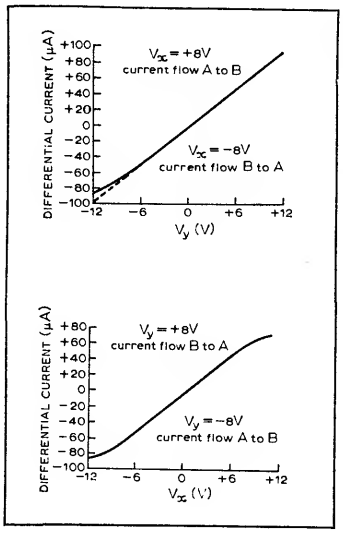
Set 29: Analogue multipliers—8

Translinear multiplier



Typical data
Tr_{1-4} 1/5 CA3086
R_1 47kΩ ±5%
R_2 46.6kΩ (trimming required)
R_3, R_4, R_5, R_7, R_8 100kΩ ±5%
R_6 68.7kΩ (trimmed)
R_9, R_{10} 50kΩ IC_1 741
R_{11} 100kΩ R_{12}, R_{13} 10kΩ
V_c ±15V
V: ±12V V_s: ±15V
N.B. Pin 13 of CA3086 must be connected to most negative potential.



Circuit description

The circuit currents above are related to a defined current unit I, by the following:
$I_1=(1+X)I/2$ $I_2=(1-X)I/2$
$I_3=(1+Y)I$
where X and Y are controlled variables, and I_{diff} between Tr_2 and Tr_3 collectors is XYI. The circuit operates in the current domain and depends for its temperature independence on the proportionality of bipolar transistor g_m (transconductance) to the collector current. Currents I_1, I_2, I_3 are ideally current sources, and the above network comprising V_x, V_y, resistors R_3 to R_7 is an attempt to simulate such a condition e.g. I_3 is approximately equal to $-V_c/(R_7+R_{11}/2)\approx 100\mu A$ plus a multiple of 100μA defined by V_x/R_4 where V_x is increased in steps of 1V. These calculations assume that the base-emitter junction voltages are negligible. To obtain a balanced condition where $I_{diff}=0$ if either V_x or V_y is zero demands trimming of resistor R_6 and R_2 to allow for the 1.2V potential at the emitters of Tr_2, Tr_3. Linearity of I_{diff} is shown in accompanying graphs. Note, that if $V_x=+8V$, this is equivalent to eight units of current, and if $V_y=+2V$, two units of current. Resulting product is 16.

Parameter changes

If $X=Y$, the output function is a squared function of those variables. Graphs of the resulting current variation are given above. For each graph, the effect of Y being negative causes a slight deviation from the true square law. Possibly due to inexact compensation for V_{BE} drops with network employed.

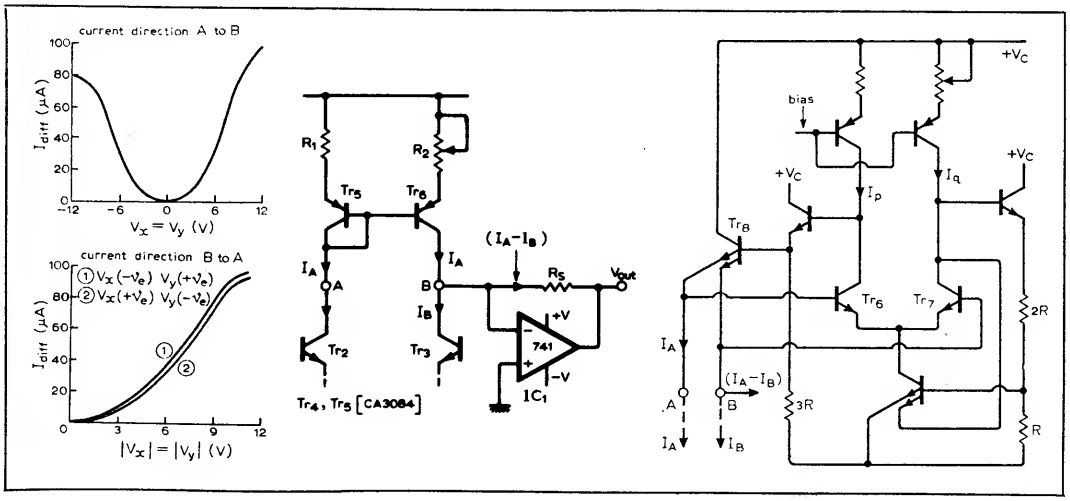
Component changes

Circuit is supply sensitive, especially at the low levels of current I. At $V_c=\pm 15V$, a 20% reduction of V_c provides a −3% error for $I_{diff}=81\mu A$, but at 9μA, +30% error.

Circuit modifications

- Use of transistors Tr_4, Tr_5 in a current mirror configuration will permit the differential current to be obtained with respect to ground. R_1 and R_2 are adjusted to be similar to obtain equal collector currents in Tr_4, Tr_5. This current is converted to an equivalent voltage by driving into IC_1, such that $V_{out}=-(I_A-I_B)R_S$.

A more sophisticated technique[2], with a wide frequency response, is shown extreme right. Transistor Tr_8, which has a double emitter, could be derived from a monolithic package by paralleling collectors and bases. The bias voltage which should be the silicon bandgap voltage (1.205V) minimizes the current ratio I_p/I_q drift with temperature. If $I_p=I_q$, then the base-emitter junction voltages of Tr_6 and Tr_7 are equal (for equal emitter areas). This implies that the emitters of Tr_8 are at the same potential, and hence the currents are equal.



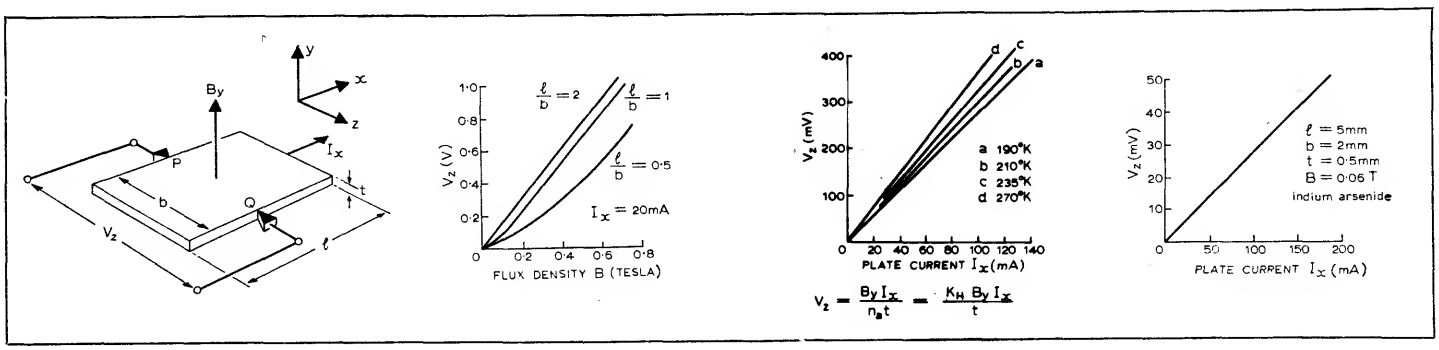
Further reading

1 Gilbert, B. Translinear circuits: A proposed classification, *Electronics Letters*, 9 Jan. 1975. vol. 11, no. 1.
2 Gilbert, B. Wideband negative current mirror, *Electronics Letters*, 20 March, 1975. vol. 11, no. 6.
3 Korn & Korn. Electronic analogue and hybrid computers. McGraw Hill 1972.

Related circuits

Set 6, card 4
Set 23, card 5

wireless world circard

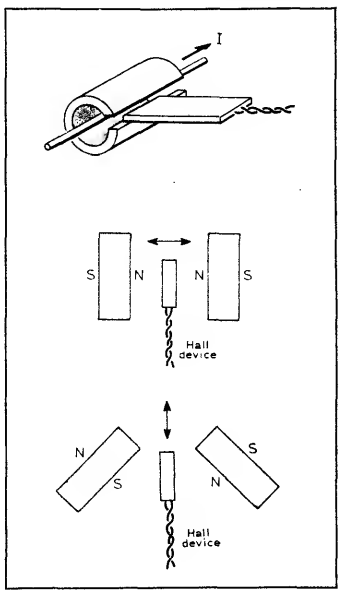


Hall-effect multiplier

Hall-effect multiplier
In a practical Hall plate, point electrodes between which the Hall voltage is developed are connected midway between the end-electrodes. Materials used for the plate are high mobility bulk semiconductors, with low conductivity: indium arsenide, germanium, indium antimonide.

Background
The device produces an output voltage dependent on the product of two inputs—the plate current I_x, and an external magnetic field B_y (Tesla). Current flow is due to electrons n, charge q and drift velocity v_x. Hence current density
$J_x = I_x/bt = nqv_x$.
Deflecting force on electrons in direction Z due to B_y is
$F_z = B_y q v_x$.
At equilibrium, this just balances the field force due to electron deflection, i.e. qE_z,
$B_y q v_x = qE_z$ and $E_z = B_y v_x = B_y I_x/btnq$
The Hall voltage is $V_z = E_z b$
$V_z = B_y I_x/mqt = K_H B_y I_x/t$
K_H is known as the Hall coefficient and should be as large as possible for maximum output. Conductivity is $\sigma = qn\mu_n$ where μ_n is electron mobility
$K_H = 1/qn = \mu_n/\sigma$
High mobility, low-conductivity optimizes device Hall voltage for specific thickness t.

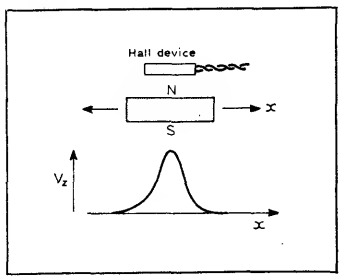
Applications
- An appropriately dimensioned device can be inserted within the air gap flux-path of a rotating electrical machine to determine flux density variations, when I_x is maintained constant.
- Both I_x and B_y can be generated by suitable voltages, and assuming fixed orientation between the Hall device and the field, then $V_z \propto V_x V_y$, where V_x and V_y may assume an alternating or direct voltage



identity.
Typical dimensions for transverse devices for insertion in thin gaps 0.006in and for axial probes 0.063in in diameter.
- A recent development[1], is a Hall-effect magnetic field detector for translating information on the polarity and field strength of a magnetic field into a differential output current using integrated circuit technology (Mullard TCA450A). This device offers a high level of sensitivity, low offset flux and is self-balancing. Typical supply voltage 4-16V. Magnetic sensitivity 0.4V/Tesla. Offset flux density $\pm 7.5 \times 10^{-3}$ Tesla.
Possible applications include isolated current sensing and control in high current situations, conversion of magnetic quantities into proportional currents, detection of positional movements of a rotating shaft.

- **Current measurement.** Very small alternating and direct currents may be measured by concentrating the flux established around the conductor via the magnetic cylinder shown.

- **Linear displacement transducer.** The Hall device will produce a voltage which is a function of the motion

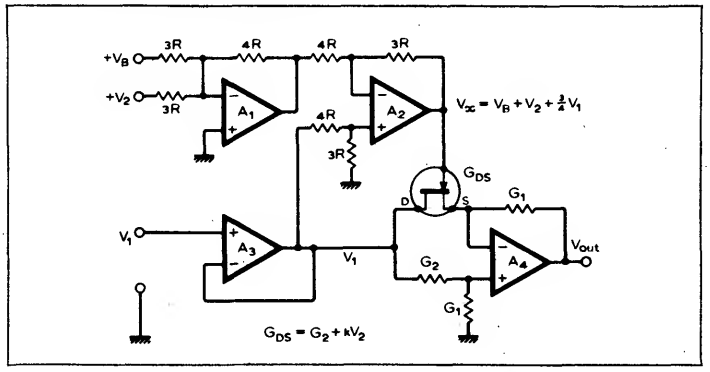


between the device and a stationary magnetic field. Displacement laterally between the magnets will produce an output voltage when the device is moved from the mid-position. An alternative arrangement will provide a linear output proportional to the displacement direction shown. In this case the magnetic field strength varies along a central plane.

- **Proximity detector**
A non-contact proximity switch may detect the presence of a magnetic field or the disturbance of a field due to the presence of ferrous material. Hall voltage, V_z, variation in relation to relative position of magnetic and Hall device would be as shown.

References
Chasmer, R. P., Cohen, E., Holmes, D. P. Design and performance of a Hall-effect multiplier, *Proc. IEE* 106 Part B. Supplement 16, 1959.
Newsome, J. P. Application of the Hall effect. *Electronics & Power*, April 1966.
1. Mullard News Bulletin, 1975.

F.e.t. analogue multiplier



Circuit description

The conductance G_{DS} of the junction field-effect transistor depends on the voltage V_x. To linearize the f.e.t. in its pre-pinch-off region V_x must comprise one half of the sum of the separate drain and source voltages with respect to ground. In this case, that is equivalent to $\frac{1}{2}(V_1+V_1/2)$. The total gate-voltage is then a fixed bias voltage V_B, a signal voltage V_2 and the required $\frac{3}{4}V_1$ is obtained via A_3 and A_2. With then the equivalence of conductances G_1, the output voltage V_{out} is linearly proportional to the product of signals V_1 and V_2, when G_{DS} is equal to G_2 plus an incremental value proportional to V_2. Equating the potentials at the inverting and non-inverting inputs of amplifier A_4 and using the parallel generator concept then

$$\frac{V_1(G_2+KV_2)+V_{out}G_1}{G_1+G_2+kV_x}=\frac{V_1G_2}{G_1+G_2}$$

This gives

$$V_{out}=-\frac{KV_1V_2}{G_1+G_2}$$

The drain current drain-source voltage relationship is

$$I_D \propto (V_G-V_p-\frac{V_D+V_S}{2})V_{DS}$$

If V_G does comprise V_B, V_2 and $(V_D+V_S)/2$, then $G_{DS}=I_D/V_{DS} \propto (V_B-V_P+V_2)$ for pre-pinch-off.

If the constant of proportionality $K_1=K$, and is such a value that $K_1(V_B-V_p)=G_2$, then a linearised relationship between the output and the product V_1V_2 is achieved.

To demonstrate the principle, the circuit is simulated by Fig. 2, where if $R_4=R_5=6R$, $R_6=R$, then $V_x=\frac{3}{4}V_1+V_2'+V_B'$.

To obtain the best linearity, these values of resistors need to be chosen empirically. This is most easily performed using an oscilloscope with an X−Y facility, where the input V_1 and output for V_2 zero volts are applied X−Y inputs respectively. Any non-linearity or offset can then be minimized by varying the resistors.

A more practical circuit (see reference) includes temperature compensation by making G_2 another voltage dependent conductance, using a matched field-effect transistor (above). For maximum signal amplitudes, f.e.ts with a high pinch-off should provide a wider working range. Also if the gate bias V_B is arranged to be one half the pinch-off value, then

$$G_{DS}=K(-\frac{V_p}{2}+V_2)$$

i.e. $G_2=-\frac{KV_p}{2}$

and if $G_1=G_2$, then

$$V_{out}=-V_1V_2K/2G_2=\frac{V_1V_2}{V_p}$$

Typical pinch-off is −10V for results quoted, but no signal levels are identified.

Accuracies claimed are within ±1% over a temperature range of 50K in the frequency range 0 to 20kHz, using matched f.e.ts whose conductances are within ±5%.

Typical data (simulation)
IC SN741 Tr_1 2N5457
R_1, R_3 330Ω, R_2 1kΩ
R_4, R_5 22kΩ, R_6 6.8kΩ
frequency 1KHz
V_1 maintained at 100mV pk-pk to achieve the best linearity.
Linearity obtained is demonstrated on the graph.

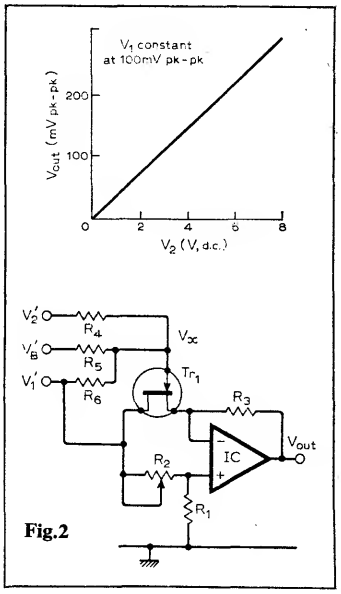


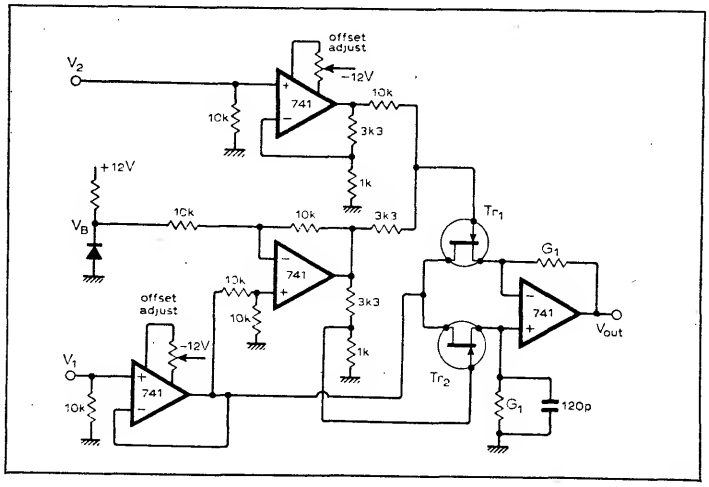
Fig.2

Reference

Miller, A. Temperature compensated analogue multiplier, *Electronics Letters* 9 Sept. 1971, vol. 17, no. 18.

Related circuits

Set 22, card 7



wireless world circard

Set 29: Up-date

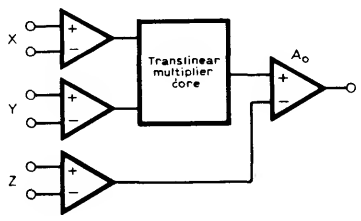
Analogue circuit design is on the edge of another of its periodic revolutions. The development includes analogue multipliers of performance that permits function-synthesis to an accuracy that is limited mainly by the external passive components. One variant has three separate differential-input transconductance amplifiers: two drive a translinear multiplier core whose output is summed with that from the third to produce the final output via a high gain amplifier. The signals are processed throughout in current form but inputs and outputs are voltages with the usual scaling factor so that W =

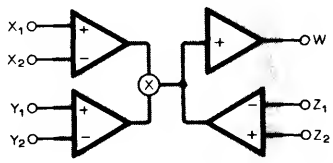
$$\frac{_0(X_1-X_2)(Y_1-Y_2)+Z_2-Z_1}{10}$$

Normally overall feedback together with the large value of A_0 ensures that the bracketed term tends to zero and the implicit identity

$$\frac{(X_1-X_2)(Y_1-Y_2)}{10} = Z_1-Z_2$$

follows. The operation is analogous to that at the summing junction of an op-amp. A similar flexibility is obtained with higher order functions to that which we have become used to in linear





circuit design. To avoid the inconvenience of the scaling factor when devising new configurations it is helpful to write the variables in normalized from x, y, z:

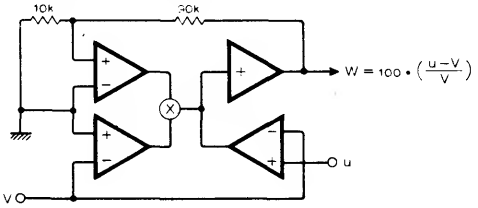
$$(x_1-x_2)(y_1-y_2) = z_1-z_2.$$

To avoid confusion with the terminology of X and Y as multiplier inputs the more general input and output variables are written as U, V and W or u, v, w when normalized.

The reference article offers more than 20 applications many of them novel, and is essential reading for anyone who wants to exploit the possibilities of these new multipliers. At present they are precision devices laser-trimmed and are correspondingly priced but it is to be hoped that designers will overcome these limits and produce them at mass-market costs. A couple of examples indicate the simplicity of the solutions that are made possible by such circuits: at the other extremes more complex configurations are claimed to yield trigonometric conversion functions with accuracies down to 0.01%.

The first circuit implements a percentage deviation computer in which, for two input variables u and v, each of up to 10V, the output is one volt for each 1% difference between the variables

$$W = 100\,\frac{U-V}{V}$$



This is established by observing

$X_1 = W/10 \quad Y_1 = 0 \quad Z_1 = V$
$X_2 = 0 \quad\quad Y_2 = V \quad Z_2 = U$

and substituting the second identity

$$\frac{(W/10)(-V)}{10} = V-U$$

$$W = 100\frac{U-V}{V}$$

The feedback ratio can be adjusted to give 0.1V/% to 10V/% and the only restriction is that V must be positive.

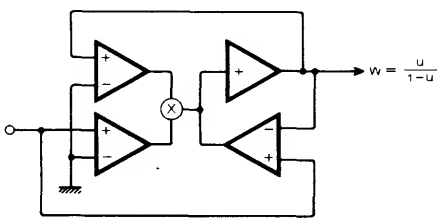
An even simpler configuration has, in normalized form,

$x_1 = w \quad y_1 = u \quad z_1 = w$
$x_2 = 0 \quad y_2 = 0 \quad z_2 = u$

Hence $wu = w-u$ and

$$w = \frac{u}{1-u}$$

This non-linearity is the exact inverse of that associated with a conventional Wheatstone bridge viz u = v/(1+v). Hence a single multiplier can linearize the output of such transducers as strain-gauge bridges. The functions can be implemented by conventional multipliers but may need additional summing amplifiers and inverters, which in turn limit the accuracy and bandwidth claimed ±0.25% and 1MHz with 35V/μs slew-rate.



References

Gilbert, B. New analogue multiplier opens way to powerful function-synthesis, *Microelectronics*, 1976, vol.8, pp.26-36.

Set 30: Non-linear circuits—r.m.s./log/power laws

Familiar mathematical functions—squares, square roots (page 136), cube law, r.m.s. conversion, resolvers, logarithms, frequency doubling (page 132)—are implemented in this set using a variety of techniques, including the use of the integrated multiplier (pages 135 & 140) introduced in set 29. No pretences at high precision are made in these circuits. Typically linearity is 1 or 2%, but as the following article points out errors often vary over the dynamic range because of the non-linear nature of the circuits. Manufacturers should be consulted directly over particular solutions to problems requiring greater precision.
On page 135 the output from the precision rectifier is now correctly shown as being taken from the junction of the R_1-diode series combination. And in connection with Barie Gilbert's circuits, there were two additional brackets needed to enclose the last two terms in the expressions for I_A and I_B.

Introducing non-linear circuits

Logarithmic, power and r.m.s. laws

A growing need for a variety of mathematical function generations has led to a variety of circuit solutions. The problems range from the use of resolvers in servo systems in which sine/cosine function generation is needed, to the measurement of the true r.m.s. value of non-sinusoidal waveforms.

If we restrict ourselves to one or two variables, then Fig. 1 shows a sample of the functions that might occur in practical systems – either because the output of a system is required in some particular form such as a decibel representation of a voltage gain, or to correct for some non-linear property of a transducer. Few of these functions can be obtained directly from existing devices and circuits unless limited accuracy is acceptable. For example, the field-effect transistor has a square-law term in its I_D/V_{GS} characteristic and this has been exploited to provide such functions as X_2 and XY.

However, the circuits have been fairly complex, have resulted in significant departure from the ideal law or have drifted badly with change in temperature and/or supply.

Some of these functions can be obtained by indirect means such as the parametric techniques of Hall-effect devices or varactor diodes. Others can be obtained via modulation processes as in the multiplier/divider circuits of Circards Set 29. The most valuable tool available to the designer in this area is the transistor, not because of its amplifying properties, but because the I_C/V_{be} characteristic follows a particular non-linear law precisely and over a wide range of currents.

In its simplest form that law can be written as: $I_C = k \exp V_{be}$. This hides a number of inconvenient factors such as its dependence on temperature, but is an accurate representation of the shape of the characteristic. As indicated in the previous article this is the basis of logarithmic amplifiers in which the output voltage is a logarithmic function of the input voltage.

From the basic properties of logarithms various power-law operations can be implemented.

one variable	two variables
X^2	XY
$\sqrt{X}$	$\frac{X}{Y}$
$1/X$	$\frac{X^2}{Y}$
aX^2+bX+c	$\sqrt{X^2+Y^2}$
$\log_e X$	$\sqrt{X^2 \quad Y^2}$
e^x	
$\cos X$	
$\sin X$	
$\sqrt{\overline{X^2}}$	

Fig. 1. Common functions that can be obtained by passing X, Y through circuits with corresponding transfer functions.

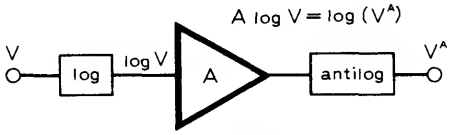


Fig. 2. Logarithmic circuits are based on natural logarithms rather than $\log_{10}$ because of the way diode/transistor characteristics are expressed.

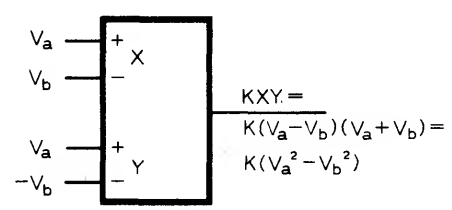


Fig. 3. Circuit produces an output that, after filtering and passing through a square-rooting circuit, would give the vector difference between two input variables. More elegant solutions are available using feedback/feedforward.

Let $V_a = K \log_e V_1$ and $V_b = K \log_e V_2$.

Then $V_a + V_b = K \log_e (V_1 V_2)$ 1

$V_a - V_b = K \log_e (V_1/V_2)$ 2

$nV_a = nK \log_e V_1 = K \log_e (V_1^n)$ 3

Thus adding, subtracting or amplifying the input variables all of which are within the scope of normal linear circuit design, result in outputs that involve the product, ratio or powers of those variables. The remaining problem is that the output is still a logarithmic function; if it is succeeded by an antilog circuit then the process is completed. A typical configuration is shown in Fig. 2.

A second family of circuits makes use of existing functional blocks such as the multiplier *(XY)* or the multiplier/divider *(XY/Z)*. Using various feedback and feedforward configurations, a number of the other functions such as square, square root and division can be performed. As an example, consider the circuit of Fig. 3. It illustrates how complex functions can be built up piecemeal. With care and ingenuity elegant and efficient solutions to such problems can be found using various interconnections to remove the need for additional functional blocks.

A group of four transistors in which the base-emitter voltages have a relationship of the form $V_1 + V_2 = V_3 + V_4$ must result in a corresponding collector current relationship $I_1 I_2 = I_3 I_4$ once the log characteristics are taken account of (see previous article). This leads directly to the implementation of a multiplier by making, say, I_2 constant and forcing I_3, I_4 to be proportional to the two input variables. Other interconnections of these transistors can yield functions such as square, vector sum, and division.

Some novel solutions demand devices not readily available to the average user – devices developed by manufacturers for use in their own instruments.

One such that shows an old idea brought very firmly up-to-date is given in Fig. 4. It uses what is effectively a balanced bridge to determine the true r.m.s. value of an input voltage. If two identical transistors are separately heated by equal resistors then they will remain in balance only if the flow of

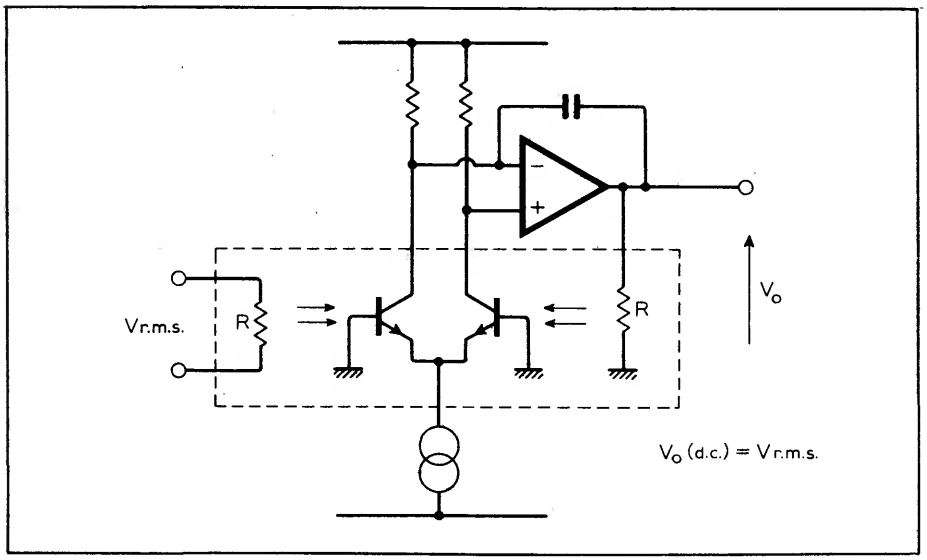


Fig. 4. Two identical transistors are heated separately by resistors supplied from an unknown input voltage and the output of an op-amp. High gain forces the transistors into balance by increasing V_0 until the power it supplies matches that delivered by $V_{r.m.s.}$

heat to each is equal. Any unbalance is amplified by the operational amplifier forcing the direct output voltage to deliver the same power to the right-hand resistor as the input delivers to the other. Hence the r.m.s. values of the two voltages are equal. A neat idea, though one that requires a very carefully constructed chip if the sensing transistors are each to respond to only one of the heat sources.

A severe problem in many of these ideas is that of identifying and neutralizing the error sources. Because of the non-linear equations involved, the relative errors are different at all parts of the range. Manufacturers of modules and i.cs directed at these applications devote a great deal of effort to this topic, and readers would be well-advised to consult them if high-precision functions are needed.

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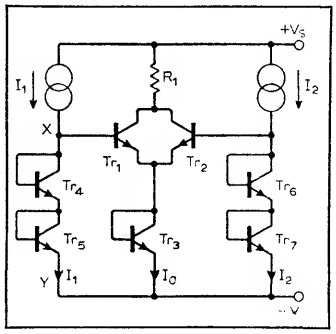
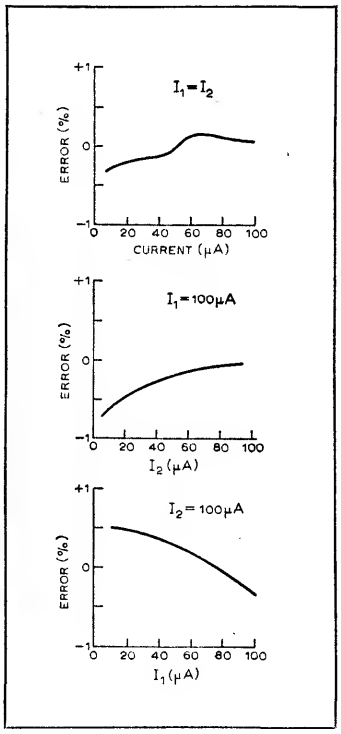
Set 30: R.m.s./log/power laws—1

Root-law array



Typical data
Tr_1-Tr_3 3/5 of CA3086
Tr_4-Tr_7 4/5 of CA3086
Vs ±5V R_1 33kΩ
For graphs, currents I_1 and I_2 are derived from calibrated current sources.
$I_O=\sqrt{I_1^2+I_2^2}$. Percentage error shown in graphs.



Circuit description
This circuit is a special case of a general root law circuit[1], using bipolar transistor-array packages. The performance depends on the fairly precise relationship which exists between the collector current I_C and the V_{BE} of a transistor. Assuming that the common-base current gain $\alpha=1$, then $I_C=k \exp V_{BE}/V\varphi$, where $V\varphi$ is the thermal potential. As $V_{BE}=V\varphi \log I_C/k$, then in the path XY, $V_X=2V\varphi \log I_1/k$ because there are two diodes in series. There is only one diode in the Tr_3 path and hence $V_E=V\varphi \log I_O/k$. I_O can be written in terms of the base-emitter voltage of Tr_1, giving

$$I_O=k\sum_1^m \exp (V_X-V_E)/V\varphi$$

where m is the number of paths like XY.

Hence by substituting for $V_X/V\varphi$ and $V_E/V\varphi$

$$I_O=\sum_1^m k\,(I_1/k)^2.\,(k/I_O)$$

$$=\sum_1^m I_1^2/I_O$$

giving $I_O=\left[\sum_1^m (I_1)^2\right]^{\frac{1}{2}}$. Above, $m=2$, $I_1=I_2$ and $I_O=(I_1^2+I_2^2)^{\frac{1}{2}}$. Current flow directions of I_1 and I_2 should be as shown. If these currents are to be derived from an alternating voltage source, then circuits must be provided to ensure the above polarities are maintained.

Circuit modifications
- The circuit has been used as a frequency doubler[2] dependent on a similar mathematical relationship, and in this case, a sinusoidal input voltage drives current into the circuit of Fig. 2 to obtain unidirectional current flow, which is independent of the load. Current i_1 is drawn from the current mirror Tr_8, Tr_9 in the same direction no matter the polarity of i_{in}. When i_{in} is positive-going, the current mirror comprising transistors Tr_{10} and Tr_{11} is active, and the resulting collector current of Tr_{11} is mirrored by Tr_8, Tr_9. When therefore i_{in} is negative-going, an equivalent current is delivered by current mirror Tr_{12}, Tr_{13}. P-n-p transistors are required for those current mirrors and are obtained in the CA3084 i.c. A voltage output is available via R_1.
- An alternative arrangement for obtaining unidirectional current is shown in Fig. 3 using an inverting amplifier, and a complementary pair in the feedback loop. This avoids the crossover distortion that may exist in the Fig. 1 arrangement due to the finite V_{BE} drops of transistors Tr_{10}, Tr_{12}, though if $v_{in} \geqslant 0.6V$ this effect might be acceptable. The resistors R_3 and R_4 must be closely matched to optimise the current mirror action. RV_1 of Fig. 4 replaces R_3, R_4 and allows an alternative manual adjustment to match the collector currents.
- Another arrangement using the translinear multiplier[4] concept is shown in Fig. 5. While this may be a configuration more likely met in a i.c. multiplier, transistor-array packages could be used, with Tr_{16}, Tr_{17} being implemented by paralleling transistors.

Further reading

1 Barker, R. W. J. and Hart, B. L., *Electronics Letters* vol. 10, 1974, pp. 439/40.
2 Barker, R. W. J., *Electronics Letters* vol. 11, 1975, pp. 106/7.
3 Barker, R. W. J. and Hart, B. L. *Journal of Physics E.* vol. 8, 1975, pp. 721/2.
4 Gilbert, B. *Electronics Letters* vol. 11, 1975, pp. 14-6.

Related circuits
Set 30, cards 10, 5.

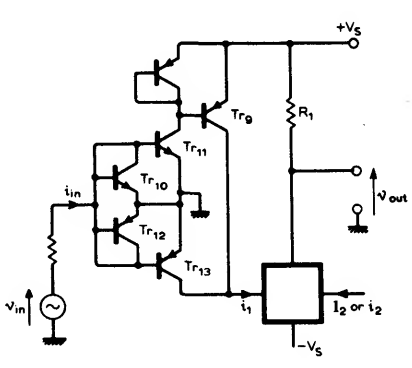


Fig. 2

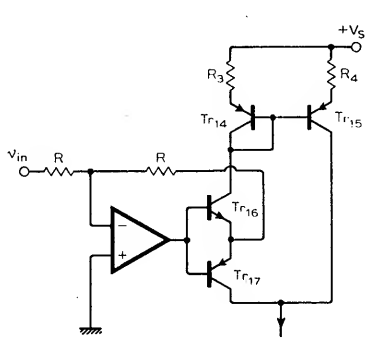


Fig. 3

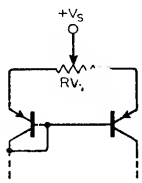


Fig. 4

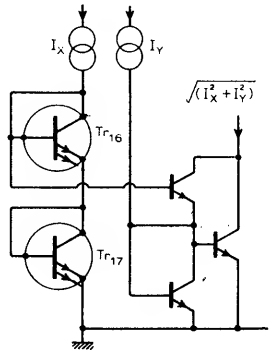


Fig. 5

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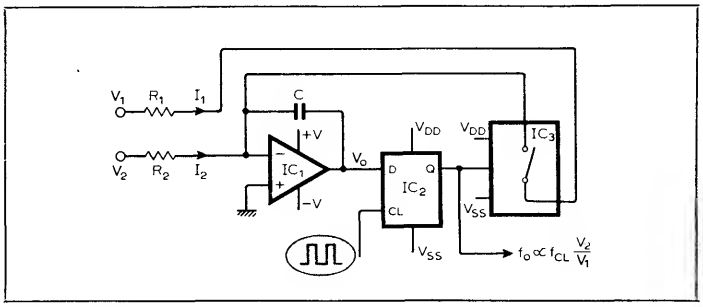
Voltage divider

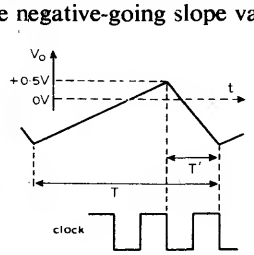


Typical performance

IC_1 741 op-amp ±7.5V supplies
IC_2 ½ of CD4013, D-type flip-flop
IC_3 ¼ of CD4016 f.e.t. switch
V_{DD} +7.5V, V_{SS} −7.5V
Clock pulses 3V pk-pk square wave, mean value zero, frequency 10kHz.
V_2 −7.5V, V_1 positive
R_2 1MΩ, R_1 100kΩ
C 2.2nF

Circuit description

Voltage V_2 is a negative voltage which will cause the integrator IC_1 to ramp positively. The slope of this is slow since R_2 is large. When I_1 is permitted to flow to the summing junction (f.e.t. switch of IC_3 closed), the op-amp will ramp downwards provided $I_1 > I_2$. In ramping downwards V_O will go below the threshold level of the D-type flip-flop IC_2 and on the occurrence of the next negative going edge of the clock Q will go low, the switch will open; I_1 is thus cut-off and the op-amp will begin to ramp positively again. This will continue until D is high on the trailing edge of a clock pulse when I_1 will again be switched in. The trace above shows a typical V_O (IC_1 output). The lower level of this waveform varied somewhat (from −2V for a large V_1 to −0.25V for a small V_1). The slope of the positive ramp is, of course, constant for constant V_2 but as V_1 is varied the negative-going slope varies.



Clearly in a complete period T the charge put in by V_2 is cancelled by the charge withdrawn by V_1 as the starting and finishing voltages are the same.

i.e. $I_2 T = I_1 T'$

$$\frac{1}{T} = \frac{I_2}{I_1 T'} = \frac{V_2}{V_1}\frac{R_1}{R_2}\frac{1}{T'}$$

i.e. $$f_o = \frac{V_2}{R_2}\frac{R_1}{V_1} f_{CL}\frac{1}{V_1}$$

Hence, if R_1, R_2, and the clock frequency are constant we obtain a frequency proportional to V_2/V_1.

We fixed V_2 at −7.5V for convenience and varied V_1. For V_1 in the range 1.5V to 6.5V the frequency f_o varied from 865Hz to 3472Hz, the product $V_1 f_o$ remaining constant within 0.2% proving the division to be accurate.

Note that T′ need not be one clock period as shown but will be an integral multiple of the clock period. Furthermore, in our description we have implied that the switching level of the D-type flip-flop is zero volts and this need not be so.

Component changes

With the values of R_1 and R_2 quoted, C, which does not appear in the expression for f_o, can be varied over a range of about 10:1. Low values of C cause saturation of IC_1 before the flip-flop changes state and high values caused what appeared like subharmonic locking of some sort. This might have been obviated by use of a lower clock frequency.

Changing R_1 to 10kΩ, R_2 to 1MΩ and C to 22nF made little difference to the results. One would expect R_2 max to be of the order of 1MΩ to prevent op amp input currents affecting the operation although since this is a constant effect it should not seriously affect the frequency of oscillation. The lower limit to R_1 is set by the fact that the on resistance of the f.e.t. switch is approximately 300Ω i.e. $R_1 \gg 300\Omega$.

The max. V_2 is not seriously limited but V_1 is limited to be less than V_{DD} − the positive supply of the c.m.o.s. f.e.t. switch IC_3.

Circuit modifications

- In essence we have been supplying voltage-controlled currents I_2 and I_1 to the integrator. There are several ways of doing this (e.g. ref. 1). One method is as shown below in which the two dotted sections are accurate voltage to current converters, i_1 for example being V_1/R_1. This circuit is very similar to the one shown above with the addition of an inessential comparator but has the disadvantage that V_2 is referred to V_S. This can be modified so that V_2 is referred to ground (refs 2, 3).

Note that f_o is proportional to the ratio of two voltages, the numerator one in our case being fixed. Many v-f converters operate on the same principle but keep the denominator term fixed. Such v-f converters therefore can be converted to act as divider circuits. In fact the circuit shown above is identical to the delta-sigma voltage-to-frequency converter on card 3, set 21.

- Another such v-f converter is the simple unijunction v-f converter (card 1, set 21).

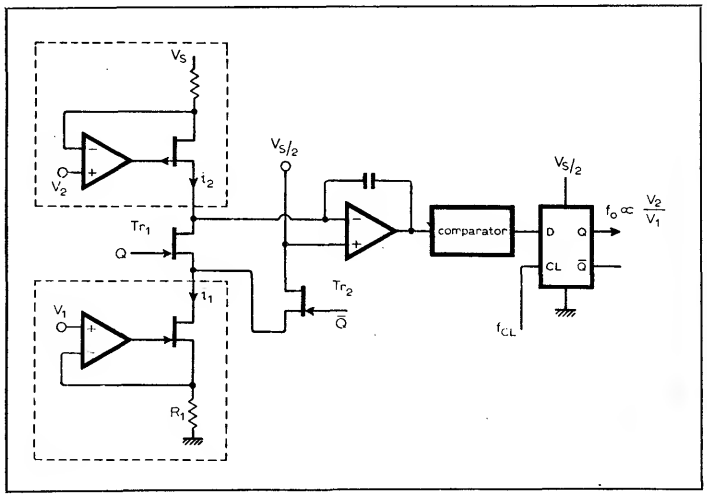
Many multipliers require not only the two voltages to be multiplied but a reference voltage which appears in the denominator of the output voltage expression e.g. set 29, card 4.

References

1 Set 6, Constant-current circuits, card 1.
2 Ljung, E. Accurate wide range analog multiplier, *Electronic Engineering*, July 1975.
3 Alusten, B. and Ljung, E. Accurate voltage dividing circuit, *Int. J. Electronics*, vol. 39, pp. 353-6, 1975.

Related circuits

Set 21, card 3
Set 29, card 4



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Ramp to sinewave converter

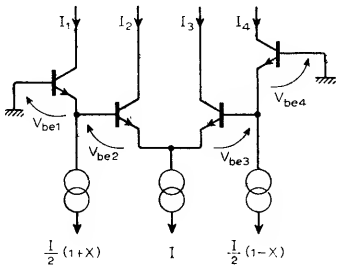
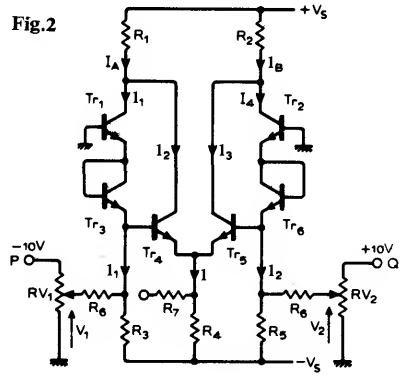
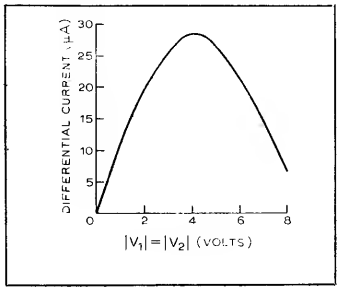


Fig. 1

Fig.2



Typical data
Tr_1, Tr_2 2/5 of CA3086
Tr_3–Tr_6 4/5 of CA3086
V_S ±10V
R_1, R_2 47kΩ, R_3–R_8 100kΩ
RV_1, RV_2 10kΩ
Above values are chosen to simulate the current-source relationships indicated in Fig. 1 and provide the d.c. characteristic shown in the graph



Circuit description
The circuit is based on the translinear circuit of Fig. 1. Currents I, $(1+X)I/2$, $(1-X)I/2$, are controlled current sources, and the values are chosen to have a specific relationship. It is assumed that all the transistors are matched (Tr_1, Tr_2 must be on the same chip, and also Tr_3–Tr_6). Summation of the base-emitter voltages in Fig. 1 gives

$$V_{BE_1}+V_{BE_2}-V_{BE_3}-V_{BE_4}=0.$$

Because the collector currents are of the form $I_C=I_S \exp qV_{BE}/kT$ then by substitution

$$(kT/q)\times\left[\log\frac{I_1}{I_S}+\log\frac{I_2}{I_S}-\log\frac{I_3}{I_S}-\log\frac{I_4}{I_S}\right]=0$$

and hence $I_1 I_2=I_3 I_4$. Hence any one current can be chosen to be a dependent output current. In Fig. 2, an extra diode in each branch means an additional V_{BE} drop must be considered, and the current relationship is then

$$I_1^2 I_2=I_3 I_4^2$$

With $I_1=(1+X)I/2$, $I=I_2+I_3$, $I_4=(1-X)I/2$ it is easily shown that

$$I_A=I_1+I/[(I_1/I_4)^2+1]$$
and $$I_B=I_4+I/[(I_4/I_1)^2+1].$$

Hence the differential current

$$I_A-I_B=IX\frac{(1-X^2)}{(1+X^2)}$$

With $-1<X<1$, this difference-current is claimed to approximate a sine function within ±0.4% full-scale. Over the range of control voltages used above ($V_1=V_2=0$ to 10V) the differential current is acceptably sinusoidal over half the range.

Circuit modifications
- Fig 3 permits zero-setting of the differential current when factor $X=0$.
- If terminals P and Q of Fig. 2 are driven from a ramp-function generator, via an inverting amplifier, then opposing ramp control voltages will produce a sinusoidal output in accordance with the first half of the graph over. The ramp inputs must be such a level to reach the point of inflexion of the curve, in this case about 4V.
- To obtain a single-ended voltage output from a differential current-input, a subtracting circuit such as Fig. 5 can be used, but in this case, matching of resistors R is necessary.
- An alternative differential current-to-voltage converter is achieved using the current mirror of Fig. 6. Resistor R_2 must be trimmed to optimise current-mirror action. If balancing is such that $I_1=I_2$, then for zero voltage output, I_3 must equal I_1. Typical performance of this circuit provides a symmetrical 5.8V pk-pk cisoidal output for a 4V drive ramp signal. Maximum frequency 3.5kHz, when slight peak distortion may be encountered. Harmonic distortion is in fact quite small. Figures are quoted for a 1kHz drive signal.

2nd harmonic	−45dB
3rd harmonic	−43dB
4th harmonic	−70dB
5th harmonic	−65dB

Further reading
Gilbert, B. Translinear circuits: a proposed classification, *Electronics Letters*, vol 11, pp. 14-6.
Errata to above: *Electronics Letters*, vol. 11, p. 136.

Related circuit
Set 29, card 8.

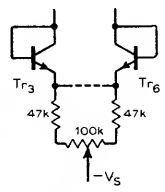


Fig. 3

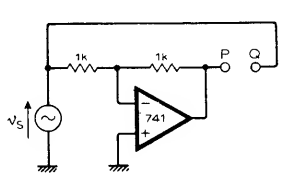


Fig. 4

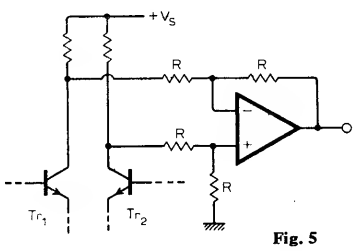


Fig. 5

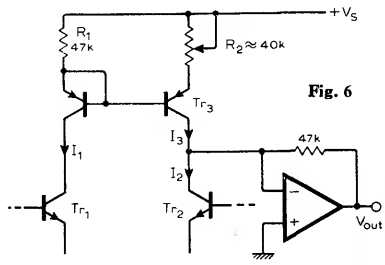


Fig. 6

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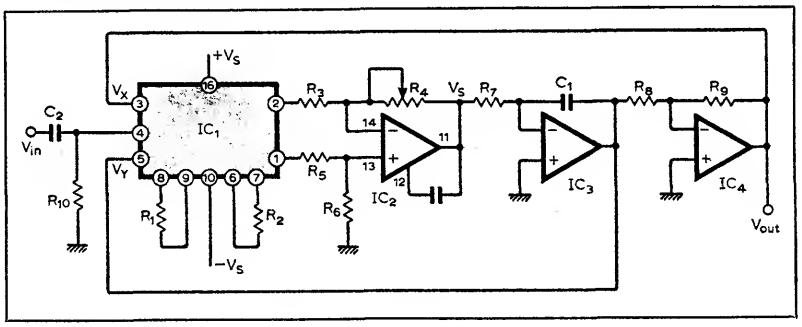
r.m.s. to d.c. converter



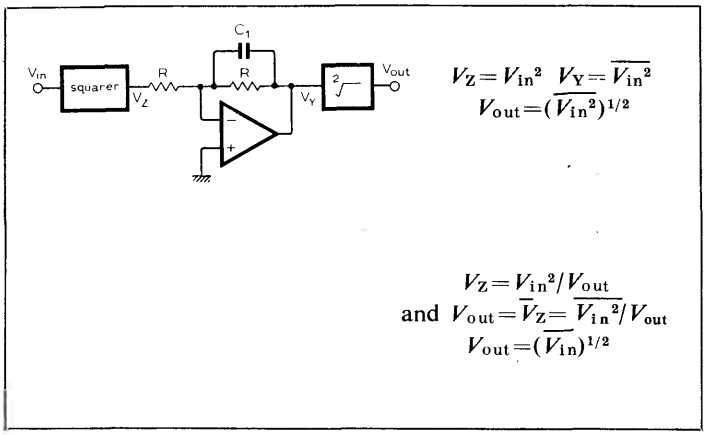
Typical data
IC_1 XR2308 V_S ±10V
IC_2 (included in IC_1)
IC_3, IC_4 SN741, R_{10}, R_7 47kΩ
R_1, R_2 22kΩ, R_8, R_9 10kΩ±0.1%
R_3, R_5 56kΩ, R_6 100kΩ
R_4 100kΩ potentiometer
V_{in} 1-5V r.m.s. C_1, C_2 1μF
frequency 1kHz
V_{out} 1-5V d.c.

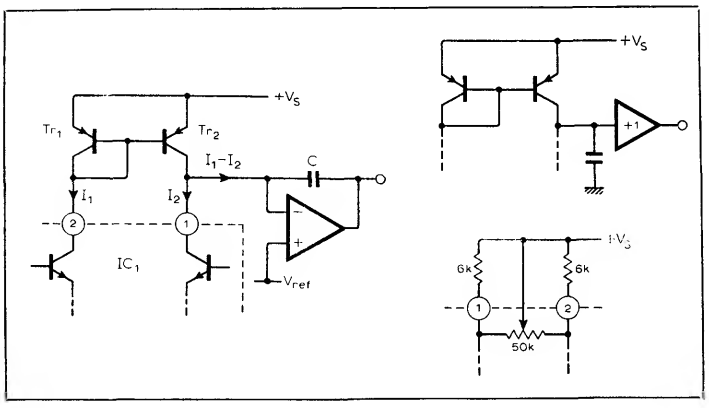
Circuit description

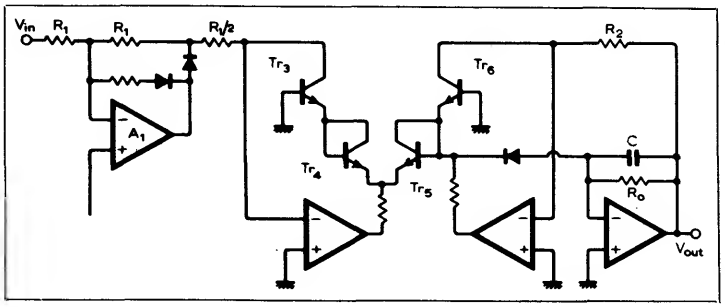
This circuit is based on an approach implemented in ref. 1, via an argument based on the explicit (Fig. 1) and implicit methods of establishing the r.m.s. value of a signal (Fig. 2). Notice that the squarer divider would require a device that would give an *XY*/Z output for X, Y, Z inputs (type AD433J). In each case, the integrator filters the fluctuating d.c. signal. The arrangement above is based on a i.c. multiplier. IC_2 is connected as a subtractor to provide a single-ended output from the differential output currents of the multiplier section of the i.c. This is then proportional to the product $(V_{in}-V_{out})(V_{in}+V_{out})$ i.e. $(V_{in}^2-V_{out}^2)$. Under steady-state conditions, the d.c. feedback via V_X and V_y will force the mean value of this voltage, V_S, to be zero, any a.c. components being filtered by IC_3. Hence $V_{out}=(\overline{V_{in}^2})^{1/2}$
Initial setting up of the circuit to obtain the output equal to the input requires adjustment of R_4 which may shift the output zero level for $V_{in}=0$. Zero adjustment is obtained via the circuit of Fig. 3, though further adjustment of R_4 may be necessary, etc. The inverting-gain amplifier must be precisely −1, either by trimming or using accurate values of R_8, R_9.

Circuit modifications

- If pins 1 and 2, 3 and 5 are reversed, a negative d.c. output can be obtained without loss of accuracy.
- If terminals 1 and 2 (see Fig. 4) are connected to a current mirror comprising transistors Tr_1 and Tr_2, then the integrator may be driven directly without using the internal op amp, or this may be used as the integrator. The reference potential of the non-inverting input cannot be grounded, it must be maintained fairly positive to ensure it's within the range of potential of terminal 1.
- Another possibility is shown in Fig. 5, where because the current mirror is a current source, the capacitor can be connected directly and the output derived from a unity gain non-inverting amplifier. Fig. 6 (ref. 2) is an example of the implicit method of conversion, where A_1 amplifier is arranged as an absolute rectifying circuit and transistors Tr_3-Tr_6 form a transconductance multiplier. To implement the circuit it is essential to optimise the frequency response and compensate for the limitations of the op-amps and transistors and some design guidance is given in the reference.







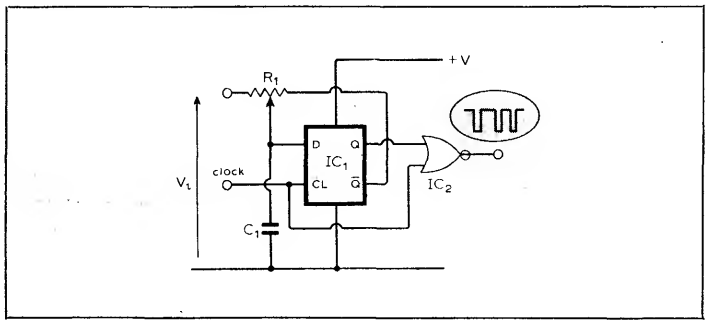
Further Reading

Gilbert, B. RMS-DC Conversion, *Electronic Letters*, vol. 11, 1975, p.181.
Handler, H. True r.m.s. voltage conversion, *Electronic Design*, vol. 4, 1974, pp. 66-72.

Related circuits

Set 30, cards 9, 3.

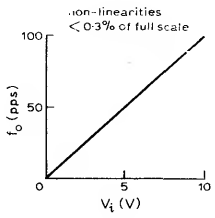
D-type delta-sigma converter



Typical performance

IC	½ of CD4013AE
IC_2	¼ of CD4001AE
Supply	+10V
R_1	100kΩ pot
C_1	10nF
Clock freq.	100kHz
V_i	0-10V
f_o	$\propto V_i$

Note $\frac{f_o}{f_{clock}} \approx \frac{V_i}{V_S}$



Circuit description

The delta-sigma modulator is a powerful tool in the processing of signals. Conceptually it requires a number of different sections: a D-type flip-flop, an analogue gate, a reference voltage, a comparator, an integrator. Previous designs have combined the functions of gate, reference and comparator into the flip-flop itself, using the facts that (i) the threshold level of the flip-flop is sharply defined, obviating the need for a comparator in simple applications (ii) the gate/reference section is only required to define the feedback during the pulse on-state. This is achieved for a stable supply voltage by direct feedback from the Q output since c.m.o.s. outputs switch virtually to supply levels.

This leaves the op-amp integrator as the only analogue element in the svstem. If the feedback is taken from the $\bar{Q}$ output to the D-input with a capacitor to ground then a virtual-earth action is achieved without the need for an operational amplifier. This remarkable simplification has one drawback—the virtual earth has an offset voltage equal to the threshold voltage of the D-type flip-flop. This varies from device to device but is (i) a relatively fixed fraction of the supply (ii) varies little with temperature. Without any precautions, and setting R_1 to its centre value, the output pulse rate has an average value that is a linear function of V_i (typically to much better than 1%). It is possible to remove the offset by the configuration shown. If the clock pulse together with the Q output is fed to a NOR gate, then when the input voltage is low the D-input will tend to drop. Once below the threshold the clock pulses keep $\bar{Q}$ high raising the D-input again. The $\bar{Q}$ output will need to be high most of the time. This implies that Q is only high occasionally and few pulses are obtained at the output—a direct representation of the low input voltage assumed. Set V_i to zero and adjust R_1 until the output pulses are just barely inhibited. The setting is generally close to the centre-tap because the threshold is around $V/2$. This zero-setting varies the slope of the characteristic so that sensitivity controls must be adjusted after zero-setting.

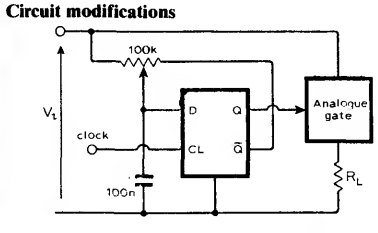
Circuit modifications

- The basic circuit is a tool that can be used to implement square, square-root and multiplier functions.
- **Squaring circuit**. The flip-flop is set up for $f_o = kV_i$ as above. V_i is also applied via an analogue gate to the load. Hence the mean load voltage is proportional to $(V_i)^2$—the voltage of magnitude V_i is applied to the load for a fraction of the time proportional to V_i. In this mode the output pulses are not used directly and the NOR gate is not needed—unless transmission of the original variable V_i in serial form is desired.
- **Square root circuit**. This is achieved by the implicit method. Q, $\bar{Q}$ gate the analogue switches, but R_3 C_2 smooth the $\bar{Q}$ output so it is the mean value at $\bar{Q}$ that is gated. Hence the mean voltage applied to R_2 is a function of the square of the mean output. If the input is applied with respect to ground the output is obtained from $\bar{Q}$ to the negative line. (The smoothed version across C_2 can be used directly if a high resistance is used). $V_o \propto \sqrt{V_i}$.
- If positive supply/input operation is desired the gating is reversed and the output taken with respect to the positive rail.
- If the output is required as a pulse train, simply gate $\bar{Q}$ and the clock pulses with a NOR gate and the output pulse rate is proportional to $\sqrt{V_i}$. When the initial zeroing has been correctly carried out, the square and square-root laws are followed with errors of <1% of full-scale. As noted earlier the scaling factor is affected by the zero-setting.

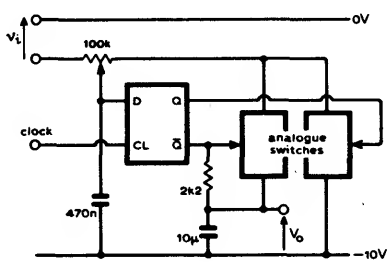
Related circuits

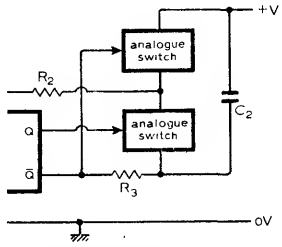
Set 30, cards 1, 10
Set 29, card 3

Circuit modifications



squaring circuit





square-root circuit

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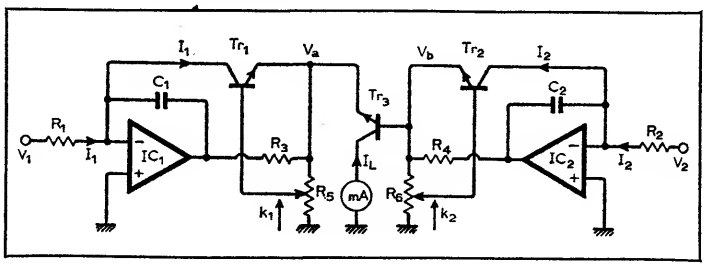
Cube-law generator



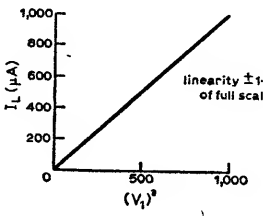
Components

R_1, R_2 10kΩ
R_3, R_4 220Ω
R_5, R_6 1kΩ
C_1 100pF, C_2 1nF

IC_1, IC_2 741
V_S ±10V
Tr_1, Tr_2, Tr_3 1/5 of CA3086
k_1 0.667 k_2 0.5

Performance

With V_1 at 10V, V_2 was adjusted so that I_L=1mA, achieved with V_2=8.65V. V_1 was then varied and produced the graph of I_L versus V_1^2 shown.



Circuit description

In the following equations the subscripts 1, 2, 3 refer to transistors Tr_1, Tr_2 and Tr_3 respectively

$V_{be1}=k_1V_a-V_a=(k_1-1)V_a$
$\therefore V_a=-V_{be}/(1-k_1)$
Similarly $V_b=-V_{be2}/(1-k_2)$.
Writing $1/(1-k_1)$ as n and $1(1-k_2)$ as m one obtains
$V_{be3}=V_b-V_a=nV_{be1}-mV_{be2}$
In general $V_{be}=(kT/q)\log I/I_S$, which results in

$$I_L=I_S\frac{V_1^n}{V_2^m}\frac{R_2^m}{R_1^n}\frac{1}{I_S^{n-m}}$$

As I_S is temperature dependent one can achieve some temperature compensation by maintaining $(n-m)=1$. Temperature dependence due to the kT/q terms is eliminated if all the transistors are at the same temperature.

Components R_3, R_4, C_1 and C_2 do not enter into this analysis. They are used to reduce the loop gain round the i.cs so that instability, which is always a problem with these circuits, does not occur. Previous experience suggested that both C_1 and C_2 should be 100pF but on this occasion for reasons unknown this was not so.

Note that the transistors used obey the log law most closely at currents below 1mA. This constrains R_1 and R_2 to be dependent in large measure on the values of V_1 and V_2. Furthermore, the op amp input currents will have an appreciable effect if I_1 and/or I_2 are less than 1μA.

Note also that for cube law generation $V_a=3V_{be}$ and $V_b=2V_{be}$. As V_a is the larger we examine its effect on the op-amp output current. If $V_a=3V_{be}$ (i.e. about 2V) then the op-amp must deliver I_1 to Tr_1 and current $(=V_a/R_5)$ to R_5. Hence to avoid current saturation R_5 has to be large (e.g. R_5=100Ω is too low). On the other hand, if R_5 is a potentiometer one requires that the transistor base current is negligible compared with the current through R_5, otherwise the voltage on the pot. arm will not be k_1V_a. This indicates the need for a low value of R_5. If the current gain of the transistors is taken as 50 then the value of 1kΩ for R_5 is about the maximum useful.

Accuracy and range of circuits such as this is much affected by operational amplifier offset voltage, bias current and offset current. Op-amps such as the LM108 or a f.e.t. input stage op-amp such as the CA3130 are preferable to 741s.

Circuit modifications

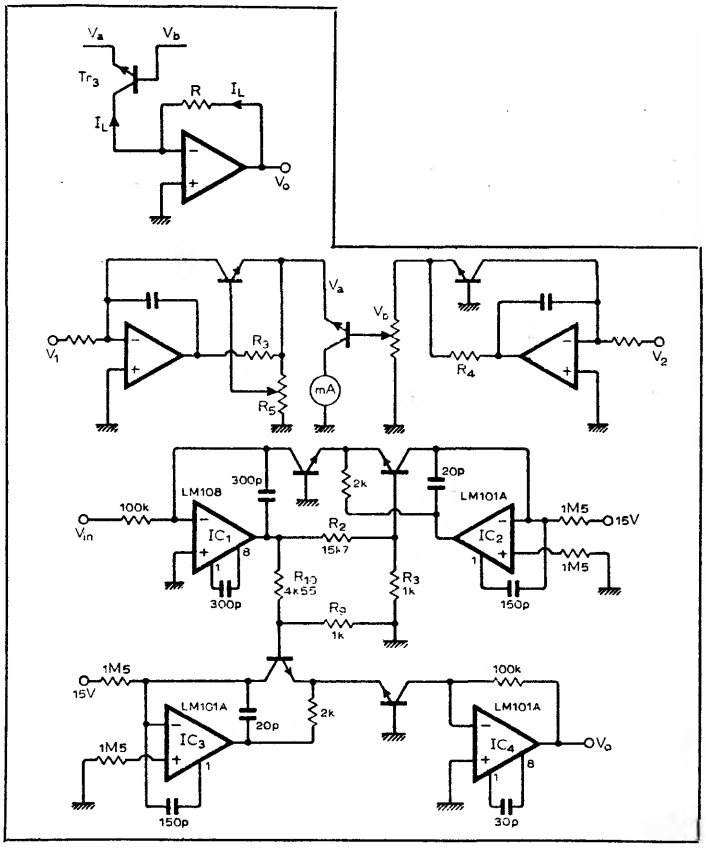
● If one requires a voltage output rather than a current output then the modification above will suffice. V_O is given by $V_O=I_L.R$ where I_L is the current in Tr_3.

The circuit is described as a cube generator, but from the expression for I_L it is clear that any power law can be generated, with the provisos that $n-m=1$ for temperature compensation, and that n an m are both greater than 1. This allows one to obtain $V_O=V^{-2}$ but keeping V_1 constant and using V_2 as the input ($n=3, m=2$), but does not allow one to obtain fractional power laws. This can be overcome by implicit power law generation i.e. by putting a power law device $y=x^k$ (y output, x input) in the feedback path of an op-amp so that $V_O=V_{in}^{1/k}$. A partial alternative is to modify the original circuit so that instead of $V_a=nV_{be1}$, $V_b=mV_{be2}$ where n and m are greater than 1 one obtains the same form for V_a and V_b but with m less than 1. Such a modification is shown centre. This enables one to obtain negative fractional indices. Positive fractional indices with temperature compensation cannot be obtained in this way.

The circuit shown bottom is a cube law generator (Ref. 1). More generally $V_O=V_{in}^a$, where $a=16.7R_9/(R_9+R_{10})$ so that one can obtain any positive power law. Like the original circuit two transistors are fed from potentiometers (R_2-R_3, R_{10}-R_9). The circuit is very similar to the multiplier in ref. 2.

References

1 National Semiconductor application notes AN30.
2 Set 29, card 4
Set 30, card 7



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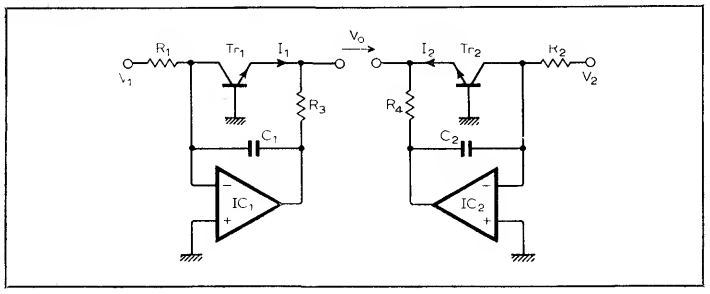
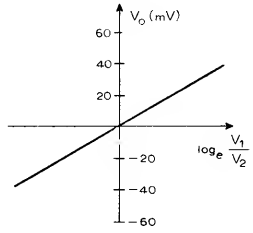
Logarithmic amplifier



Components
R_1, R_2 10kΩ
R_3, R_4 2.2kΩ
C_1, C_2 100pF
IC_1, IC_2 741 ±7.5V supplies
Tr_1, Tr_2 1/5 of CA3086

Performance
With V_2 set at 0.25V the graph shown was obtained. Origin corresponds to V_1=0.25V, slope is 17.8mV/octave and



range of V_1 two decades, from 0.03V to 4.0V. Linearity better than 1%.

Circuit description
The following equations can immediately be given

$V_O = V_{be1} - V_{be2}$

$V_{be1} = \frac{kT}{q}\log_e\frac{I_1}{I_S}, V_{be2} = \frac{kT}{q}\log_e\frac{I_2}{I_S}$

$I_1 = \frac{V_1}{R_1}, I_2 = \frac{V_2}{R_2}$

Hence $V_O = \frac{kT}{q}\log_e\frac{V_1}{V_2}$

i.e. if V_2 is held constant then Vo is proportional to the log of V_1. At room temperatures $kT/q \approx 26$mV and for any octave change in V_1/V_2, Vo will change by approximately 18mV.

Inclusion of R_3 and C_1 around IC_1 and of R_4 and C_2 around IC_2 prevents oscillation of the amplifiers. Considering IC_1, the loop gain includes the transistor gain.
The transistor Tr_1 is in common-base mode and hence has a voltage gain $g_m R_1$, R_1 being the load on Tr_1 and is by superposition connected to ground. The loop gain can be very high. Resistor R_3 reduces the proportion of the output voltage fed to Tr_1 and hence reduces the gain. Likewise, high frequency gains are reduced to zero by the inclusion of C_1 across the amplifier.

Despite these safeguards the circuit does have a tendency to oscillate and care must be taken with wiring. Note that the transistor g_m is linearly related to the current so the problem is increased for high current levels. Further, at high current levels bulk resistance effects in the transistor come into play and destroy the simple logarithmic relationship. It is, therefore, important to keep V_1/R_1 and V_2/R_2 to levels which the transistors will accept.

Circuit modifications
Methods of temperature compensation using transistor arrays have recently been reported, refs. 1, 2. A simpler method has been devised using two of the transistors in the CA3086 package so that a controlled temperature can be achieved in this package at the same time as using two of the remainder for the logarithmic amplifier. Details will appear in a future set. The circuit shown above acts in a manner very similar to the basic circuit overleaf. It is easy to show that

$V_O = \frac{R_3 + R_4}{R_4}(V_{be2} - V_{be1})$

from which

$V_O = \frac{-kT}{q}\left(\frac{R_3 + R_4}{R_4}\right)\log_e\left(\frac{V_1 R_2}{R_1 V_2}\right)$

Note that Vo is now referred to ground potential. Further, if $R_3 \gg R_4$, and if R_4 is a temperature-controlled resistor, then compensation is possible. As T is in Kelvins, Vo will change by 0.33% per deg. C.

This circuit with the bias and compensation networks shown is described in some detail in ref. 3. It is claimed to have a dynamic range of 100dB. The circuit is slow, the output typically taking several milliseconds to settle within 1% of final value. The LM108 does not have great bandwidth but does have a low input current, making it suitable as an input stage. To speed up the system by replacing the LM108 by an LM101 requires some modification, shown above right. The LM102 is connected as a voltage follower so that the combination of LM102 and LM101A with Tr_1 in the feedback path is the same as that of the figure on the left expect that the LM102 effectively diode connects Tr_1. This reduces the dynamic range (80dB is possible) but allows feedforward compensation on the LM101A, thereby increasing the speed of response by about two orders of magnitude. Very little current will flow through the 1kΩ resistor between the output of the LM102 and the LM101A and the input terminal of that LM101A is a virtual earth so that

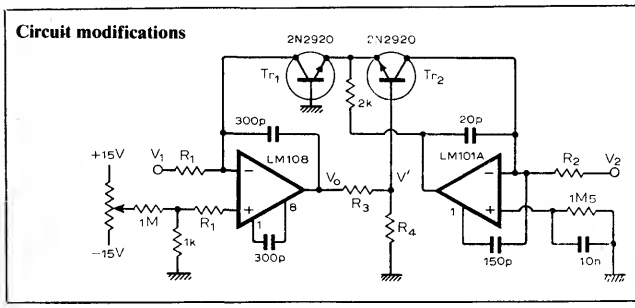
$V_O = \frac{R_3 + R_4}{R_4}(V_{be2} - V_{be1})$

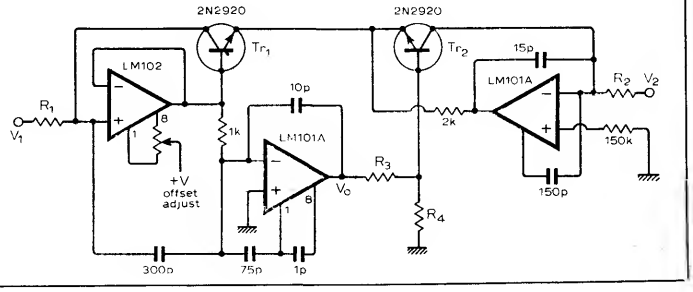
For further details see ref. 3.

References
1 Shah, M. J. Using transistor arrays for temperature compensation, *Electronics*, April 12, 1973, p. 103.
2 Shah, M. J. Self-regulating temperature stabilised reference, EDN, May 20, 1974, pp. 74-6.
3 National Semiconductor application notes AN30.

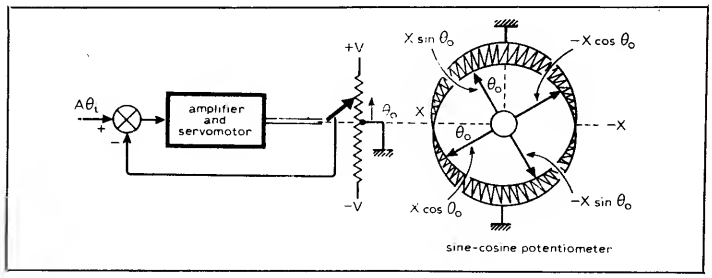
Related circuits
Set 29, card 4
Set 30, card 6

Circuit modifications





Resolvers



A resolver is a device which with input v produces an output proportional to sin v or cos v: frequently both outputs are available giving $a = R\sin v$ and $b = R\cos v$ i.e. the vector $R \angle v$ is resolved into its two rectangular components. These devices are used widely in navigation and range instrumentation, where high bandwidth is not required. The circuit above left consists of a simple servomechanism which will rotate through θ_o degrees in response to some input. If $A = 1$ then $\tau_o = \theta_i$ in the steady state in response to a step.

In addition to the normal feedback potentiometer there is also attached to the shaft a sine-cosine potentiometer generally wound through 360° and having four slider arms as shown. The shaft of this potentiometer will rotate through the same angle as the output shaft. Such arrangements suffer from all the usual disadvantages of potentiometers, wear, resolution, accuracy, etc. By using a gear box between motor shaft and sine-cosine potentiometer shaft one can improve the accuracy and resolution to less than 0.5% (static). Use of a gear box requires scaling of the input to suit. Dynamic accuracy depends largely on the servomotor.

In the induction resolver (below) the sine-cosine potentiometer is replaced by an induction machine shown, having a stator winding and two mutually perpendicular rotor windings. The device is best regarded as a transformer, the output voltages being generated in the rotor windings by induction. The angle θ shown in the output expression is the angle between the axes and is obtained by the servo arrangement shown left or by any other equivalent. The carrier frequency is usually 400Hz. Induction resolvers have the considerable advantage of being relatively maintenance-free since there are no rubbing contacts, apart from slip rings. The main problem is the production of an accurate modulation/demodulation system.

By the addition of a second stator winding with input X, perpendicular to that shown one can obtain outputs

$U = -X\sin\theta + Y\cos\theta$

$V = X\cos\theta + Y\sin\theta$

which enable one to perform co-ordinate transformations.

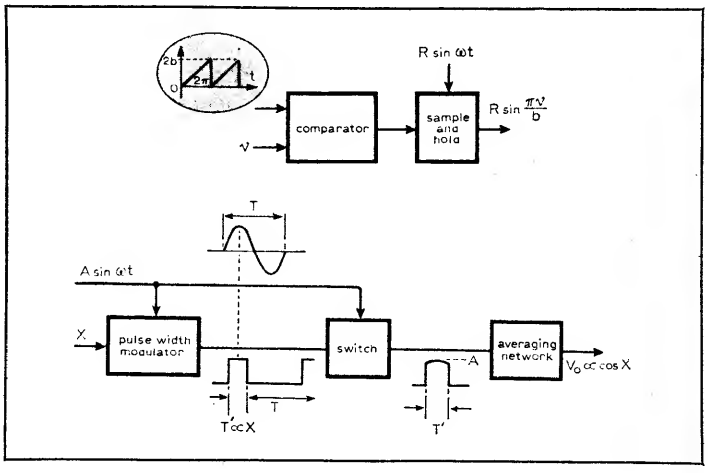
Electronic resolvers are not so common as the electromechanical types. The most common type is that using a diode function generator as described in the quarter squares multiplier card (set 29, card 1). The cost of such a resolver depends on the range of input being considered, the simplest being that corresponding to 0°→90°.

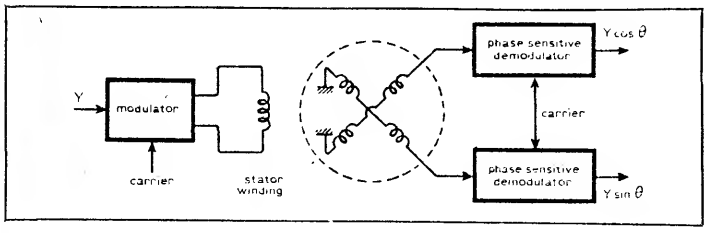
The diagram below (top) shows a different approach which conceptually is very simple. A comparator is arranged to trigger a sample and hold circuit when its sawtooth input exceeds v. It is essential that the sawtooth be synchronous with the input to the sample and hold circuit. This can be done fairly simply by generating the sawtooth from an integrator with a direct input voltage. This produces a ramp output voltage which has to be reduced to zero every 2π radians. This can be done by inserting a f.e.t. in parallel with the feedback capacitor and triggering the f.e.t. from a monostable fed from $R\sin\omega t$ via a comparator.

If $R\sin \pi v/b$ and $R\cos \pi v/b$ are required simultaneously then one can use two sample and hold circuits, both fed from the same comparator if $R\sin \omega t$ and $R\cos \omega t$ can be generated simultaneously. Both of these signals are generated in the two integrator loop (set 26, cards 6 and 7).

If only one signal source is available then use two sample and holds, each fed with $R\sin \omega t$, but triggered from different comparators, one fed from the sawtooth ramping from 0 to $2b$, the other ramping from $-b/2$ to $+3b/2$. In the last case the bias voltage must be able to go negative to obtain angles in the fourth quadrant.

Other electronic methods use pulse width modulation and averaging circuits. Such a scheme is the one shown left which produces an output proportional to cos X. The modulator produces pulses of width $(\pi - 2X)/\omega$ symmetrically placed about the peaks of the sinusoidal input. When these are fed to the switch, e.g. CD4016AE analogue transmission gate, the output is a chopped sinusoidal waveform whose average can be shown to be proportional to cos X. If the output pulses from the pulse width modulator are centred about the zero-crossings of the sinusoid, the output will be proportional to sin X.





Reference

Schmid, H. Integrated circuits replace the electromechanical resolver, *Electronics*, Jan. 1966.

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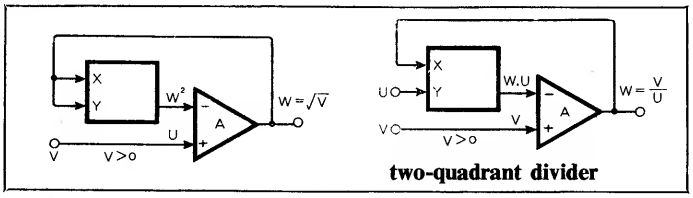
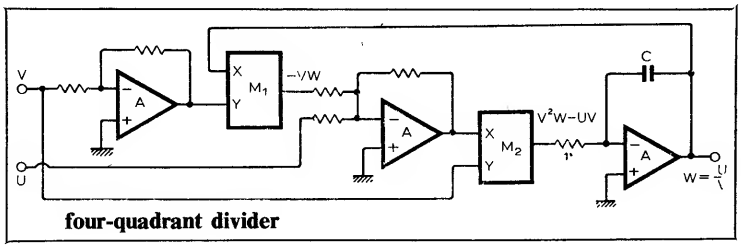
Set 30: R.m.s./log/power laws—9

Applications of i.c. multipliers



two-quadrant divider



four-quadrant divider

Many multiplier modules are now available on the market (e.g. MC1594L, XR2308, AD433J). The reduced cost and improved capability and accuracy of them has produced an increasing usage; unfortunately the existence of different types has produced confusion to the uninitiated. There are at least three distinct types: those having two inputs X and Y, the output being KXY, with K a scale factor; those which have two differential inputs X and Y, the output being KXY; those having three inputs X, Y and Z the output being KXY/Z—this last one is obviously a combined multiplier/divider. Adding to the confusion is the apparently magical way in which some functions are generated. It is easy to see that the final answer is correct but there is never a logical thought process shown by which the answer was arrived at.

Many of the uses of multipliers involve the implicit solution of some equation. This means that the output is fed back in some manner, thereby affecting itself. All of the circuits in this card involve an implicit solution.

Above left is shown a circuit for the generation of $\sqrt{V}$. The output W is fed to a multiplier with both input terminals connected together to form a squarer. This squarer is in the feedback path of an op-amp A. As the differential input voltage of the op-amp must be zero, $V-W^2=0$ i.e. $W=\sqrt{V}$. Note that V must be positive, as otherwise negative feedback round the loop is lost and latch-up will occur.

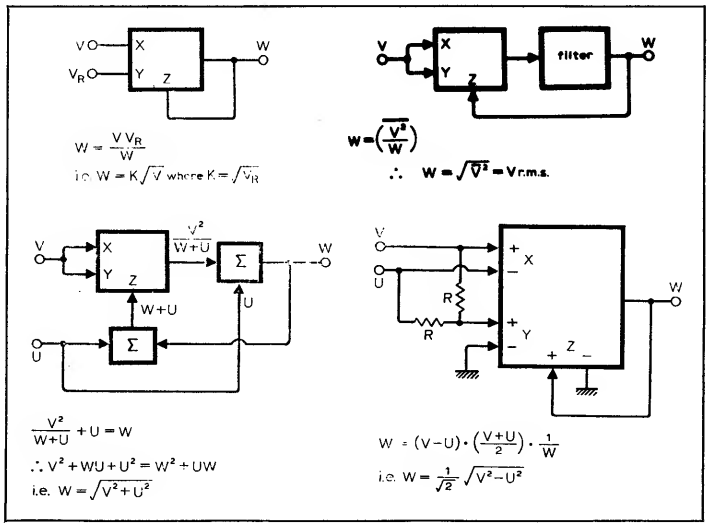
Above centre is a multiplier connected in the feedback path of an op-amp to provide an overall division function. Polarity inversion through the multiplier must be avoided to prevent positive feedback and this restricts U to being positive. On the other hand V can be either positive or negative so that in the U-V plane one is allowed to operate in the two quadrants for which U is positive. It is clearly impossible for U to be zero but additionally if U is very small one obtains a very small feedback signal so that offset voltages and currents can cause latch up.

Above right is a four-quadrant divider in which the output of M_2 is V^2W-UV. If the inputs are d.c. then in the steady state the integrator output must be constant implying $V^2W-UV=0$ i.e. $W=U/V$. It is claimed (ref. 1) that U and V can even go through zero together in this circuit. It also claimed that improved accuracy and stability are achieved. Both of these characteristics appear to reside in the action of the integrator whose output must change till the input is zero and whose output, moreover, cannot change rapidly.

Turning now to the more complex multipliers, note the circuit simplicity of Figs 1 to 4. Fig. 1 shows a square rooting circuit, Fig. 2 an r.m.s. to d.c. converter (compare card 4) and Figs 3 and 4 show vector sum and vector differencing circuits. Note the vector sum relationship can also be obtained by mechanising the relationship $V^2/(W-U)-U=W$. The apparent simplicity vaporizes to an extent when one examines the actual implementations recommended by the module manufacturers. The modules are liberally surrounded by assorted external components the aim of which is to minimize errors. Fortunately these recommendations are fairly specific since the questions of errors and bandwidth are difficult for multipliers alone; when combined in complex circuits the analysis really is awkward.

Another point which must be mentioned is that of scaling: it is always necessary to ensure that the design of a circuit is such that the multipliers do not saturate. This may seem obvious but with as many as six inputs, possible with the module of Fig. 4, it is all too easy to overlook this aspect or even to make a simple miscalculation.

The above circuits are intended only as a representative sample of some things that are possible with multipliers. Other applications will be found in the amplitude stabilization of oscillators (ref. 2), the design of voltage controlled oscillators, phase detectors and sample-and-hold circuits (ref. 3) and in the linearisation of a transducer output signal (ref. 4) among many.



References

1 Korn and Korn, Electronic analog and hybrid computers, 2nd edition, McGraw-Hill.

2 Vannerson and Smith, Fast amplitude stabilisation of an R-C oscillator, *IEEE J. Solid State Circuits*, vol. SC9, No. 4, Aug. 1974.

3 Ryan, C. R. Applications of a four quadrant multiplier, *IEEE J. Solid State Circuits*, Feb. 1970, pp. 45-8.

4 Trofimenkoff and Smallwood, Analog multiplier circuit linearises transducer output, *IEEE Trans.* vol. IM23, no. 3, Sept. 1974.

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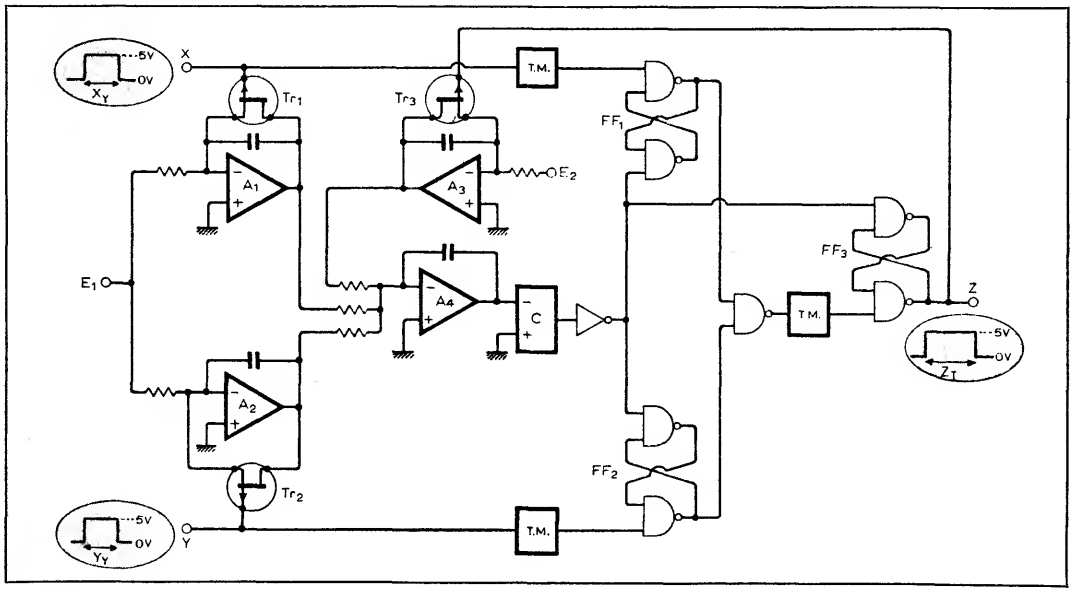
Computation of $(x^2+y^2)^{\frac{1}{2}}$



Analogue information x and y is contained in the input pulse widths x_T and y_T respectively.

On the occurrence of the pulse x, the f.e.t. switch Tr_1 opened and integrator A_1, fed from the d.c. signal E, ramps down and integrator A_4 rises in a parabolic manner to a voltage of A_4 rises to $Ax_T^2+By_T^2$. At the end of this operation the R-S flip flops $FF_1$and FF_2 combine with FF_3 to open switch Tr_3 allowing E_2 (negative) to integrate via A_3 and feed A_4. This causes the output of A_4 to fall. When this fall reaches zero, the comparator C changes state and becomes high causing FF_3 to become low and switching off Tr_3. The time for which E_2 is applied is

$$z_T=\left(\frac{Ax_T^2}{C}+\frac{By_T^2}{C}\right)^{\frac{1}{2}}$$

With the circuit elements chosen, $A/C=B/C=1$, giving the required relationship.

Performance data
All resistors 50kΩ,
capacitors 10nF
Tr_1–Tr_3 1H5012
C (comparator) SN72810
All logic SN7400
T.M. ≡ trailing edge triggered monostable (see figure below)
$z_T=(x_T^2+y_T^2)^{\frac{1}{2}}$ within ±1%
for x_T in range 0 to 2ms
and y_T in range 0 to 1ms
E_1 +1.0V, E_2 −1.0V
Ax_T^2, when the signal y is applied A_2 ramps giving an additional component By_T^2 to the output of A_4. y may appear before, during or after x.
Whatever the case, the output

Reference
Ikeda, H. *Electronics Letters*, 30 Oct. 1975, vol. 11.

Related circuits
Set 19, card 4
Set 15, cards 4, 6
Set 30, card 1

Alternative circuit
This circuit (middle) has the advantage that the inputs can be simple voltages, rather than pulse widths, but is restricted to two inputs (the previous scheme is readily extended to more than two inputs) and is less accurate.

The circuit is an analogue computer type circuit for the solution of
$v(t)+\omega^2v(t)=0$
where $v(t)$ is the inverter output voltage, ω is the "gain" of each integrator and the inverter gain is assumed to be −1. The solution of this equation is
$v(t)=z\sin(\omega t+\varphi)$
where $z=(v(0)^2+(v(0)/\omega^2)^{\frac{1}{2}}$.
Hence if the initial conditions (i.c.) on the two integrators are made equal to the analogue voltages x and y, the resulting oscillation has a peak value $(x^2+y^2)^{\frac{1}{2}}$. Peak detectors suitable for this purpose are discussed in Set 4, card 2.

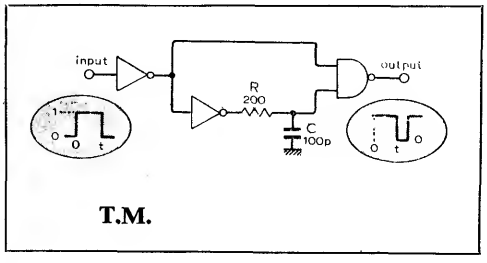
An arrangement suitable for the application of the initial conditions on the integrators is shown below right, in which the switches may be f.e.ts or analogue transmission gates such as the CD4016AE. For normal integration S_1 is closed, S_2 and S_3 are open. When applying the i.cs, S_1 is opened and S_2 and S_3 are closed. If $r_1=r_2$ then the integrator output rises to the i.c. voltage with time constant r_2c which should be made short by choice of r_2. If the op-amps are capable of supplying current to (r_1+r_2) and to the following integrator/inverter then S_3 may be dispensed with.

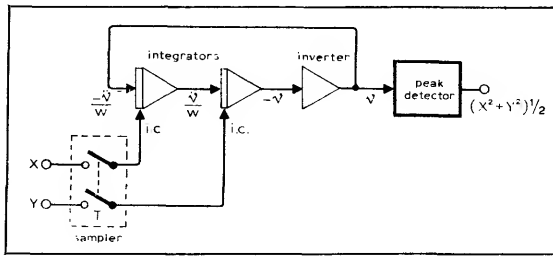
Using an integrator time constant of 1s, an inverter gain of 0.9 and a sampling period of 2s, J. S. C. Tan has reported an accuracy of ±2% (approx) over a useful range of x and y, amplifier finally limiting the accuracy.

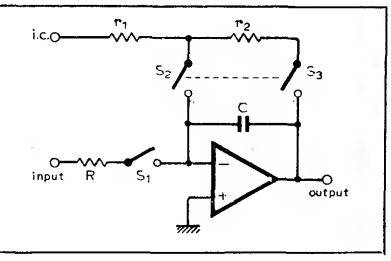
Note that the system is a two integrator loop oscillator (Set 26, cards 5, 6, 7) with no mechanism for amplitude stabilization so that continuous updating of x and y is essential i.e. $T\gg 2\pi/\omega$ is undesirable.

Reference
Tan, J. S. C. *Electronic Letters*, 31 Oct. 1974, vol. 10.

Related circuit
Set 30, cards 1, 5.







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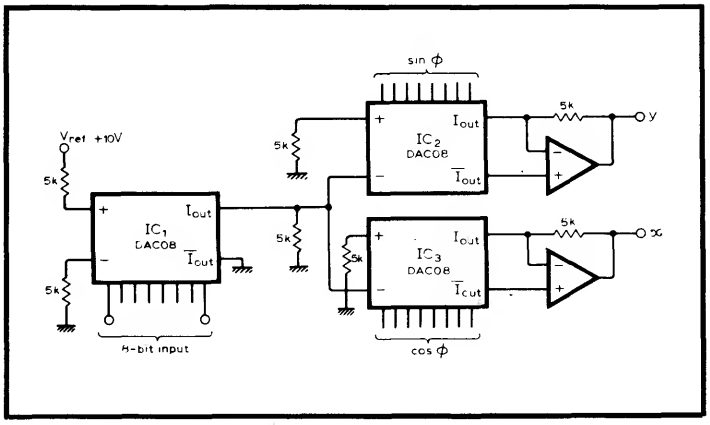
Set 30: Up-date

The above system employing multiplying d.a.c. converts digital polar co-ordinate information (r, sin θ, cos θ) into analogue form. The output from IC_1 is converted directly to a voltage through a resistive load, which is proportional to the digital value of r. This is then the source of the variable reference currents for IC_2 and IC_3 The output current is the product of the reference input current and the digital input representing the sine or cosine information. The op-amps convert the currents into a positive-going voltages e.g. an all-ones r input provides −10V at IC_1 output, and hence a 2mA reference current into the next stage, the output current then depending on the digital sine or cosine entered. For all-zeros at r, the input reference current to IC_2, IC_3, is zero, giving zero output current and hence zero output voltage at X and Y.

Electronic Eng., Jan. 1976, Applied ideas.

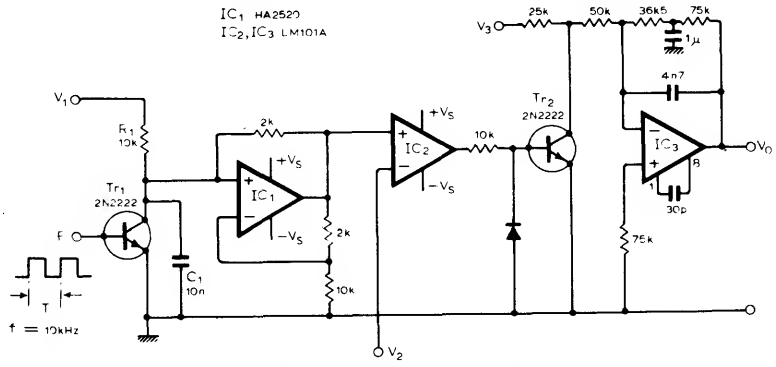


Charging current of C_1 is effectively V_1/R_1 which generates a ramp voltage at the input of IC_2, used as a comparator. Capacitor C_1 periodically discharged by the pulse train into transistor Tr_1. The ramp voltage at the output of IC_1 will reach V_2 after a time

$$t = CV/I = C_1V_2R_1/V_1.$$

Hence $t/T = C_1V_2R_1/V_1T$, where T is duty cycle at the output of A_2. This modulates the input to the active filter IC_3, which provides an output

$$V_O = -C_1V_2R_1V_3/V_1T.$$



If T is made equal to R_1C_1, then $V_O = -V_2V_3/V_1$. If V_1 is kept constant, the circuit acts as a multiplier. If V_2 is maintained constant, then an analogue divider is implemented. Input levels should be less than +10V (all signals must be positive) and V_2 should be less than V_1.

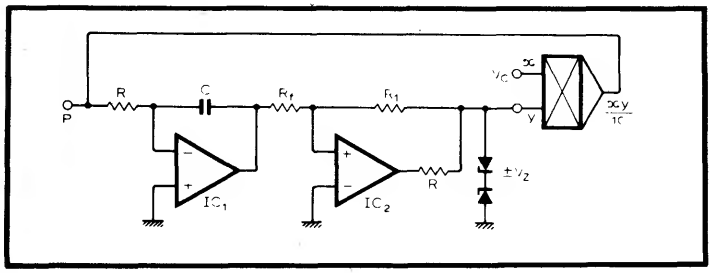
Reference

Clark, R. S. *Electronic Design*, Jan. 5, 1976. p. 118.

This circuit provides a means of controlling the frequency of the square/triangle generator comprising an integrator (IC_1) and Schmitt comparator (IC_2). The input signal to y is constrained by the back-to-back zener diodes to be $\pm V_z$. This is multiplied by the control voltage V_c, and hence multiplies the voltage at P by the same factor, which therefore modifies the charging rate of capacitor C and hence the frequency of oscillation.

Reference

Graeme, G. J. Applications of Operational Amplifiers, McGraw Hall, 1973.



Contents of Circuit Designs 1

Contents of Circuit Designs 2

circuit designs

3

PWilliams/JCarruthers/JHEvans/JKinsler