

# THINK TANK

By John J. Yacono

## Derby Finale

We are now at the end of our pinewood derby exhibition. This month we'll present the last quality pinewood-derby circuits that made it in on time. The contributors will be rewarded with a *Think Tank II* book and, as a bonus for taking part in our derby mania, MCL1010 chips.

With regard to the pinewood-derby contributors, I say a hearty thank you. As it turns out, although they required more work on the part of the entrants, I received more pinewood-derby circuits than any prior specially requested submissions! You've probably helped a lot of community organizations, and, if nothing else, gave some of us a feeling of community

spirit again. Thanks for making the effort worthwhile.

Next month, I promise to get back to our introductory topic, "Logic IC's." For now, though, let the players take the field . . .

### MULTIPELXED DERBY

Regarding the request from Stephen Guye about a circuit for a six-lane race judge, I think I have just the thing. The circuit consists of six 7-segment displays (one per lane) that are driven by six BCD-to-7-segment latch/decoder/drivers that are enabled by the outputs of a hex D-type flip-flop.

Figure 1 shows the flip-flop portion of the circuit. When power is first applied to the circuit, capacitor C1, which is connected to the clear ( $\overline{CLR}$ ) input of U2 at pin 1, initially acts a short, pulling pin 1 low. After that, capacitor C1 begins to charge through R1. When C1 is fully charged (about a second later), a high is placed on both the D1 and  $\overline{CLR}$  inputs. That sets U2 for the first pulse delivered to the clock (CLK) input—all the outputs are cleared (low) and there is a high waiting at the D1 (pin 3) input.

Notice from the display section (shown in Fig. 2) that all the binary inputs of the six 4511 display drivers (only one is shown) have their like inputs connected together and tied to ground through four pull-down resistors (R2-R5). Those resistors cause the display drivers to initially show a 0 on each display.

Notice also from the detector diagram (in Fig. 3) that each binary input on

the drivers (except for D, which corresponds to the 8 input in BCD and is not used) is connected to one or more outputs from the detector (phototransistor) circuits. If you follow the lines leading from the collector of each

phototransistor, you'll see that Q1 is connected to the A input(s) only. That means that when Q1 is triggered, the display driver that is latched will only receive a BCD 1 since all the other inputs are tied to ground through their pull-down resistors. Likewise, Q2 is connected only to the B (or BCD 2) input, Q3 is connected to both the A and B inputs (producing a BCD-input value of 3), and so on.

Capacitors C2 through C7 at the collectors of Q1-Q6, respectively, force their input signals to appear as short pulses across R6 through R11 (10k resistors). Keeping the pulses brief prevents pulses (and thus BCD data) from separate lanes from obscuring one another should their car's finish close to one another. Those pulses are fed to the input of U1-a and, through U1-b, and then fed to the clock (CLK) input of U2 (back in Fig. 1).

Phototransistors Q1 through Q6, which are placed on the track and receive normal room lighting, are switched on by that light and effectively connect each of the 1.5k resistors (R6 through R11) to ground. The low keeps the display-driver inputs from receiving a pulse that would change their state until a car passes, blocking

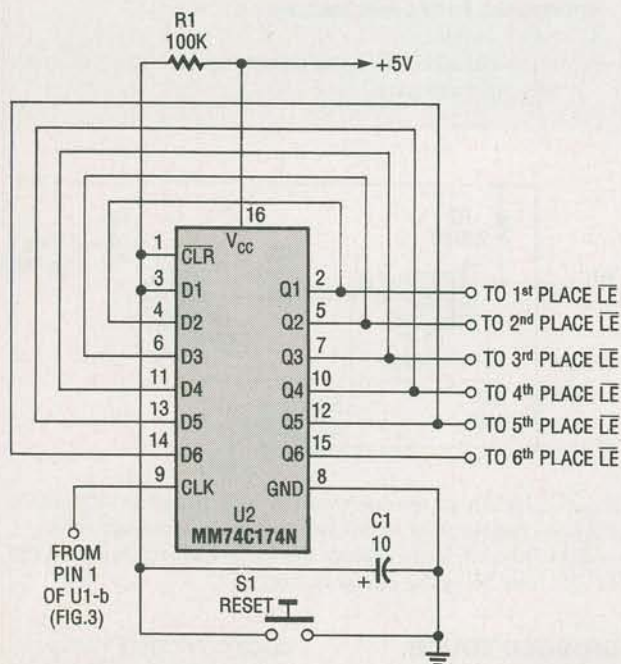


Fig. 1. This hex flip-flop indirectly receives clock pulses from the dark detectors and activates each place-display circuit one at a time. Components R1 and C1 initially set-up the flip-flop and those components can be reactivated by depressing S1 to initialize the flip-flop for future races.



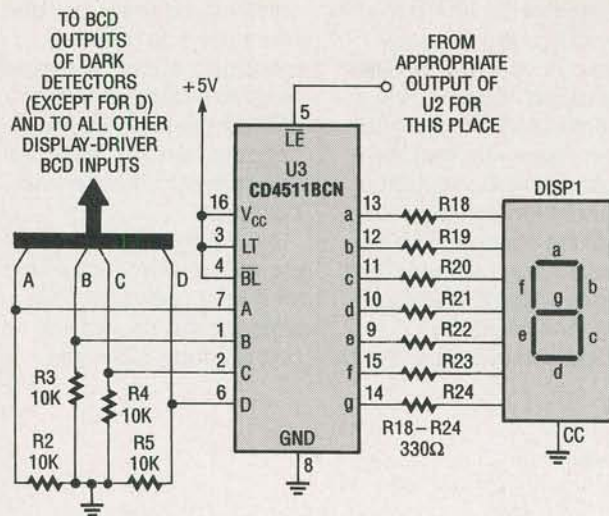


Fig. 2. Each display circuit receives BCD data from the dark-detector/BCD-encoder circuitry, but only the display circuit that is latched by U2 (in Fig. 1) will hold and display the current lane number.

the light to a phototransistor.

When a car passes over a phototransistor, it turns off, producing a high at its collector. That high is fed through its respective capacitor and diode(s), placing a high across the resistor connected to the input(s) of its respective display driver. After a very short time, the capacitor charges and the voltage across the resistor once again goes low, so the next car that comes along and turns-off a phototransistor won't experience any interference from the previous one.

Phototransistor Q1 should be placed in lane 1, Q2 goes in lane 2, and so on down the line to Q6, which is, naturally, placed in lane 6. Likewise, the displays should be placed in order; i.e., display one should be placed first, display 2 second, and so on so that display six shows the car that comes in last. If that layout is followed, each display will show the lane number for the car that

finished in that place.

For example, at the moment a phototransistor turns off, the capacitor at its collector begins to conduct, placing a high at one or more inputs to the display drivers and at the input to U1-a. That gate along with the resistor connected to the input(s) of its respective display driver. After a very short time, the capacitor charges and the voltage across the resistor once again goes low, so the next car that comes along and turns-off a phototransistor won't experience any interference from the previous one.

Phototransistor Q1 should be placed in lane 1, Q2 goes in lane 2, and so on down the line to Q6, which is, naturally, placed in lane 6. Likewise, the displays should be placed in order; i.e., display one should be placed first, display 2 second, and so on so that display six shows the car that comes in last. If that layout is followed, each display will show the lane number for the car that

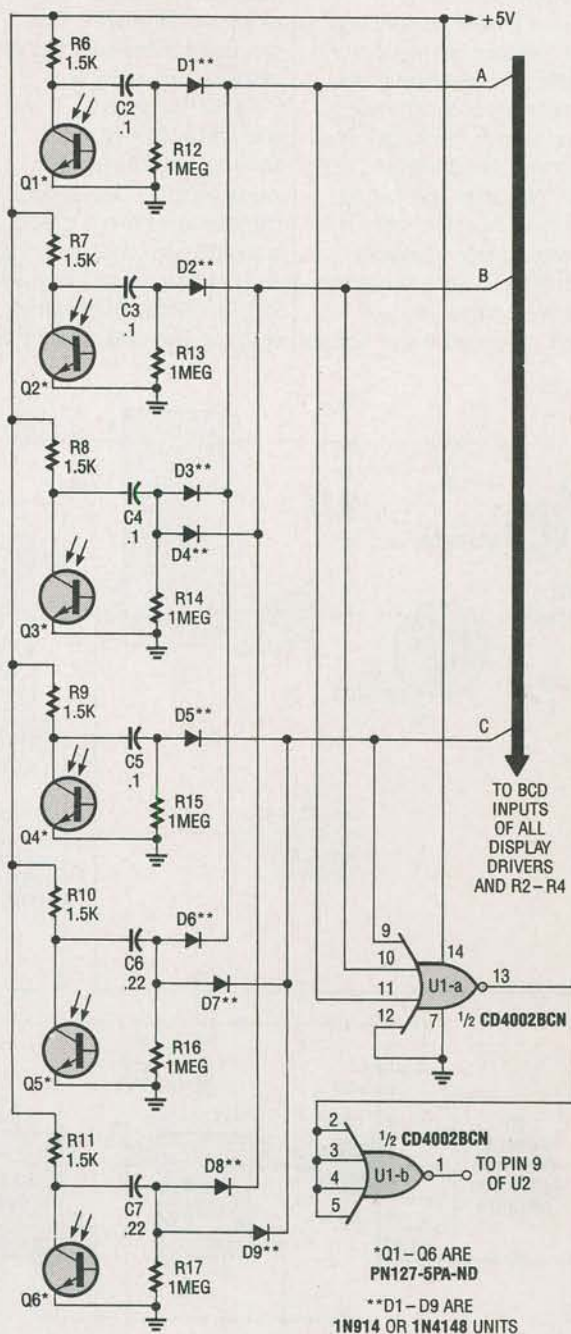


Fig. 3. The two 4-input NOR gates are used to OR the output of all the dark detectors to produce a clock pulse when each car crosses the finish line. The output of each detector is BCD-encoded by the diodes in order to transcribe its lane number onto the display-driver bus.

After the race, the circuit can be reset by pushing S1, a normally open momentary-contact switch. When S1 is pushed, the D1 and CLR inputs of U2 go low long

enough to clear the flip-flop outputs. When the outputs go low, the displays are no longer latched, and once again they display zero data at their BCD in-



puts, and the track is ready for another race.

For a power supply, you can use four series-connected D-cells. Since the circuit can draw as much as a 1/2 amp, I wouldn't use batteries smaller than D-cells. Although the circuit can be operated from a supply voltage ranging from 5 to 15 volts, if you use higher voltage you will need to increase the values

of the resistors that connect the display drivers to the displays. Otherwise, the chips will overheat and the display may burn out.

As for the sensors, if you use PN127-SPA-ND's for Q1-Q6, you can solder each lead to one of the conductors from a piece of speaker wire and then tape the phototransistor and wire to the middle of the track, and run the wire down the

center of track so that the wheels of the cars don't hit anything and the track won't have to be modified. Be sure to tape the entire length of wire to the track and make sure that the light hitting the transistors shines from overhead so that the shadow from the car passing over will block out the light, thereby turning the transistor off.

You can assemble the cir-

cuit any way you like. You can even be really lazy and assemble it on a cheap breadboard. Just be sure to observe proper handling procedures for the chips because CMOS circuits are susceptible to electrostatic discharge.

All of the components are available from Digi-Key for a total of around \$30, although the project will cost less than \$20 if you

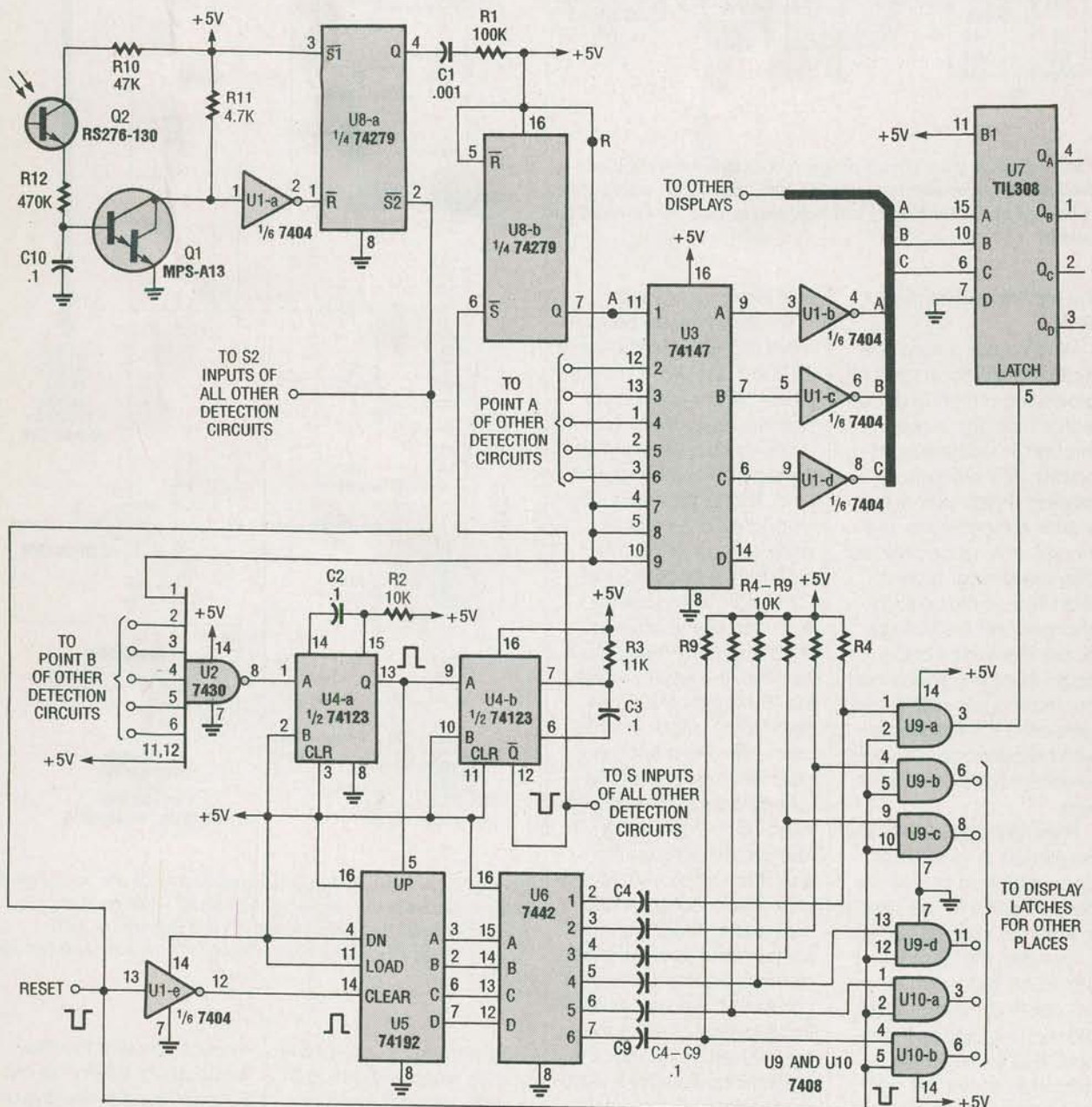


Fig. 4. This schematic diagram shows the circuitry require to monitor one lane of the pinewood-derby. The detector/latched display circuit shown here must be duplicated for each lane (say, the 2nd through 6th) included in your derby-judging system.



happen to have the six displays already. You can also cut power consumption considerably by placing a transistor between each display and ground and using a clock circuit to strobe them on in turn.

—Guy Lamrouex,  
Sarasota, FL

*You really cut down on parts by using diodes as a BCD-data generator and U2 as a shift-register style latch enable. I suppose if an octal flip-flop (or 8-bit shift register) were used in place of U2, you could take advantage of the unused display-latch inputs by adding two more lanes. Of course, the additional dark detectors would have to be appropriately multiplexed, with the last lane (number 8) connected to the unused input of U1-a.*

## OVER THE LINE

I was pleasantly surprised to read the call for pinewood-derby finish detectors. Years ago, a friend of mine asked me to build one because a genuine fist fight had erupted during the previous year's competition.

The first thing that I considered was how to display the results. I decided to use six 7-segment latched displays to reveal the contestants' finishing order (see Fig. 4). So the left-most display in my system indicates the lane that finished first, the display to the right of that shows the second-place winner, and so on.

Each lane's photodetector (Q2 in the schematic diagram) sets an RS flip-flop (represented by U8-a) that is unique to that lane. The flip-flop's state change is sent through a capacitor and pull-up resistor to edge trigger a second RS flip-flop (U8-b) that is connected to the lane-number input of a

binary encoder (U3). After that pulse, the encoder's output-data lines contain the lane number.

The same edge-triggered pulse that sets the second flip-flop is sent to an eight-input NAND gate (U2) that triggers a very fast monostable multivibrator (U4-a). In turn, the monostable's output pulse advances a binary counter (U5) and triggers another very fast monostable (U4-b). The counter output is decoded and sent to a pulse generator that latches the display corresponding to the counter contents. The output of the second monostable is designed to allow the expiration of the latch pulse before resetting the second RS flip-flop (which is locked out until a master reset is activated). The lane number data is present on the latch data lines before the latch pulse occurs, and is stable throughout. After latching the data, the lane is locked out.

Two types of displays were used. One of the displays was based on the classic 7475, 7447, and 7-segment display arrangement (not shown). The second used the Texas Instruments TIL308 display, which has a built-in latch and 7-segment decoder, as shown.

—Kenneth J. Michael,  
Palos Hills, IL

*Having the display list the finishing order is a nice change from the usual lined display. If nothing else, it allows the builder to set up a track with more lanes than there are places of merit.*

That's all for now, and for the pinewood derby. Until next month, take care and send your best efforts to: *Think Tank*, **Popular Electronics**, 500-B Bi-County Blvd., Farmingdale, NY 11735. ■