THE DIGITAL MODEL TRAIN – PART 7

by T. Wigmore

The seventh part in the series deals with the circuit description of the main unit in the Elektor Electronics Digital Train System. The construction and testing will be the subject of next month's instalment.

The main unit consists essentially of a single-board processor system based on a Z80 as shown in Fig. 47. This processor was chosen not only for its very low price, but also because the special Z80 peripheral chips (PIO – parallel input/output – and CTC – counter timer control) make it possible to use the powerful Z80 interrupt structure without the need of additional logic. Since the train system requires a number of asynchronous processes to be carried out more or less simultaneously, this is a very worthwhile aspect.

Apart from the standard Z80 design, consisting of the processor proper, memories and a CTC for general timing functions, the unit also contains various I/O structures.

Reading of the locomotive controls is carried out by an analogue-to-digital (A-D) converter that has 16 multiplexed analogue inputs. The results of the A-D conversions and the position of the function switches associated with the locomotive controls are read via a PIO port. Set locomotive addresses are read on to a separate bus via a diode matrix. This matrix may be considered a primitive 16-byte manual access memory (MAM), which has the advantage that no knowledge of programming is required to set the addresses. The setting may be carried out with the aid of diodes, DIL (dual-in-line) switches or thumbwheel switches.

Main features

- independent control of up to 81 locomotives
- accepts up to 16 manual controls
- on-board locomotive addressing
- controls up to 324 turnouts (points) and signals (648 solenoids)
- manual control of turnouts (points) via keyboards
- stand-alone or computer-controlled operation via RS232 interface
- integral interface for monitoring signals via the track
- compatible with Märklin Digital
- low-cost Z80 microprocessor; 2.45 MHz, 8 K ROM; 8 K RAM
- excellent price/performance ratio

The keyboards are connected to the Z80 bus via a 20-way connector and the keyboard interface. The 20-way connector indicates that, in contrast to the Märklin system, the keyboards are driven in parallel. Märklin's serial keyboard drive requires a microprocessor for each keyboard. Since our keyboards do not need a microprocessor, the relevant circuits have remained fairly simple. The cost of this is, of course, a 20-way connector between the main unit and the keyboards but, since keyboards are normally located next to the main unit anyway, that is hardly a disadvantage.

The main unit also has a serial output to the booster. The serial signals (binary coded trinary data) are generated by a special function IC. One timer of the CTC is used as the clock for the serial-signal generator, so that the baud rate may be adjusted with the aid of software. This is necessary, because switching instructions for signals and turnouts (points) need to be sent at higher speeds than the locomotive control commands.

Finally, there is a bidirectional serial (semi duplex) RS232 interface, but this does not make it necessary for the train system to be controlled via a computer: the unit is perfectly suitable for stand-alone operation. However, the RS232 interface makes the system considerably more versatile.

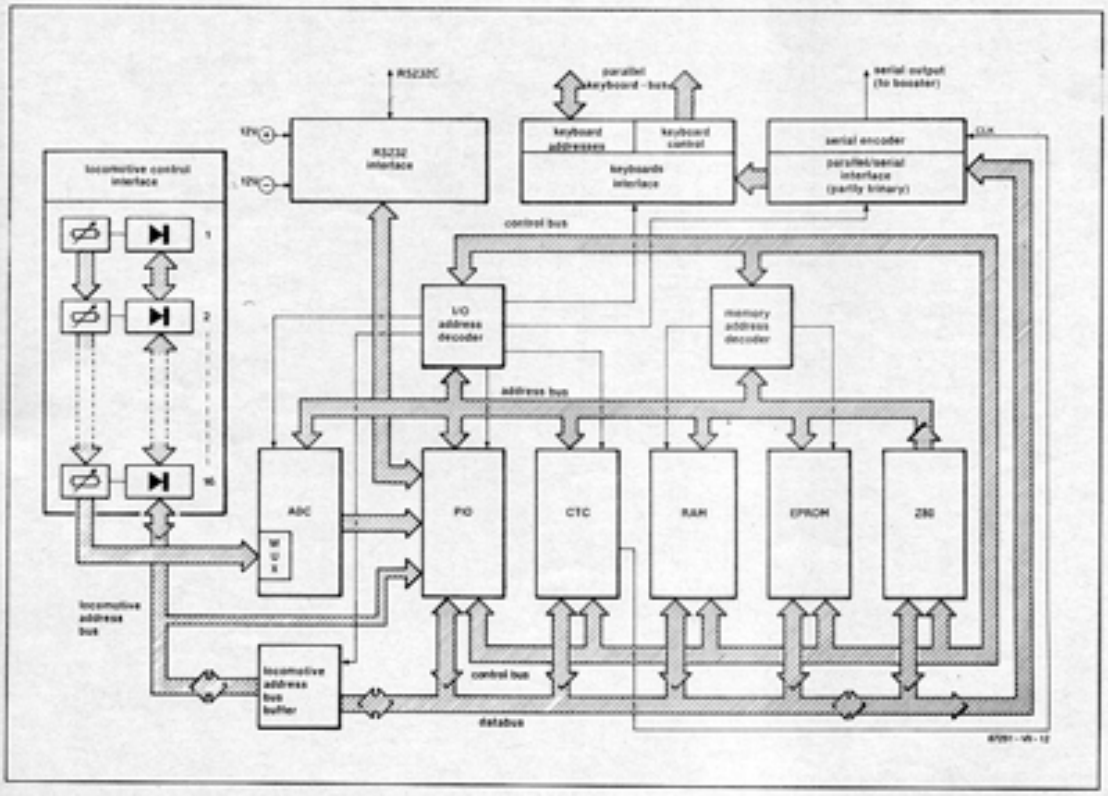


Fig. 47. Block schematic of the main unit, which is essentially a Z80-controlled single-board computer

Circuit diagram

The 5-V supply at the top left in the circuit diagram of Fig. 48 is a standard design, except for D36. This diode ensures that the current through the keyboard

LEDs (taken from V** via K19) does not load smoothing capacitor C25. This is necessary, because this current may be quite substantial (several amperes) if a large number of keyboards is used. This is also the reason that D38–D41 are heavy-duty types.

The supply for the RS232 drivers in IC10 is provided by IC15 and IC16. These components are necessary even if the RS232 interface is not used, because two gates in IC10, N2 and N5, are used for driving the booster. The input voltages for IC15 and IC16 (+20 V and –20 V respectively) are derived from the booster circuit.

The serial control data are encoded by IC27. Inputs D1–D4 are driven via electronic switches ES1–ES4. These four bits form the address section of the control data and are defined in three-state logic, that is, they are '1', '0' or 'undecided'.

The data section, D5–D9, functions with binary logic and is, therefore, connected direct to the outputs of IC17. Output latches IC17 and IC23 ensure that the serial data remain stable during transmission. As soon as the address part of a data byte is placed into IC23, the start instruction for serial transmission ($\overline{TE}$) is given via N6.

The clock for IC27 is derived from the second timer in the CTC, IC12, to enable the speed of the serial transmission via the software. The clock is divided by two in FF3 to obtain a 50% duty factor, which is necessary for the correct operation of IC27.

The clock pulses to IC27 are counted by the CTC. After 200 pulses, a data byte is transmitted twice and an interrupt is generated. The interrupt routine prepares the next data byte to be transmitted and starts the next transmission cycle.

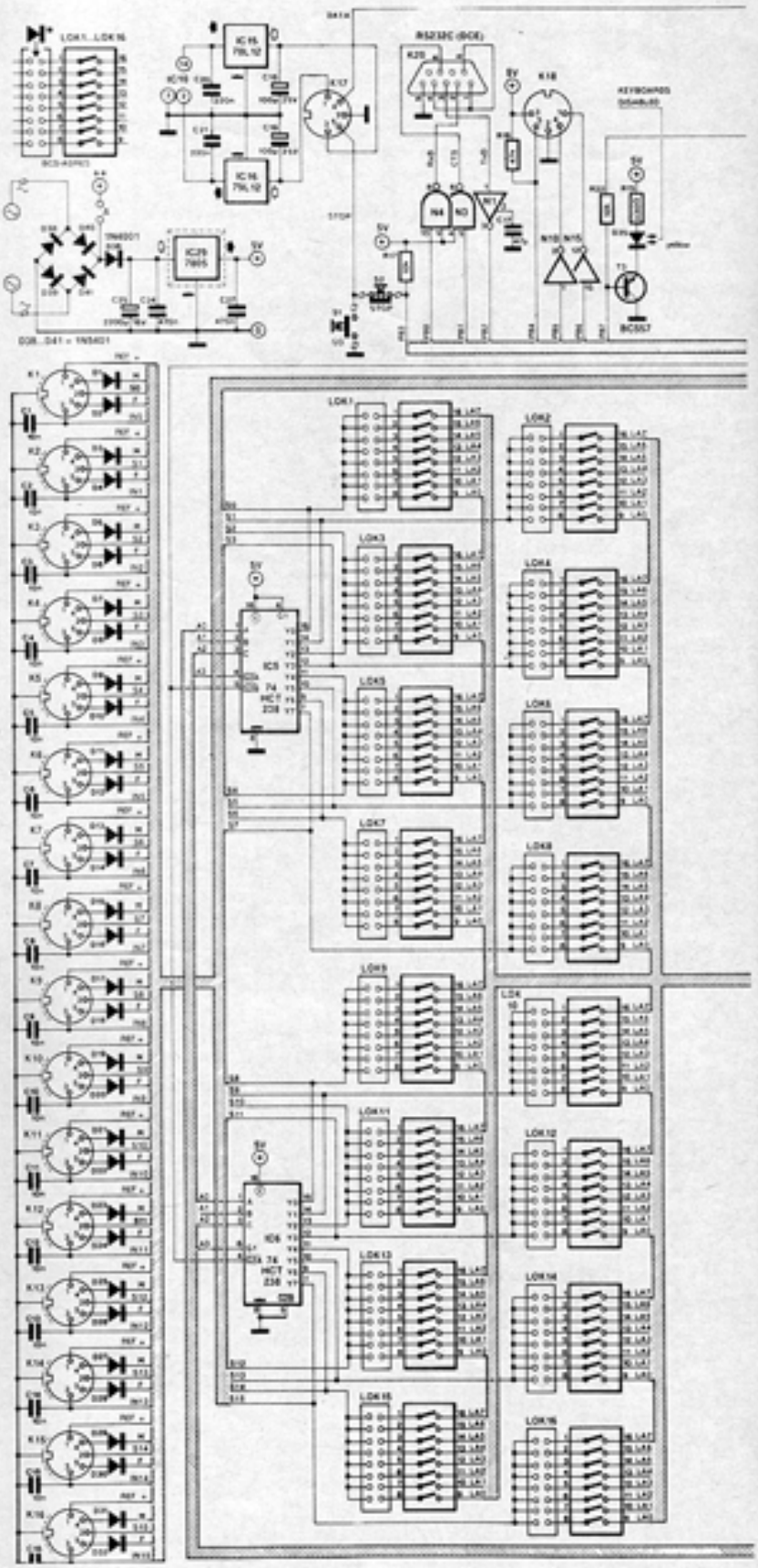
The output signal of IC27, which swings between 0 V and 5 V is amplified and made symmetric (±12 V) by N5. Since the signal is inverted by this gate, it is inverted again by N2 and then passed to the booster via Re1 and K17.

Output Q6 of IC17 is used to drive relay Re1. When the relay is not energized, the output of the unit, and that of the booster, is high-impedance, so that no voltage is applied to the track.

The oscillator, N11-N12, is followed by binary scaler IC8, whose output QA delivers the 2.45 MHz system clock. This frequency was chosen, because it enables both the baud rate of the RS232 interface and the various frequencies for the serial transmitter to be derived from it. Output QC provides a 614 kHz signal that is used as the clock for the A-D converter.

The circuit around the CPU (central processing unit), IC4, the PIO, IC3, and the CTC, IC12, is entirely standard and will not be discussed here.

The address decoding for the memories is carried out by IC28. This circuit splits the addressable memory locations of up to 64 kbyte into eight pages of 8 kbyte each. Page 0 (0000–1FFFH) contains the control program for the system, which is available as an EPROM, coded ESS572 (see the Readers services page towards the back of



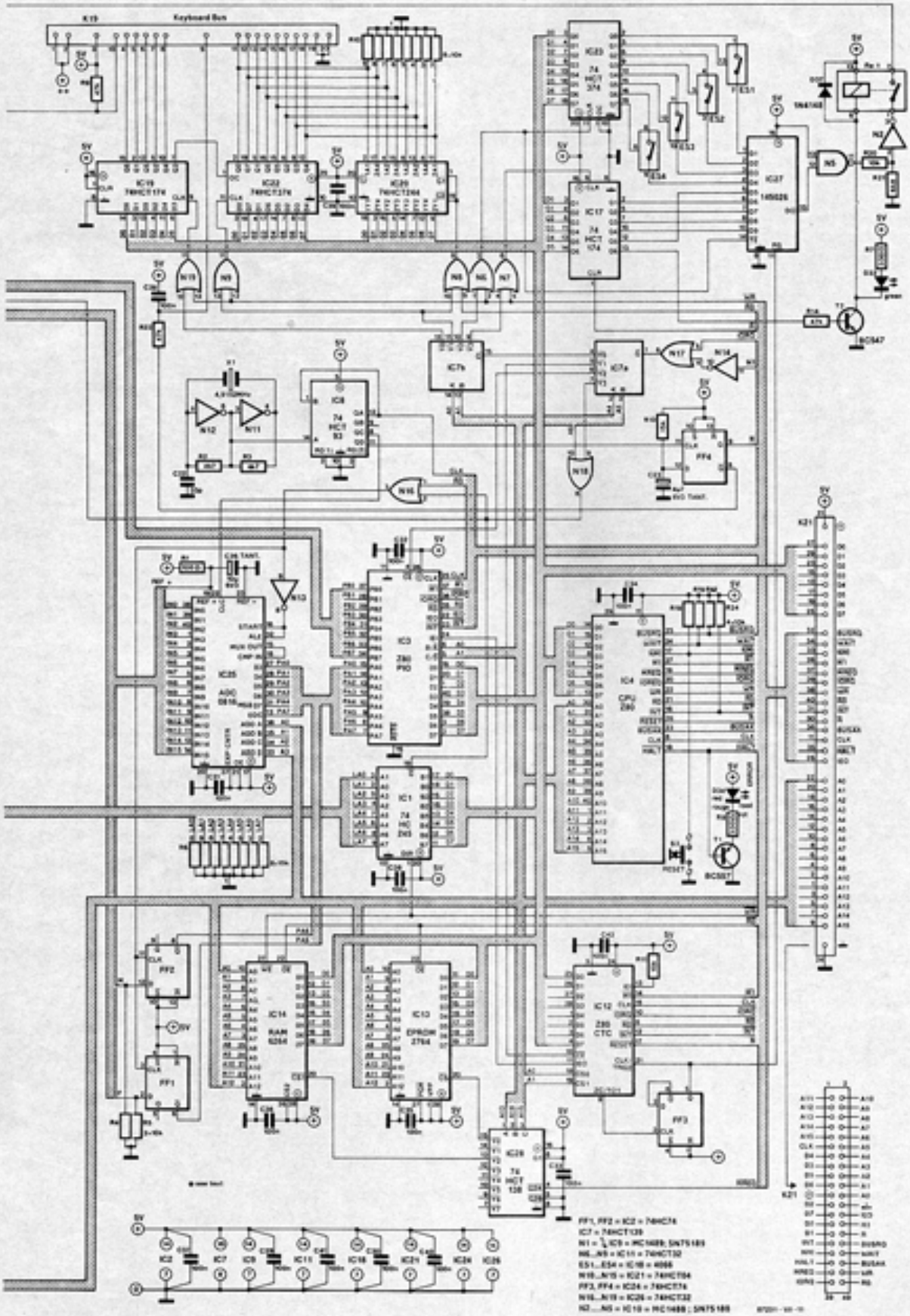


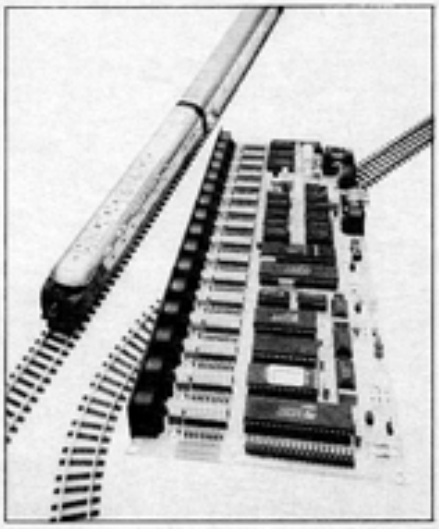
Fig. 48. Circuit diagram of the main unit of the Elektor Electronics Digital Train System

this issue. The EPROM contains unallocated space that may be used for any future extensions of the program.

The RAM is contained on page 2 (4000H –5FFFH) and this page is also largely unused. The system uses 2 kbyte, a further 2 kbyte is reserved for possible future extensions and 4 kbyte is available for downloading of user programs that are actuated via special RS232 commands. Table 5 shows the memory mapping.

The I/O addresses that are available on outputs A0–A7 of the CPU during read or write instructions are decoded by IC7. Here again, some space is not used and 32 I/O addresses are reserved for possible future extensions. See also Table 6.

The locomotive addressing is carried out via IC5 and IC6. Up to 16 selections may be made: S0–S15. If a selection signal is made active, that is, '1', the relevant lines LA0–LA7 (LA= locomotive address) that are connected to the selection line via a diode will also go high. Lines without a diode are held low ('0') by a pull-down resistor (contained in array R6).



The locomotive addresses, which are in BCD (binary-coded decimal) format, are read via buffer IC1. The reason that IC1 is a bidirectional buffer although the locomotive addresses can only be **read** by the diode matrix is that in future a select-and-display board may be used for the locomotive addressing.

At the relevant locomotive control, the address is set via the RS232 interface and written to the display board via IC1. This ensures that the display at all times shows to what address a given control is set. The practical implementation of the diode matrix will be described in next month's instalment.

At the same time the locomotive address is read, the position of the function controls is read into bistables FF1 and FF2, one of the 16 analogue inputs of the A–D converter is selected and a conversion is started. The analogue input, address at A0–A3, is taken to the converter via the address-latch-enable signal at pin 32. The conversion start signal is available at pin 16.

When the end-of-conversion signal (EOC at pin 13) becomes active, the converted signal is applied to the PIO. Five bits are used: four for the speed and one for the direction. The remaining two inputs of gate A of the PIO, PA5 and PA6, are used to read the position of the function switches.

Gate B of the PIO is used for the start/stop line (also the booster overload signal line), the interface for the monitors and the RS232 interface. The output lines are buffered.

Gates N10 and N15 ensure the provision of adequate current to the (relatively) capacitive load presented by the monitor bus.

Gates N3 and N4 adapt the logic 0–5 V level to the ±12 V RS232 level. Gate N1 does the opposite for incoming RS232 signals.

Control of the RS232 is entirely via software and will be dealt with in detail in a forthcoming article in this series.

Integral test program

Testing of the board is facilitated by the test routines incorporated in the system program. The most important of these is the service loop. This is actuated when the power is switched on while the GO switch is (kept) depressed. As long as S1 is closed, the service loop will remain active. During sustained testing it is, therefore, advisable to short-circuit the switch.

The service routine places VLF (very low frequency) square wave signals on the various output ports. These signals may be checked with a multimeter. Also, a yellow LED (D35) flashes in a 1 Hz rhythm and the LEDs on the keyboards will be driven sequentially. The service routine is disabled by opening S1.

If the booster was connected (which is not required during service checks), it may be necessary to press stop key S2 briefly to actuate the service loop.

A standard multimeter (analogue: R_i = 20 kΩ/V or digital) and an oscilloscope or frequency meter are required for testing and checking. If an oscilloscope or frequency meter is not available, not all recommended test can be carried out, which results in a somewhat greater uncertainty factor. However, if the construction has been carried out carefully, there is not much risk of anything going wrong, particularly not since the circuit has no calibration points whatsoever.

0000H	system control program ESS 572	EPROM 2764 (IC13)	
1FFFH		page 0	
2000H	not used		
3FFFH		page 1	
4000H	locomotive input buffer	RAM 6264 (IC14)	
401FH			
4020H	key-buffer		
4023H			
4030H	interrupt vector table		
4040H	system variables		
4100H	locomotive output-buffer	page 2	
4150H			
4200H	turnouts (points) status-buffer		
4300H	monitor buffer		
4400H	reserved buffer space		
4500H	RS232-input-buffer		
4600H	RS232-output-buffer		
4700H			
47FFH	stack		
	reserved for system extensions		
5000H	user defined entries		
5FFFH	downloaded from host		

Table 5. Memory mapping

I/O-address		I/O-device	
binary	HEX		
XX00XX00	C0H	drive	keyboard
XX00XX01	C1H	address-bus	
XX00XX10	C2H	adress section	serial encoder (IC27)
XX00XX11	C3H	data section	
XX01XX00	D0H	counter/ timer 0	CTC
XX01XX01	D1H	counter/ timer 1	
XX01XX10	D2H	counter/ timer 2	
XX01XX11	D3H	counter/ timer 3	
XX10XX00	E0H	gate A data	PIO
XX10XX01	E1H	gate A control	
XX10XX10	E2H	gate B data	
XX10XX11	E3H	gate B control	
X0110000	B0H	locomotive address bus & ADC-multiplexer	
X0111111	BFH		
01110000	B0H	spare	
01111111	BFH		
11110000	F0H	I/O-addresses	
11111111	FFH		

X = don't care

Table 6. Input/output mapping