Ten ways to reduce noise pickup in ICs

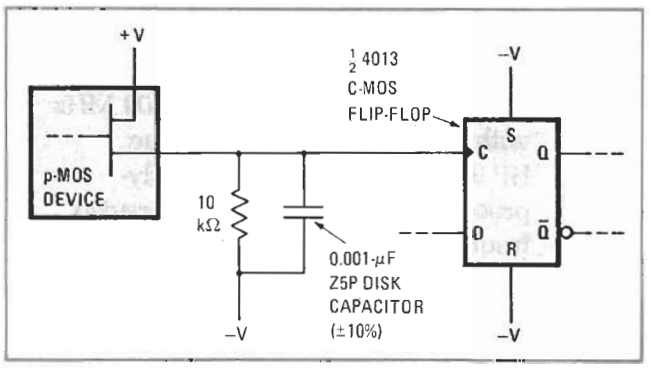
by Peter A. Goodwin
Loblolly Associates, Wayland, Mass.

Engineers who struggle to minimize noise pickup in equipment built with integrated circuitry know that there is no magic procedure for eliminating interference caused by lightning hits on power lines, chattering relays, motor-starting transients, electrical discharges to or near the equipment, radio-frequency fields, and the like. Instead, they fight noise by meticulous attention to details of bypassing, grounding, shielding, decoupling, and circuit layout—all used with understanding of the particular characteristics of the ICs involved.

TTL devices exhibit low-impedance, current-mode characteristics and are particularly susceptible to potential differences between devices caused principally by conducted interference.

MOS devices exhibit high-impedance, voltage-oriented characteristics and are therefore susceptible to radiated interference. A secondary susceptibility to conducted interference arises by induction from a neighboring conductor that is carrying the current of an electrical discharge.

Linear integrated circuits have high input impedances and low output impedances, and lack the guaranteed-true voltage regions that are characteristic of digital circuits. Noise spikes can enter a high-gain amplifier through the supply-voltage bus.



Noise suppression. Typical application of capacitor to bypass p-MOS output line that feeds edge-triggered C-MOS device. (Bypassing would be same for n-MOS device and pullup resistor, except that n-MOS would have V– supply and resistor would connect to V+.)

The following design practices will reduce the susceptibility of IC equipment to electromagnetic interference.

1. Bypass everything. An inexpensive general-purpose ceramic disk capacitor (0.01-microfarad) should be placed across the supply-voltage bus near each integrated circuit. TTL circuits are also improved by the presence of a 6.8-μF tantalum bypass capacitor for every 15 chips or so. Bypass MOS output lines that feed edge-triggered C-MOS devices, because only a passive device exists to provide the pullup or pulldown function. Use the minimum capacitance that gives acceptable rise time, and specify a temperature-stable 10% disk capacitor. See the figure for an illustration of typical components. No similar problem exists with C-MOS-driven devices, because C-MOS devices feature a totem-pole output structure.

2. *Allow sufficient printed-circuit conductor width.* Most interference is at radio frequencies, which travel on the surface of the conductors. Conductor width is particularly important in a TTL environment, where supply currents are substantial and the rate of change of current is on the order of 10^7 amperes/second. Supply-conductor widths of 100 mils or more are not uncommon in this environment. Use a ground plane wherever possible; the ground plane should be connected to the power-supply return.

3. *Distinguish between "earth" and "common" (system ground or power-supply return).* The earth conductor should never be used to transfer power. "Earth" and "common" conductors should be brought into contact at only one point in the system; otherwise a ground loop can radiate noise into the circuit.

4. *Run a separate supply bus for high-current devices.* This practice keeps transients off the busses that supply power to the logic circuitry. Remember also that conductors carrying current spikes couple inductively to neighboring conductors and that those carrying voltage spikes couple capacitively to their neighbors. Therefore, be careful in laying out these conductors.

5. *Keep pulldown resistors as small as possible* unless power consumption or other considerations are overriding factors. This is particularly true in MOS circuits.

6. *Don't overdo the fast-rise signals,* even though they are great for TTL devices. The lower the rise time, the less interconductor coupling.

7. *Don't let unused inputs float.* In the TTL discipline, connect them to V– or pull them up to V+ through a 1-kilohm resistor, as appropriate. In the MOS discipline, pull to V– or V+ as appropriate—a floating input is a true "maybe" condition.

8. *In general, use 1% resistors and capacitors in linear-circuit feasibility models.* The exceptions are pulldown resistors and bypass capacitors, where 20% variations can obviously be tolerated. After the design is optimized, then investigate the effects of component tolerance variations.

9. *Remember that decoupling is particularly suited to the low-current requirements of MOS circuitry.* A 1-ohm series resistor inserted in the supply bus on the supply side of the input bypass capacitor provides good isolation from high-frequency power variations.

10. *Avoid one-shots if pulse-width is critical.* The trouble is, their manufacturing tolerances are loose. Instead of

using one-shots, arrange to derive pulses from the clock.

If all else fails, line filtering and unit shielding offer attractive although more expensive possibilities. Metal or conductively coated nonmetallic equipment enclosures provide marked attenuation to external interference. Windows over displays, dials, and meters can be covered with copper screening. Line filters offer resistance to power-line-conducted noise, but generally should be matched to the equipment by enlisting the aid of the filter manufacturer. □