Multi-flash Trigger Unit

Instrument triggers up to five flash units at intervals from 11ms to 11s

by Ralph Lewis

There are many times when the output of commercial stroboscopic flash units is completely inadequate to deal with a particular photographic problem. I am thinking essentially of cases similar to one described by Victor Blackman in his "Cameravaria" column in *Amateur Photographer* when he was required to take sequence photographs of a springboard diver in flight. To have used a strobe flash, even of a power considered high for strobe circuits, would have necessitated the pool being in complete darkness, otherwise ambient illumination would have obliterated the flash images. Because it was obviously dangerous to attempt a dive under those conditions, he ended up making a montage from photographs taken during separate dives.

Stroboscopic flash design to deliver the same amount of energy per flash as the high power single flash units (often 1,000 to 5,000 joules) in use in many studios today, is impracticable because of problems encountered in cooling the flash tube and building up energy in the capacitor rapidly enough. The usual way out of this difficulty, where short sequences are required and it is not essential for the light to issue from exactly the same point each time, is to arrange for a number of capacitors to be charged simultaneously and discharged in succession; each one through a separate flashtube; often, but not necessarily, mounted in one reflector.

A simpler and less expensive method is to make use of conventional commercial single flash units and connect them to a device that will trigger them in the required manner. Making use of standard designs means that they can be obtained as and when needed from the several firms offering equipment hire facilities.

The circuit of such a device, which will trigger up to five flash units at equal increments of time throughout periods of 11 seconds to 11 milliseconds, is illustrated in this article. The periods are continuously variable to suit the duration of the event to be photographed.

Circuit operation

Transistors Tr_1, Tr_2 and Tr_3 (Fig. 1) with their associated components make up a monostable multivibrator which is switched from the stable to the unstable state by a negative pulse applied to the base of Tr_2. This is provided by the closing of the camera shutter contacts which connect to the socket labelled sync. The pulse causes the collector current of Tr_2 to rise and switch on the thyristor SCR_1, which in turn triggers the first flash of the sequence connected to FL_1. If C_1 were directly connected to the collector of Tr_2, it would, together with the input resistance of Tr_3, greatly increase the rise time of the collector potential of Tr_2.

To overcome this, an emitter follower Tr_1 is inserted between Tr_2 collector and C_1 which provides a much lower impedance for C_1 and Tr_3 to shunt. To begin with, C_1 is charged to the supply voltage minus the base potential of Tr_3. When Tr_2 is switched on, its collector rises almost to the voltage of the positive rail carrying the emitter of Tr_1 with it. Because the charge on C_1 cannot change instantaneously, the base of Tr_3 is taken to almost twice the potential of the positive rail above earth which cuts off its collector current until such time as the charge has sufficiently leaked away via R_5

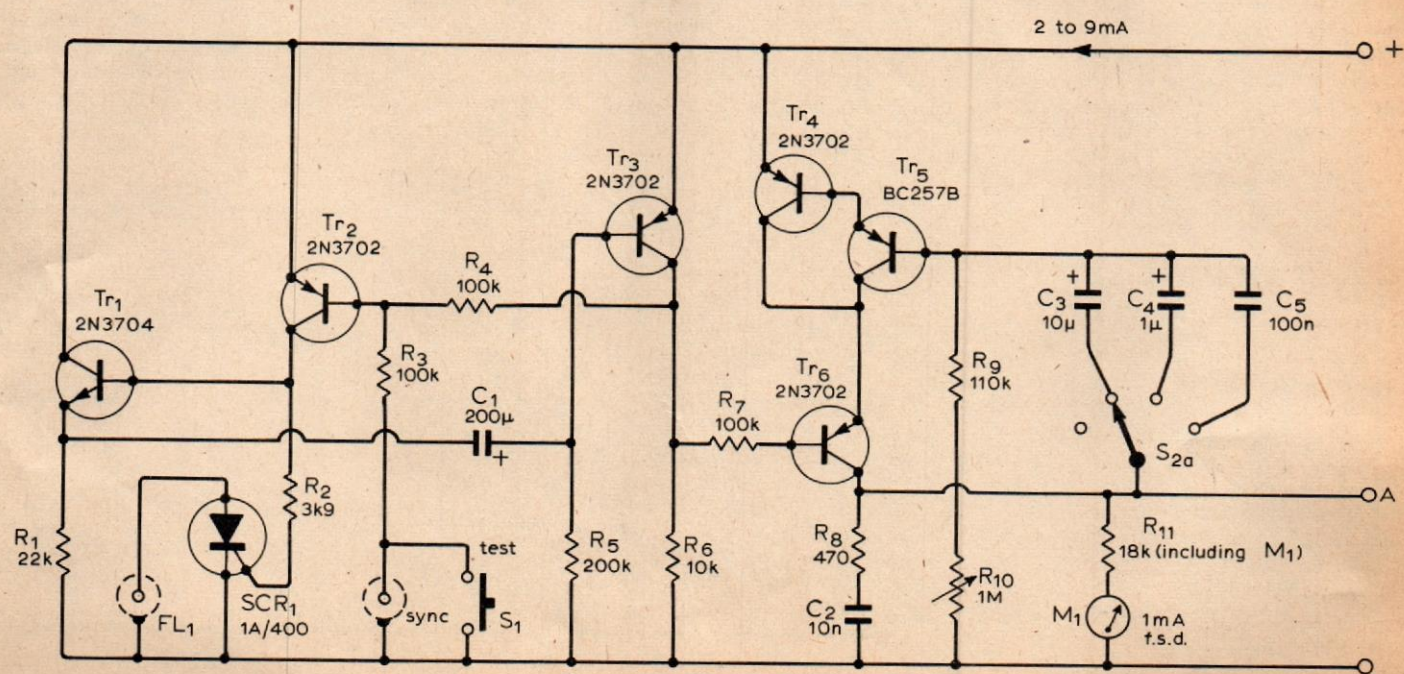


Fig. 1. Camera shutter contacts trigger the monostable circuit which turns on the thyristor to provide the first flash trigger. If C_1 were directly connected to Tr_2 collector, rise time would be too great. Timing circuit provides ramp output at A.

to allow it to conduct once more. The time this takes, ignoring the emitter-collector voltages of Tr_1 and Tr_2 and the base-emitter potential of Tr_3 which are small compared to the supply voltage, is

$$t \approx C_1 R_5 \log_e (2V_{cc}/V_{cc}) \approx 0.69 C_1 R_5$$

When the base of Tr_3 is biased to cut off its collector falls to earth potential and negatively biases the base of Tr_2, holding it in the conducting state. When the charge on C_1 has sufficiently leaked away to allow Tr_3 to conduct once more, its collector rises until it is within 0.2 volts of the positive rail, which is sufficient to cut off Tr_2 through R_4. The circuit now holds this condition until another negative pulse is applied to Tr_2 base.

The timing circuit is a transistor version of a Blumlein integrator, more usually referred to as a Miller integrator. A basic circuit is shown in Fig. 2 using an n-p-n transistor for ease of explanation although the final circuit makes use of p-n-ps so that a positive going ramp is obtained.

At the start, the switch S is open, the capacitor C is charged to a potential of $V_{cc} - V_{eb}$ and a current flows through R equal to $(V_{cc} - V_{eb})/R$. When the switch is closed the immediate tendency is for a collector current to flow through R_L equal to $(V_{cc} - V_{ce}\,\text{sat.})/R_L$, provided the current in R is large enough to cause saturation in the transistor, and for the collector to take up a position about 0.2 volts above the negative rail. If that were to happen, the collector current would be cut off because the voltage across C cannot change instantaneously and any change in collector potential is immediately transferred to the base. Obviously this is impossible, so a condition develops where the base potential is just sufficiently positive to allow C to discharge through the transistor, which allows the collector voltage to fall slowly in a linear manner. This occurs for the following reason. Electron current flows away from the base via R and into the base from C. The result is a difference current which is the base current during the discharge.

The greater the current gain in the transition, the smaller the change in base current required to satisfy the voltage change at the collector as the capacitor discharges. The base current is thus very small compared to I_R and changes very little during the discharge. The smaller the base current is, the smaller the difference between I_R and I_C and the more constant V_{eb}. A constant voltage across R produces a constant current through it; therefore the nearer I_C approaches I_R the closer it comes to constancy. As constant current flowing into or out of a capacitor raises or lowers the potential across it, according to the basic expression $V = It/C$, it follows that the voltage across C falls linearly with respect to time. As one plate is connected to a hardly changing V_{eb} and the other plate is joined to the collector, the collector voltage must fall in like manner.

When the capacitor is completely discharged, the collector potential is equal to V_{eb}, the base current is again provided by R only and the collector falls a fraction further to $V_{ce}\,sat.$

If the switch is now opened, C recharges via the base of the transistor and R_L.

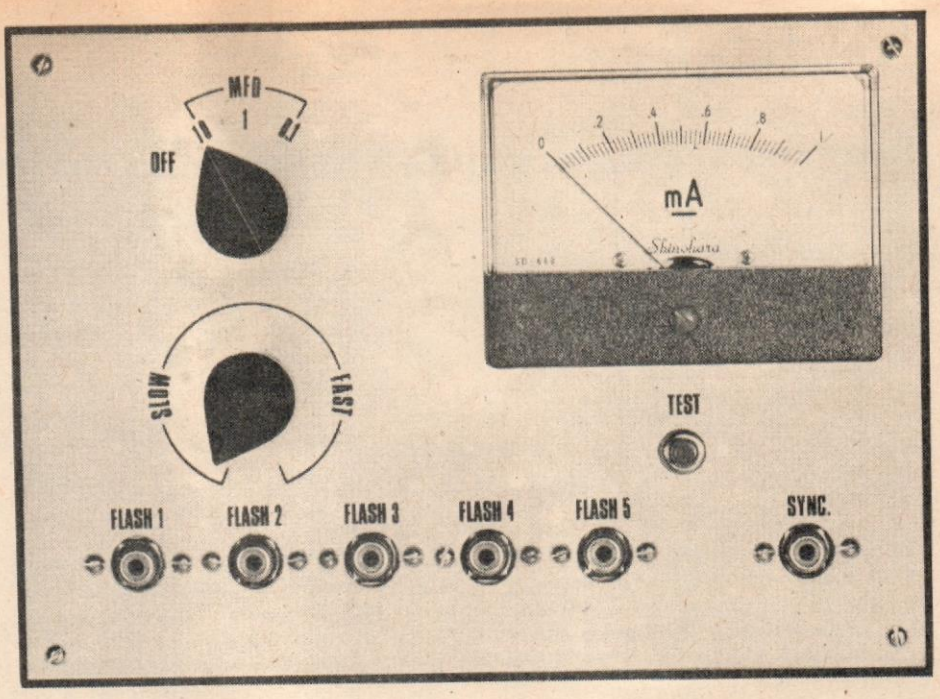
The time for the linear portion of the voltage ramp can be expressed essentially by

$$t = \frac{VC}{I_C} \approx \frac{(V_{cc} - V_{eb})C}{(V_{cc} - V_{eb})/R}$$

$$\approx CR \text{ seconds, as } I_C \approx I_R.$$

Because linearity is dependent upon a high value of beta, a Darlington pair is used in the final circuit and Tr_6 acts as the switch. Leakage in the capacitor, represented by R_C in Fig. 2, must be kept to a minimum because it provides a shunt negative feedback path, bypassing the capacitive loop; reducing the gain of the amplifier and consequently the linearity of the ramp. For this reason, tantalum capacitors are recommended for C_3 and C_4 if the expense of polyester types is considered prohibitive.

Linearity also depends on a high voltage gain which is a product of $h_{FE} i_b R_L$. This makes the choice of R_L a compromise as h_{FE} and R_L are interdependent. Too large a resistance could limit the collector current to a value which would seriously reduce the



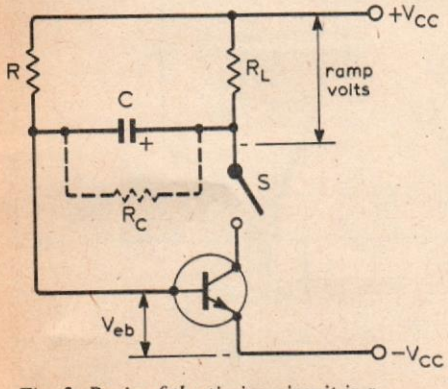


Fig. 2. Basis of the timing circuit is a Blumlein (Miller) integrator, the linear portion of the ramp being about CR seconds long.

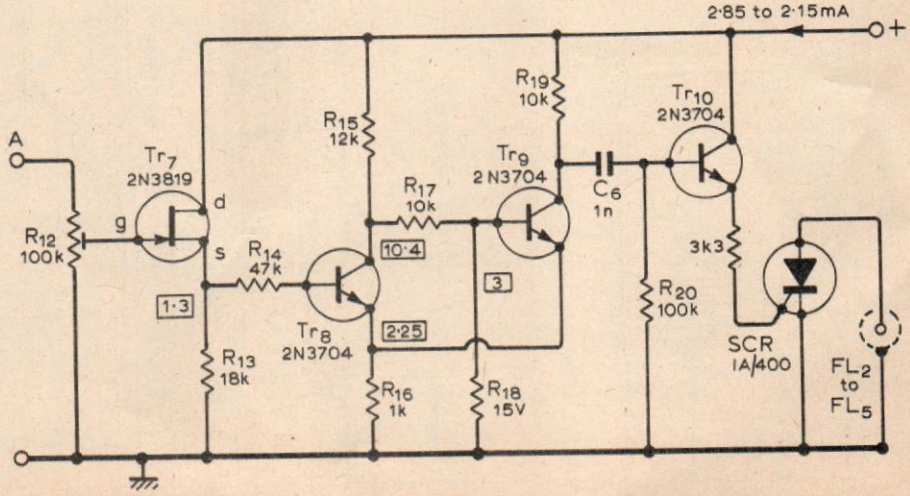


Fig. 3. Four voltage-operated switches, all identical to this circuit, are set to trip at different points of the ramp waveform.

current gain factor. This is especially so in the present circuit where the collector current of Tr_5 can only be a fraction of that of Tr_4. The effective load resistance of Tr_4 and Tr_5 is made up of R_{11} and four R_{12}s in parallel and works out at approximately 10.5kΩ, giving adequate linearity for the purpose with the transistors shown, though no doubt others would give an equal or even better performance. The ones chosen had the merit of being inexpensive and were close to hand.

The meter provides a quick check of the correct functioning (or otherwise) of the timer; enables, on the 10μF range, the time of the ramp to be compared with the duration of the event to be photographed; and facilitates the setting up of the voltage level switches.

The circuit of a switch is shown in Fig. 3 and as four are required the components are labelled A to D. The switches are arranged to operate sequentially at equal intervals during the ramp. Transistors Tr_8 and Tr_9 are connected as a Schmitt trigger and the potential at A is applied to the base of Tr_8 via an f.e.t. source follower which serves to isolate the switches one from another and prevents variable shunting of R_{11} by the change in input resistance of Tr_8 as it changes state.

With A at zero potential, Tr_8 is non-conducting and Tr_9 is in saturation. Tr_8 emitter potential is provided by the emitter current of Tr_9 flowing through R_{16} and is normally about 2.25 volts. When the voltage at the base of Tr_8 is sufficient to initiate conductance, its first effect is to raise the emitter voltage (emitter follower action), but this tends to bias off Tr_9 thus reducing the current which provided the voltage in the first place. As Tr_8 base continues to rise, its collector voltage falls, reducing the base voltage of Tr_9 and consequently its emitter current. This reduces the emitter voltage of Tr_8 which causes still heavier conduction until such time as saturation occurs and its collector potential is very little more than its emitter. When this state is reached, Tr_9 base is at a lower potential than its emitter, due to the divider action of R_{17} and R_{18}, and is cut off.

Because the action is regenerative, the collector of Tr_9 can be raised from 2.3 volts to 19.5 volts when the base of Tr_8 reaches a critical point on the ramp which is set by adjustment of R_{12}. This voltage change is converted to a current pulse by C_6, R_{20} and the emitter follower Tr_{10}. Gate resistor limits the current peak to a value that will reliably turn on the thyristor.

A circuit that relies for its operation upon somewhat precise voltage levels obviously requires a stable supply voltage. The circuit of the battery supply and voltage regulator is shown in Fig. 4 and follows common practice. The quiescent battery current is 16mA rising to 21mA during the timing period. It is left to the constructor as to whether he fits PP3s or PP6s as a lot depends on how much one plans to use it.

Construction

If tantalum capacitors are used for C_3 and C_4 their values should be measured as the tolerance of some of them is as wide as

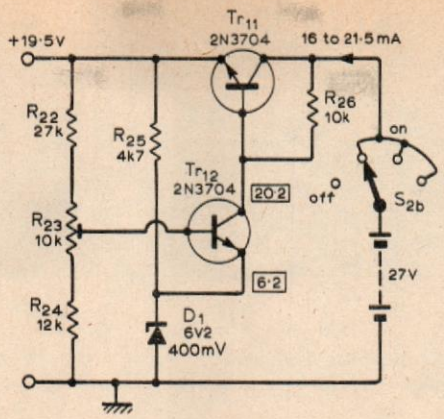


Fig. 4. Stabie battery supply circuit.

electrolytics in general (+100 −10%) and can double the time of the ramp if one is not careful. If a bridge is not available, it would be advisable, though more expensive, to use polyester types if anything like the suggested times are looked for.

The period $0.70C_1R_5$ must be longer than the period of the longest timing run, i.e. 11 seconds, for the ramp to reach maximum before Tr_6 is turned off. It can with advantage be twice as long to aid the setting of the voltage level switches and the rail voltage. Because the leakage resistance of electrolytic capacitors aids their discharge, a capacitor of 200μF is used which works out at 28 seconds but in practice gives about 20 seconds.

The circuits are made up on individual pieces of 0.15-in Veroboard (see Fig. 5) and board wiring diagrams are available from the editorial office at *W.W.*

Use is made of mounting tags broken out of a length of tag strip to secure the Veroboard to the front panel. The timer and voltage regulator assemblies are secured by means of the meter studding and the switches by the nuts and screws used to fasten the phono sockets, see Fig. 5.

When making panels for instruments I usually make a layout on a piece of white board in black drawing ink and label it with Letraset. I then make a fine negative of it and from that, a single weight bromide enlargement to the size required. A brief exposure to a 15-watt lamp at 6 to 7 feet is given to the paper before development and a light grey print with black lettering results. This is fixed to a piece of 14 s.w.g. aluminium with dry mounting tissue and a coat of clear polyurethane "varnish" is applied to the surface of the paper. When dry, the holes are cut out and the panel trimmed to size, but before trimming, the boundary lines of the panel are scored through to the aluminium surface with a sharp knife, so that a neat edge is obtained by filing as close to the line as possible. Holes are drilled small and enlarged to size with forward strokes of a file only, to avoid lifting the top surface of the paper. After cleaning off the swarf and filings with a cloth moistened with methylated spirit, I give it a final coat of polyurethane, paying particular attention to the edges of the panel and the insides of the holes. In this way, a neat, durable, and professional appearance is given to the finished product if a little care is taken.

Setting up

To set the rail voltage, select the 0.1-μF range and press the test button. The meter will move rapidly to full scale and hold for about 20 seconds. This gives time to adjust R_{23} so that the needle rests just short of the far stop which represents approximately 18.5 volts.

Setting up the switches is most easily done if a small electronic flash unit is used. Firstly, select the 10-μF range, and to enable a more precise observation of the exact point at which the switch triggers, connect an 8-μF capacitor in parallel, temporarily. Press the button and make sure that the ramp time does not exceed the turn on time of Tr_6. If

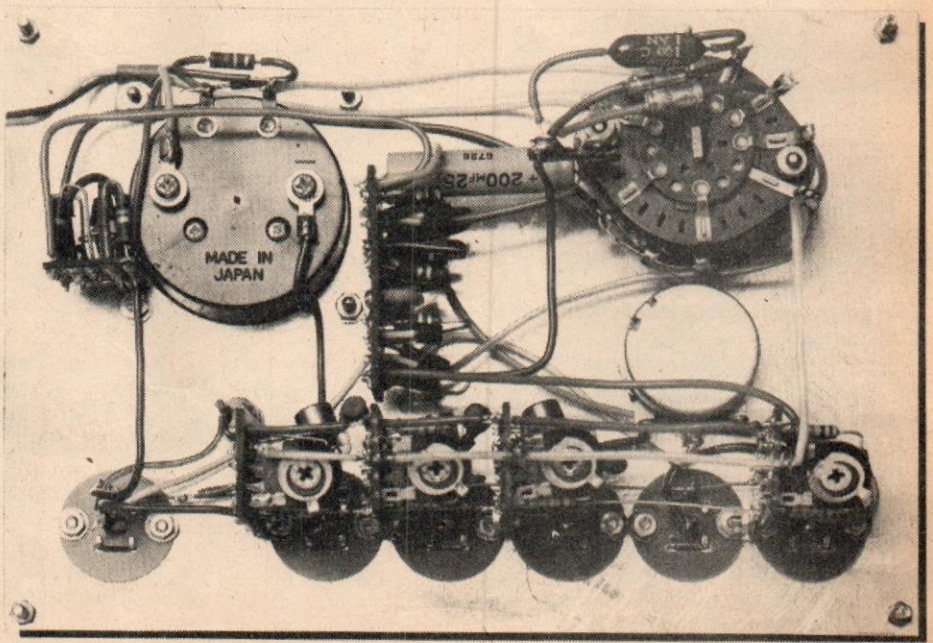


Fig. 5. Four circuit boards of voltage-operated switches are mounted vertically above the trigger sockets. Send s.a.e. to WW for board wiring diagrams.