stall the watchdog timer (IC43) and JU15, and set the timeout for approximately 1 second (by substituting a 1-megohm resistor for R19). Do not install any other IC's. Apply power and confirm that the oscillator is operating by observing the signal at pin 56 of the microprocessor. Pin 24 of the microprocessor should go low each time S2 is pressed and each time IC43 times out. If those operations appear normal, remove power and install a ROM with a simple JMP −1 instruction where the reset vector normally goes (FØØØ:FFF Ø). Now, if all is well, you should see a nice tight loop by observing the address bus on an oscilloscope.

You can trigger your scope easily on that signal and actually use your scope as a poor-man's bus analyzer. Observe the RD line and select a cycle for analysis. Note the exact position of the RD strobe on your scope. Now probe the DØ line. Is it high or low when RD is low? Write it down. Do the same for all of the data and address lines. You have just decoded the entire state of the microprocessor for that RD cycle: the address being read and the next instruction in the ROM.

Next, fill a ROM with NOP's (Ø9Øh) and execute a jump to the beginning of the ROM. Scope the address lines. You should see a ØlØl sequence on AØ, a ØØll sequence on A1 and so on. Each address line will appear at half the frequency of the preceding line.

What if things are not as they should be? This is where the watchdog timer (IC43) comes to our rescue. Set it for a timeout of a few milliseconds, trigger your scope on the reset pulse from the microprocessor (pin 57), and observe the first few RD cycles at the ROM. Here are a few things to look for:

1. Is the chip select line to the ROM (pin 20) active? If not, there could be a problem in the address-decoding circuitry or the address latches. Perhaps one or more of the microprocessor signals ALE, DEN, DT/R, RD, or WR are lost.

2. Are the address lines correct? They should all be high except for AØ–A3; those lines will toggle. Watch for voltage levels that are neither high nor low; two lines may be shorted, or the address decoder may not be functioning correctly.

3. Decode the first few instructions on the data bus. Do they accurately represent the contents of the ROM? Are the voltage levels correct? Incorrect voltage levels are caused by bus contention, shorted traces, ungrounded IC's, unpowered IC's, capacitors attached to data lines, and many others we have not (yet) had the pleasure of encountering.