CPLD autonomously powers battery-powered system

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A common industrial and consumer application is a system that samples an environmental condition, such as GPS (global-positioning-system) location, voltage, temperature, or light, at a wide interval, such as once every minute. This type of system is becoming increasingly wireless and battery-powered; it wakes up every minute, takes a sample, transmits data to a central data-collection terminal, and then goes back to sleep. This Design Idea uses a small portion of an Altera (www.altera.com) EPM240-T100 CPLD (complex programmable-logic device) with a few discrete capacitors, resistors, diodes, and MOSFETs to autonomously wake a CPLD-based system from a full power-down state to an on state using an RC-timer circuit. This approach results in minimal

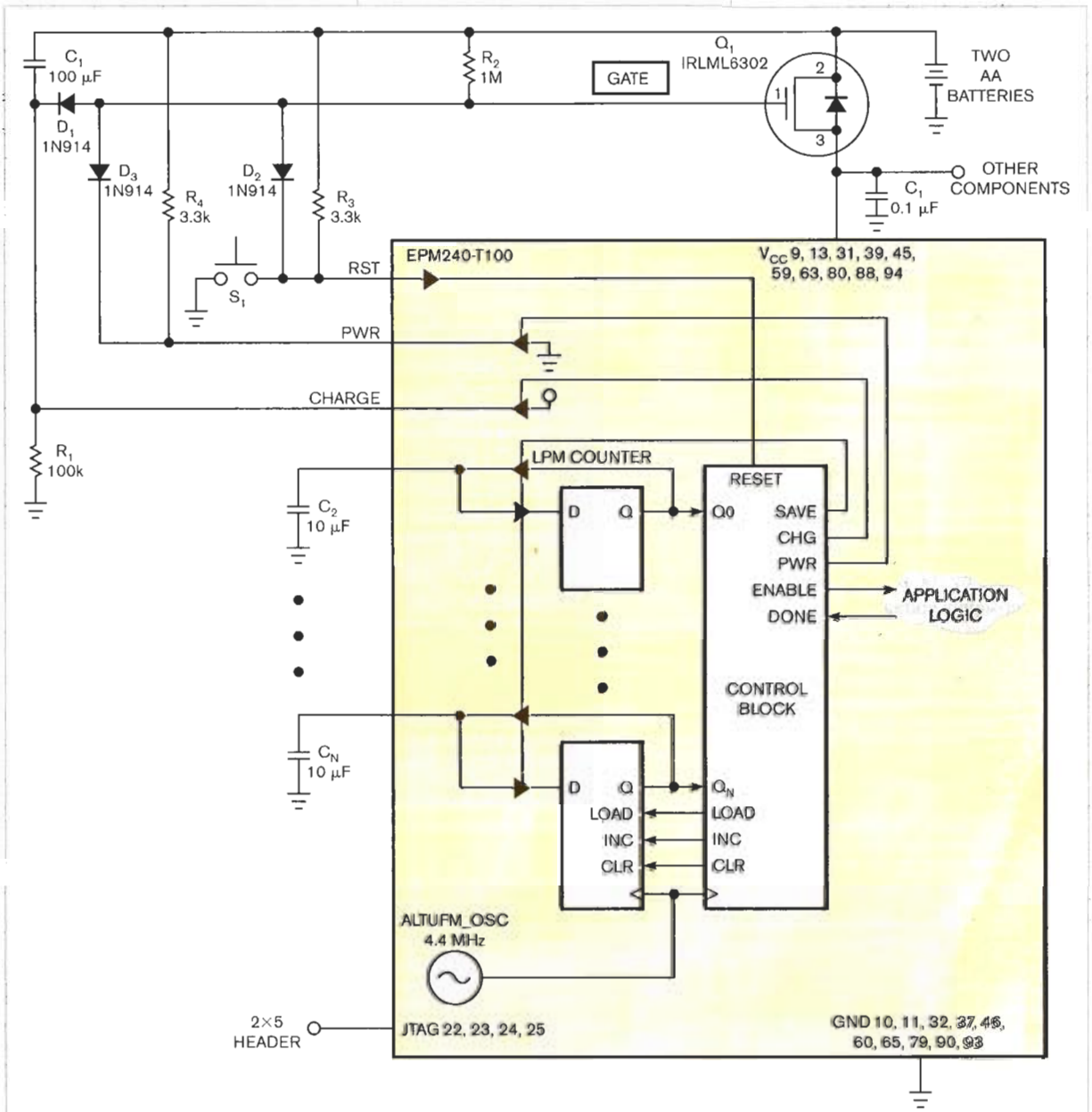

Figure 1 The CPLD comprises a control block, a 4.4-MHz internal oscillator, a 3-bit register, and six I/Os.

power consumption during samples when the power is on and between samples when the system, except for the RC circuit, is effectively off.

Figure 1 shows the basic CPLD on/off timer. Q_1, an IRLML6302 P-channel MOSFET, is the power-control switch for the system. When the gate node is at V_{CC}, which R_2 pulls up, the power to the CPLD and the entire system is off, leaving only the RC circuit to use a minute amount of power. The CPLD comprises a control block, a 4.4-MHz internal oscillator, a 3-bit register, and six I/Os.

Figure 2 shows the state machine of the control block. The outputs in the state box are high, and all others are low. The dashed line from power-down to power-up represents the time delay, which the RC circuit comprising R_1 and C_1 measures when the system is off. Switch S_1 turns on and initializes the circuit. When S_1 closes, D_2 drives the gate node low, consequently turning on Q_1 when the gate voltage is 0.7V below V_{CC}. The EPM240-T100 is then operating in the power-up state less than 200 µsec after Q_1 applies power. The power-up state drives the power node low, which holds the gate voltage at 0.7V, keeping Q_1 on after the switch is open. The power-up state also drives the charge node to V_{CC}. This action charges the negative terminal of C_1 to V_{CC}. Because reset=0, the control block goes to the reset state and Register 1 gets reset. Once S_1 opens, the control block goes to the enable state and drives the enable signal to one.

The sample-and-transmit circuit then begins operation and drives the done signal to zero. Once the sample and transmit are complete, the done signal becomes one, and the control block goes to the save state. The save state charges capacitors C_2 to C_N based on the value in Register 1. The save state is active for 100 µsec, allowing the outputs to fully charge the 10-µF capacitors. After 100 µsec, the control block goes to the power-down state, which stops driving the charge and power nodes. R_4 pulls the power node high, leaving R_2 to pull up the gate node.

CAPACITORS C_2, C_3, AND C_4 ACT AS NONVOLATILE MEMORY, STORING THE COUNT OF PREVIOUS POWER CYCLES.

Once the gate node reaches $V_{CC} - V_{TQ1}$ at about 2.3V, Q_1 shuts off power to the system. All EPM240-T100 I/O is in a high-impedance state and does not affect the gate or charge nodes. The charge node starts at V_{CC} and begins to discharge through R_1 once power is off. Once the charge node drops to 2.3V, D_1 pulls down the gate node. Once the charge node reaches 1.6V, the gate node reaches 2.3V, and Q_1 turns on. The time for Q_1 to turn on is slightly less than the τ of R_1 and C_1. Off time equals $R_1 \times C_1 = 100{,}000 \times 0.0001 = 10$ sec.

The device powers up in the power-up state but moves quickly to the sample state. The sample state reads the value on capacitors C_2, C_3, and C_4. These capacitors act as nonvolatile memory, storing the count of previous power cycles. If the Register 1 value sampled on C_2 through C_4 is less than 7, then the control block goes to increment, and the Register 1 value increments by one. Then, the control block again goes to the save state to charge C_2 through C_4 to a new binary value, 001. The device powers down again. On the eighth power cycle, or about 80 seconds after power-up, the control block moves to the enable state, thus enabling a new sample-and-transmit sequence. This process repeats every 80 seconds. You can change the period by adjusting C_1 and R_1 and by changing the Register 1 size and count between enable cycles. Based on an 80-second period comprising eight smaller power-up samples, test, and power-down cycles, the duty cycle for power is less than 3%; therefore, this approach increases battery life by as much as 33 times. EDN

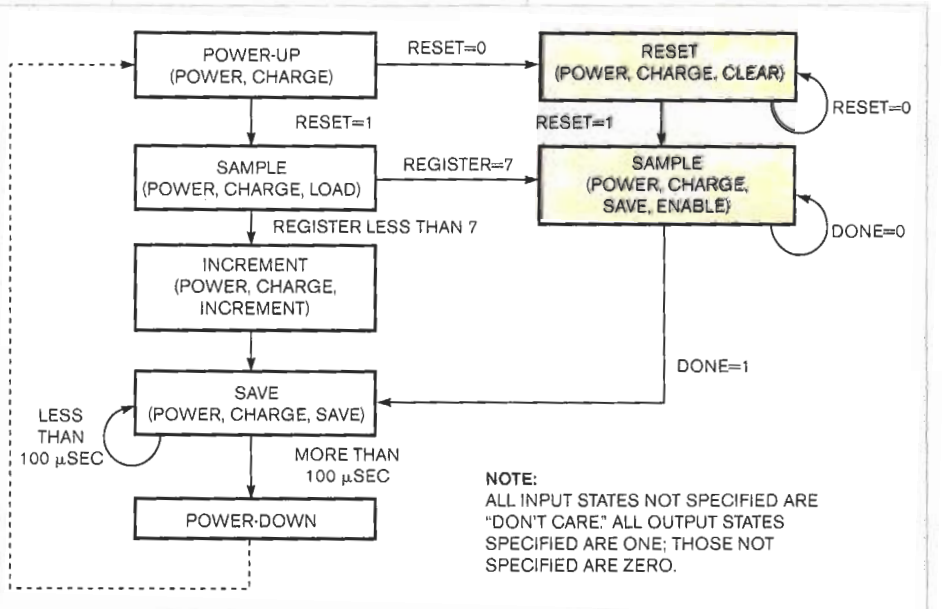

Figure 2 In the state machine of the control block, the outputs in the state box are high, and all others are low.

constant comprising the inductance under test and resistors R_L and R_R. The time the waveform takes to change its state is directly proportional to the inductance, and, for one-half cycle, it approaches $T_{HALF}=L/100$. The period of a full oscillation cycle is twice that amount, or $T_{FULL}=L/50$. Solving for the inductance yields $L=50\times T_{FULL}$. As an alternative, the frequency is inversely proportional to the inductance, or $f_{OSC}=50/L$. Using a frequency counter allows measurement of inductance as $L=50/f_{OSC}$.

The circuit's finite switching speed of approximately 10 nsec imposes a lower floor of 1 µH on its measurement range. You can measure a small inductance by connecting it in series with a larger inductance, noting the reading, measuring the larger inductance alone, and subtracting the two measurements.

Although the circuit imposes no upper limit on inductance values, when the inductor's ESR (equivalent-series resistance) exceeds approximately 70Ω, the circuit stops oscillating and reverts to bistable operation. The circuit measures values of all inductors and transformer windings except for small, low-frequency iron-core devices that present a high ESR. For greatest accuracy, use a low-input-capacitance instrument to measure the frequency of oscillation.

A single NiCd (nickel-cadmium) or NiMH (nickel-metal-hydride) rechargeable cell provides power for the circuit. These cells present a relatively flat voltage-versus-time discharge characteristic that enhances the circuit's measurement accuracy. The circuit consumes approximately 6 mA during operation. **EDN**

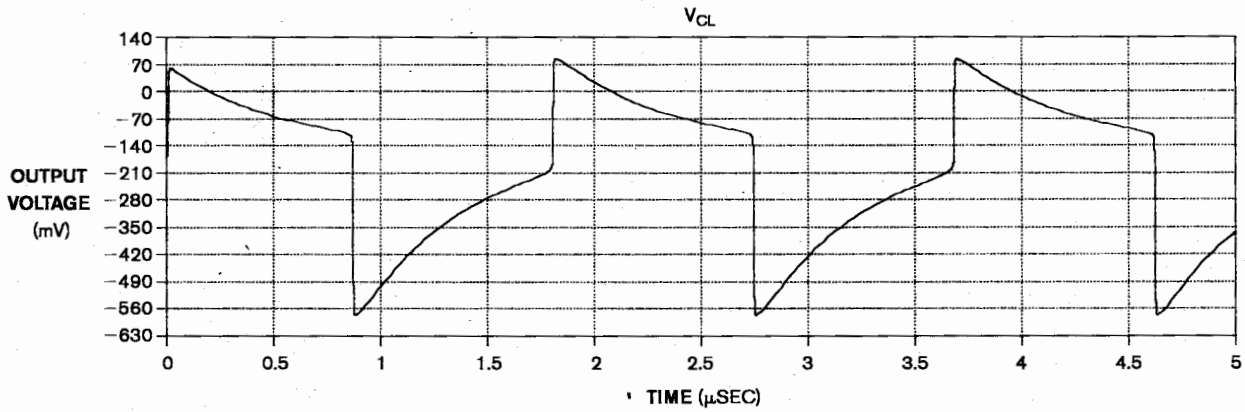

Figure 2 Testing an inductor with a value of approximately 100 µH produces this output waveform.