BY JIM WILLIAMS AND MARK THOREN LINEAR TECHNOLOGY

Novel measurement circuit eases battery-stack-cell design

A TRANSFORMER AND DIODE ON EACH CELL ALLOWS ISOLATED MEASUREMENT.

Automobiles, aircraft, marine vehicles, uninterruptible power supplies, and telecom hardware use series-connected battery stacks. These stacks of individual cells may contain many units, potentially reaching hundreds of volts. In such systems, it is desirable to accurately determine each individual cell's voltage. Obtaining this information in the presence of the high common-mode voltage that the battery stack generates is more difficult than you might suppose.

The "battery-stack problem" has been around for a long time. Its deceptively simple appearance masks a stubborn problem. Designers have tried various approaches to isolated-cell-voltage measurement with varying degrees of success (see **sidebar** "Some battery-cell-measurement techniques just don't work" at the Web version of this article at www.edn.com/ms4255).

Figure 1's voltmeter measures a single-cell battery. Beyond the obvious benefits, the arrangement works because no voltages other than the single cell lie in the measurement path. The ground-referred voltmeter encounters only the voltage it is measuring.

Figure 2's stack of series-connected cells is more complex. The voltmeter must switch between the cells to determine each cell's voltage. Additionally, the voltmeter, normally composed of relatively low-voltage breakdown components, must withstand input voltages relative to its ground terminal. This common-mode voltage may reach hundreds of volts in large series-connected battery stacks, such as those in an automobile. Such high-voltage operation is beyond the voltage-breakdown capabilities of most practical semiconductor components, particularly if the application requires accurate measurement. The switches present similar problems. Attempts at implementing semiconductor-based switches encounter difficulty due to voltage-breakdown and leakage limitations. A practical method is necessary that would accurately extract individual cells' voltages and reject common-mode voltages. This method should not draw any battery current and should be simple and economical.

Figure 3's concept addresses these issues. To determine battery voltage, $V_{BATTERY}$, a pulse excites a transformer, T_1, and records its primary clamp voltage after settling occurs. The diode and the battery-voltage shunt primarily set this clamp voltage and similarly clamp T_1's secondary. The diode and a small transformer term are predictable errors, and the circuit's final stage substracts them out, leaving the battery voltage as the output.

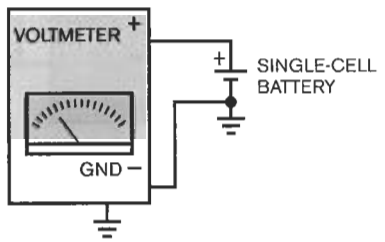

Figure 1 Common-mode voltage does not affect a voltmeter measuring a ground-referred single cell.

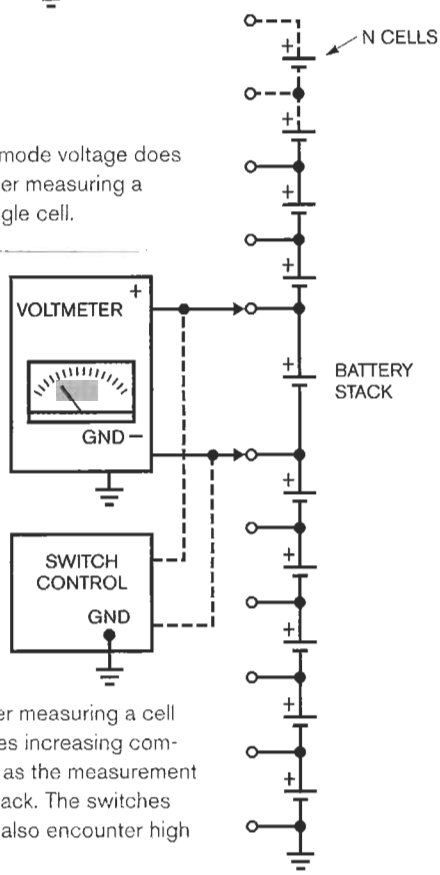

Figure 2 A voltmeter measuring a cell in a stack undergoes increasing common-mode voltage as the measurement proceeds up the stack. The switches and switch control also encounter high voltages.

DETAILED CIRCUIT OPERATION

Figure 4 details the transformer-based sampling voltmeter. It closely follows **Figure 3** with some minor differences, which

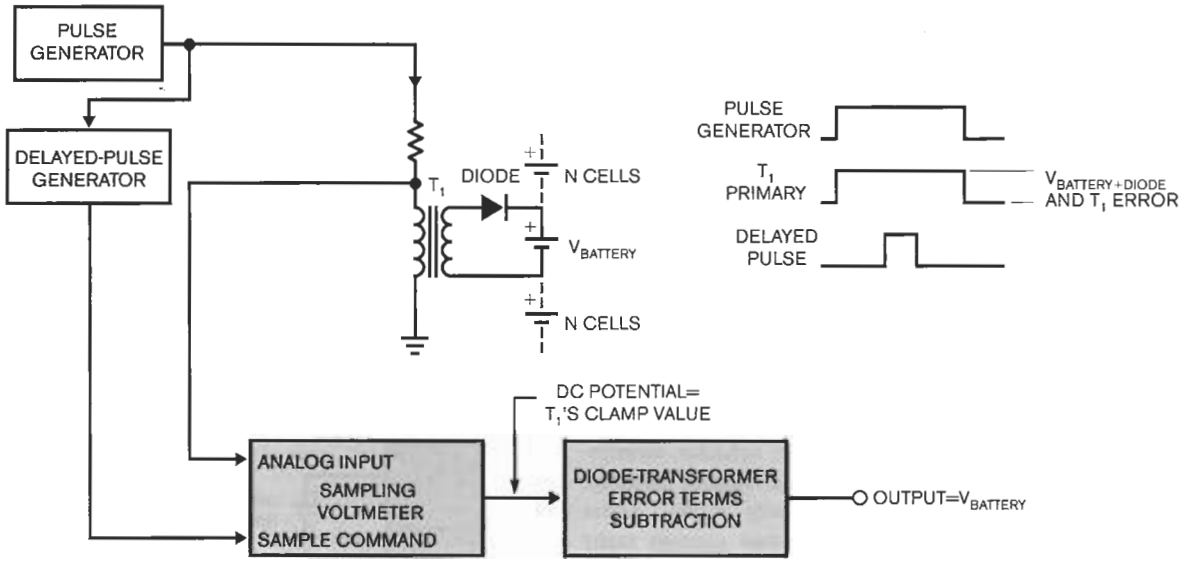

Figure 3 A transformer-based sampling voltmeter operates independently of high common-mode voltages. The pulse generator periodically activates T_1. The delayed pulse triggers a sampling voltmeter, capturing T_1's clamped value. Residual error terms are corrected in the following stage.

this article later describes. The pulse generator produces a 10-μsec-wide event (Trace A, **Figure 5**) at a 1-kHz repetition rate. The pulse generator's low-impedance output drives T_1 through a 10-kΩ resistor and triggers the delayed-pulse generator. T_1's primary, Trace B, responds by rising to a value representing the sum of the diode voltage and the battery voltage, along with a small fixed error that the transformer contributes. T_1's primary becomes clamped at this value. After a time, the delayed pulse, Trace C, generates a pulse, Trace D, closing S_1, allowing C_1 to charge toward T_1's clamped value. After a number of pulses, C_1 assumes a dc level identical to the voltage on T_1's clamped primary. A_1 buffers this potential and feeds differential amplifier A_2. A_2, operating at a gain near unity, subtracts the diode- and transformer-error terms, resulting in a direct reading of battery-voltage output.

Accuracy critically depends on transformer-clamping fidelity over temperature and clamp-voltage range. The carefully designed, specified transformer yields **Figure 6**'s waveforms. Primary, Trace A, and secondary, Trace B, clamping details appear at a highly expanded vertical scale. Clamping flatness is within millivolts; trace-center aberrations derive from S_1-gate feedthrough. Tight transformer-clamp coupling promotes good performance. Circuit accuracy at 25°C is 0.05% over a 0 to 2V battery range with 120 ppm/°C drift, degrading to 0.25% at a battery voltage of 3V. Designers of this circuit used a floating variable-potential battery (see **sidebar** "Floating-output, variable-potential battery simulator" at the Web version of this article at www.edn.com/ms4255).

Several details aid circuit operation. The circuit substitutes the transistor's base-emitter voltage for diodes, providing more consistent initial matching and temperature tracking. The 10-μF capacitor at Q_1 maintains low impedance at frequency, minimizing cell-voltage movement during the sampling interval. Finally, synchronously switched Q_2 prevents T_1's negative-recovery excursion from deleteriously influencing S_1's operation.

This approach's advantage is that its circuitry does not encounter high common-mode voltages; T_1 galvanically isolates the circuit from common-mode potentials associated with the battery voltage. Thus, you can employ conventional low-voltage techniques and semiconductors.

MULTICELL VERSION

The transformer-based method is inherently adaptable to the multicell-battery-stack-measurement problem. **Figure 7**'s conceptual schematic shows a multicell-monitoring version. Each channel monitors one cell. You can read any channel by biasing its appropriate enable line to turn on a FET switch, enabling that channel's transformer. The hardware for each channel typically includes only a transformer, a diode-connected transistor, and a FET switch.

AUTOMATIC CONTROL AND CALIBRATION

This scheme suits digital techniques for automatic calibration. **Figure 8** shows pulse generators, calibration channels, and measurement channels, which feed **Figure 9**'s PIC-16F876A microcontroller. As before, even though the cell stack may reach hundreds of volts, the transformer's galvanic isolation allows the signal-path components to operate at low voltage. The design includes an automatic calibration-circuit microcontroller and reset sections (**Figure 9**) and an automatic calibration-circuit USB interface for development only (**Figure 10**).

A further benefit of processor-driven operation is the elimination of **Figure 4**'s base-emitter-voltage diode-matching requirement. In practice, engineers tested a processor-based

board at room temperature with known voltages at all input terminals. They then read the channels, which furnished the information necessary for the processor to determine each channel's initial base-emitter voltage and gain. The engineers then stored these parameters in nonvolatile memory, permitting a one-time calibration that eliminates both base-emitter-voltage-mismatch- and gain-mismatch-induced errors.

Channels 6 and 7 provide 0 and 1.25V reference voltages, representing cell-voltage extremes. The room-temperature values reside in nonvolatile memory. As temperature changes occur, you use readings from channels 6 and 7 to calculate a change in offset and a change in gain that you apply to the six measurement channels. The calibration continues as temper-

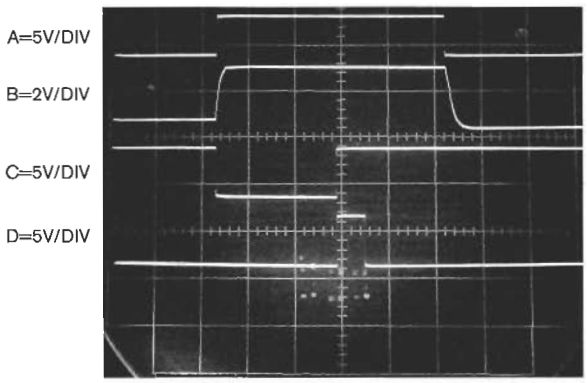

Figure 5 Figure 4's waveforms include the pulse-generator input (Trace A), the T_1 primary (Trace B), the 74HC123's $\overline{Q2}$ delay-time output (Trace C), and S_1's control input (Trace D). Timing ensures that sampling occurs when T_1 settles in the clamped state.

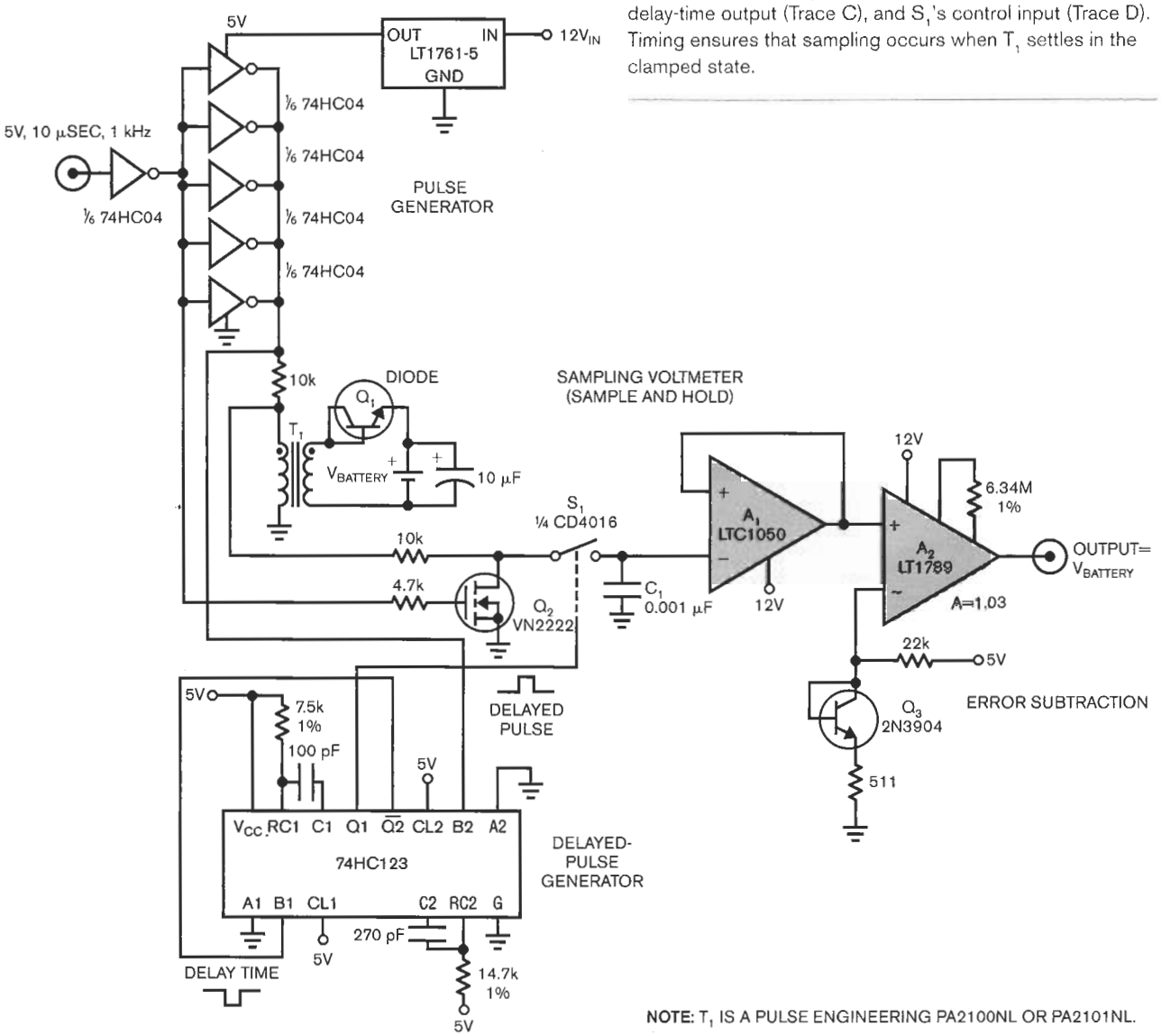

Figure . This transformer-fed sampling voltmeter closely follows Figure 3's concept. Error-subtraction terms include Q_3's compensation for Q_1 and resistor/gain corrections for errors in T_1's clamping action. Transistors Q_1, Q_2, and Q_3 replace diodes for more consistent matching. Q_2 prevents T_1's negative-recovery excursion from influencing S_1.

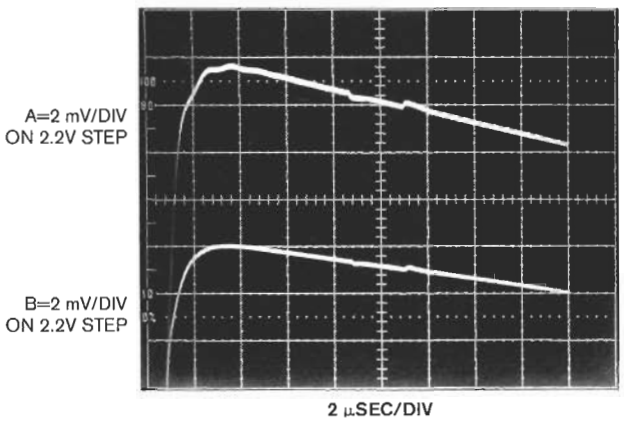

Figure 6 T_1's primary (Trace A) and secondary (Trace B) clamping details have a highly expanded vertical scale showing the primary's and secondary's clamping flatness to be within millivolts. The trace aberrations at the center derive from S_1's gate feedthrough.

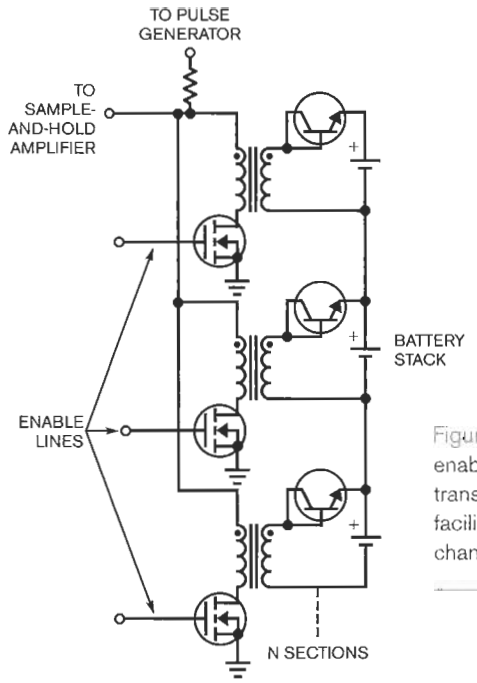

Figure 7 Adding enable lines and transistor switches facilitates multiple channels.

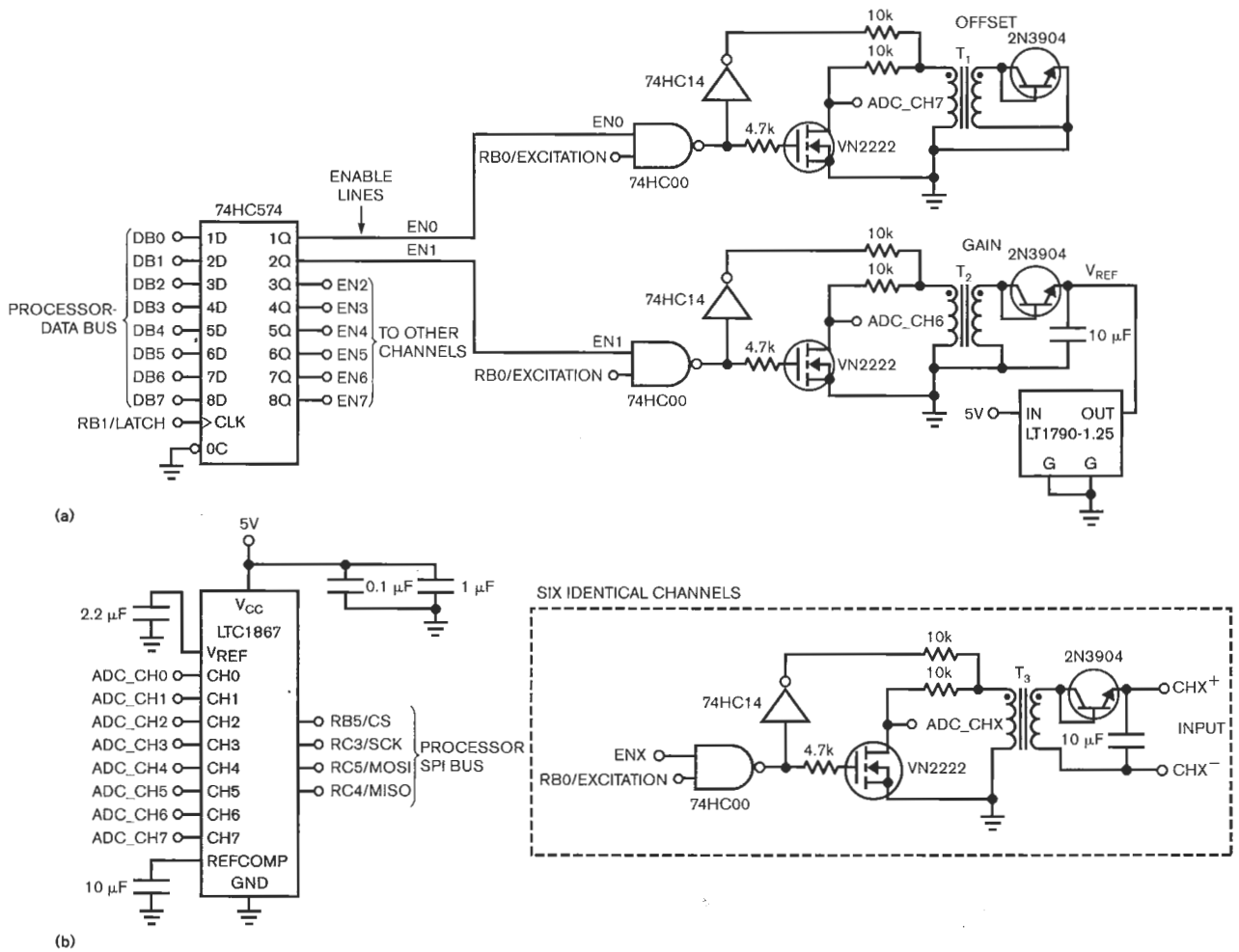

Figure ADC-calibration channels eliminate base-emitter-voltage-matching requirements (a) and compensate for temperature-dependent errors (b).

ature varies because each channel's −2-mV/°C base-emitter-voltage-drift slopes are nearly identical. Similarly, gain errors from channel to channel are nearly identical.

Because you are continuously calibrating the gain and offset, the gain and offset of the LTC1867 drop out of the equation. The only points that must be accurate are the 1.25V reference voltage, which an LT1790-1.25 IC provides, and the 0V measurement, which is easy: Just short the Channel 6 inputs together. The LTC1867 internally amplifies its internal 2.5V reference to 4.096V at the reference-comparator pin, which sets the full scale of the ADC: 4.096V for unipolar mode and ±2.048V in bipolar mode. Thus, the absolute maximum cell voltage that you can measure is 3.396V. And, because the offset measurement is nominally 0.7V at the ADC input, it is never in danger of clamping at 0V. A 0V reading results if the LTC1867 has a negative offset and the input voltage is any positive voltage less than or equal to the offset. Accuracy of the processor-driven circuit is 1 mV over a 0 to 2V input range at 25°C. Drift drops to less than 50 ppm/°C—almost three times lower than that in in **Figure 4**.

The complete firmware code, **Listing 1**, is available with the Web version of this article at www.edn.com/ms4255. The code for this circuit is a good starting point for an actual product. Data appears on a PC screen through an FTDI (Future Technology Devices International, www.ftdichip.com) FT242B USB-interface IC. The PC has FTDI's virtual-communications-port drivers installed, allowing control through any terminal program. Data for all channels continuously appears on the terminal, and simple text commands control program operation.

A timer interrupt occurs 1000 times per second. It controls the pulse generators and ADC and stores the ADC readings in an array that you can read at any time. Thus, if the main program is reading the buffer, the most out of date any reading is is 1 msec.

The software also includes automatic calibration routines. Two functions store a zero reading and a full-scale reading for all channels, including the calibration voltages you apply to channels 6 and 7, to nonvolatile memory. You subsequently use these functions to calibrate out the initial gain and offset errors, as well as the temperature-dependent errors. The entire procedure is to apply 0V to all inputs and issue a command to

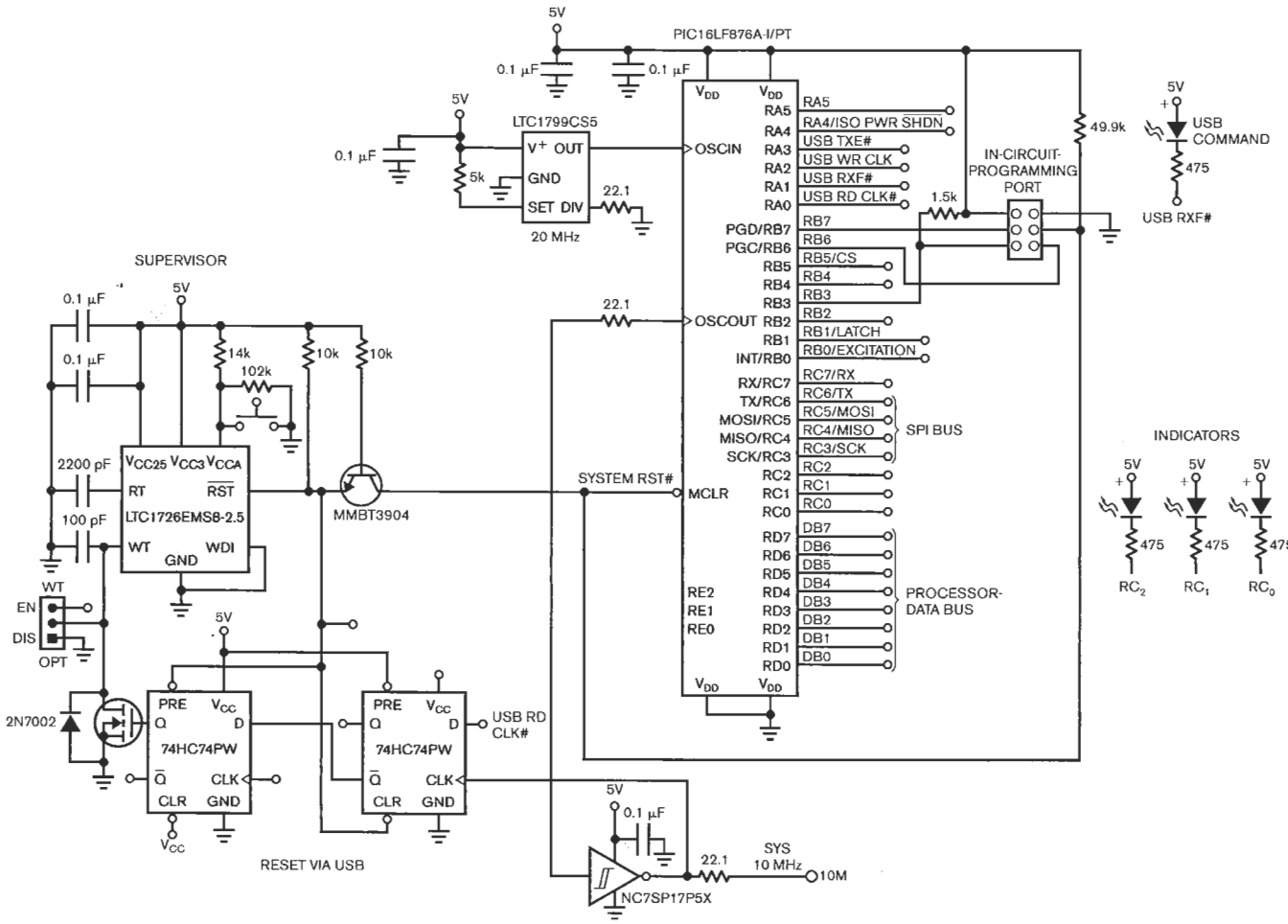

Figure 9 The design includes an automatic-calibration-circuit microcontroller and reset sections.

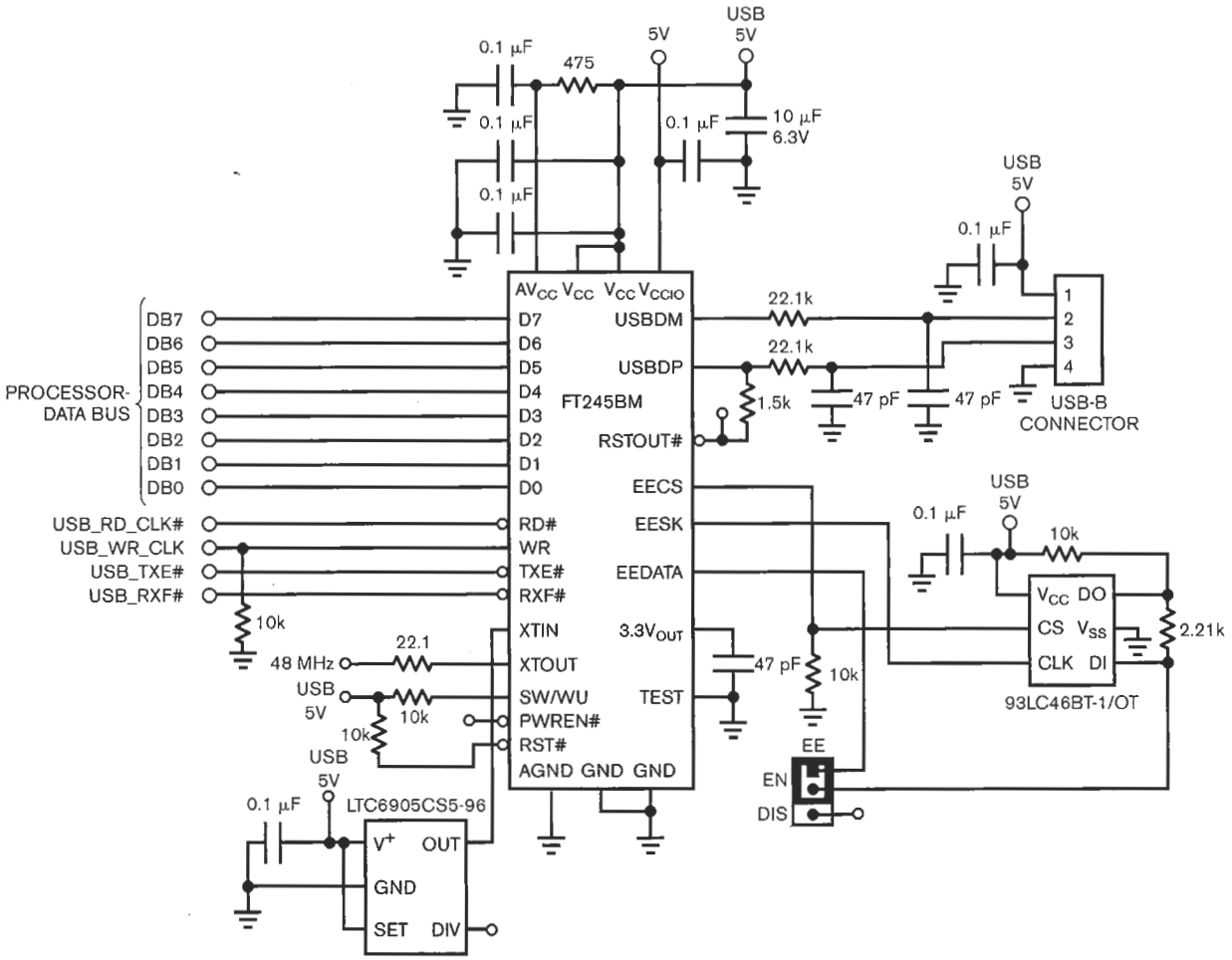

Figure 1 The design includes an automatic-calibration-circuit USB interface for development only.

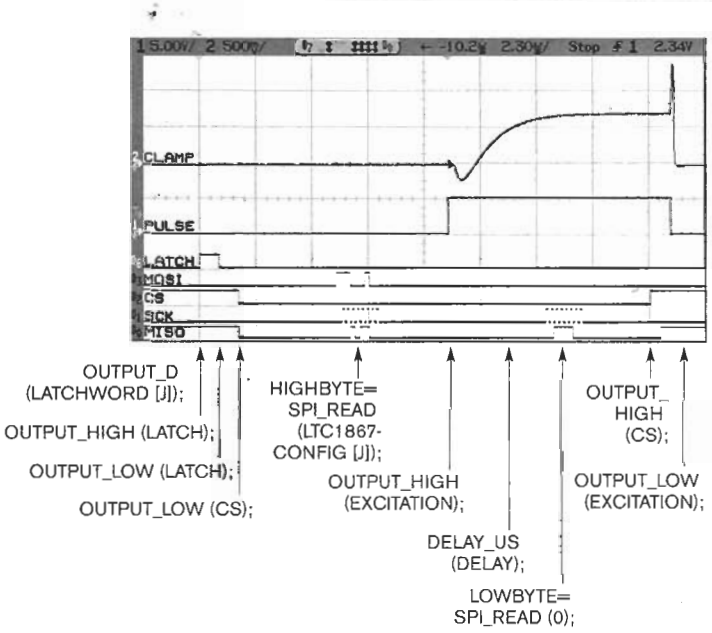

Figure 1 The interrupt-service routine monitors digital signals, excitation pulse, and clamp voltage at the ADC input along with the C code that performs these operations.

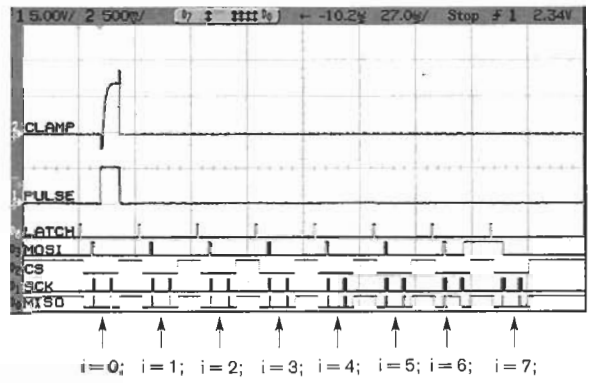

Figure 12 The interrupt-service routine scans eight channels.

store the zero calibration, then apply 1.25V to all inputs and issue a command to store the full-scale calibration. Note that this procedure is no more complicated than a basic performance test that would be part of any manufacturing process. The 1.25V factory-calibration source can be from a voltage calibrator or from a selected LT1790-1.25 that you keep at a stable temperature.

The software also includes a digital filter for testing purpos-

es. The filter is a simple exponential IIR (infinite-impulse-response) filter with a constant of 0.1. This filter reduces the noise in the readings by a factor of the square root of 10.

MEASUREMENT DETAILS

To take a reading from a given channel, the processor must apply the excitation to the transformer, wait for the voltage signal to settle out, take a reading with the ADC, and then remove the excitation. To perform these tasks, an interrupt-service routine occurs once every millisecond. For the details, see **Listing 1** at www.edn.com/ms4255. **Figure 11** shows the digital signals, excitation pulse, and clamp voltage at the ADC input along with the C code that performs these operations. Loading a 3-bit byte high into the 74HC574 latch enables individual channels.

Note that you apply the excitation after 8 bits of the LTC1867 data are read out. This situation is perfectly acceptable, because no conversion is taking place, and all of the data in the LTC1867 output register is static. Depending on the timing of the processor you use, you can apply excitation before reading any data, in the middle of reading data, or after reading the data but before initiating a conversion. If the serial clock is slow—1 MHz, for instance—applying excitation before reading any data would result in the excitation being applied for 16 µsec, which is too long. The only constraints are that the voltage at the ADC input must have enough time to settle properly and that you do not leave the excitation on for too long. **Figure 12** shows the same signals over the entire interrupt-service routine. Similar analog signals are at each transformer and the other LTC1867 inputs.

Many ways exist to add channels to this circuit. **Figure 13** shows a 64-channel concept that decodes the 64 channels in-

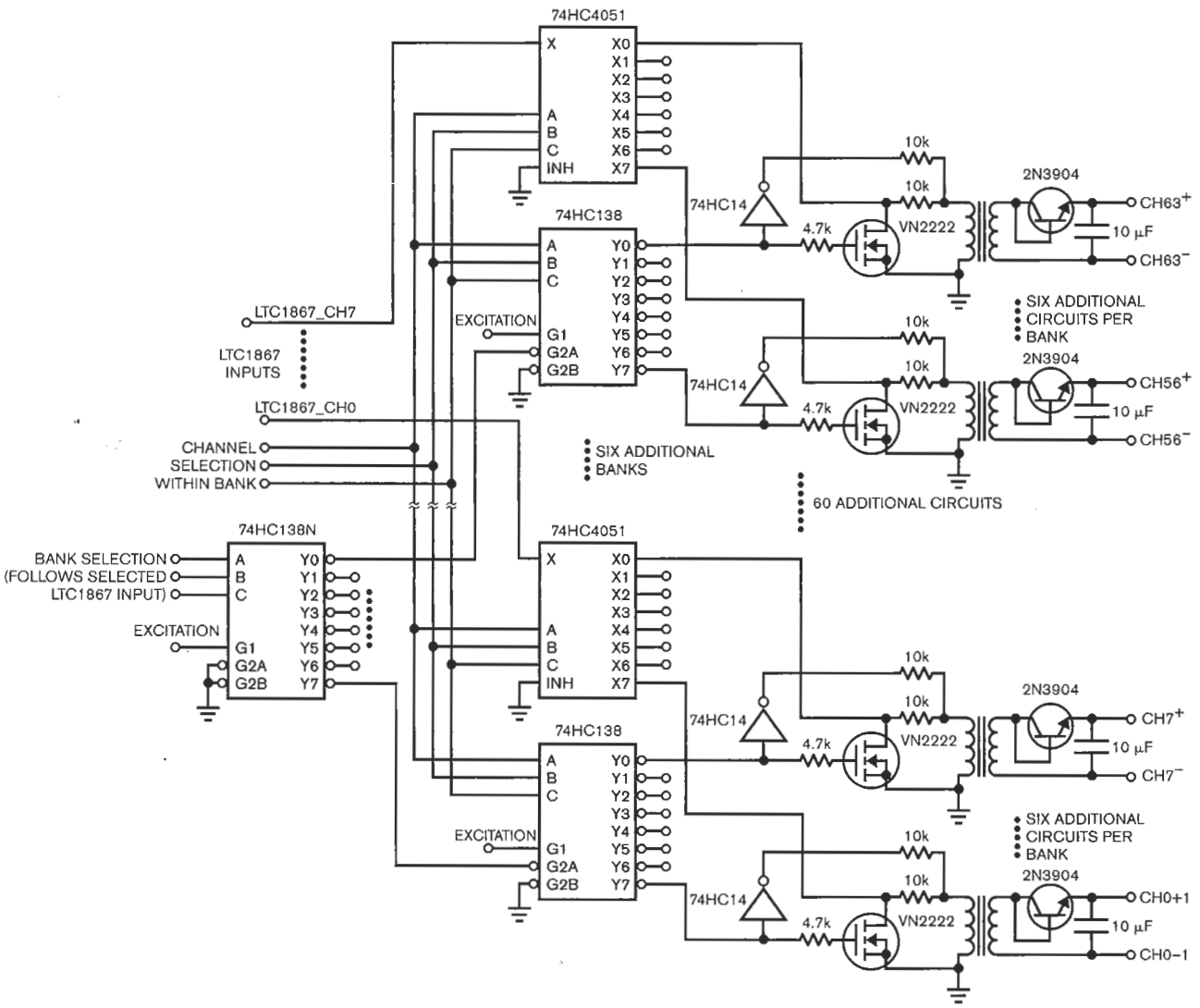

Figure A 64-channel concept decodes the 64 channels into eight banks of eight channels using 74HC138 address decoders.

to eight banks of eight channels using 74HC138 address decoders. The selected bank corresponds to one LTC1867 input that is programmed through the SPI. Some 8-to-1 74HC4051 analog switches perform the additional analog multiplexing. A single 74HC4051 feeding each LTC1867 input gives 64 inputs. The LTC1867, rather than a single-channel ADC, is still a great choice in high-channel-count applications, because it is good idea to break up multiplexer trees into several stages to minimize total channel capacitance. The LTC1867 takes care of the last stage. With a maximum sample rate of 200k samples/sec, it can digitize as many as 200 channels at the maximum 1k-sample/sec limitation of the sense transformer. That's a lot of batteries. EDN

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