Gate Drive Characteristics and Requirements for Power HEXFETs®

By STEVE CLEMENTE

Introduction

The conventional bipolar transistor is essentially a current-driven device. As illustrated in Figure 1(a), a current must be applied between the base and emitter terminals to produce a flow of current in the collector. The amount of a drive required to produce a given output depends upon the gain, but invariably a current must be made to flow into the base terminal to produce a flow of current in the collector.

The HEXFET is fundamentally different; it is a voltage-controlled power MOSFET device. A voltage must be applied between the gate and source terminals to produce a flow of current in the drain (see Figure 1b). The gate is isolated electrically from the source by a layer of silicon dioxide Theoretically, therefore, no current flows into the gate when a DC voltage is applied to it — though in practice there will be an extremely small leakage current, in the order of nanoamperes. With no voltage applied between the gate and source electrodes, the impedance between the drain and source terminals is very high, and only a small leakage current flows in the drain until the applied voltage exceeds the drain-to-source avalanche voltage.

When a voltage is applied between the gate and source terminals, an electric field is set up within the HEXFET. This field modulates the resistance between the drain and source terminals, and permits a current to flow in the drain in response to the applied drain circuit voltage.

Although it is common knowledge that HEXFET transistors are more easily driven than bipolars, a few basic considerations have to be kept in mind in order to avoid a loss in performance or outright device failure.

Gate Voltage Limitations

Figure 2 shows the basic HEXFET structure. The silicon dioxide layer between the gate and the source regions can be easily perforated if the gate-to-source voltage exceeds 20V, even if the current is limited to a very low value.

Since the perforation of this oxide layer is one of the most common causes of device failure, great care should be exercised not to exceed the gate-to-source maximum voltage rating. It should be kept in mind, also, that even if the applied gate voltage is kept below the maximum rated gate

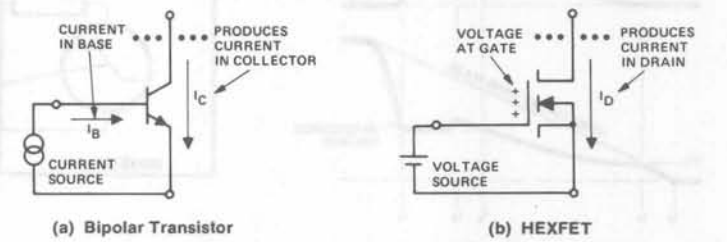


Figure 1. Bipolar Transistor is Current Driven, HEXFET is Voltage Driven

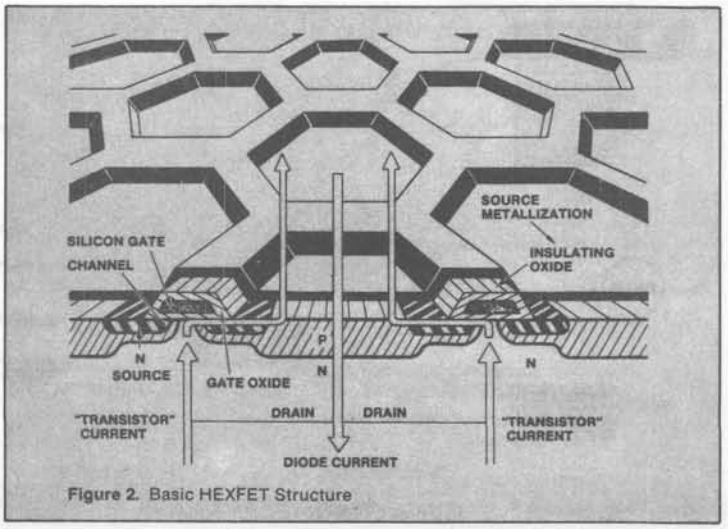


Figure 2. Basic HEXFET Structure

voltage, the stray inductance of the gate connection, coupled with the gate capacitance, may generate ringing voltages that could lead to the destruction of the oxide layer. Overvoltages can also be coupled through the drain-gate self-capacitance due to transients in the drain circuit. A small resistor or a ferrite bead located physically close to the gate lead will normally be adequate to swamp out undesired oscillations.

The Impedance of the Gate Circuit

In comparing power HEXFETs to bipolar transistors, the point is often made that the former require hardly any drive power. This is certainly true, and is the main reason why the drive circuit is normally an order of magnitude simpler than for the bipolar counterparts.

However, whenever more than mediocre performance is required, careful thought should be given to the design and layout of the drive stage, particularly as far as its equivalent internal impedance is concerned. For this reason, a word is in order on the bearing that this internal impedance has on the device performance.

For a device to be turned ON, a certain charge has to be supplied to the gate to raise it to the desired voltage, whether in the linear region, or in the "saturation". Ideally, the best way to achieve this is by means of a voltage source, capable of supplying any amount of current in the shortest possible time. If the device is operated as a switch, a large transient current capability of the drive circuit reduces the time spent in the linear region, thereby reducing the switching losses. On the other hand, if the device is operated in the linear mode, a relatively large current capability in the gate drive circuit minimizes the relevance of the Miller effect, improving the bandwidth of the stage and reducing the harmonic distortion.

The above considerations can be identified with a detailed analysis of the basic switching waveforms at turn-ON and turn-OFF for a clamped inductive load, as shown in Figures 3 and 5. Figure 3 shows the waveforms of the drain current, drain-to-source voltage and gate voltage during the turn-ON interval. For the sake of simplicity, the equivalent impedance of the drive circuit has been assumed

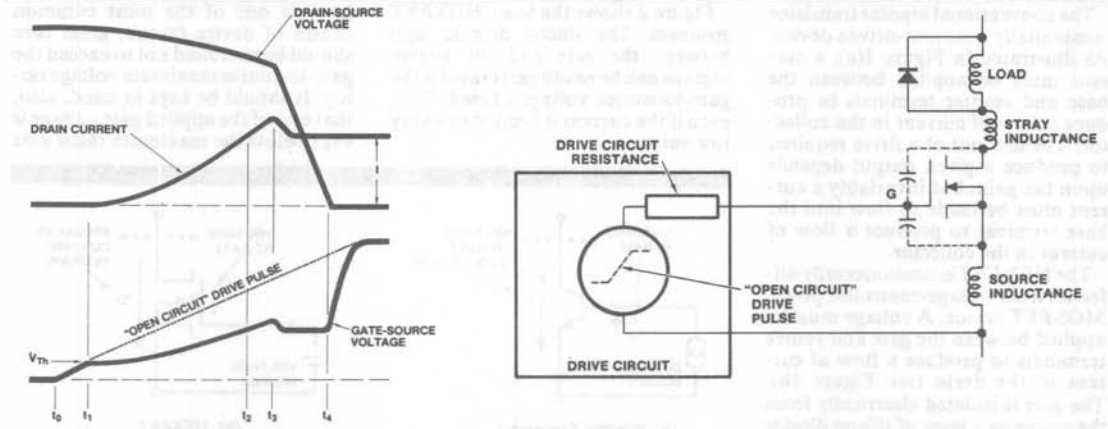


Figure 3. Waveforms at Turn-On

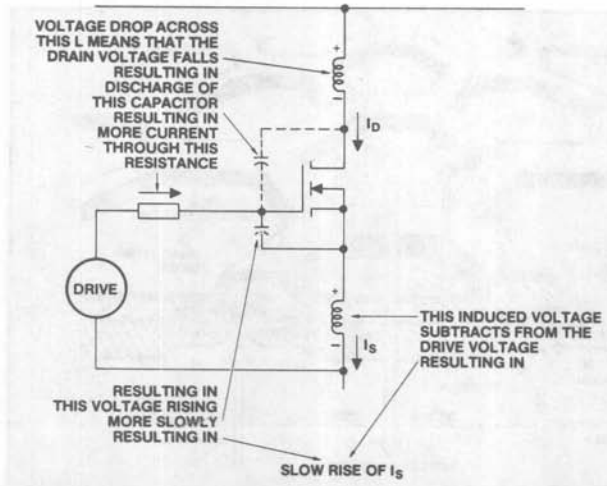


Figure 4. Diagrammatic Representation of Effects When Switching-ON

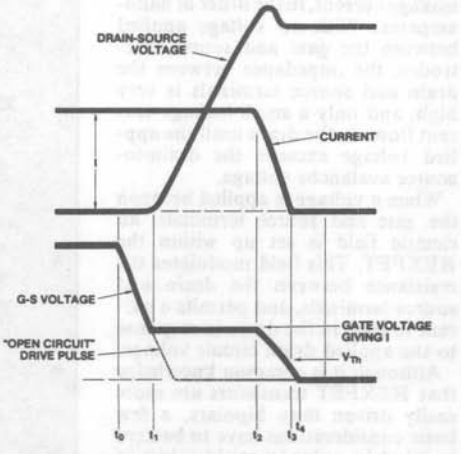


Figure 5. Waveforms at Turn-OFF

as purely resistive.

At time, t_0, the drive pulse starts to rise. At t_1 it reaches the threshold voltage of the HEXFET, and the drain current starts to increase. At this point, two things happen which make the gate-source voltage waveform deviate from its original "path". First, inductance in series with the source which is common to the gate circuit develops an induced voltage, as a result of the increasing source current. This voltage counteracts the applied gate drive voltage, and slows down the rate of rise of voltage appearing directly across the gate and source terminals; this in turn slows down the rate of rise of the source current. This is a negative feedback effect; increasing current in the source produces a counteractive voltage at the gate, which tends to resist the change of current.

The second factor that influences the gate-source voltage is the so-called "Miller" effect. During the period t_1 to t_2 some voltage is dropped across "unclamped" stray circuit inductance in series with the drain, and the drain-source voltage starts to fall. The decreasing drain-source voltage is reflected across the drain-gate capacitance, pulling a discharge current through it, and increasing the effective capacitive load on the drive circuit. This in turn increases the voltage drop across the source impedance of the drive circuit, and decreases the rate of rise of voltage appearing between the gate and source terminals. Obviously, the lower the impedance of the gate drive circuit, the less this effect will be. This also is a negative feedback effect; increasing current in the drain results in a fall of drain-to-source voltage, which in turn slows down the rise of gate-source voltage, and tends to resist the increase of drain current. These effects are illustrated diagramatically in Figure 4.

This state of affairs continues throughout the period t_1 to t_2, whilst the current in the HEXFET rises to the level of the current, I_M, already flowing in the freewheeling rectifier, and it continues into the next period, t_2 to t_3, whilst the current increases further, due to the reverse recovery of the freewheeling rectifier.

At time t_3 the freewheeling rectifier starts to support voltage, whilst the drain current and the drain voltage start to fall. The rate of fall of drain voltage is now governed almost exclusively by the Miller effect, and an equilibrium condition is reached, under which the drain voltage falls at just the rate necessary for the voltage between gate and source terminals to satisfy the level of drain current established by the load. This is why the gate-to-source voltage falls as the recovery current of the freewheeling rectifier falls, then stays constant at a level corresponding to the drain current, whilst the drain voltage is falling. Obviously, the lower the impedance of the gate-drive circuit, the higher the discharge current through the drain-gate self-capacitance, and the faster will be the full time of the drain voltage.

Finally, at time t_4, the HEXFET is switched fully ON, and the gate-to-source voltage rises rapidly towards the applied "open circuit" value.

Similar considerations apply to the turn-OFF interval. Figure 5 shows theoretical waveforms for the HEXFET in the circuit of Figure 4 during the turn-OFF interval. At t_0 the gate-drive starts to fall. At t_1 the gate voltage reaches a level that just sustains the drain current, I, and the device enters the linear mode of operation. The drain-to-source voltage now starts to rise. The Miller effect governs the rate-of-rise of drain voltage, and holds the gate-to-source voltage at a level corresponding to the constant drain current. The lower the impedance of the drive circuit, the greater the charging current into the drain-gate capacitance, and the faster will be the rise time of the drain voltage. At t_3 the rise of drain voltage is complete, and the gate voltage and drain current start to fall at a rate determined by the gate-source circuit impedance.

In some circuit configurations, even if the performance is of no great concern, it may be important to minimize the impedance in the gate drive circuit to minimize unwanted voltage transients on the gate. With reference to Figure 6, when one HEXFET is turned ON or OFF, a step of voltage is applied between drain and source of the other device on the same leg. This step of voltage is coupled to the gate through the gate-to-drain capacitance, and it can be large enough to turn the device ON for a short instant.

To prevent this from occurring, the gate circuit impedance and/or the rate-of-rise of the step have to be reduced to the extent that the voltage coupled to the gate is below the threshold voltage or some other suitably chosen safe value.

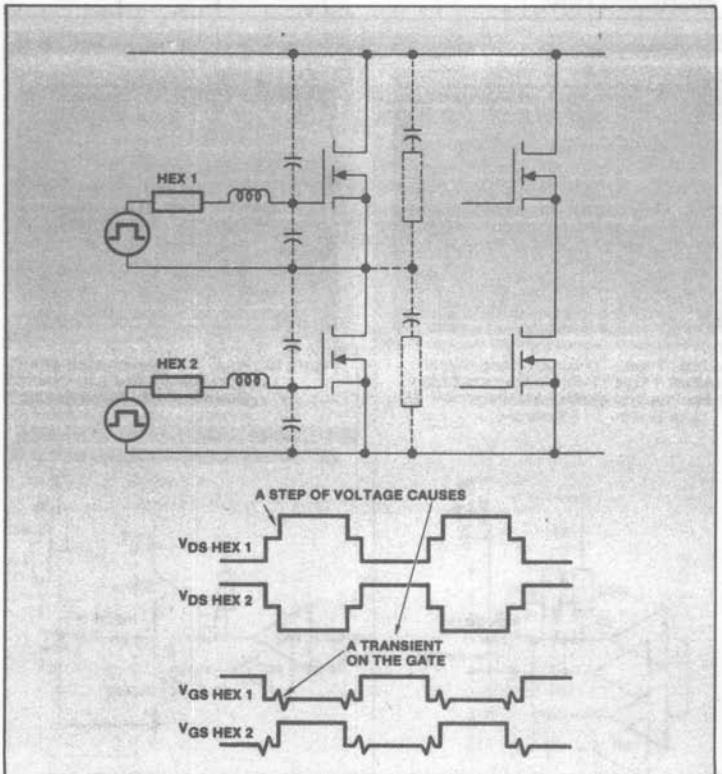


Figure 6. Transients of Voltage Induced on the Gate by Rapid Changes on the Drain-to-Source Voltage

Driving HEXFETs From TTL[1]

Table 1 shows the guaranteed sourcing and sinking currents for different TTL families at their respective voltages. From this table, taking as an example the 74LS series, it is apparent that, even with a sourcing current as low as 0.4 mA, the guaranteed logic one voltage is 2.4V (2.7 for 74LS and 74S), and that is lower than the possible threshold of a HEXFET. The use of a pull-up resistor on the output (Figure 7) would take this voltage up to 5V, but it would still not be sufficient to guarantee "saturated" switching of the HEXFET, unless the current to be switched is substantially less than the rated value of the HEXFET.

More specifically, with reference to the output characteristics (Figure 3 of the data sheet), it can be seen that for a low voltage device (e.g., IRF130) the drain current corresponding to a gate voltage of 5V is approximately half its DC rated value, while for a high voltage device (e.g., IRF330) it is higher than the DC rated current. It should be emphasized though, that the curves show typical values and that, with a V_{GS} = 5V, saturation is not guaranteed for either DC or pulse rated conditions for any device.

Figure 8 shows a typical application of a TTL inverter driving a IRF320 with the waveforms that would normally be expected. The 74LS05 is an open collector device, but waveforms do not change significantly for a totem pole device. With reference to the drain voltage (bottom waveform) it is apparent that the device turns on much more slowly than it turns off. This is because the gate-to-source and gate-to-drain capacitances are charged exponentially through the pull-up resistor, while they are discharged through a saturated bipolar

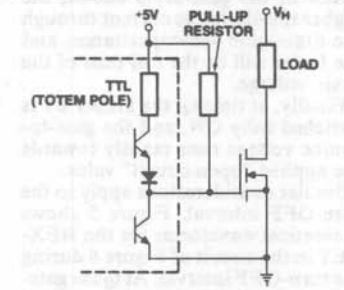
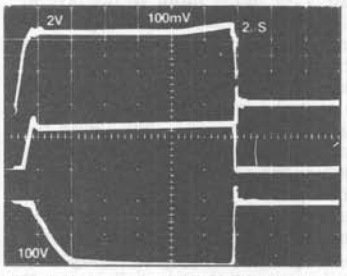


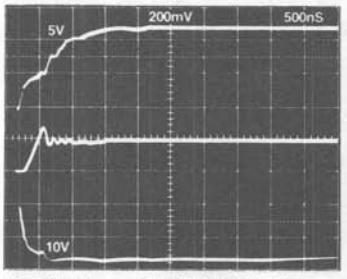
Figure 7. Direct Drive from TTL Output

Table 1. Driving HEXFETs from TTL (Totem Pole Outputs)

Logic Conditions	54/74	54H/74H	(54L)/ 74L	(54LS)/ 74LS	74S
Logic Zero Min. sink current for V_{OL}	16mA ≤0.4V	20mA ≤(0.4V)/	(2)/3.6mA ≤(0.3V)/ 0.4V	(4)/8 ≤(0.4V)/ 0.5V	20mA 0.5V
Logic One Max. source current for V_{OH}	-0.4mA ≥2.4V	-0.5mA ≥2.4V	-0.2mA ≥2.4V	-0.4mA ≥(2.5)/ 2.7V	-1.0mA ≥2.7V
Typical Gate Propagation Delay	10ns	7ns	50ns	12ns	4ns



Top Trace: Gate Voltage 2V/div.
Middle Trace: Drain Current 1A/div.
Bottom Trace: Drain Voltage 100V/div.
Time Scale: 2μs/div.



Top Trace: Gate Voltage 5V/div.
Middle Trace: Drain Current 2A/div.
Bottom Trace: Drain Voltage 10V/div.
Time Scale: 500ns/div.

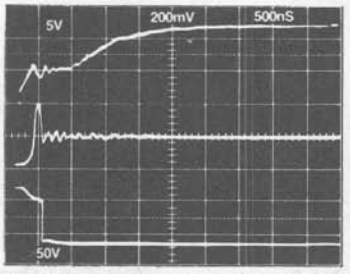


Figure 10. Waveforms Associated with the Circuit in Figure 9, at Different Drain Voltage. Same Scales except Bottom Trace: 100V/div.

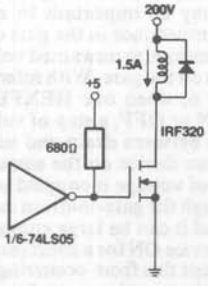


Figure 8. Waveforms Associated with a HEXFET Driven by a TTL Gate

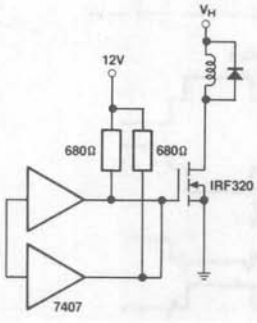


Figure 9. Waveforms Obtained with High Voltage TTL Driver

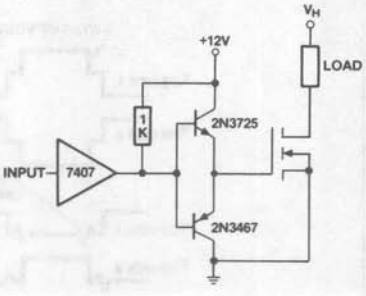


Figure 11. Simple Interface to Drive HEXFETs from TTL

[1]International Rectifier also manufactures logic level HEXFETs. For more information, please refer to AN-971, "Switching Characteristics of Logic Level HEXFET Power MOSFETs".

transistor. The waveforms show also, that the device stays in the linear region for 9 microseconds and that, at the end of this time, the gate is finally free to rise to 5V, after the gate-to-drain capacitance has been fully charged. The main reason for such a poor performance is, of course, the fact that the maximum voltage available on the gate is 5V. The performance improves substantially if two or three gates are connected in parallel to charge or discharge this capacitance.

For guaranteed "saturation" and fast switching, high voltage open collector buffers can be used (7406, 7407, etc.), possibly with several devices connected in parallel.

Figure 9 shows the waveforms that can be obtained with two parallel high voltage drivers pulled up to 12V. Whilst a dramatic improvement can be seen with respect to Figure 8, the performance is still well below what can ultimately be obtained from a HEXFET. The waveforms in Figures 9 and 10 are for the same device, with the same drive circuit and the same drain current, but with different drain voltages. At higher voltages, C_{GD} takes a longer time to discharge, so the device stays in the linear region for more than 0.5 microseconds before reaching saturation.

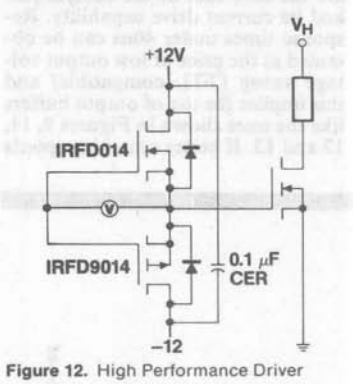


Figure 12. High Performance Driver

Whenever better switching performance is required, interface circuits should be added to provide fast current sourcing and sinking to the gate capacitances. One simple interface circuit is the one shown in Figure 11.

It is a complementary emitter follower stage, capable of sinking or sourcing approximately 1A. The choice of the output transistor is important when switching times have to be in the order of 40ns.

They should have good gain at high currents to be capable of delivering whatever current is required by the Miller effect during the allowed switching time. To gain a better insight on the operation of these transistors, we can attempt a rough calculation of the current they have to supply in a switching operation. Disregarding for a moment the Miller effect, if C_{GS} is 700pF (IRF330) and we want to charge it linearly to 12V in 40ns, a current pulse is required equal to:

$$I = \frac{C_{GS} \times V_{GS}}{t_s}$$

$$= \frac{0.7 \times 10^{-9} \times 12}{40.10^{-9}} = 0.21A$$

In the simplistic assumption that the gate-to-drain capacitance is discharged in the same time, assuming a drain voltage of 200V, we have:

$$I = \frac{C_{DG} \times V_{DS}}{t_s}$$

$$= \frac{40 \times 0.10^{-12} \times (200-12)}{40\ 10^{-9}} = 0.188A$$

In the final assumption that the two currents add up and that the switching frequency is 100kHz, we can obtain an approximate figure for the power lost in one driver transistor:

$P = V_{CE} \times I_C \times t_s \times f = 1 \times 0.398 \times 40.10^{-9} \times 100\ 10^3 = 1.6mW$

The conclusion is that the driver devices have to be capable of supplying 0.4A without significant voltage drop, but that hardly any power is dissipated in them. Core drivers (2N3725, 2N3244), seem to be the most suitable devices. Unfortunately, the gain of these devices drops very fast for currents over 0.5A. Audio drivers (2N5320, 2N5322), have better gain at high currents but are slower. A double buffer stage may be advisable in some applications with fast switching bipolar devices (2N-2369A and 2N4208 or MPS2369 and MPS3640) driving two HEXFETs, as shown in Figure 12.

Buffer stages can also be implemented with special purpose integrated circuits like the ones shown in Figure 13. These buffers have guaranteed switching times and high current sourcing and sinking capability. Furthermore, they are directly compatible with 5V TTL.

Driving HEXFETs from C-MOS

While the same general considerations presented above for TTL would also apply to C-MOS, there are three substantial differences that should be kept in mind:

1. C-MOS has a more balanced source/sink characteristic that, on a first approximation, can be thought of as a 500 ohm resistance for operation over 8V and a 1k ohm for operation under 8V (Table 2).
2. C-MOS can operate from higher supply voltages than 5V so that HEXFET saturation can be guaranteed.
3. Switching times are longer than TTL (Table 2).

When C-MOS outputs are directly coupled to the gate of a HEXFET, the dominant limitation to performance is not the switching time, but the internal impedance (assuming that C-MOS are operated from a 10V

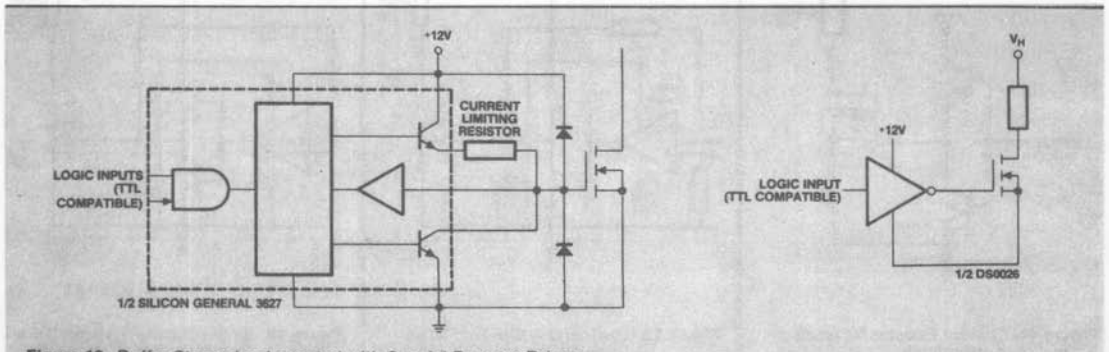


Figure 13. Buffer Stages Implemented with Special Purpose Drivers

or higher voltage supply). It will certainly not be able to turn OFF the HEXFET as fast as the TTL, while the turn-ON waveform will be slightly better than what can be achieved with a 7407 with a 680 ohm pull-up resistor. Of course, gates can be paralleled in any number to lower the impedance and this makes C-MOS a very simple and convenient means of driving HEXFETs. Drivers can also be used, like the 4049 and 4050 which have a much higher current sinking capability (Table 2), but they do not yield any significant improvement in current sourcing.

For better switching speeds, buffer circuits should be considered, not only to provide better current sourcing and sinking capability, but also to improve over the switching times of the C-MOS output itself. The circuit shown in Figure 11 (without the pull-up resistor which would not be needed), and Figure 12 will improve the drive capability, while the circuits in Figure 13 will improve both drive capability and switching times, but require a TTL compatible drive signal (5V). Another possibility, of course, is to interface C-MOS to TTL and then use the TTL drive circuits.

Driving HEXFETs From Linear Circuits

The complementary emitter follower configuration of Figure 11 can also be used in linear applications to improve drive capability from an op-amp or other analog source (Figure 14).

Table 2. Driving HEXFETs from C-MOS (Buffered)

	Standard Buffered Outputs			4049/4050 Drivers		
Logic Supply Voltage / Logic Conditions	5V	10V	15V	5V	10V	15V
Logic Zero: Approximate sink current for $V_{OL} \leq 1.5V$	1.5mA	3.5mA	4mA	20mA	40mA	40mA
Logic One: Minimum source current for V_{OH}	-0.51mA ≥4.6V	-1.3mA ≥9.5V	-3.4mA ≥13.5V	-1.25mA ≥2.5V	-1.25mA ≥9.5V	-3.75mA ≥13.5V
Typical switching times of logic drive signals:						
RISE	100ns	50ns	40ns	100ns	50ns	40ns
FALL	100ns	50ns	40ns	40ns	20ns	15ns

If the driving signal is generated by an operational amplifier, the use of power operational amplifiers (e.g., μA791) that can supply as much as 1A can be considered. In practice, their slew rate is so low (0.5V/μs) that their current capability would be redundant and the usable bandwidth would be less than 25kHz. A larger bandwidth can be obtained with better operational amplifiers followed by a current booster, like the ones shown in Figures 15 or 16. For a system bandwidth of 1MHz, the op-amp bandwidth must be significantly higher than 1MHz and its slew rate at least 30V/μs. Presently, there are several devices capable of this performance, e.g., LF157, LM110, μA715, HA2620, etc. If a larger bandwidth is needed, special purpose current amplifiers can be used, like the HA2630 (bandwidth 8MHz, slew rate 500V/μs, 0.4A output current) or very fast operational amplifiers like the NE5539 (bandwidth 48MHz, slew rate 600V/μs) followed by a current booster.

When analog signals determine the switching frequency or duty cycle of a HEXFET, as in PWM applications, a voltage comparator is normally used to command the switching. Here, too, the limiting factors are the slew rate of the comparator and its current drive capability. Response times under 40ns can be obtained at the price of low output voltage swing (TTL compatible) and this implies the use of output buffers like the ones shown in Figures 9, 11, 12 and 13. If better switching speeds

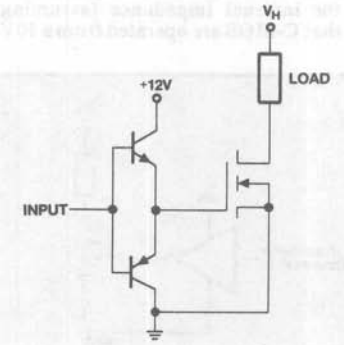


Figure 14. Current Booster for Analog Applications

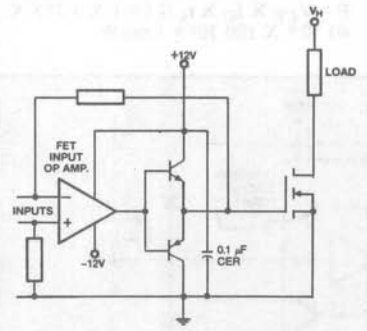


Figure 15. Dual Supply Op-Amp Drive Circuit

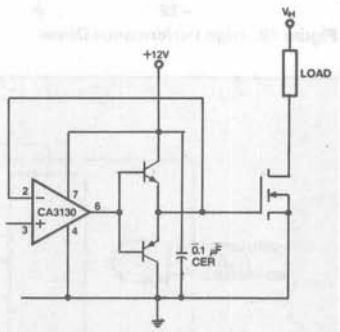


Figure 16. Single Supply Op-Amp Drive Circuit (Voltage Follower)

are desired, a fast op-amp should be used. Figure 17 shows a typical comparator connection.

In many applications, when the HEXFET is turned on, current transfers from a freewheeling diode into the HEXFET. If the switching speed is high and the stray inductances in the diode path are small, this transfer can occur in such a short time as to cause a reverse recovery current in the diode high enough to destroy it. For this reason, it may be necessary to slow down the turn-on of the HEXFET while leaving the turn-off as fast as practical. Pulse shaping circuits can be used for this purpose, like the ones in Figures 18 and 19.

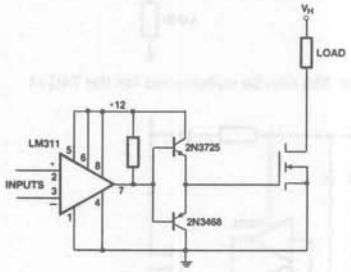


Figure 17. Comparator Drive

In linear applications, the use of special circuits like the LM391 audio driver with an output booster can be considered. The LM391 has separate source and sink outputs.

Drive Circuits Not Referenced to Ground

To drive a HEXFET into saturation, an appropriate voltage must be applied between the gate and source. If the load is connected between source and ground, and the drive voltage is applied between gate and ground, the effective voltage between gate and source decreases as the device turns on. An equilibrium point is reached in which the amount of current flowing in the load is such that the voltage between gate and source maintains that amount of drain current and no more.

For this reason, it is often advantageous to have the gate drive circuit referenced to the source rather than to the ground. There are basically three ways of floating the gate drive circuit with respect to ground:

1. By means of optically coupled isolators.
2. By means of pulse transformers.
3. By means of DC to DC chopper circuits with transformer isolation.

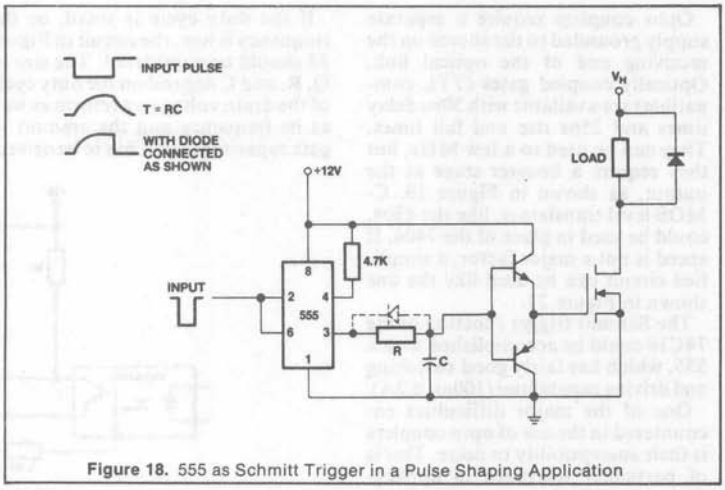


Figure 18. 555 as Schmitt Trigger in a Pulse Shaping Application

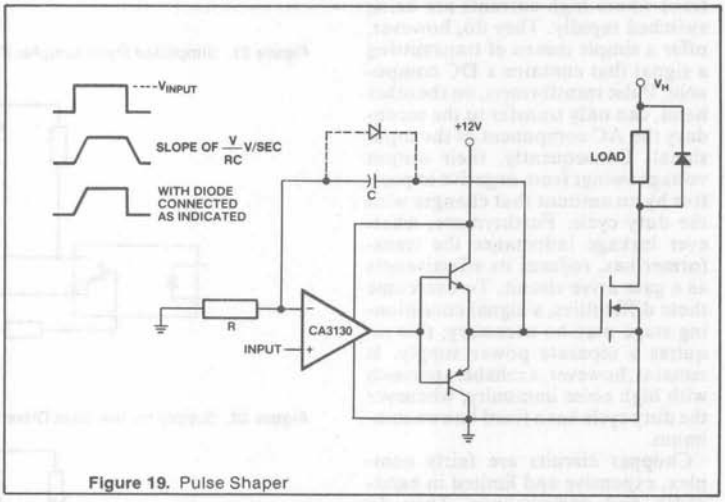


Figure 19. Pulse Shaper

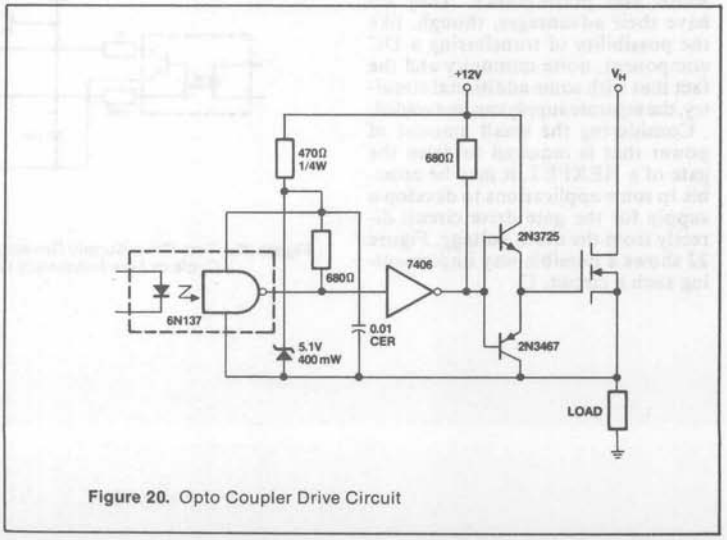


Figure 20. Opto Coupler Drive Circuit

Opto couplers require a separate supply grounded to the source on the receiving end of the optical link. Optically coupled gates (TTL compatible) are available with 50ns delay times and 25ns rise and fall times. They can be used to a few MHz, but they require a booster stage at the output, as shown in Figure 20. C-MOS level translators, like the 4504, could be used in place of the 7406. If speed is not a major factor, a simplified circuit can be used like the one shown in Figure 21.

The Schmitt trigger function of the 74C14 could be accomplished with a 555, which has fairly good switching and driving capabilities (100ns, 0.2A).

One of the major difficulties encountered in the use of opto couplers is their susceptibility to noise. This is of particular relevance in applications where high currents are being switched rapidly. They do, however, offer a simple means of transmitting a signal that contains a DC component. Pulse transformers, on the other hand, can only transfer to the secondary the AC component of the input signal. Consequently, their output voltage swings from negative to positive by an amount that changes with the duty cycle. Furthermore, whatever leakage inductance the transformer has, reduces its effectiveness as a gate drive circuit. To overcome these difficulties, a signal conditioning stage may be necessary; this requires a separate power supply. It remains, however, a reliable approach with high noise immunity, whenever the duty cycle has a fixed known minimum.

Chopper circuits are fairly complex, expensive and limited in bandwidth and performance. They do have their advantages, though, like the possibility of transferring a DC component, noise immunity and the fact that with some additional circuitry, the separate supply can be avoided.

Considering the small amount of power that is required to drive the gate of a HEXFET, it may be possible in some applications to develop a supply for the gate drive circuit directly from the drain voltage. Figure 22 shows a possible way implementing such a circuit. □

If the duty cycle is small, or the frequency is low, the circuit in Figure 23 should be considered. The size of Q, R, and C depend on the duty cycle of the drain voltage waveform as well as its frequency and the amount of gate capacitance that has to be driven.

Obviously, this circuit will not work if the HEXFET may be kept in the on-state for an undetermined period of time and there is lower frequency limit below which C becomes quite large and the circuit is not attractive any longer. □

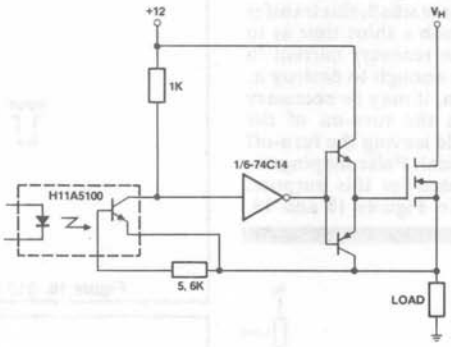


Figure 21. Simplified Opto Coupler Drive. 555 can be substituted for the 74C14

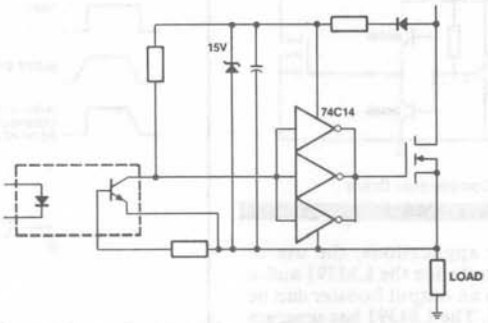


Figure 22. Supply for the Gate Drive Circuit Developed from the Drain Voltage

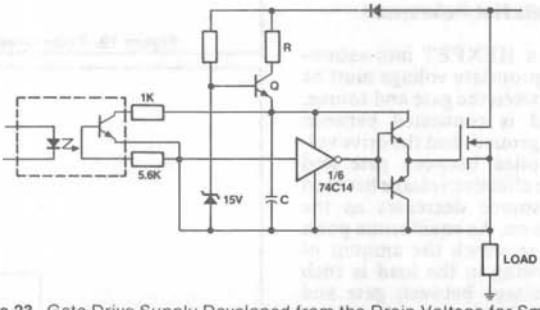


Figure 23. Gate Drive Supply Developed from the Drain Voltage for Small Duty Cycle or Low Frequency Operation