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100-kW DC-DC Converter Employs Resonant π-Filter

Adapted from an ac-output resonant half-bridge inverter circuit, the resonant CLC (capacitor-inductor capacitor) dc-dc converter employs a π-filter loaded by a rectifier.

High-frequency power conversion has established both industry standards and proven good typical design solutions. There are a number of favorite technical solutions for a variety of applications. However, if the required output power exceeds the 100-kW level, the situation is not so clear. No well-known solution operating at a sub-kilowatt power level can successfully scale up to provide 100 kW or more of output power.

The "heart" of each high-power converter is the power inverter, built of semiconductor switches — usually IGBTs. The modern low-power IGBTs are fast and can operate reliably in a hard-switching mode. Otherwise, the high-power IGBTs are significantly slower. Furthermore, they cannot be instantly turned off because of significant parasitic tail current, which is "enemy No. 1" for high-frequency operation. The zero-voltage switching mode eliminates turn-on losses, but very dangerous turn-off stress and associated power losses are still present. Unfortunately, no existing technical solution can eliminate tail-current-related problems completely for regulated dc-output converters. However, it is possible to reduce the harmful tail-current influence to an acceptable level.

One promising solution is suggested here. Its name, first introduced here, is a CLC-inverter, because it is based on a resonant CLC π-filter loaded by a rectifier. The main idea of a CLC-inverter came from a resonant half-bridge inverter, widely used in the electronic ballasts and induction heaters. Fig. 1 shows the simplified schematic of that inverter.

C1 is a dc-blocking capacitor, while C2, L1 and C3 make up a resonant CLC π-filter for the load-impedance matching. This type of inverter must operate in a zero-voltage switching mode; otherwise, energy stored in C2 can destroy power switches. In this circuit, IGBT turn-off switching loss and transitional peak power is dramatically reduced due to low dV/dt across IGBTs after turn-off. Input filter capacitor C2 works as a very efficient snubber, reducing IGBT collector voltage rise speed. For example, the tail current of the typical 300-A, 1200-V rated high-speed IGBT decays near exponentially with 200-ns to 500-ns time constant. Therefore, if a snubber capacitor slows down IGBT voltage rise time to 3 μs, then the total IGBT turn-off energy loss becomes three to five times lower than that without snubber capacitor.

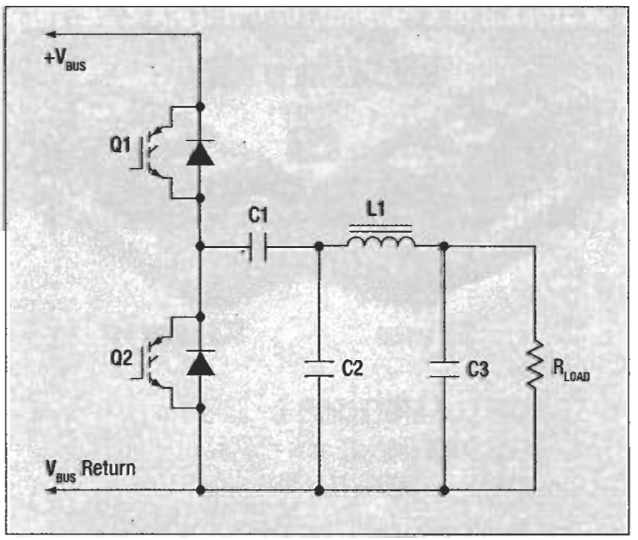

Fig. 1. Basic resonant half-bridge inverter circuit in which C1 is a dc-blocking capacitor, whereas C2, L1 and C3 create a resonant CLC π-filter for the load-impedance matching. This inverter must operate in a zero-voltage switching mode, otherwise energy stored in C2 can destroy power switches.

It is very important that the peak-output ac voltage on the load is lower, equal or higher than bus voltage. Therefore, that topology is intrinsically buck-boost. That type of inverter easily generates many kilowatts of clear sine-wave ac-power on the properly matched load. Zero-voltage turn-on and very soft turn-off guarantee both high efficiency and high reliability of IGBT operation at 50 kHz and even higher frequencies.

Despite the fact that this type of inverter was originally designed and widely used for ac-output power, it also can

be adapted successfully to provide dc power. The dc-output CLC-inverter can operate either in a half-bridge or full-bridge configuration. Fig. 2 shows a full-bridge CLC-inverter. The CLC π-filter is indirectly composed of snubber capacitors C1 through C4, resonant inductor L_{RES} and a resonant capacitor C_{RES}, connected across the bridge rectifier input. For the sake of simplicity, the output transformer is not shown, although it is always present in the real circuits.

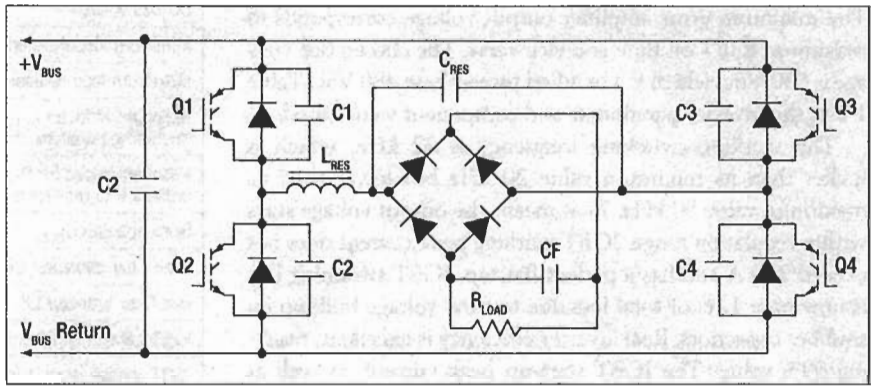

Fig. 2. The dc-output CLC-inverter can operate in either a half-bridge or full-bridge configuration, which is shown here.

The dc-output voltage on the R_{LOAD} is actually a real output voltage, reflected to primary winding of the power transformer (i.e., divided by transformer turn ratio). A resonant capacitor C_{RES} value is also reflected to the primary side via turn ratio squared.

The output voltage can exceed bus voltage; therefore, this topology is intrinsically buck-boost. However, the best power-conversion efficiency is reached when the reflected output voltage equals bus voltage.

That type of inverter can operate under different control modes (algorithms). The simplest and the most intuitively understandable operation mode is fixed-dead-time variable-frequency (FDT) mode. Under this operation mode, IGBTs are driven in such a way that dead time (i.e., all IGBTs are off) is fixed. Its good real value is 4 µs to 5 µs. Furthermore, its on-time (Q1 and Q4 as well as Q2 and Q3 are driven simultaneously) can vary within established brackets from some maximum value (for example, 21 µs to some minimum value such as 6 µs). Therefore, the switching frequency is not constant; it varies during normal operation from 20 kHz to 50 kHz. The π-filter component values must be properly chosen to guarantee zero-voltage switching and proper impedance matching at the full range of switching frequencies. Fortunately, this is possible but with some restrictions, which is explained further.

Changing switching frequency and keeping dead time constant is a simple way to control output power. The higher the switching frequency, the higher the resonant inductor L_{RES} impedance and the lower the resonant capacitor C_{RES} impedance. This means that by increasing switching frequency, output power is reduced and vice versa. The output voltage, reflected to the primary side, could exceed bus voltage, which is impossible for any PWM topology. This control method is a good alternative to standard fixed-frequency PWM control, which does not work properly in resonant-mode inverters. However, the FDT control is not enough flexible to realize all the advantages of a CLC-inverter.

FULL-BRIDGE CLC-INVERTER SIMULATION

The inverter-circuit simulation is done using a special tool kit, developed in Russia, called a virtual prototype. A virtual prototype accelerates and improves a complex system development and design process. Unlike SPICE-type simulation tools, this method does not suffer from multiple limitations. Virtual prototype is extremely realistic, because it includes all parts and aspects of the real system operation rather than a simplified model of a small part of the entire system. All electrical, magnetic, thermal, mechanical and other physical phenomena in the real complex system that operation is based on can be organically included into the virtual prototype. Ten years of using this tool confirmed its efficiency for the power-converter circuit simulation, as the results obtained are always very close to that of a real prototype — typically within measurement accuracy.

A fixed-dead-time control circuit is relatively straightforward, although it is not considered here in detail. It is composed of a noise-immune steering logic, proportionally integrating error amplifier and voltage-to-frequency converter.

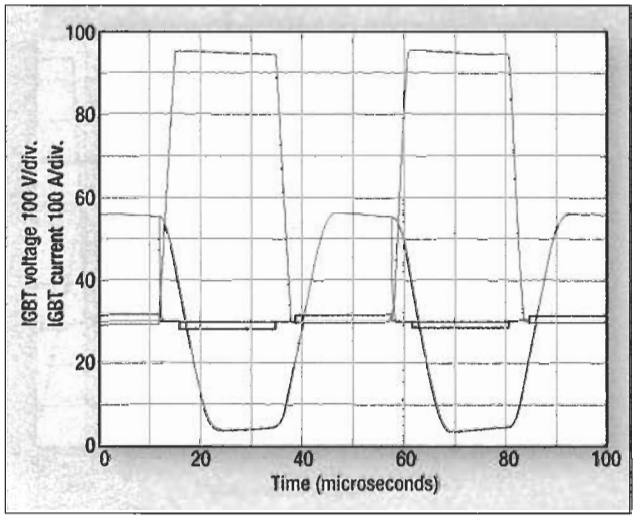

Fig. 3. CLC-inverter waveforms at full output power in which both resonant-inductor current and IGBT voltage have perfect trapezoidal waveforms, which is good for high-voltage rectifier operation. In the figure, the purple line = L_{RES} current; the red line = IGBT collector current; and the blue line = IGBT (or C1) voltage.

The minimum error amplifier output voltage corresponds to maximum IGBT on time and vice versa. The chosen bus voltage is 650 Vdc, which is a rectified three-phase 480 Vac. Table 1 lists the inverter parameters and component values used.

The working switching frequency is 22 kHz, which is higher than its minimum value 20 kHz but lower than its maximum value 50 kHz. That means the output voltage stays within regulation range. IGBT working peak current does not exceed 260 A and has a perfect flat top. IGBT switching loss is now only 12% of total loss due to slow voltage buildup on snubber capacitors. Real inverter efficiency is excellent, reaching 99% value. The IGBT start-up peak current, as well as short output current, is almost twice as high and can exceed 500 A. Although it is safe for 300-A rated IGBT blocks, the soft-start and overcurrent protection circuit is desirable. The soft-start can be realized by slow ramping up of bus voltage or by starting inverter operation at maximum switching frequency. The first way is better, but it requires an SCR-based phase-control line-voltage rectifier.

This inverter can successfully operate at a reduced output power, because its output voltage is still in regulation — even at 30% of full load. The open-load operation is safe for the inverter, but its output voltage gets out of regulation. It can stay in regulation even at open-load condition (capacitor bank charge mode) if L_{RES}-C_{RES} resonant frequency is reduced from 39 kHz to 30 kHz. However, it somewhat compromises a full-load operation efficiency. Fig. 4 shows the light-load operation waveforms, and Table 3 presents the simulation test results.

The switching frequency is now 46 kHz; it is still in a regulation range. A resonant-inductor current waveform is now close to sine wave. The total IGBT power loss is reduced

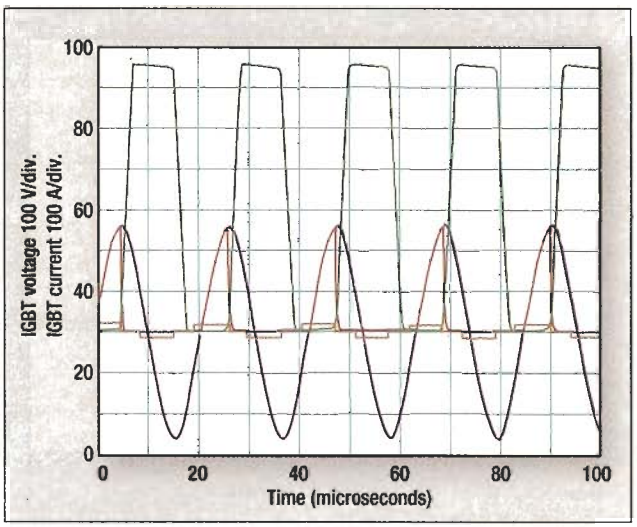

Fig. 4. CLC-inverter waveforms at low output power show that it can operate successfully at a reduced output power, because its output voltage is still in regulation at 30% of full load. In the figure, the purple line = L_{RES} current; the red line = IGBT collector current; and the blue line = IGBT (or C1) voltage.

DC bus voltage	650 V
Minimum load resistance (full power)	4 Ω
Maximum load resistance (33% of full power)	12 Ω
Resonant inductor L_{RES} (including transformer-leakage inductance)	20 µH
Resonant capacitor C_{RES} (reflected to primary side)	0.8 µF
Bus capacitor C_{BUS}	200 µF
Load filter capacitor CF (reflected to primary side)	400 µF
Bus filter inductor LF	100 µH
IGBT parallel snubber capacitors C1...C4	0.47 µF
IGBT voltage drop at low current	1.2 V
IGBT parasitic series resistance	10 mΩ
IGBT tail current decay time constant	200 ns
Minimum IGBT on-time (switching frequency 50 kHz)	6 µs
Maximum IGBT on-time (switching frequency 20 kHz)	21 µs
IGBT fixed dead time	4 µs

Table 1. Simulation circuit parameters.

by 35%, but the switching loss contribution is now 39% of total loss. There is an interesting result: IGBT total power loss is not proportional to the inverter's output power. Note that resonant capacitor C_{RES} works at high ac-voltage, about two times the output dc-voltage peak-to-peak at 46 kHz. Mica is the best dielectric for this capacitor.

IGBT switching losses are very much dependent on snubber capacitors' (C1 through C4) values. The higher the capacitance, the lower the switching losses. However, there is a real danger of getting out of zero-voltage switching mode if snubber capacitors are too large. The reason for this is because resonant-inductor current cannot completely discharge that large capacitor during IGBT dead time prior to the next IGBT turn-on. If that happens, the residual snubber capacitor energy is dissipated in the IGBT every switching cycle and results in IGBT overheat. The inverter can operate without

Established switching frequency	22 kHz
Reflected output voltage	654 V
Input RMS and average current	170.80 A and 170.76A
Output power	107000 W
IGBT peak current	260 A
IGBT average current	90 A
Each IGBT total power loss	361 W
Each IGBT conductive power loss	317 W
L_{RES} RMS current	224 A
Snubber capacitor (C1-C4) RMS current	37 A
C_{BUS} and CF RMS current	124 A and 114 A
C_{RES} RMS current	95 A
Output ripple voltage p-p	3.1 V

Table 2. Full-load simulation results.

Established switching frequency	46 kHz
Reflected output voltage	660 V
Input RMS and average current	70.1 A and 70 A
Output power	36300 W
IGBT peak current	260 A
IGBT average current	46 A
Each IGBT total power loss	234 W
Each IGBT conductive power loss	142 W
L_{RES} RMS current	187 A
Snubber capacitor (C1-C4) RMS current	57 A
C_{BUS} and CF RMS current	122 A and 98 A
C_{RES} RMS current	142 A
Output ripple voltage p-p	0.97 V

Table 3. Light-load simulation results.

snubber capacitors at all, but very high turn-off loss dramatically reduces the maximum switching frequency to 8 kHz or less for reliable, continuous operation.

The fixed-dead-time control mode is convenient for multiphase operation, because one clock signal can synchronize multiple inverters with appropriate phase shift. However, this mode is not intrinsically protected from a lethal IGBT zero-voltage switching violation. Therefore, all critical component values must be properly chosen to guarantee normal operation under all possible working conditions.

Because of its high reflected output voltage and fixed duty-cycle near 50%, the converter's IGBT peak current is about two times lower than that of any PWM or resonant inverter of the same output power. Due to its excellent tolerance to the bus voltage variation, it can operate from three-phase ac-line rectifier without filter capacitors, which improves power factor. Additionally, the smooth voltage and current transitions guarantee very low EMI level. It is the best topology for the megawatt-level dc-output power supplies, as well as for large capacitor bank chargers.

The virtual prototype was found to be an extremely efficient method for modeling and analyzing CLC-inverter operation. It allows the gathering of complete information about the entire circuit operation as well as every single component. It is especially important because no formulae or equations are derived for that type of power inverter.

The results of CLC-inverter simulation are quite promising — they usher in a new era of high-power-conversion technology. ⏻