Eliminating current spiking from dc-to-dc converters

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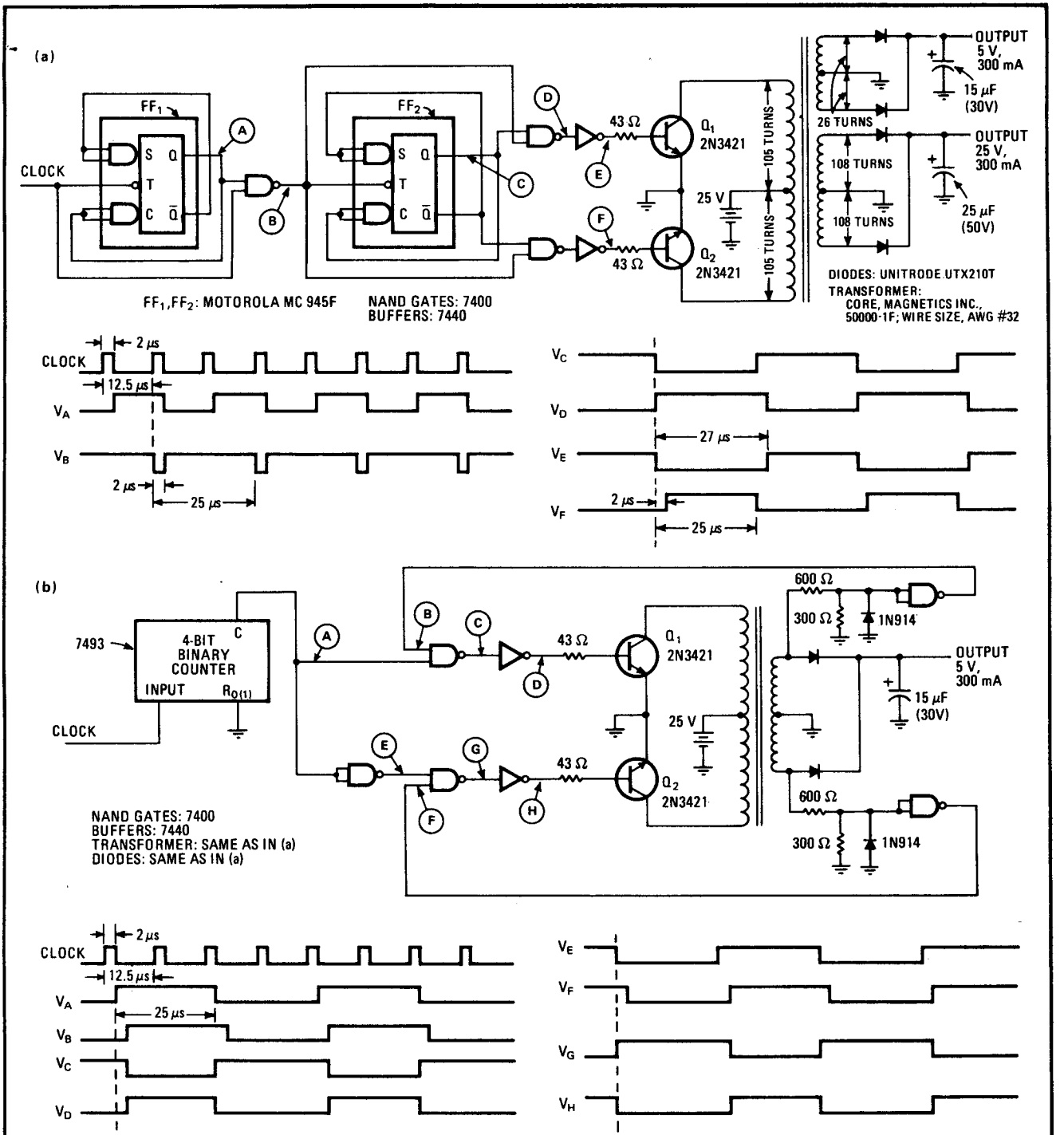
When the two inverter transistors in a push-pull dc-to-dc converter conduct at the same time, current spiking will occur and at worst destroy the circuit, at least degrade its efficiency. These undesirable effects can be prevented by delaying a clock pulse train with standard logic circuits.

Ideally one transistor turns on as soon as the other turns off. But because of their storage time constants, one is often still on when the other is beginning to conduct. All risk of simultaneous conduction will, however, be eliminated if the square-wave base drive signals to the transistors are made asymmetrical. The delay provided by logic gates ensures that, for a short length of time, there is no current drive signal at all. This delay can be fixed (constant) or controlled by feedback.

The figure shows two ways of designing a nonspiking static push-pull dc-to-dc converter. In (a), the current-drive delay time is fixed, and in (b), the delay depends on a feedback signal. In both cases, the transistor on-time is made smaller than the transistor off-time.

There are two output voltage levels for the converter in (a)—5 and 25 volts at a current of 300 milliamperes. The converter in (b) has just the one 5-V 300-mA output. Although a clock pulse generator operating at 80 kilohertz is used to synchronize each converter, the



Improving dc-dc converter efficiency. These dc-dc converters employ push-pull inverter transistors that switch at 20 kilohertz. Conventional digital ICs are used to delay the drive signals to the switching transistors so that these devices cannot conduct simultaneously, causing unwanted current spikes. The converter in (a) has a fixed delay, while the delay of the converter in (b) depends on a feedback signal voltage.

switching frequency is only 20 kHz in each case, and the nominal transistor on/off time is 25 microseconds (total period of 50 μs).

In the fixed-delay circuit of (a), flip-flops FF_1 and FF_2 generate the basic square-wave drive for transistors Q_1 and Q_2. The flip-flops divide the clock frequency down from 80 to 20 kilohertz, and the NAND gates provide the delays for the transistor drive signals.

The resulting asymmetrical driving waveforms have an on-time of 23 μs and an off-time of 27 μs. This means that each transistor experiences a 2-μs delay in its drive signal. For the transistors used here, this delay prevents current from flowing into the transformer primary for 0.5 μs. The width of the delay pulse (2 μs here) is too wide if the converter's output ripple voltage increases and too narrow if there is no deadband for the transformer primary current.

In the feedback-adjusted-delay circuit of (b), a binary counter, rather than flip-flops, divides the clock frequency down to 20 kHz. NAND gates again provide the

appropriate delays for producing asymmetrical transistor drive signals.

The feedback voltage, which is taken from the transformer secondary, determines when the transistors turn on, while the reference voltage from the counter output determines when they turn off. To delay the turn-on feedback signal properly, the storage time of the rectifier diodes, as well as the flux flyback time of the transformer, must be taken into account. For circuit (b), the deadband time is 0.3 μs. □

BIBLIOGRAPHY

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