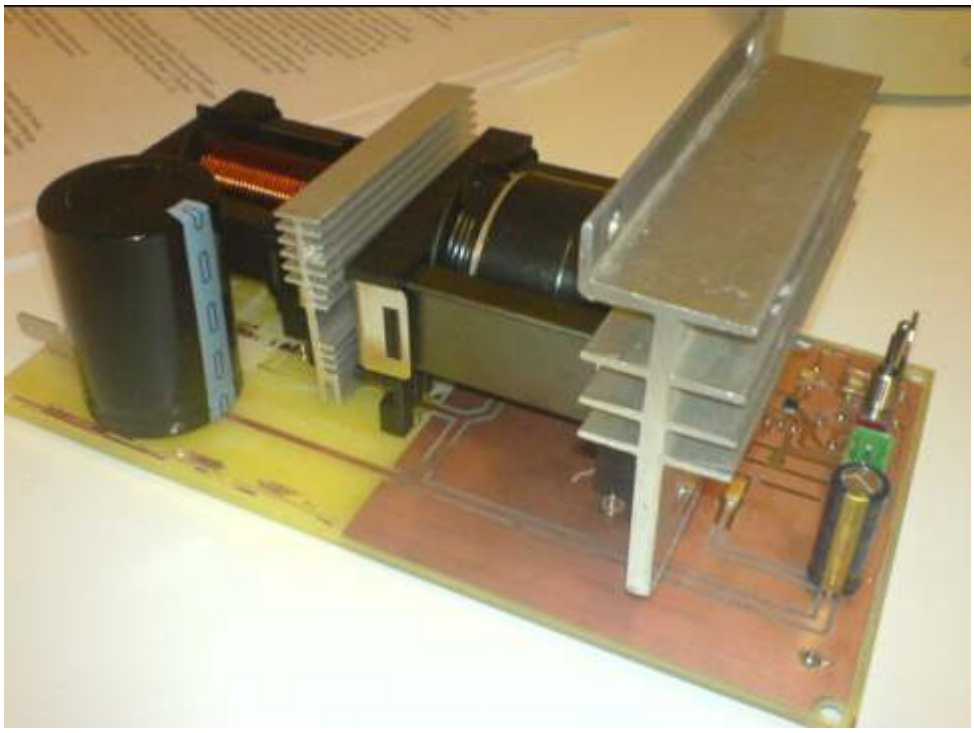
High Speed 2kW DC/DC Converter



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Thesis work 20p, D-level

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3 May 2007

Abstract

This report investigates the possibilities of constructing a DC/DC converter to power an industrial ABB robot so that it can operate without any access to a 3-phase socket. The work is performed at Mälardalens University in Västerås.

The paper is initiated with a theoretical part explaining some fundamentals of power semiconductors in order to provide a deeper understanding of how they behave in high frequency applications.

The work includes two major parts: simulation and building a prototype. Simulations are carried out to get a deeper knowledge in how switched converters behave and to get some help in designing a final prototype. Results from both parts are compared and discussed with the help of figures.

Finally, the work is summarized with a conclusion and some suggestions of improvements that can be made to the prototype developed during this thesis work.

Sammanfattning

I denna rapport presenteras möjliga lösningar för att konstruera en DC/DC omvandlare till en industrirobot så att den kan drivas utan tillgång till ett 3-fas nät. Arbetet är utfört på Mälardalens Högskola i Västerås.

Rapporten inleds med ett teoriavsnitt där grundläggande förståelse för halvledare tas upp, för att få en djupare förståelse för hur dessa beter sig i högfrekventa applikationer.

Arbetet innehåller två stora delar: simulering och framtagning av en prototyp. Simuleringarna utförs för att få en djupare förståelse för hur switchade omvandlare beter sig och som hjälp för att designa en slutgiltig prototyp. Resultaten från båda delarna jämförs och diskuteras med hjälp av figurer.

Slutligen sammanfattas arbetet med en slutsats och ett avsnitt där förbättringar föreslås till den slutgiltiga prototypen som framtagits under arbetets gång.

Terms

Symbol	*Description*	*Unit*
A_e	effective cross-sectional area of core	mm^2
A_L	inductance factor	mm^2
B	magnetic flux density	T
B_r	remanence	T
B_s	saturation flux density	T
C	capacitance	F
f	frequency	Hz
G	Gap length	µm
H	magnetic field strength	A/m
H_c	coercivity	A/m
I	current	A
V	voltage	V
L	inductance	L
N	number of turns	-
V_e	effective of core	mm^3
µ	absolute permeability	-
$µ_0$	magnetic constant ($4π \times 10^{-7}$)	-
$µ_e$	effective permeability	-
$µ_i$	initial permeability	-
$µ_r$	relative permeability	-
ρ	resistivity	Ωm
ESR	Equilavent series resistance	-

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1. Introduction

1.1 Purpose

The purpose of this study is to carry out research on different DC/DC converters. The work should include an extensive background research on different Push-Pull topologies and simulations will be done with a simulation program on the chosen topology.

During the thesis work a couple of prototypes will be built to verify the theoretical simulations.

1.2 Background

Hybrid vehicles demand highly efficient conversion of electrical energy from one voltage level to another. Thanks to modern techniques of DC/DC converters, these allow higher power levels and higher efficiency. The main reason is development of faster semiconductors, but mainly on more efficient ferrite materials working in the range up to 1 MHz. Therefore further development of higher efficient products such as hybrid vehicles is possible today.

Constructing DC/DC converters for high power levels and high efficiency demands high frequency operation. This in turn means higher current levels switched in a high speed.

To be able to construct these converters one has to have a good knowledge in making calculations and how to place components on the PCB board to minimize losses occurring from noise. The noise is an unwanted effect that increases power losses mainly due to its disturbance on the surrounding areas.

2. Theory

2.1 Related work

It is hard to find related work concerning general push-pull, half-bridge and full-bridge topologies. Most of the previous research deals with resonant converters, which are improvements of the general topologies. One method of operating around 1 MHz region is to build up a novel resonant converter. This type of converter introduces soft-switching, which is imperative at high frequencies [1]. The proposed solution introduces two additional switches, which however complicates the switching compared to a general push-pull based topology using only two switches.

However there are some studies that discuss modeling of uninterruptible power supplies using standard push-pull topologies. Using an advanced application of PSpice has shown that problems that could arise in a final prototype can be avoided by first simulating. This requires a good model including parasitic elements. While Puglisi, Ferrari, Tenca & Rebora [2] includes parasitic elements in the model by testing, Ionescu [3] builds a simulation model from a complete prototype, calculating the parasitic elements such as inductances in copper traces to show how un-symmetry can affect the overall function of the power supply.

2.2 DC/DC Topologies

A switched mode DC/DC converter is simply a device that converts a voltage from one level to another. The input can be a rectified line voltage or a battery.

Comparing the linear power supply and a switched mode power supply the benefits with a switched mode converter over the linear one is: size, weight and efficiency [4]. This is due to higher frequencies, allowing the usage of smaller transformers using ferrite cores. The power supply even provides the power supply function through low loss components such as transformers, capacitors, inductors and the use of switches that operate in two stages: on or off mode. Thereby the switches dissipate little power in either state and a higher overall efficiency of the converter is accomplished.

Even though the benefits over a linear power supply are significant, there is one major downside: noise! These noises are caused by high switching speeds. Higher frequencies also increase switching losses and the transformer core losses.

There are several switched mode DC/DC topologies. The ones focused on in this paper are doubled ended push-pull topologies, which mean that the flux swing in the transformer primarily is bi-directional (see fig. 1). This allows more power handling compared to single ended ones, which use a uni-directional core excitation where only the positive first quadrant is used [5].

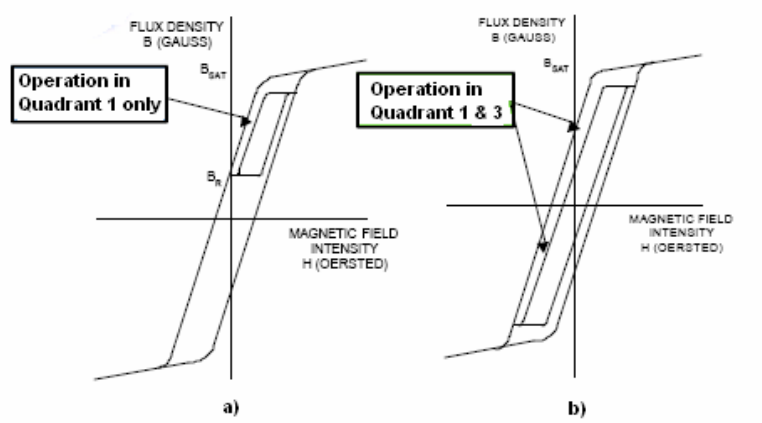

Figure 1 – Uni-Directional and Bi-Directional flux swing

2.2.1 Push-Pull

The push-pull converter operates by switching two transistors alternately, which mean that they are never on at the same time (see fig. 2 for schematics).

When transistor M1 is turned on the input voltage is forced on the upper primary winding. On the secondary side a negative voltage will appear on the lower winding turning on the bottom diode. The opposite occurs when transistor M2 is turned on [6].

An important factor to consider when constructing a push-pull is that the switching transistors have to handle a voltage twice the input voltage. Therefore a Push-Pull converter is suitable for low input voltage applications.

The frequency on the secondary side voltage pulses twice the switching frequency of the transistors [7].

A disadvantage of Push-Pull converters is that a good matching of the switching transistors is required, this to prevent saturation of the transformer core. There are also two primary windings and two secondary windings, which makes the winding by hand more difficult.

The output voltage can be expressed by equation 1:

$$V_{OUT} = 2 \cdot V_{IN} \cdot D \cdot \frac{N_S}{N_P} \tag{1}$$

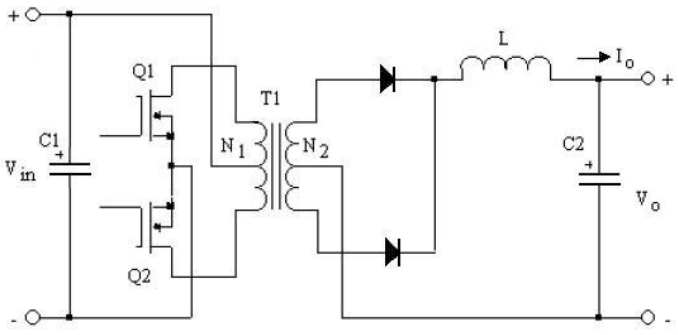

Figure 2 - Push-Pull topology

2.2.2 Half-Bridge

Compared to a Push-Pull converter, the Half-Bridge converter does not have a center tap on the primary side. The input capacitors split the input voltage equally so that the primary only faces half the input voltage when either transistor is turned on [8].

The output voltage can be expressed by equation 2:

$$V_{OUT} = \frac{V_{IN}}{2} \cdot D \cdot \frac{N_S}{N_P} \tag{2}$$

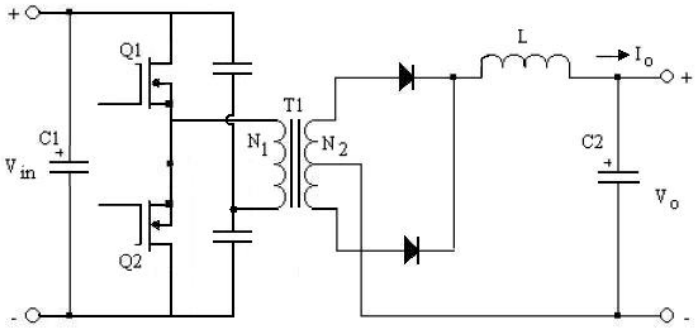

Figure 3 – Half-bridge topology

2.2.3 Full-Bridge

The full-bridge topology uses four switching transistors. They are switched pair wise alternately. Due to the high cost and complexity, the full-bridge topology is often used in very high power applications where AC line is used to power the application [9].

The output is a full wave bridge configuration with approximately half the number of secondary turns.

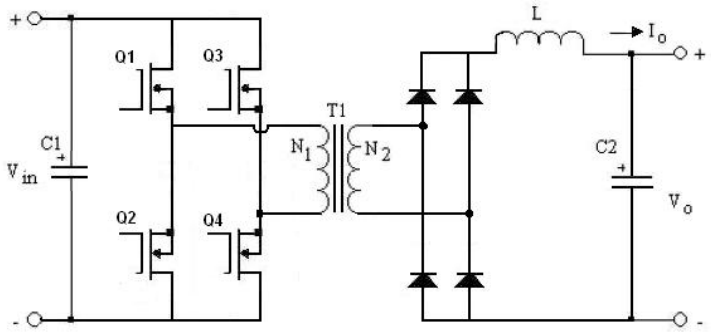

Figure 3 – Full-bridge topology

2.3 Power Semiconductor switches

2.3.1 Introduction

The development of semiconductor devices has made converters more affordable in a large number of applications. This is due to increased power capabilities, easier control and reduced cost of modern power semiconductors.

Currently the power semiconductors can be classified into three groups according to their controllability [10]:

1. *Diodes* controlled by the power circuit
2. *Controllable switches* turned off and on by a control signal
3. *Thyristors*, latched on by a control signal but turned off by the power circuit

2.3.2 Diodes

A diode begins to conduct when it is forward biased. The voltage drop across the device is small, on the order of 1 V depending on the diode type. When the diode instead is reversed biased, a small negligibly leakage current will flow until the reverse breakdown voltage level is reached [11].

A diode can be considered as an ideal component at turn-on because it turns on more rapidly than the transients in the power circuit. At turn-off the current instead reverses for a time t_{rr} before it falls to zero. This phenomenon occurs because excessive carriers have to be swept out and block a negative voltage.

The circuit symbol can be seen in figure 4a, the steady-state i-v characteristic in figure 4b, and its idealized characteristics in figure 4c.

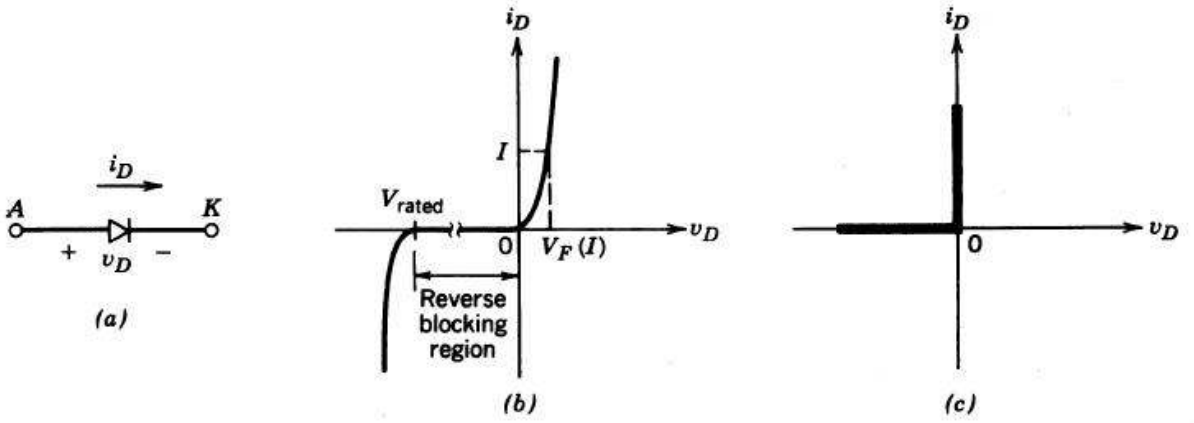

Figure 4 – Diode characteristics

Today there are also various types of diodes on the market. The choice of type depends on the application requirements [12]:

1) *Schottky diodes* – When a low voltage drop is required, suitable for converters with a low output voltage.

2) *Fast recovery diodes* – Suitable for high frequency applications where small t_{rr} is needed.

3) *Line frequency diodes* – When a very low on-state voltage is required, the disadvantage is that t_{rr} is large compared to the other two types.

2.3.3 MOSFET

The MOSFET is a voltage controlled device. A symbol of an n-channel MOSFET can be seen in figure 5. It is fully open when the gate-source voltage reaches a level above the threshold voltage (V_{GS_th}) and off when it is approximately below V_{GS_th}.

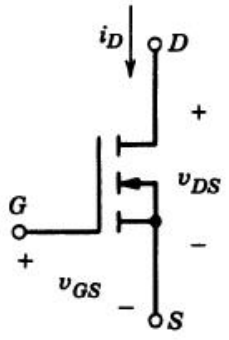

Figure 5 – MOSFET symbol

The switching times for a MOSFET device is very short, between a few tens of nanoseconds to a few hundred [13], therefore it is suitable for very high frequency applications up to 1 MHz region compared to other semi conductors such as GTO, IGBT and MCT. These can instead handle higher currents but has the disadvantage of not being able to operate in several hundreds of kilohertz.

When the device is on its on-state, resistance $r_{DS(on)}$ increases rapidly with the device blocking voltage rating. This means that only MOSFET's, that have low voltage rating, have a low on-state resistance and therefore low conduction losses.

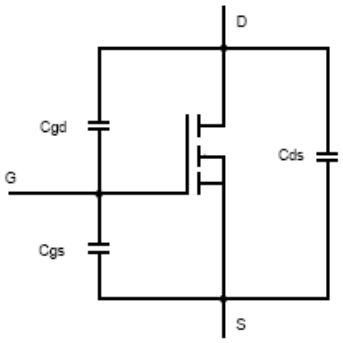

Figure 6 – Internal capacitances

Switching behavior

The switching times of a power MOSFET are determined by the speed at which its internal capacitances (see fig. 6) can be charged and discharged by the chosen drive circuit [14].

Therefore the switching characteristics of the power MOSFET are determined by its three internal capacitances. These capacitances are not fixed but are a function of the voltages between the MOSFET's terminals.

Switching performance

Turn-on

During the turn-on phase the following parameters are of relevance [15]:

- Turn-on time

- Turn-off loss
- Peak dv/dt
- Peak dI/dt

The turn-on time is simply determined by the speed of which the drive circuit can charge the gate.

The average current that has to be supplied is:

$$I_{on} = \frac{Q}{t_{on}} \tag{3}$$

For repetitive switching the average current requirement is:

$$I = Q \cdot f \tag{4}$$

Turn-on losses occur simply during the initial phase when the current flows in the MOSFET. The V_{DS} is also active during the phase. To minimize the loss the turn-on time is required to be as small as possible. Therefore the drive circuit must be able to supply the initial peak current of following magnitude:

$$I_{pk} = \frac{V_{GG}}{R_g} \tag{5}$$

Another problem associated with MOSFET's switched at high speed is the rate of changes in voltage and current. High dv/dt can cause coupling through parasitic capacitances, which can give rise to noise on signal lines. Even high dI/dt can react to trace inductances, which causes unwanted transients and overshoot voltages in the circuit.

Turn-off

During the turn-off phase the following parameters are of relevance [16]:

- Turn-off time
- Turn-off loss
- Peak dVds/dt
- Peak dId/dt

In comparison to the turn-on sequence the turn-off procedure is nearly an inverse process. The main difference is that the current charging C_{gd} must flow through both the load impedance and the gate impedance. For that reason high load impedance will slow down the turn-off speed.

As a conclusion the speed of a power MOSFET is determined by how fast the internal capacitances can be charged and discharged by the drive circuit.

Losses

Power losses in a MOSFET can be divided into four main groups [17]:

Conduction losses – The conduction losses is given by equation 6:

$$P_C = I_D^2 \cdot R_{DS(on)} \tag{6}$$

Switching losses – Switching losses can be neglected at low frequencies but are dominant at high frequencies. As the MOSFET turns off much slower than it turns on the main switching loss occurs during the turn-off state.

The losses can be reduced by using snubber components connected between source and drain. This has the effect of reducing the rate of rise of voltage. Even turn-on losses can be reduced by connecting inductors in series with the MOSFET.

Diode losses – This loss occurs when an anti-parallel diode inherent in the MOSFET structure is used. The size of the dissipation can be calculated by multiplying the forward voltage drop and the average current carried by the diode.

Gate losses – Losses in the gate are given in *equation 7:*

$$P_G = \frac{Q_G \cdot V_{GSD} \cdot f \cdot R_G}{R_G \cdot R_{DR}} \tag{7}$$

where R_G is the internal resistance, R_{DR} the external gate drive resistance, V_{GSD} is the gate drive voltage and Q_G is the peak gate charge.

2.4 Transformer

2.4.1 Core material

Usage of higher switching frequencies reduces the size of transformers and thereby the whole converter. In earlier days the limitations of switching frequency were dependant on semiconductors. Today power MOSFET's are capable of switching frequencies beyond 1 MHz. Therefore the transformer has become the limiter of using higher frequencies and thereby a limit in reducing converter size.

There are two types of ferrites: Soft ferrites and hard ferrites. Soft ferrites contain zink, nickel or manganese compounds and have low coercivity. The most common combinations are MnZn and NiZn. MnZn main features are high permeability (μ_i) and high B_S. NiZn instead characterize of higher resistivity (lower losses) and are suitable for high frequency applications over 1MHz.

In general, ferrites are characterized by their high permeability (100-10000), low losses and high frequency handling. A major disadvantage is though a low B_S, which means that the transformer can saturate easier. One solution for this problem is to use a ferrite core with an air gap [18].

Ferrites consist of tiny particles. Each particle shows its own magnetic behavior. Without any magnetization the particles are directed in different directions. If a magnetic field is present the particles will start to direct in the same direction as the field. This will increase the magnetic field density until all the particles are directed in the same direction. When this happens the core is saturated and the permeability is 1, the same as if there would not be any core present. When the magnetic field is reduced the magnetic flux density will not reduce linearly and become zero. It will instead cross the magnetic field density axis at a point B_r [19]. If the magnetic field strength continues becoming more negative the core will eventually get saturated once again. If the magnetic field is reversed once again the field strength will again be zero with an added magnetic field, this is called magnetic coercivity. If the field strength continues getting more positive the core will once again get saturated. The loop that is created is called a hysteresis curve (see fig. 7).

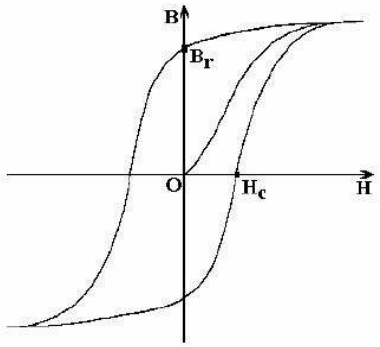

Figure 7 – Hysteresis curve

The size of the area determines the size of the losses. For low losses the area should be as small as possible.

2.5 Pulse-Width-Modulation (PWM)

PWM stands for Pulse Width Modulation. The switch duty cycle (D) is defined as the ratio of the on duration to the switching period [20].

In DC-DC converters the transformation of a DC level to another is accomplished by using one or more transistors and hence controlling the switch on (t_{on}) and off (t_{off}) durations.

PWM can be identified with two parameters: the duty cycle and the clock cycle.

A duty cycle of various size means that t_{on} and t_{off} is varied.

In figure 8a one can see that the signal has a duty cycle of 10%. That is, the time of t_{on} is 10% of the whole period (T) and therefore off the remaining 90%. A duty cycle of 50% means that the t_{on} duration is half the clock cycle (see fig. 8b).

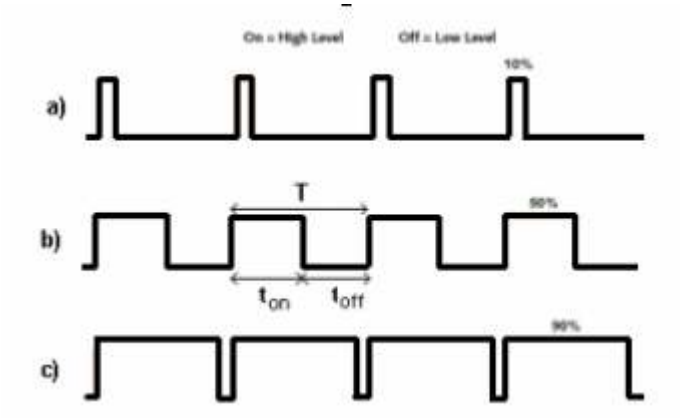

Figure 8 - PWM

2.6 PCB design

PCB stands for *printed circuit board.* The board is made of one or several layers of insulating material containing conductors. The insulator is made of different materials based on plastic, fiberglass or ceramics. During the etching process the unnecessary portions of the conductors are etched off leaving only the traces that connect the components on the board.

Designing a good PCB layout requires good knowledge of effects such as coupling of signals through parasitic capacitances and radio transmission.

2.6.1 EMI and layout considerations

Drawing a layout for switching power supplies is critical. Therefore there are a few guidelines that are helpful to design a good layout [21]:

1. Minimize lengths and areas of loops, which contain currents switched at high frequency.

2. Capacitors that bypass the supply voltage and reference pins to all ICs should be placed close to these pins.

3. Try to draw a symmetrical layout as possible.

4. The width of the traces should be based on the rated current and acceptable temperature rise.

5. Include a ground plane on both sides of the PCB to reduce noise, ground loop errors and absorbing more of the EMI radiated by the output inductor.

2.7 Simulation

Computer simulation is a good tool for analyzing circuit behavior and thus saving time and money. When it comes to power electronic systems, these consist of passive components such as diodes, thyristors and other solid-state switches. Because of this the circuit topology changes as a function of time when switches open and close. This makes it impossible and often undesirable to solve for voltages and currents in a

closed form as a function of time. On the other hand computer simulation is capable of modeling such circuits.

Simulating circuits makes it possible to calculate circuit waveforms, steady-state and dynamic performance, and the current and voltage ratings of components.

2.7.1 SPICE

There are several circuit oriented simulators available on the market such as SPICE, EMTP, and SABER among several others. In this paper a SPICE based simulator is used: PSpice.

SPICE stands for *Simulation Program with Integrated Circuit Emphasis*. The language was developed at the University of California, BERKLEY. SPICE is a language developed for simulating integrated circuits.

2.7.2 Parasitic elements

To get as realistic results as possible one has to include parasitic elements in the model. In this paper MOSFET drain, source and gate inductances are included. These inductances can be calculated by the equation *seen in figure 9.*

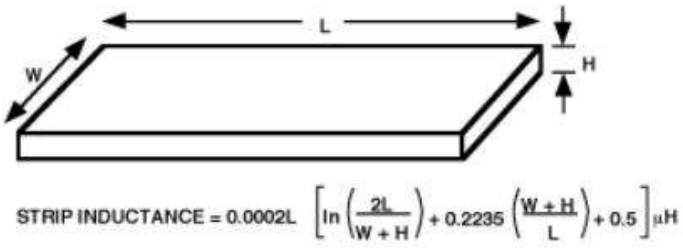

Figure 9 – Calculating strip inductance

3. Method

The work is started by collecting information about switched circuits in general and also related work done earlier. This is done by reading books and scientific articles.

Thereafter a model is constructed in an appropriate simulating program to help understanding switched converters and choosing appropriate components before designing the final prototype.

The transformer will be winded by hand using copper wire on the secondary side and copper foil on the primary side. It will be tested by building up a simple test circuit to verify if it transforms a DC voltage to the desired level.

In the end the results from the prototype are compared with the simulations to confirm if they are equivalent.

4. Design

The final proposed circuit can be seen in appendix 1.

4.1 Topology selection

The topology chosen for the final implementation is the Push-Pull, because of its easy implementation compared to the two other topologies. The disadvantage is that the winding gets a bit more complicated due to the need of two primary and two secondary windings. Also the choice of MOSFET is limited due to the fact that twice the input voltage is required and the availability of high voltage with high current ratings is limited today.

4.2 Controller

The LM5030 from National Semiconductor is chosen for the PWM controller. It includes all necessary features to implement a push-pull based converter.

Two alternating 1.5A gate drivers are included. It also includes a high-voltage start-up regulator, which handles an input range of 14V up to 100V. Oscillator frequency up to 1MHz is adjustable with a single external resistor. The frequency is calculated by using equation 8.

$$RT = \frac{(\frac{1}{f}) - 172 \cdot 10^{-9}}{182 \cdot 10^{-12}} \quad (8)$$

4.3 Switches

The choice of semiconductor type for the switches is mainly based on V_{DS}, $R_{DS(on)}$, current handling and input capacitances.

The main criterion is that the MOSFET has to be able to handle twice the input voltage, in this case 96 V. The on resistance ($R_{DS(on)}$) should be as low as possible to minimize overall conduction losses. The component should also have a low input capacitance and gate charge to reduce the drive circuit demands.

For testing with lower input voltages IRF540N is used due to its low cost. It has a V_{DS} of 100V, which is enough using a supply voltage up to 36 V. For higher than 40 V input IRF3314 is used, RF3314 has the following data.

- V_{DS} = 150V
- $R_{DS(ON)}$ = 0.042 Ω
- I_D = 43 A

4.4 Rectification diodes

The requirements of the rectification diodes is to have as low forward voltage drop as possible to minimize the overall losses, handle a minimum current of 5 A plus some

ripple, have a high reverse voltage rating exceeding 400 V with margin due to high spikes and have fast recovery.

If the output of the converter had been low voltage a fast Shottky diodes would have been most suitable for minimizing the overall losses in the converter.

Unfortunately there are not any Shottky diodes on the market with a high reverse voltage rating and a low voltage drop. Therefore a fast recovery diode that fulfils the other requirements is chosen:

DESEP12-12A, a fast recovery diode from IXYS Corporation.

- V_{RRM} = 1200 V
- I_{FAVM} = 11 A
- t_{rr} = 50 nS

4.5 Transformer design

The specification of the DC/DC converter:

Input voltage	V_{IN}	48 V
Output voltage	V_{OUT}	400 V
Output power	P_{OUT}	2 kW

Table 1- Specification

4.5.1 Bobbin

An ETD type of bobbin is used to construct the transformer. The size is ETD59, which is the biggest possible for an ETD type (see table 2).

ETD59/31/22			
Symbol	***Parameter***	***Value***	***Unit***
Σ(l/A)	Core factor (C1)	0.378	mm^{-1}
V_e	Effective volume	51500	mm^3
l_e	Effective length	139	Mm
A_e	Effective area	368	mm^2
A_{min}	Minimum area	360	mm^2
M	Mass of core half	130	G
A_L	Inductance factor	5600 ± 25%	nH
W_A	Bobbin area	366	mm^2
MWW	Minimum winding width	41.2	Mm

Table 2 – ETD59 bobbin data

For the secondary winding AWG 18 copper wire is used. It has a diameter of 1.2 mm.

There are two secondary windings, which mean that the first winding is winded back and forth and the second winding is winded the same way over the first one.

The number of turns using the wire becomes the minimum winding width divided by the wire diameter: 41.2/1.2 ≈ 34.

Both secondary windings finished at 67 turns.

The two primary windings are winded over the secondary windings using copper foil with a width of 30 mm because wider foil was not available for the time being. The desired turn ratio is 10, which means that the primary windings need to be 7 turns. Both primaries are winded parallel at the same time.

4.5.2 Core material

As the purpose of the thesis is to implement a DC/DC converter that operates at frequencies up to 1 MHz, the ferrite core is chosen to have low losses at those frequencies.

Ferroxcube is a leading supplier of ferrite components. Therefore a Swedish distributor of their components is contacted. [22]

It turns out that newer and higher frequency ferrite cores are harder to acquire because the market determines the availability of those ferrites. Industries still prefer to construct converters that operate at lower frequencies, which in turn lead to bigger converters and more use of ferrite materials suitable for lower frequencies.

The highest frequency ferrite that is kept in stock today by Ferroxcube is 3F3, which is optimized for frequencies from 200 kHz up to 700 kHz.

4.6 Output filter design

The output filter consists of a low pass LC-stage. Because the secondary effective side ripple is twice the input frequency this allows to keep the inductor dimensions small.

An ETD49 is used for the bobbin and a 3F3 ferrite core having an air gap of 0.5 mm/core to construct the inductor. The air gap minimizes the risk of getting the inductor saturated and therefore acting as a resistor. The value of A_L using a total gap width of 1 mm is 260 nH/n^2

Copper wire having a diameter of 1.2 mm is used, which gives 27 turns. Winding one layer yielded in 27 turns.

Calculating the inductance using equation 9 yields in an inductance of 190 µH.

$$L = N^2 \cdot A_L \tag{9}$$

The capacitor handles a voltage up to 450 V and has a capacitance of 470 µF. It also has a low ESR value and is intended to be used in professional switch-mode power supplies.

4.7 PCB design

Designing of the PCB is crucial. The layout is made as symmetrical as possible. A two sided layout design is made. The primary side of the transformer is the crucial part due to high current levels switched fast, therefore designing the PCB layout the main focus is laid on the primary side.

The switches are located as near as possible the primary windings to reduce the length of the traces between the drain pins and primary windings and hence minimizing trace inductances. Also the traces from the source pins to the current sensing resistor are kept short.

The rectification diodes are also located in a short distance between the transformer and output inductor.

Placing the input capacitors correctly is also essential. When the converter switches it draws current pulses from the input source, thereby the size of the source impedance is important. Even a small amount of inductance can cause spiking on the voltage at the input of the converter. Therefore placing two capacitors, one faster and one slower, near the switching converter input is preferable.

The whole PCB design can be seen in appendix 2.

4.8 Test bench for transformer

A test bench is constructed for testing the transformer.

A dual output MOSFET driver IR210494 is used to obtain two alternative pulses. The typical dead time is 540 nS compared to LM5030, which has 135 nS. The frequency is set to 10-30 kHz because of the long and hanging cables connecting everything on a test board (see fig. 10).

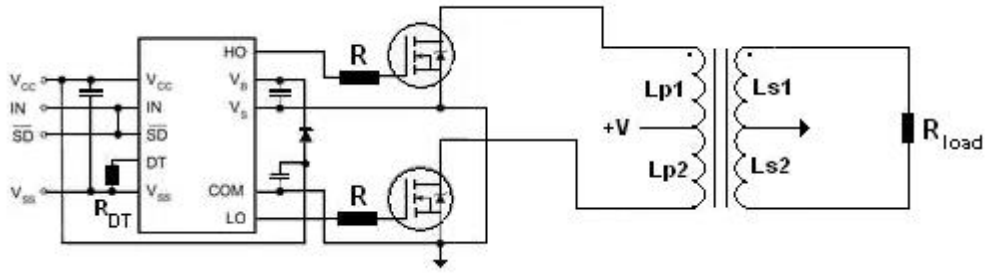

Figure 10 – Test Bench for transformer testing

5 Simulation

A model of the converter is built up in PSpice schematics. All components in the model are chosen to resemble the ones chosen for the final prototype as close as possible.

Complete models are found from respective manufacturer. Otherwise a model with similar characteristics is used. A complete model can be seen in appendix 3.

The LM5030 circuit is built up with help of the block diagram found in its data sheet (see appendix 4). The soft start function is not included in the simulation model. Therefore caution has to be taken during simulation

5.1 Alternating outputs

As a push-pull topology described earlier needs two PWM signals with 180 degrees phase shift.

The PWM block contains of one JK flip-flop, one inverter, two AND-grinds with three inputs and one SR-latch. The SR-latch is designed with two NOR-grinds because of a more straightforward translation in SPICE.

The J and K inputs are connected to 5 volts, this gives two alternating outputs Q and /Q. Q is connected to one AND-grind and the /Q to the other one.

The inverter simply inverts the clock signal, this is signal is connected to both AND-grinds.

The function of the SR-latch is to reset the current clock-cycle whenever there is a pulse at the reset input. The Q output of this latch is connected to both AND-grinds.

According to the datasheet for LM5030 the typical dead time between the falling edge of one gate driver and the rising edge of the other gate driver is about 135 nS. To achieve this dead time the pulse length of the clock signal is set to around 135nS. Because the clock signal is inverted the AND-grinds are reset for 135nS each period.

See appendix 4 for PWM block and *figure 11* for a test simulation showing the typical dead time.

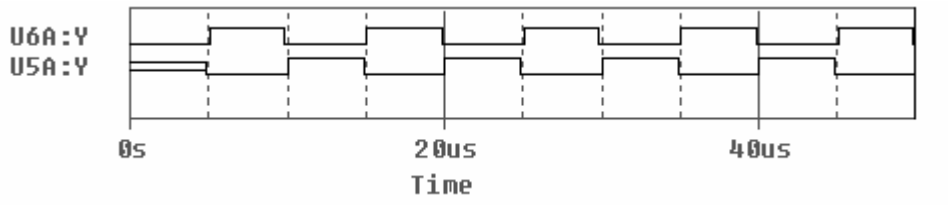

Figure 11 – PWM pulses

5.2 Gate drivers

The gate drivers for the two MOSFET transistors are built as a totem pole compilation (see appendix 6).

When the top transistor is on, the circuit will source current from the power supply. When the bottom transistor is on, the circuit will sink current to ground.

The drivers were built up by using two npn transistors and one pnp transistor.

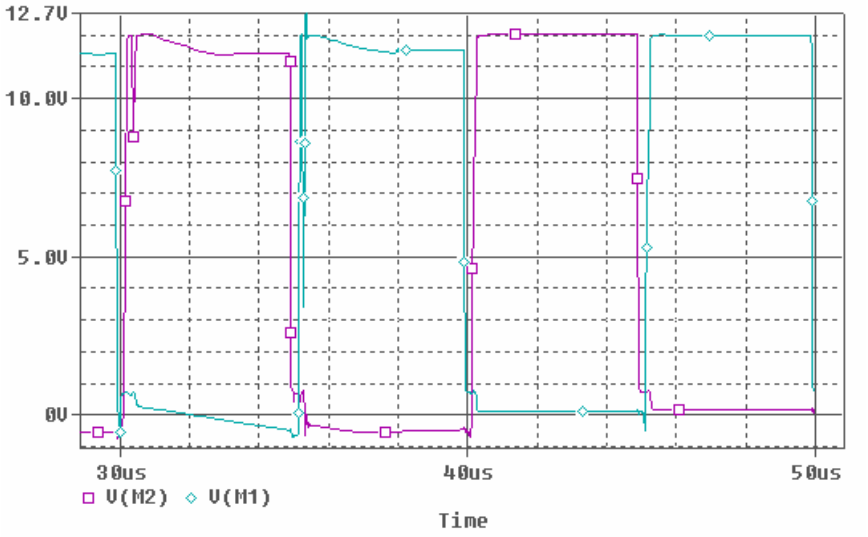

Figure 12 – Gate driver pulses

5.3 Current sense

There are two comparators included in the LM5030: one for the current sensing and one for regulating the duty-cycle.

In order to fulfill the speed requirements MAX908 comparators from MAX-IC are chosen. The part has a 40 nS propagation delay and a power consumption of 3.5 mW.

A test of the current sense part can be seen in figure 13 where a test signal rising above the threshold voltage of 0.5 V and decreasing under it is simulated.

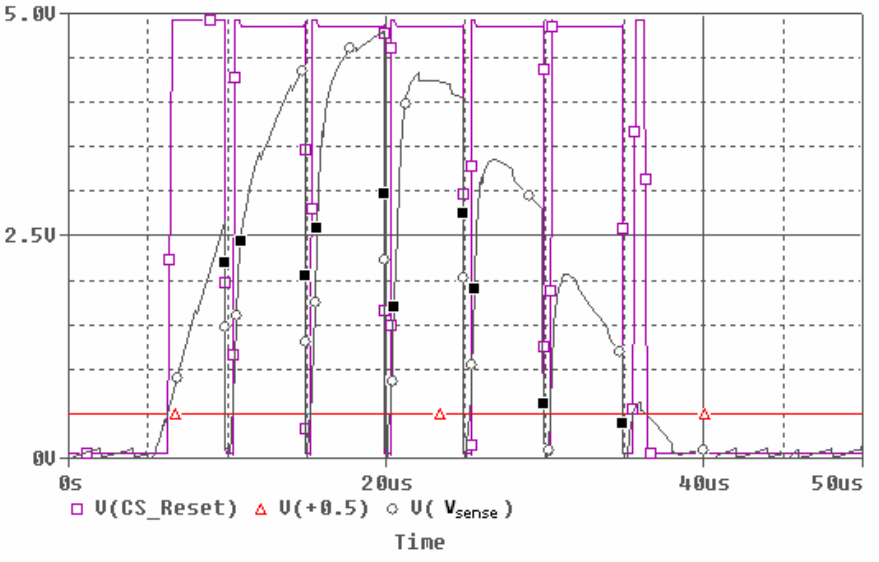

Figure 13 – Current sense

5.4 Error amplifier

The error amplifier compares the output voltage from the converter with a fixed reference set to 1.25V.

Because the linear interval for an amplifier is short the operational amplifier is designed as an inverting amplifier with a gain chosen such that the output is regulated as properly as possible depending on the output voltage level from the converter. A test of the regulator can be seen in figure 14 where an input voltage of 40 V is regulated to 150 V.

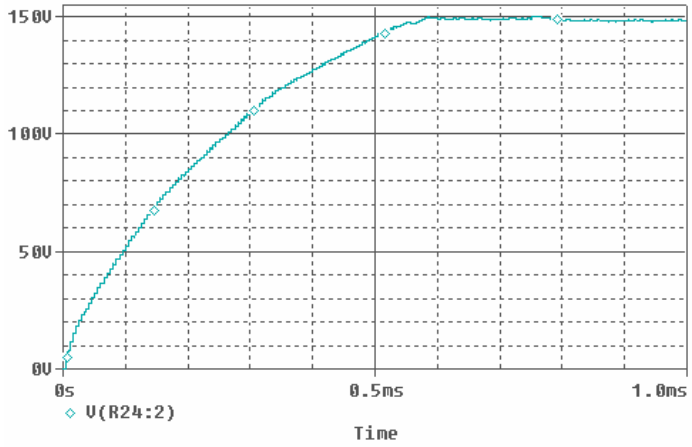

Figure 14 – Regulated output

5.5 Transformer

The transformer is a non-linear with a center tap on both primary and secondary side. The transformer is built up with four inductors connected together with using a kbreak model, which is a nonlinear model. The model connects the inductors with a model of a chosen ferrite and core size and type.

The winding relations are set by changing the values of the inductors.

5.6 Oscillator frequency

The frequency is set by using a standard clock model in PSpice.

5.7 Parasitic elements

As mentioned before the parasitic elements included in the simulation model are the MOSFET drain, gate and source inductances.

The traces for both switches are the same length, width and height due to a symmetrical design.

The following inductances are calculated from the milled PCB board using the equation seen in figure 9:

- Gate:

$$L = 0.0002 \cdot L \cdot (\ln(\frac{2 \cdot L}{W + H}) + 0.2235 \cdot (\frac{W + H}{L}) + 0.5) = 0.0002 \cdot 10 \cdot (Ln(\frac{2 \cdot 10}{5 + 0.038}) + 0.2235 \cdot (\frac{5 + 0.038}{10}) + 0.5)$$

- Source:

$$L = 0.0002 \cdot L \cdot (\ln(\frac{2 \cdot L}{W + H}) + 0.2235 \cdot (\frac{W + H}{L}) + 0.5) = 0.0002 \cdot 5 \cdot (Ln(\frac{2 \cdot 5}{5 + 0.038}) + 0.2235 \cdot (\frac{5 + 0.038}{10}) + 0.5)$$

- Drain:

$$L = 0.0002 \cdot L \cdot (\ln(\frac{2 \cdot L}{W + H}) + 0.2235 \cdot (\frac{W + H}{L}) + 0.5) = 0.0002 \cdot 10 \cdot (Ln(\frac{2 \cdot 10}{5 + 0.038}) + 0.2235 \cdot (\frac{5 + 0.038}{10}) + 0.5)$$

6. Results

6.1 Transformer test bench

Testing the transformer is made using two different supply voltages: 12 V and 38 V. The output of the transformer is heavily loaded.

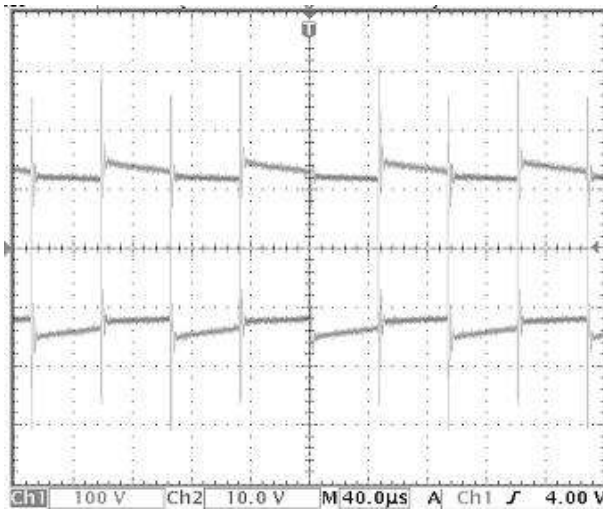

Figure 15 - Output before rectification

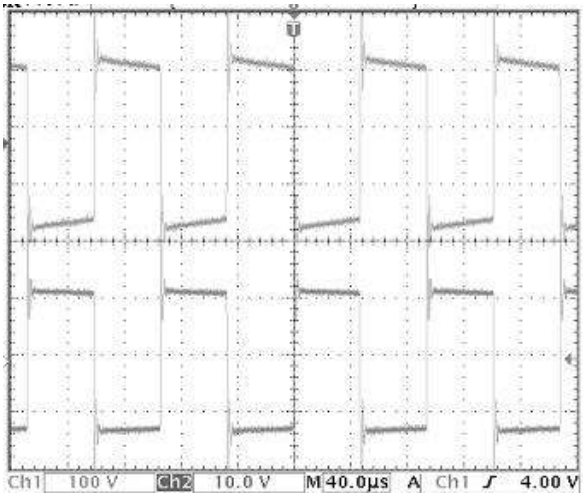

Figure 16 – Both secondary pulses

Using 12 V as input gives two alternative outputs on the two secondary windings as required. The top to bottom level is 240 V, which is about 10 times more on each winding compared to the input (see fig. 15 & 16).

This is expected to happen if the transformer windings are correctly winded and the winding relation is 67/7 ~ 10.

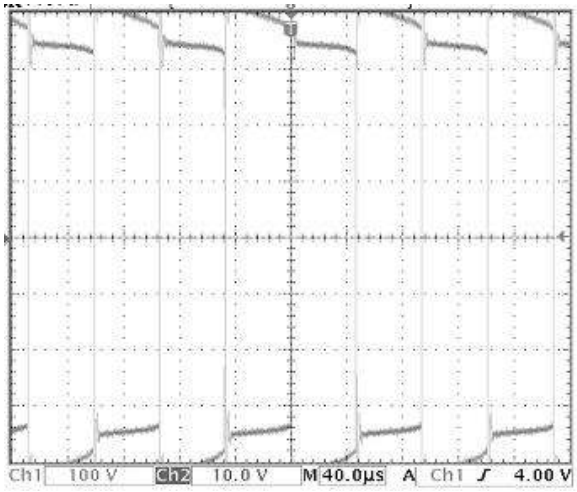

Figure 17 – Output before rectification

An input of 38V results in an output of approximately 740 V from top to bottom. This is also an expected output level (see fig. 17).

6.2 Prototype and simulations

Testing the performance of the prototype and simulation model is done using two power supplies: voltage cube and four 12 V batteries connected in series. Testing will start with a low frequency 30 kHz and then increasing it up to several hundreds of kHz. The same procedure is done with the simulation model.

For each frequency tested several measurements will be taken:

- V_{OUT}
- V_{DS}
- Current sense voltage
- V_{OUT} before rectification

Test 1 – Prototype & Simulation:

$$V_{UT} = \frac{3.9M}{12k} \cdot 1.25 \approx 406V, f = 200kHz, R_{load} = 3.4k, V_{in} = 40V$$

Figures on the left illustrate ¨results from the prototype and the ones on the right from the simulations

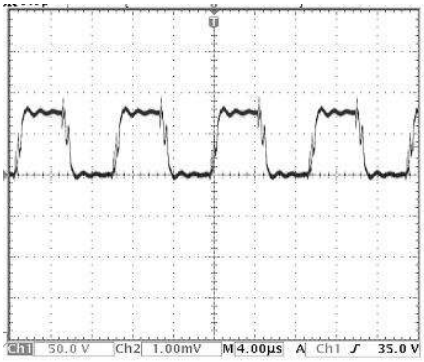

Figure 18 - V_{DS}

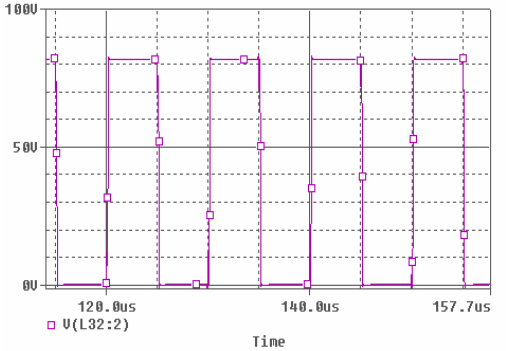

Figure 19 - V_{DS}

In the pictures above one can see that the simulation gives a more ideal curve compared to the measured.

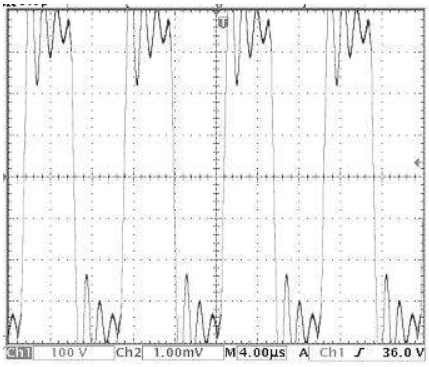

Figure 20 – V_{sec} before rectification

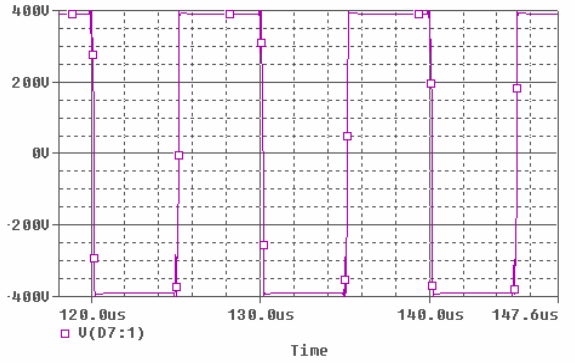

Figure 21 – V_{sec} before rectification

The same phenomena can be seen looking at the secondary voltages before rectification. Ripple is more present in the real prototype compared to the simulation model.

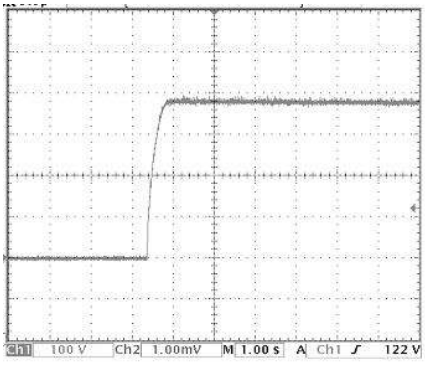

Figure 22 - V_{out}

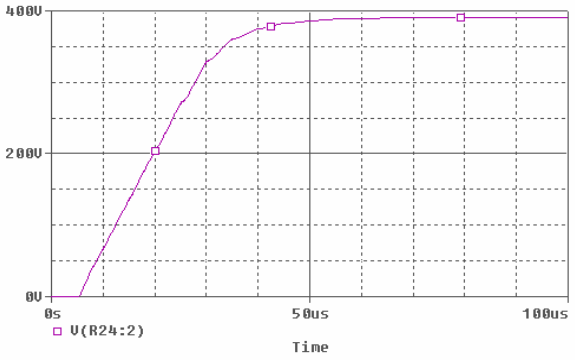

Figure 23 - V_{out}

Comparing the output signals they look very much the same expect the rise time. For the prototype it is 0.5 s and for the simulation it is only 30 µs. This shows, once again, the ideal characteristics of the model compared to the prototype. One factor that could affect the rise time for the simulation model is the output capacitor, which has a value of 1 µF during simulations. This is necessary to keep the simulations times low.

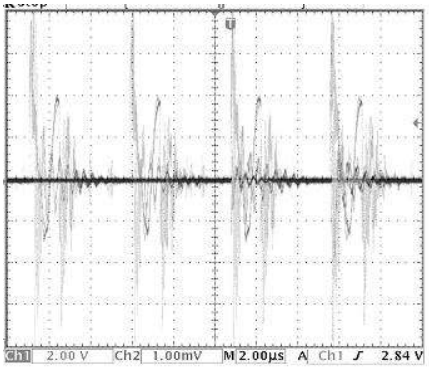

Figure 24 – Current sense

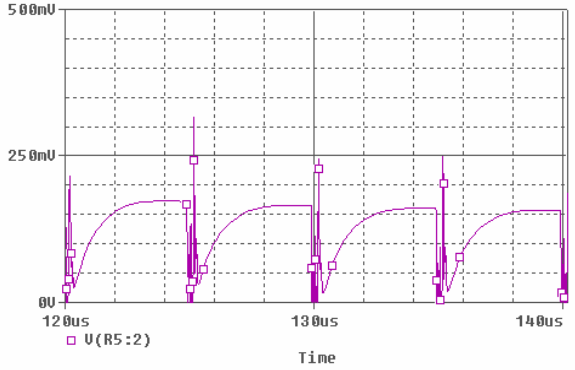

Figure 25 – Current sense

Once again comparing the current sense signal one can see in figure 24 that the signal is more distorted compared to the simulated seen in figure 25.

No more tests are able to be carried out for the prototype because the current sense signal activates the soft-start mechanism in the controller. To investigate the cause for this, several attempts are made. One is to increase the frequency to 500 kHz. This resulted in the same behavior. Another attempt to solve the issue is made by changing the resistance of the current sense resistor. A higher value results in a burned resistor because the power gets too high. A lower valued resistor does in turn not burn up, but the circuit does not deliver more power.

A final attempt is made by separating the controller part from the board. Therefore two new PCB boards are milled (see appendix 7, 8 & 9). This results in a functional circuit for lower power levels, but is not enough to obtain a fully functional converter delivering 2 kW.

Test 2 - Simulation:

$$V_{UT} = \frac{3.9M}{12k} \cdot 1.25 \approx 400V, f = 200kHz, R_{load} = 80\Omega, V_{in} = 40V$$

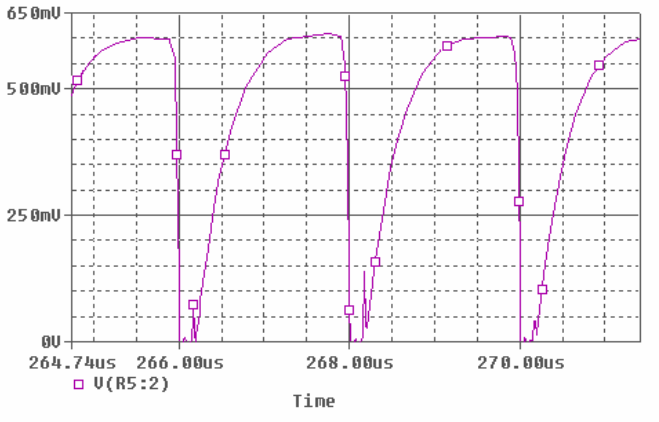

Figure 26 – Current sense signal

Figure 26 shows that the level is near the second threshold voltage. It exceeds the cycle by cycle threshold of 0.5 V, but not the soft-start level of 0.65 V. Therefore the cycle by cycle is activated and the output voltage is slightly limited.

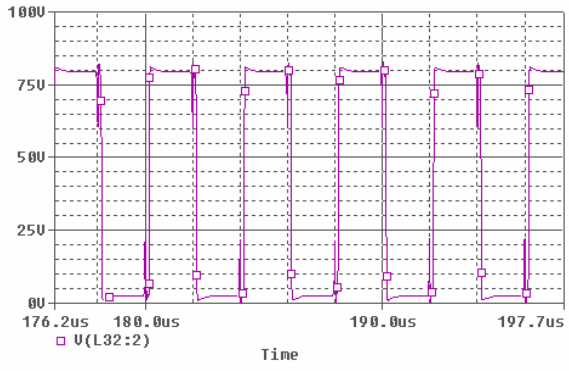

Figure 27 – MOSFET drain voltage

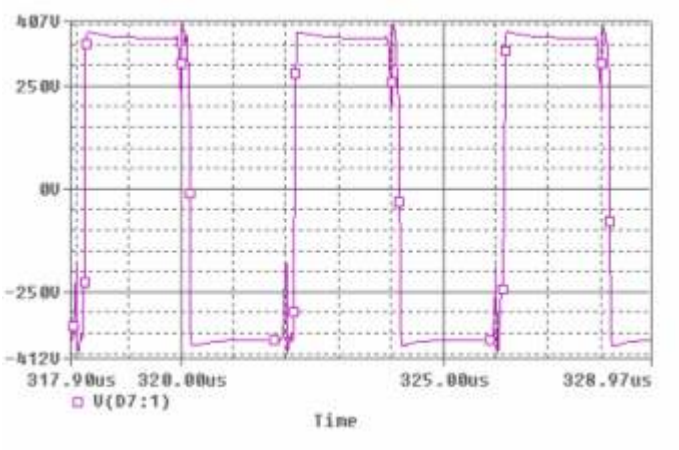

Figure 28 – Secondary output before rectification

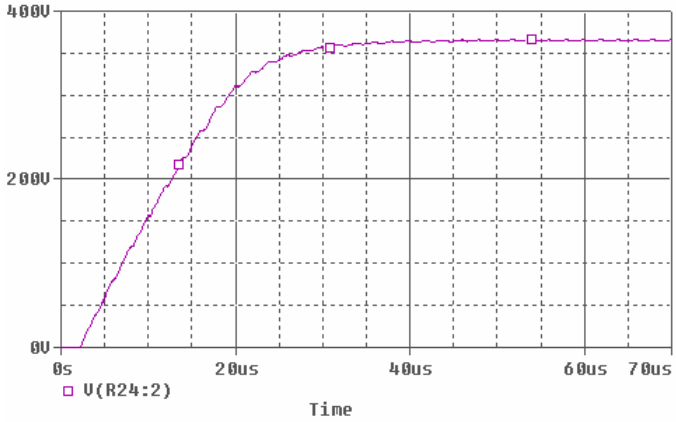

Figure 29 – V_{OUT}

As mentioned above the cycle by cycle is activated, which limits the output voltage. A higher frequency does not manage to increase the power capacity. Decreasing the value of the current sense resistor has a huge effect on the overall efficiency of the converter.

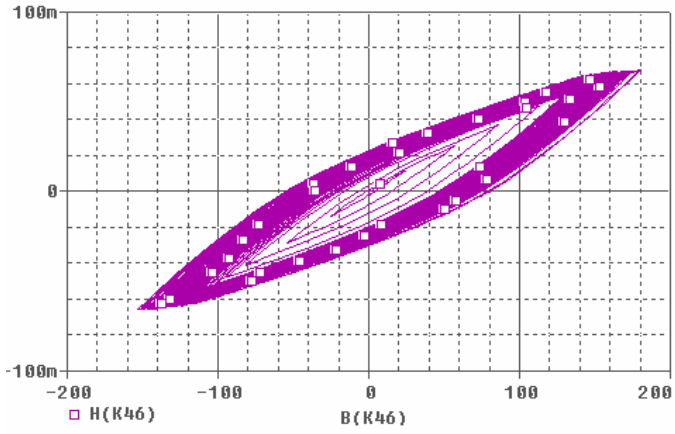

Figure 30 – Hysteresis

The hysteresis curve shows no sign of saturation (see fig. 30). On the other hand the MOSFET drain current shows a little sign of saturation as it flattens out a bit every cycle (see fig. 31). If the model is correctly used the ramping signal should be formed as a sharp triangle.

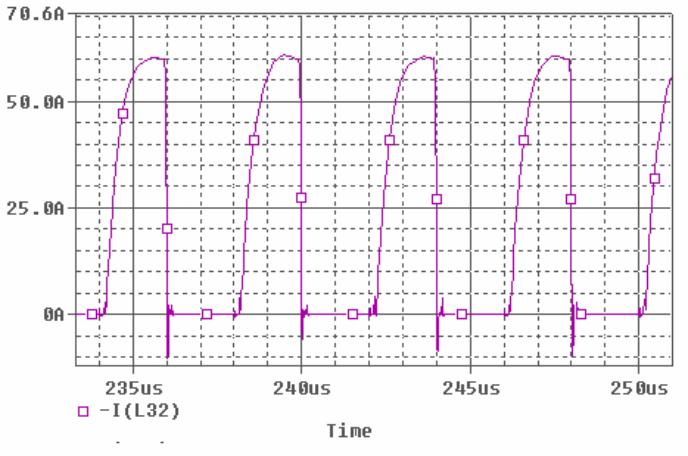

Figure 31 – MOSFET drain current

7. Summary and conclusions

The purpose of this thesis is to construct a DC/DC converter for a mobile robot so that it can be powered from several standard 12 V DC car batteries.

First a research is made on a few double ended topologies to get an understanding on how switched DC/DC converters work.

Thereafter a topology is chosen based on a few factors such as price and complexity.

A model of the final construction is drawn in PSPICE schematics using models resembling the ones used in the final prototype. The results from the simulations are used to construct a prototype and compared with the simulations to see if they are equivalent.

As for the simulations a common problem is encountered: convergence. Because of some unknown factors the whole model is not able to be simulated due to the problem. There are also some problems using the transformer model for an ETD59 type. For some reason the model does not behave exactly as a real one.

The prototype is not able to deliver the required power. The main reason for this a bad layout that causes the current sense control pin to activate. Separating the control part from the rest of the PCB is tested and also supplying it from its own power source. This correction allows using the entire controller and voltage levels up to 400 V, but not handling higher power levels.

A comparison of the simulation model and prototype show similar behavior. The prototype shows more ripple and interference on the different signals, which is expected because of several factors that are not included in the simulation model. It is confirmed that a model has to include all parasitic elements, temperature dependence and outer influences such as noise if an accurate model is to be simulated before constructing a prototype.

Still one can discuss how accurate the simulations are due to the lack of functionality of the transformer model. Research has been done on finding out how the model functions, but without any greater success.

8. Future work

Instead of using a Push-pull topology a half bridge topology can be examined. This allows using lower rated MOSFET's, which are easier to find with higher current ratings.

If this would not be sufficient switches can be paralleled. This decreases the total internal MOSFET resistances and also allows double currents being switched.

The layout of the PCB boars can be optimized further to minimize noise, especially on the ground trace.

The winding of the transformer can be improved by using copper foil that overlay the whole winding surface. This will allow more effective usage of the transformer core and thereby more power handling.

Finally, using a simulation program more suitable for power electronics circuits can be tested.

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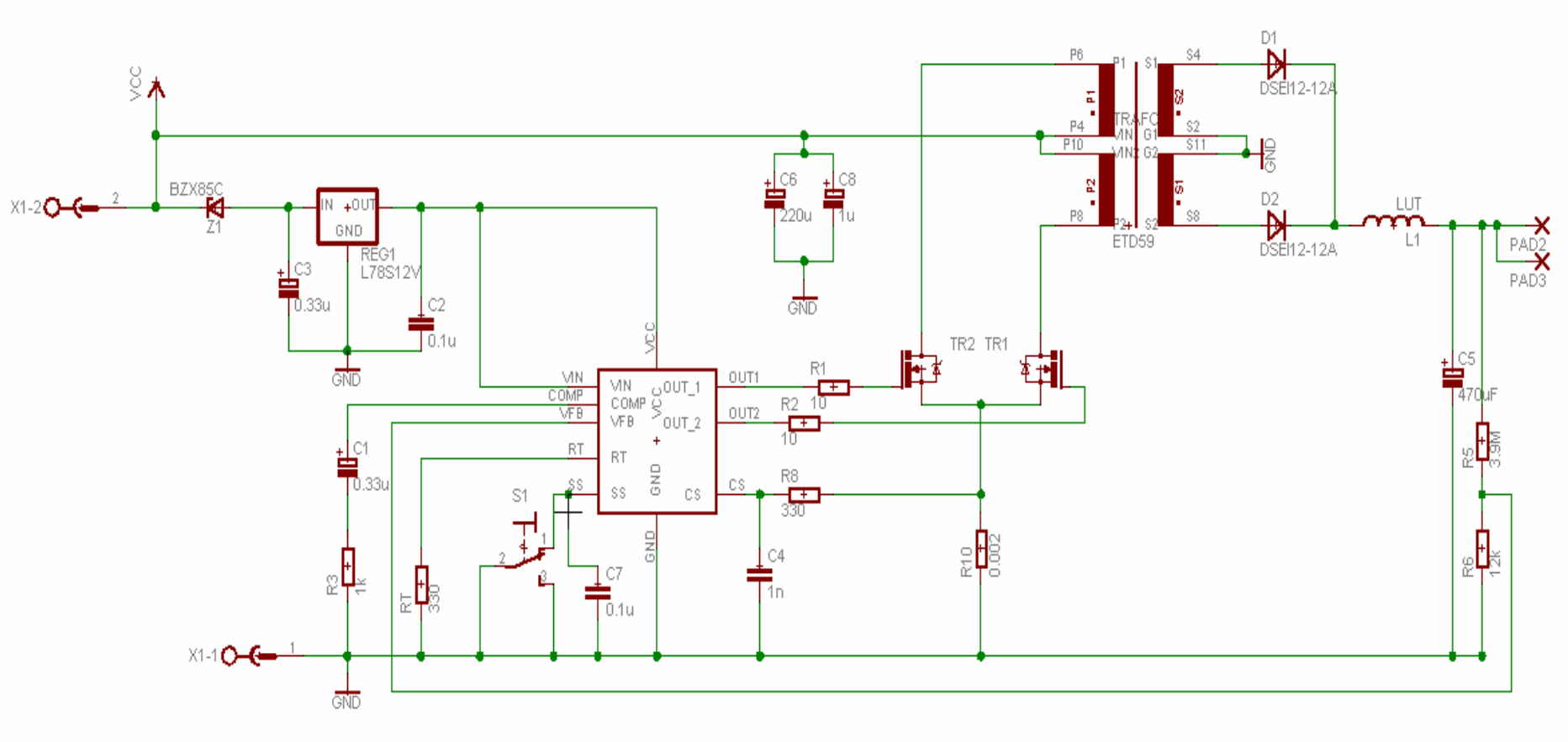
rolf.lindgren@ferroxcube.com

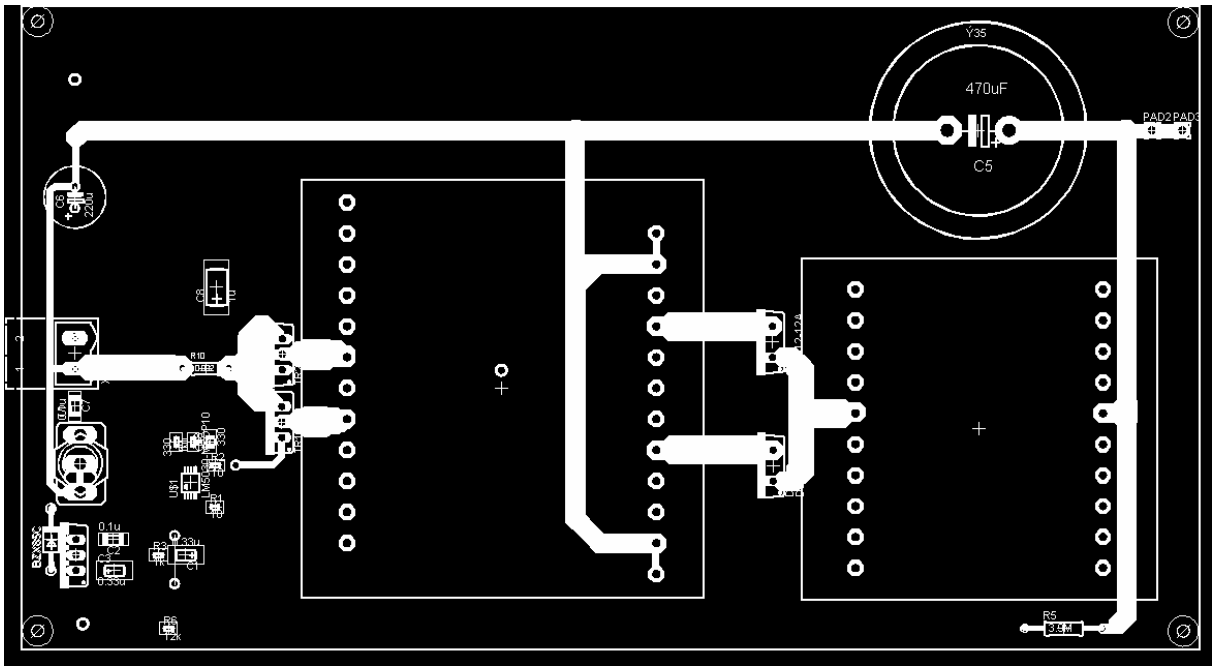
Appendix

Appendix 1

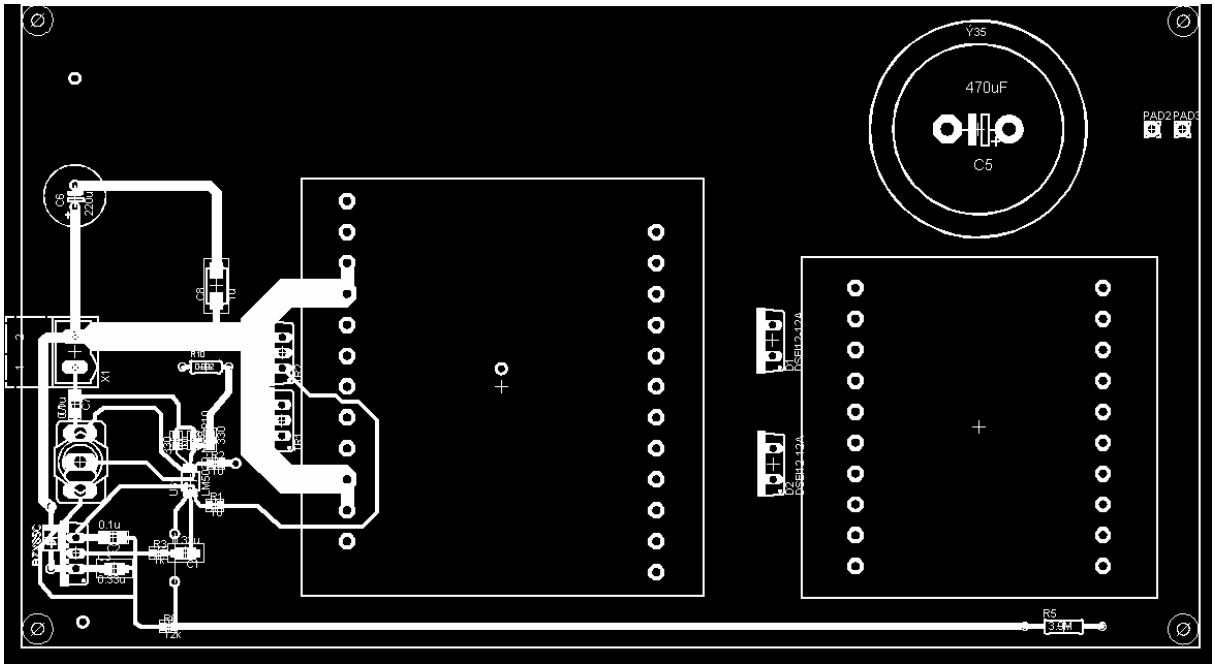


Appendix 2

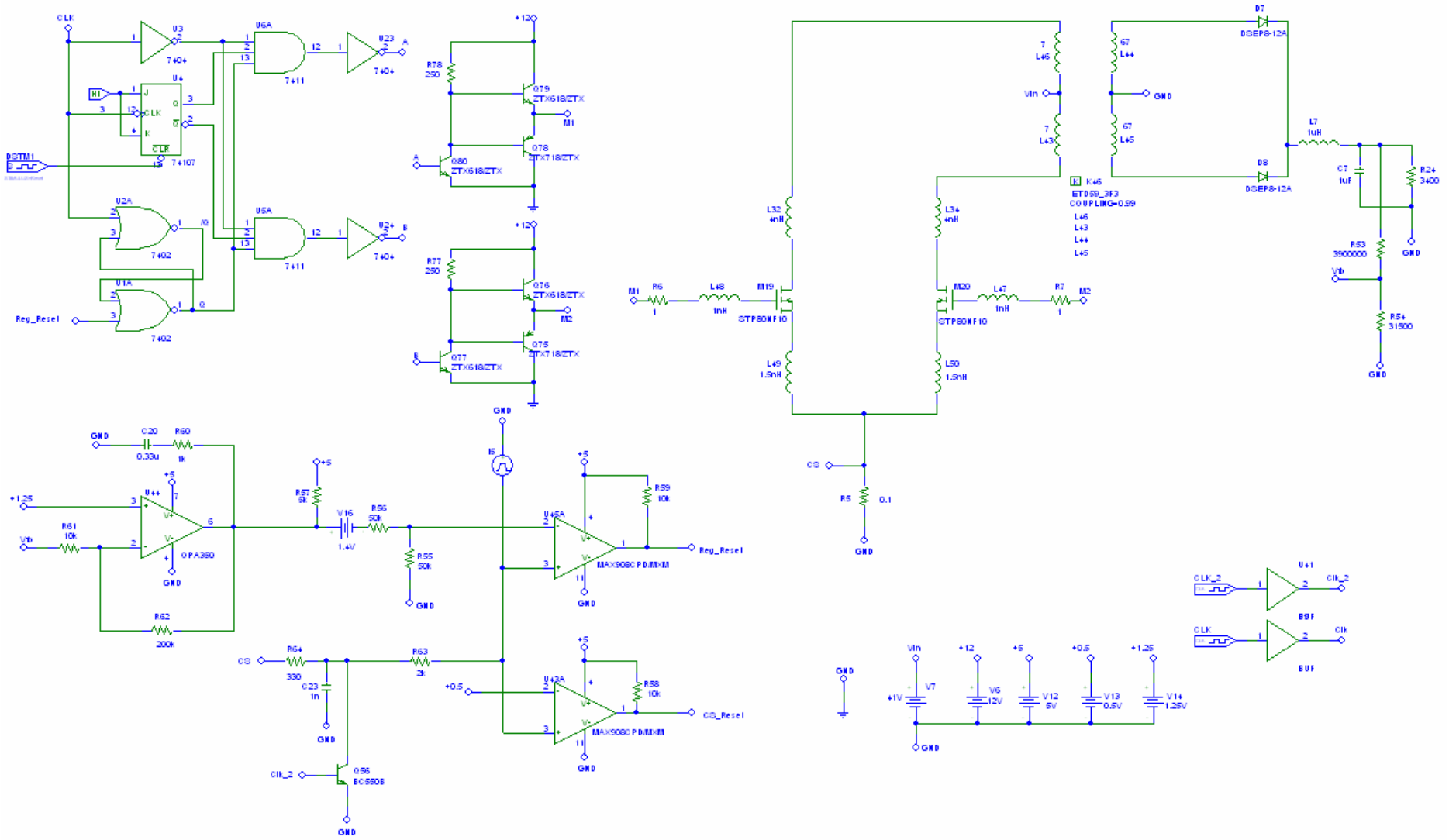
Bottom



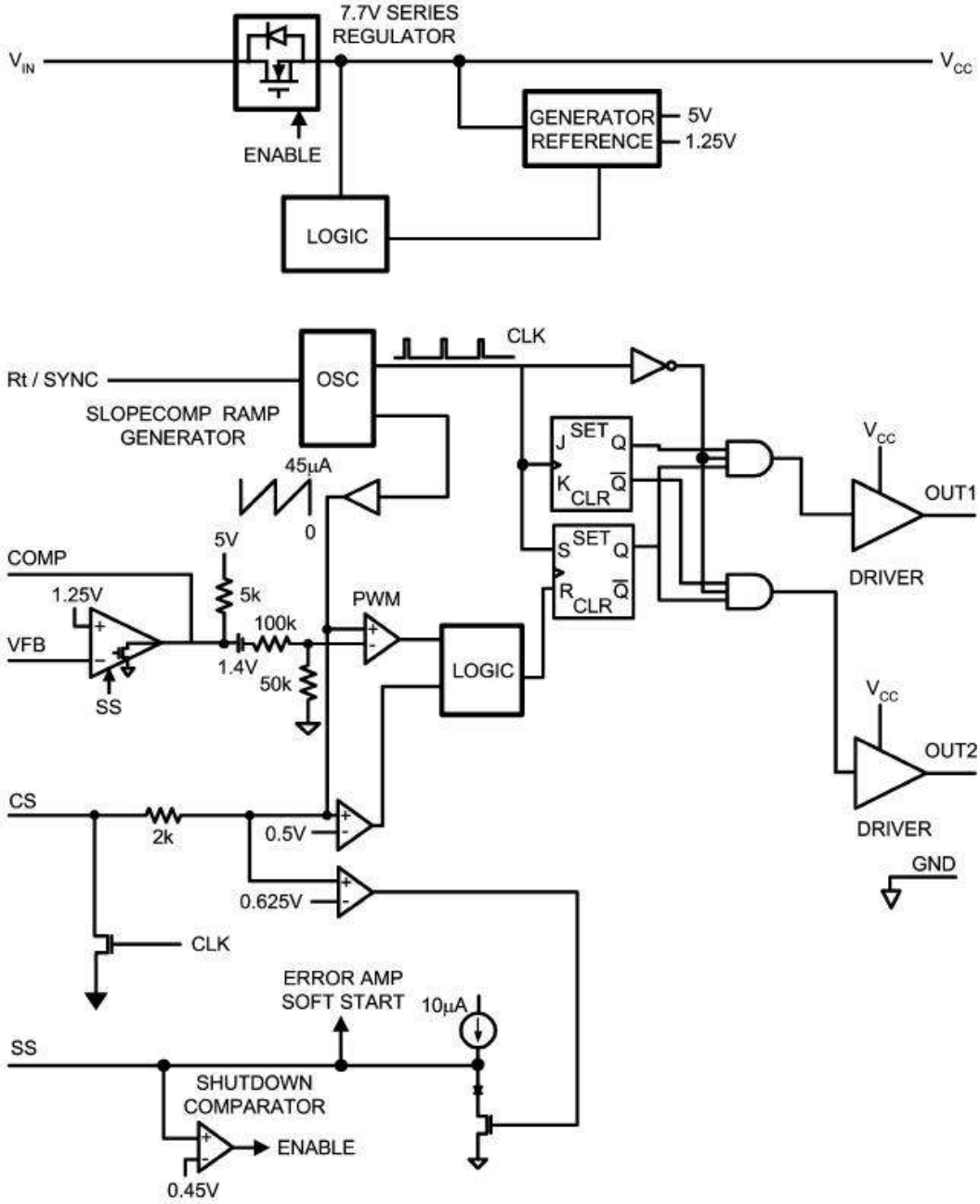
Top



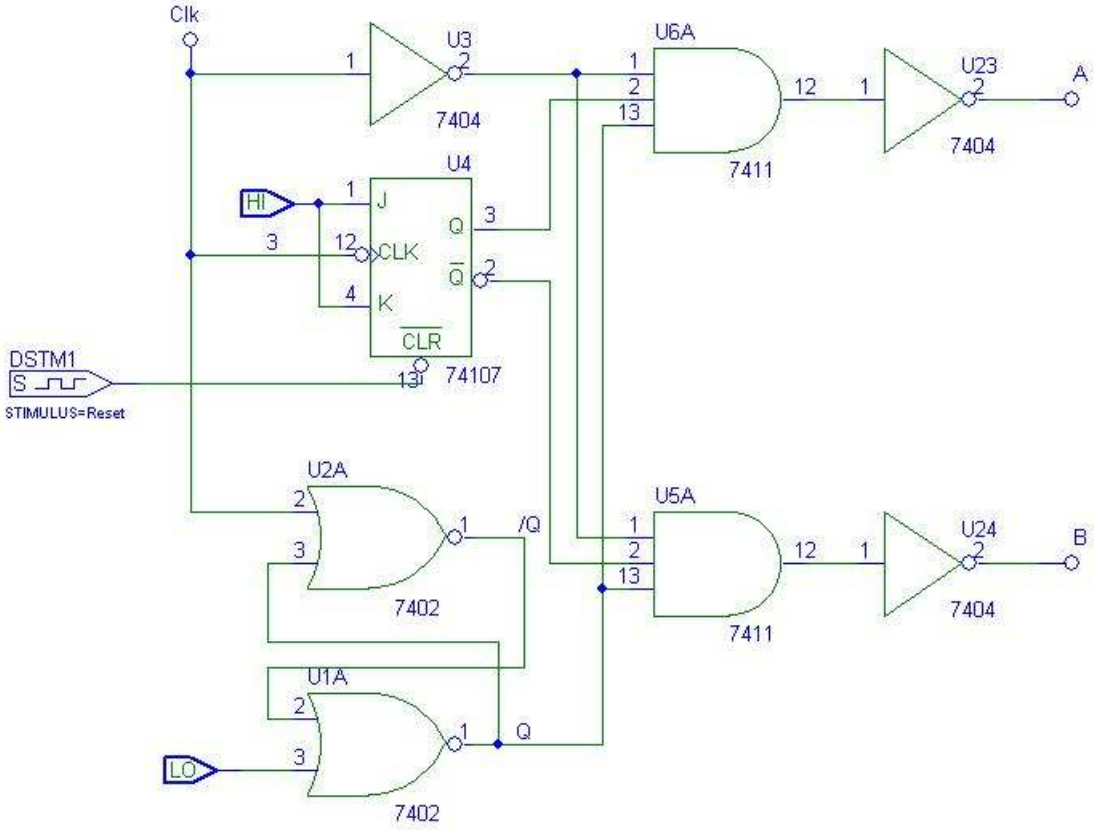
Appendix 3 – Simulation model



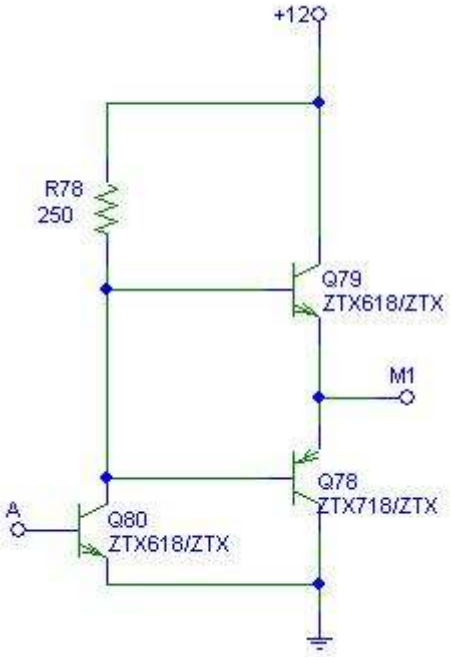
Appendix 4 – Block diagram



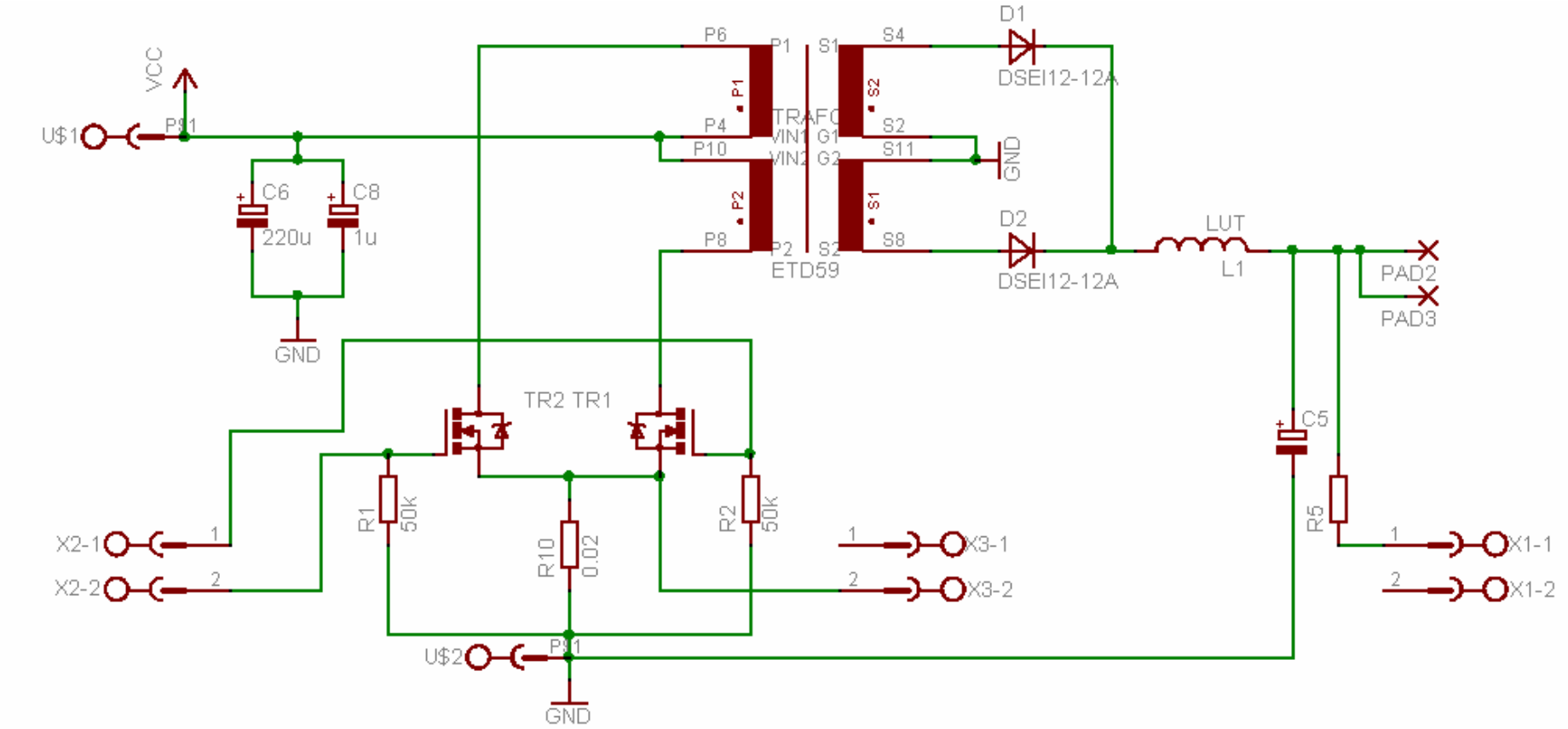
Appendix 5 - PWM



Appendix 6 – Gate driver

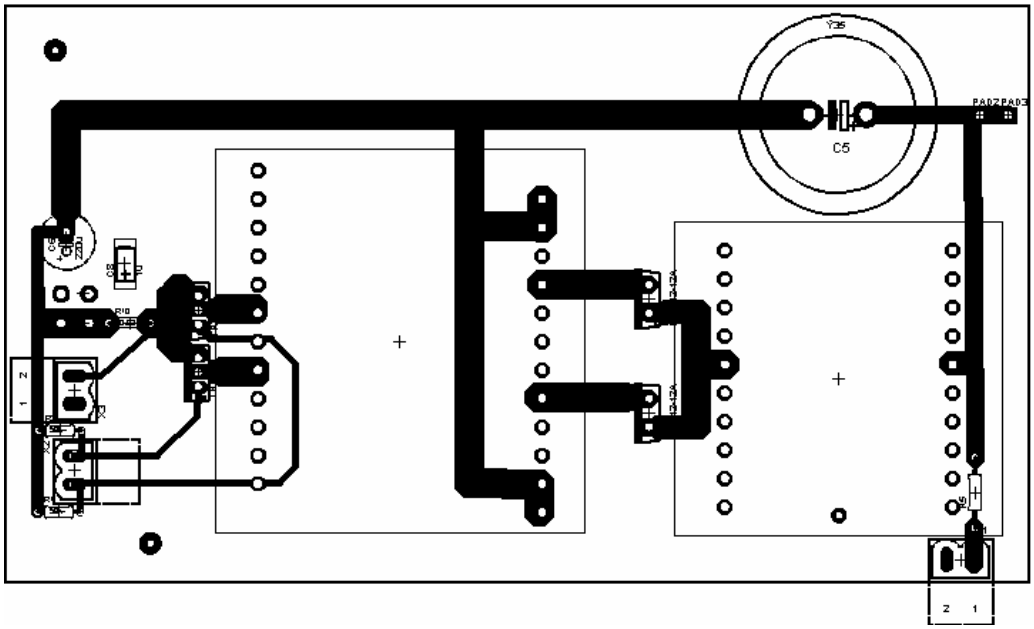


Appendix 7 – New schematics without the controller

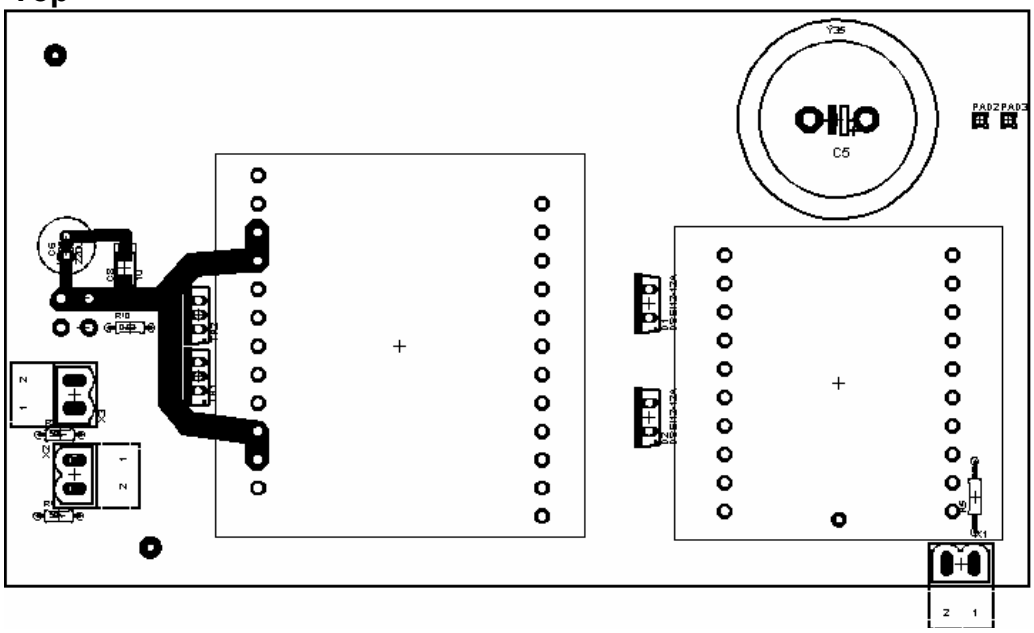


Appendix 8 – New PCB board without the controller

Bottom



Top



Appendix 9 – New Controller PCB board