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Input-Source Impedance Affects DC-DC Converter Performance

To maintain dc-dc converter stability, power-system designers typically operate under the assumption that input-source impedance should be small compared to the converter's input impedance. But, not all understand exactly why this is the case.

To ensure the stability of dc-dc converters, most power-system designers adhere to the common rule that input source impedance should be small compared to the converter's input impedance. Not all understand exactly why.

It is also a common practice for most power-system designers to use a large electrolytic capacitor across the input of the dc-dc converter. In this article, we will analyze the input impedance of a switch-mode dc-dc converter, and explain the reasoning behind the common rule and common practice.

A switch-mode dc-dc converter, regardless of its topology, presents negative incremental input impedance. This can be better understood through the following qualitative reasoning. A dc-dc converter works to maintain a constant output voltage, V_o , at a certain level of power, P_o . To do this, it will absorb, from the input source a power, P_i , given by:

$$P_i = \frac{P_o}{\eta} = V_i \times I_i \quad (1)$$

Where:

η = converter efficiency

Assume the input voltage decreases by a quantity, $-\Delta V_i$. For the converter to sustain the output power, it will increase the input current by a quantity, ΔI_i , so that the input power stays constant at P_i . Assuming infinitesimal variation for V_i and I_i , it is possible to write:

$$\frac{dv_i}{di_i} = r_{i_d} \quad (2)$$

Where:

r_{i_d} = incremental input resistance

For a negative voltage variation corresponding to a positive current variation, the incremental resistance will have a negative sign. The input resistance varies according to input conditions because it depends on power from the input voltage at which the converter is working, as well as the output power that it is delivering.

For a 24-V input converter with an input range of 18 to 36 V and working at a 200-W load, the input current at 36 V_{in} is:

$$I_i = \frac{P_i}{V_i} = \frac{P_o}{\eta \times V_i} = \frac{200}{0.83 \times 36} = 6.7 \text{ A} \Rightarrow r_i = \frac{V_i}{I_i} = \frac{36}{6.7} = -5.4 \Omega \quad (3)$$

Under the same conditions, if the voltage reduces to 18 V, the current will increase to 13.5 A and the resistance will be -1.33Ω .

It is possible to come to same conclusion using a different approach.^[1] Assuming



Fig. 1. A commercial dc-dc converter that employs zero current switching.

that the converter is 100% efficient, input power and output power have the same value, P , and it is possible to write:

$$r_i = \frac{dV_i}{dI_i} = \frac{d}{dI_i} \frac{P}{I_i} = -\frac{P}{I_i^2} = -\frac{V_i}{I_i} \quad (4)$$

A switch-mode dc-dc converter can be seen as a dc transformer, having a transformation coefficient, n , defined as:

$$n = \frac{V_i}{V_o} = \frac{I_o}{I_i} \quad (5)$$

The coefficient, n , is dynamically adjusted by the regulation loop to keep the output voltage constant, regardless of the variations in load and input voltage. With this in mind, Eq. 4 can be written as:

$$r_i = -\frac{nV_o}{I_o} = -n^2 \frac{V_o}{I_o} = -n^2 R_L \quad (6)$$

Where:

R_L = load resistance

For a basic forward converter, the value of n is:

$$n = \frac{1}{D} \quad (7)$$

Where D = duty cycle of a pulse-width modulator (PWM) converter

In the case of a zero-current switching (ZCS) dc-dc converter (Fig. 1), the control variable of the regulation loop is not the duty cycle, but the repetition frequency instead; therefore, as a first approximation:

$$r_i = -\frac{R_L}{f^2} \quad (8)$$

Fig. 1 is a dc-dc converter employing ZCS. The impedance of the source feeding the input of the ZCS module directly affects both the stability and transient response of the module. In general, the source impedance should be lower than the input impedance of the module by a factor of ten, from dc to 50 kHz. To calculate the required source impedance, use the following formula:

$$Z = -\frac{0.1(V_{LL})^2}{P_{LL}} \quad (9)$$

Where:

Z = required input impedance

V_{LL} = low line input voltage

P_{LL} = input power of the module

INPUT-SOURCE IMPEDANCE AND STABILITY

When a dc-dc converter works in a real application, it is connected to a power source having its own internal impedance, which is not zero. Also, additional input impedance may be intentionally

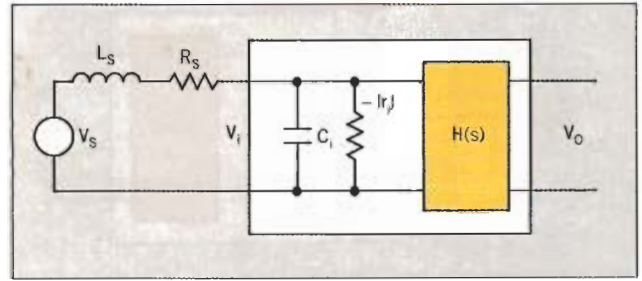


Fig. 2. A typical dc-dc converter connects to a power source having its own internal impedance, which is not zero.

added, for example with an input EMI filter. The complete block diagram is in Fig. 2.

Here, the negative incremental input impedance is indicated as: $-|r_i|$. Further, an additional internal capacitor, C_i , has also been added—as is typical for such designs—at the input stage of a dc-dc converter. Calling $H(s)$ the transfer function of the dc-dc converter:

$$H(s) = \frac{V_o}{V_i} \quad (10)$$

The overall transfer function, including the input source impedance is:

$$\frac{O}{V_S} = H(s) \frac{Z_P}{Z_P + Z_S} \quad (11)$$

This can also be written as:

$$\frac{V_o}{V_S} = H(s) \frac{1}{1 + \frac{Z_S}{Z_P}} \quad (12)$$

As a general design rule, if $Z_S \ll Z_P$ in Eq. 12, then the transfer function, $H(s)$, is not affected by the input-source impedance. This observation derives the general practical rule of keeping the source impedance at least 10 times smaller than the internal dc-dc converter input impedance.

It is possible, however, to study more accurately the source impedance effects using a detailed model. In this case, we can write:

$$Z_P = -|r_i| // x_C = \frac{-|r_i| \frac{1}{sC_i}}{-|r_i| + \frac{1}{sC_i}} = \frac{-|r_i|}{1 - s|r_i|C_i} \quad (13)$$

and

$$\frac{V_o}{V_S} = H(s) \frac{\frac{-|r_i|}{1 - s|r_i|C_i}}{R_S + sL_S - \frac{|r_i|}{1 - s|r_i|C_i}} = \frac{|r_i|}{s^2 L_S C_i |r_i| + s(|r_i| C_i R_S - L_S) + |r_i| - R_S} H(s) \quad (15)$$

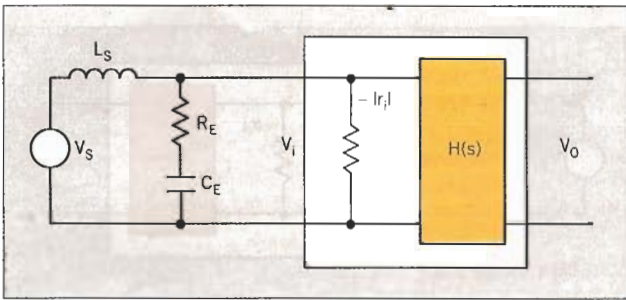


Fig. 3. A common practice is to put a large capacitor in parallel with the input stage of a dc-dc converter.

$$Z_S = R_S + sL_S \quad (14)$$

Replacing the Z_S value in Eq. 11 with the Z_S value from Eq. 14 results in:

(See Eq. 15, Pg. 25)

To verify the effect of the source impedance on converter stability, it is possible to analyze the roots of the characteristic Eq. 15 and, by the Nyquist criteria, ensure that these will fall in the left half plane of complex domain.

The characteristic equation can be written as:

$$s^2 L_S C_i + s \left(C_i R_S - \frac{L_S}{|r_i|} \right) + \left(1 - \frac{R_S}{|r_i|} \right) = 0 \quad (16)$$

The roots of this quadratic equation are:

$$s_{1,2} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \quad (17)$$

Where:

$$a = L_S C_i \quad (18)$$

$$b = \left(C_i R_S - \frac{L_S}{|r_i|} \right) \quad (19)$$

$$c = 1 - \frac{R_S}{|r_i|} \quad (20)$$

With a > 0, for $s_{1,2}$ to have negative real part, it is necessary that b > 0 and c > 0, therefore:

$$C_i R_S - \frac{L_S}{|r_i|} > 0 \Rightarrow R_S > \frac{L_S}{C_i |r_i|} \quad (21)$$

and

$$1 - \frac{R_S}{|r_i|} > 0 \Rightarrow R_S < |r_i| \quad (22)$$

ANALYZING THE RESULTS

Analyzing the results of Eq. 21 and 22, there is an important remark to be made. In fact, one

$$\frac{V_O}{V_S} = \frac{|r_i| (1 + sR_E C_E)}{s C_E (|r_i| - R_E) - 1} H(s) = \frac{|r_i| (1 + sR_E C_E)}{s^2 L_S C_E (|r_i| - R_E) + s (C_E R_E |r_i| - L_S) + |r_i|} H(s) \quad (25)$$

The impedance of the source feeding of the input of the ZCS module directly affects both its stability and transient response. Source impedance should be lower than the module's input impedance by a factor of ten, from dc to 50 kHz

obvious condition is: $R_S < |r_i|$, as discussed in the general case. However, according to Eq. 21, R_S cannot be arbitrarily small. In fact, if R_S is made too small, such as to violate Eq. 21, the system will show instability, because the RLC input network will be under-damped.

Another practical approach when designing input stages for a dc-dc converter is the common practice of adding a large capacitor in parallel. In this case the block diagram will result in Fig. 3.

Compared to the previous schematic, the resistance, R_S , has been removed to simplify the analysis. This is, in general, an advantage because a resistive element in series with the input lead causes power dissipation and penalizes the overall efficiency. The resistance, R_E , is the equivalent series resistance (ESR) of the capacitor, C_E .

The internal capacitor, C_i , has also been removed. As an approximation, it can be considered as being part of C_E . Although this is not completely correct from the model standpoint, it could be enough to show the overall effect on stability. This simplification avoids generating a third-order equation that is more difficult to study.

As before, the overall transfer function of the Fig. 3 is:

$$\frac{V_O}{V_S} = H(s) \frac{Z_P}{Z_P + Z_S} \quad (23)$$

Where:

$$Z_P = \frac{1}{\frac{1}{-|r_i|} + \frac{1}{R_E + \frac{1}{s C_E}}} = \frac{|r_i| (1 + sR_E C_E)}{s C_E (|r_i| - R_E) - 1} \quad (24)$$

Replacing the value of Z_P in the transfer function results in:

(See Eq. 25 below)

Dividing by $|r_i|$, we can rewrite Eq. 25 as:

$$\frac{V_O}{V_S} = \frac{1 + sR_E C_E}{s^2 L_S C_E \left(\frac{|r_i| - R_E}{|r_i|} \right) + s \left(C_E R_E - \frac{L_S}{|r_i|} \right) + 1} H(s) \quad (26)$$

The stability can be studied by solving the roots of the left complex plane characteristic equation:

$$s^2 \frac{L_S C_E \left(\frac{|r_i| - R_E}{|r_i|} \right) + s \left(C_E R_E - \frac{L_S}{|r_i|} \right) + 1 = 0 \quad (27)$$

This is a quadratic equation with solutions:

$$s_1, s_2 = \frac{-b \pm \sqrt{b^2 - 4a}}{2a} \quad (28)$$

Where:

$$a = \frac{L_S C_E \left(\frac{|r_i| - R_E}{|r_i|} \right)}{|r_i|} \quad (29)$$

$$b = \left(C_E R_E - \frac{L_S}{|r_i|} \right) \quad (30)$$

For the roots to be negative, both a and b must be positive, therefore resulting in:

$$\frac{L_S C_E \left(\frac{|r_i| - R_E}{|r_i|} \right)}{|r_i|} > 0 \Rightarrow |r_i| - R_E > 0 \quad \boxed{|r_i| > R_E} \quad (31)$$

and,

$$C_E R_E - \frac{L_S}{|r_i|} > 0 \Rightarrow \frac{L_S}{C_E R_E} < |r_i| \quad (32)$$

Eq. 31 states that R_E should be smaller than $|r_i|$. However, from Eq. 32, it is clear that if R_E is made too small—using high-quality input capacitors for C_E , for example—the system could be under-damped and start to oscillate.

For this reason, ceramic and film input capacitors are not recommended to restore the voltage source. The construction of these parts results in lower ESRs than devices with an electrolytic construction.

From Eq. 32, it is also possible to see that a bigger input inductance requires a larger input capacitance to compensate its effects. Also, for low-voltage systems—such as a 12-V dc-dc converter—with lower input differential resistance, r_i , larger input capacitance is needed to ensure stable operation. Once the value of the input inductor, L_S , and input incremental resistance, r_i , are known, it is possible to replace the numbers in Eq. 31 and 32 to find the optimal combination for C_E with the proper ESR. \odot

REFERENCES

R.D. Middlebrook, "Input filter considerations in design and application of switching regulators", 1976, IEEE.

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Part Number	V _{ds} (V)	ID (A)	RDS(on) (Ω)	VGS (V)	Ciss (pF)	Qg (nC)	PD (W)	Package Type
IXTP08N50D2	500	0.8	4.6	-4.0	312	12.7	60	TO-220
IXTY1R6N50D2	500	1.6	2.3	-4.0	645	23.7	100	TO-252
IXTP1R6N50D2	500	1.6	2.3	-4.0	645	23.7	100	TO-220
IXTA3N50D2	500	3.0	1.5	-4.0	1070	40.0	125	TO-263
IXTP08N100D2	1000	0.8	21	-4.0	325	14.6	60	TO-220
IXTY1R6N100D2	1000	1.6	10	-4.5	645	27.0	100	TO-252
IXTP3N100D2	1000	3.0	5.5	-4.5	1020	37.5	125	TO-220
IXTA6N100D2	1000	6.0	2.2	-4.5	2650	95.0	300	TO-263

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