Circuit manages power-up sequencing

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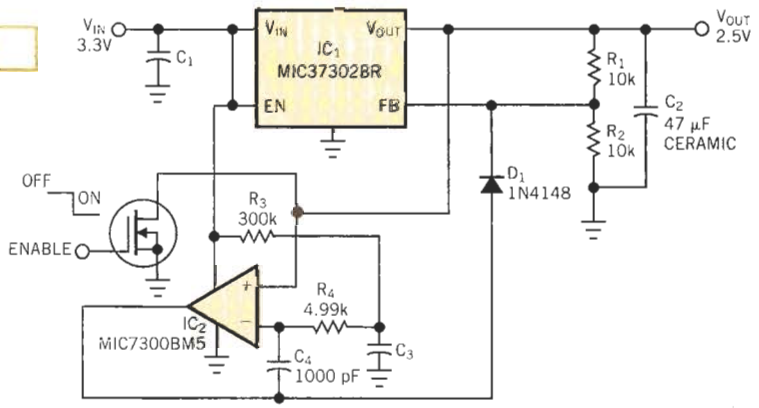
Power sequencing poses a unique problem in power management. Because improper sequencing may cause damage to many types of processors, power-up sequencing of these devices is critical. Devices that may require power-up sequencing control include FPGAs, ASICs, and DSP chips. These devices can require tracking I/O and core voltages. Requirements for power-up sequencing may change according to device type and manufacturer, so it's important that you review sequencing requirements for each device. This design use Xilinx's (www.xilinx.com) power-up requirements for the Spartan-II and Spartan-IIE families. The I/O voltage must reach full supply voltage in 2 to 50 msec. Also, the slew rate of the supply voltage must not exceed 900 mV/msec but must exceed 50 mV/msec. The circuit in **Figure 1** addresses these issues, allowing for consistent and reliable power-up sequencing.

The power-up sequencing circuit uses an RC (R_3 and C_3) timing network to control the slew rate of the output during turn-on. IC_2 compares the output of the low-dropout regulator with the voltage at the RC network. It then adjusts the output of the regulator, via the feedback voltage, to match the RC charge voltage. When the voltage between R_3 and C_3 reaches the low-dropout regulator's regulation voltage, the output of IC_2 pulls low, reverse-biasing D_1, thereby removing the power-up sequencing circuit from the control loop. R_4 and C_4 provide compensation to maintain a smooth voltage during the turn-on cycle. R_1 and R_2 provide the output regulation voltage. You can calculate R_1 and R_2 from the following expression: $R_1 = R_2 (V_{OUT}/1.240 - 1)$. **Figure 2** shows slewing characteristics of the output with various values of C_3.

Figure 1



This circuit controls the power-up sequencing for Xilinx's Spartan ICs.

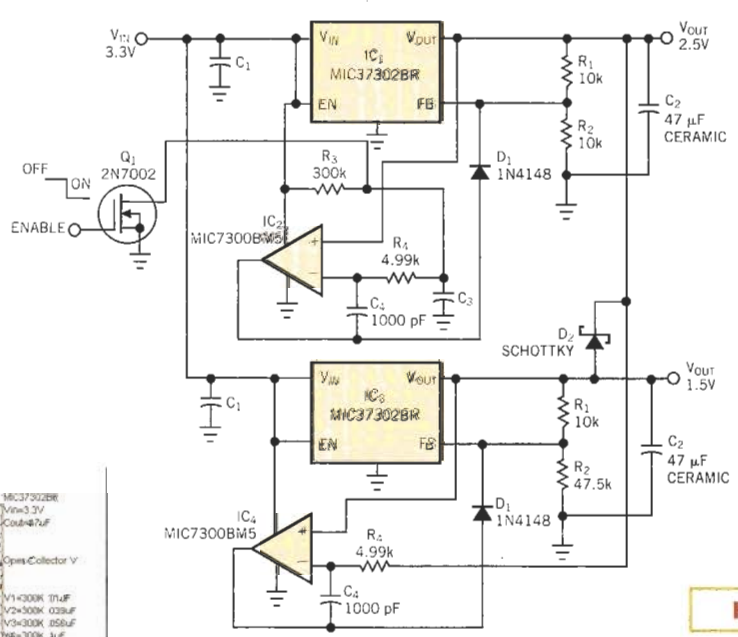


Figure 3

This circuit controls the I/O and core-voltage power-on and power-off sequencing.

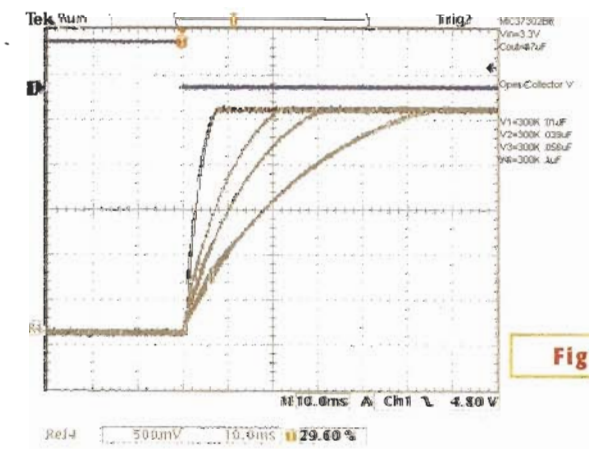


Figure 2

C_3 controls the rise time of the output of Figure 1's circuit.