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Application Note 42043

ML4803 240W Off-Line Power Supply with PFC

INTRODUCTION

Included in this Application Note are a reference schematic, ML4803 design equations, the circuit layout, and parts list. The reference schematic demonstrates how the ML4803 can meet the requirements of a PFC corrected power supply for desktop computer applications. The design features include a low-cost single sided PCB with 240W of output power, a form factor compatible with desk top computer requirements, and line frequency harmonic content compliant with IEC1000-3-2.

THEORY OF OPERATION

The ML4803 Power Factor Control section uses an input current wave-shaping technique that senses the boost inductor current. It compares the inductor current downslope during the off-time of the main power switch with a ramp programmed by the PFC output voltage variation. When the two signals intersect the off-time is terminated and the on-time is initiated for the remainder of the cycle. Any line or load transients to the PFC will cause the output to either surge or dip below its regulated value. This will either increase or decrease the programmed ramp dv/dt, increasing or decreasing the off-time of the main power switch and compensating for load demand. Unity power factor is maintained because the sensed inductor current ramp is proportional to the input voltage.

Electrical Specifications

Line voltage	85 to 265VAC
Line harmonic content	IEC1000-3-2
Switching frequency	67kHz
P_{OUT}	240W
Regulation	±0.1%
Ripple	$30mV_{RMS}$
Efficiency @ 115VAC, 240W	85%

PFC CONTROL CIRCUIT DESIGN

Internal Voltage Ramp

The internal ramp current source is programmed by way of the V_{EAO} signal voltage (see Figure 1). This current source is used to develop the internal ramp by charging the internal 30pF capacitor. Steady-state operation ensures that the V_{EAO} signal is 5V. The frequency of the internal ramp is set to 67kHz.

One-Pin Error Amp

The ML4803 utilizes a one-pin voltage error amplifier in the PFC section (V_{EAO}). The error amplifier is in reality a 35µA current sink, which forces 35µA through the output programming resistor. The nominal voltage of the V_{EAO} signal is 5V and its range is from 4V to 6V. The boost

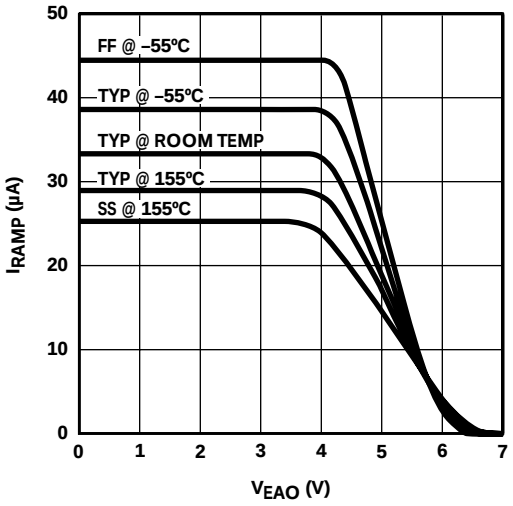

Figure 1. Internal Ramp Current vs. V_{EAO}

PFC CONTROL CIRCUIT DESIGN (Continued)

output voltage would be 400V for a 11.3MΩ resistor to the boost output voltage and 5V steady-state at the V_{EAO} pin.

$$R12 + R13 = \frac{V_{BOOST} - V_{EAO}}{I_{PGM}} = \quad (1)$$

$$\frac{400V - 5V}{35\mu A} = 11.3M\Omega$$

The I_{PGM} variation over temperature and process is 4%. Adding an additional 2% variation in the programming resistor results in a total variation of approximately 6% in the PFC output voltage. This assumes a temperature coefficient of less than 200ppm for the programming resistance. This results in a spread of 377V to 426V in the PFC output voltage, requiring a PFC output capacitor rated at 450V.

Voltage Loop Compensation

The voltage loop bandwidth must be set to less than 120Hz to limit line current harmonic distortion. A typical crossover frequency is 30Hz. Equation 2 assumes that the pole capacitor (C15) in the compensation network dominates the error amp gain at the unity gain frequency. Equation 3 places a pole at the crossover frequency providing 45° of phase margin. Equation 4 places a zero a decade prior to the pole providing the necessary phase boost. Figure 3 displays a simplified schematic of the voltage control loop.

Bode plots illustrating the overall gain and phase are shown in Figures 4 and 5.

$$C15 = \frac{P_{IN}}{R_P \times V_{BOOST} \times \Delta V_{EAO} \times C_{OUT} \times (2\pi f)^2} = \quad (2)$$

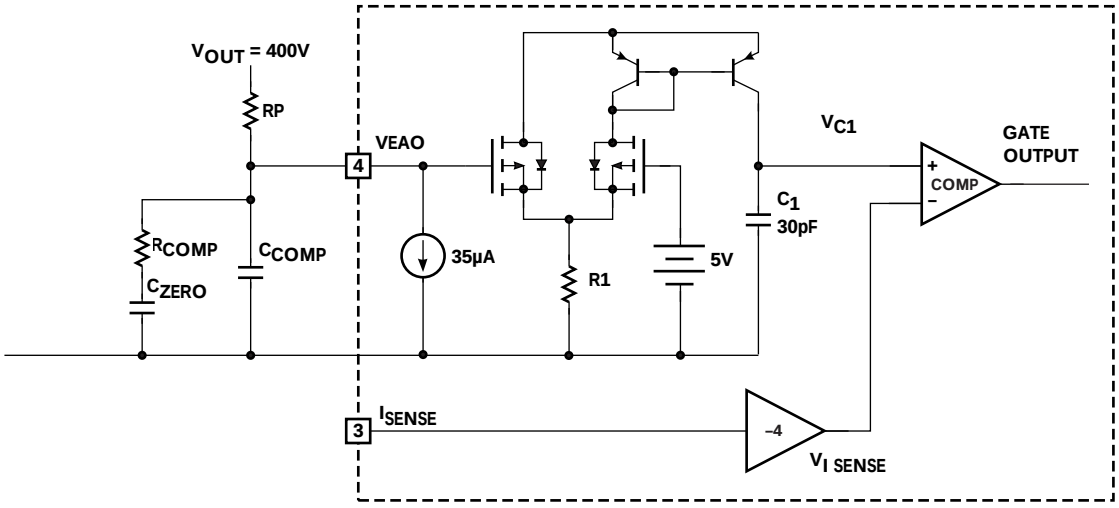

Figure 2. ML4803 PFC Control

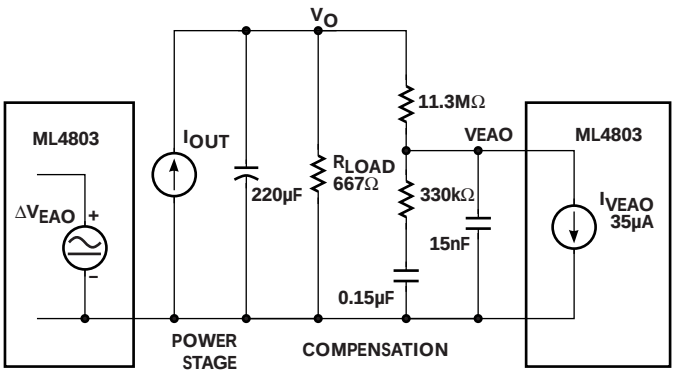

Figure 3. Voltage Control Loop

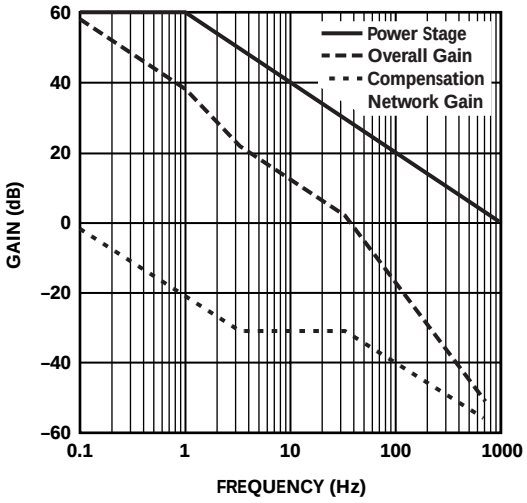

Figure 4. Voltage Loop Gain

PFC CONTROL CIRCUIT DESIGN (Continued)

$$\frac{300W}{11.3M\Omega \times 400V \times 0.5V \times 220\mu F \times (2\pi \times 30Hz)^2} \cong 16nF$$

$$R25 = \frac{1}{2\pi f \times C15} = \quad (3)$$

$$\frac{1}{2\pi \times 30Hz \times 16nF} = 330k\Omega$$

$$C8 = \frac{1}{2\pi \times \frac{f}{10} \times R25} = \quad (4)$$

$$\frac{1}{2\pi \times 3Hz \times 330k\Omega} = 0.16\mu F$$

PFC Start-Up and Soft Start

During steady state operation V_{EAO} draws 35µA. At start-up the internal current mirror, which sinks this current, is defeated until V_{CC} reaches 12V. This forces the PFC error voltage (V_{EAO}) to 12V at the time that the IC is enabled (see Figure 6). With leading edge modulation, 6V or more of V_{EAO} signal forces zero duty in the PFC output. When designing the external compensation components and the V_{CC} supply circuits V_{EAO} must not be prevented from reaching 6V prior to V_{CC} reaching 12V in the turn-on sequence. This will guarantee the PFC stage will enter soft start at turn-on. Once V_{CC} reaches 12V the V_{EAO} current sink is enabled. The V_{EAO} compensation components are then discharged by way of the 35µA current sink until the steady-state operating point is reached.

PFC POWER STAGE DESIGN

PFC Inductor

The boost inductor value should ensure that the ripple current is limited to roughly 20% of the peak input current at low line voltage. This provides for continuous conduction throughout much of the line cycle with sufficient ramp slope to trip the overcurrent comparator at the trailing edge of the "ON" pulse.

$$I_{PK} = \frac{P_{OUT} \times \sqrt{2}}{V_{AC} \times \eta} = \quad (5)$$

$$\frac{240 \times \sqrt{2}}{85V \times 0.75} = 5.3A$$

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} = \quad (6)$$

$$\frac{400 - 85 \times \sqrt{2}}{400} = 0.7$$

$$L = \frac{V_{RMS} \times \sqrt{2} \times D}{0.2 I_{PK} \times f} = \quad (7)$$

$$\frac{85V \times \sqrt{2} \times 0.7}{0.2 \times 5.3A \times 70kHz} = 1134\mu H$$

PFC Output Capacitor

The dominant consideration in selecting the output capacitor is providing sufficient holdup time at the output to sustain output regulation in the event the AC line drops out for one cycle. The voltage to which the boost cap is allowed to drop is limited by the maximum PWM duty cycle and the main transformer turns ratio (see Transformer section, following).

$$C1 = \frac{\frac{2P_{OUT} \times t_{HOLDUP}}{\eta}}{V1^2 - V2^2} = \quad (8)$$

$$\frac{\frac{2 \times 240W \times 15ms}{0.9}}{(380V)^2 - (320V)^2} = 190\mu F$$

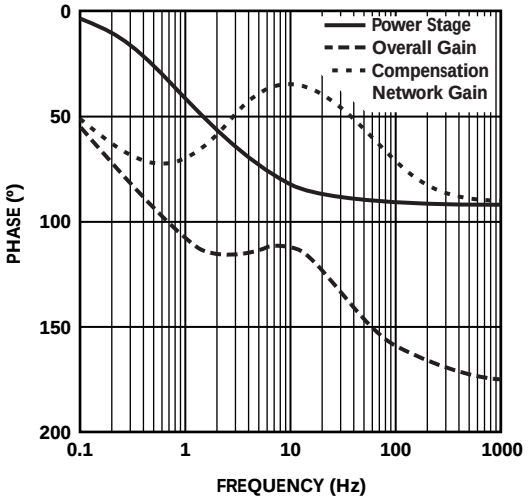

Figure 5. Voltage Loop Phase

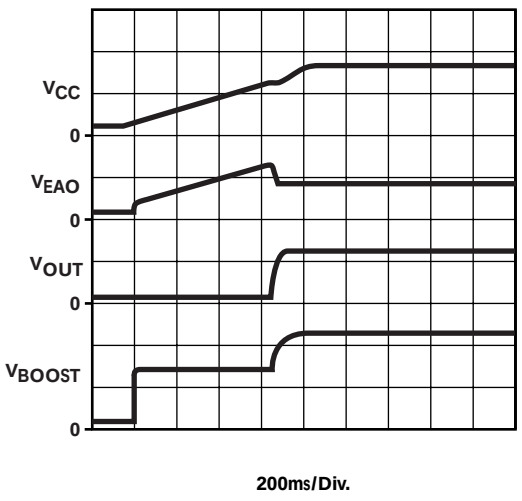

Figure 6. PFC Soft Start

PFC POWER STAGE DESIGN (Continued)

PFC Current Sense Resistor

In Discontinous Conduction Mode (DCM) the input current wave shaping technique used by the ML4803 can cause the input current to run away, forcing the PFC output to increase until the V_{CC}OVP point is reached. In order for the PWM technique to work properly under DCM, the programmed ramp must meet the boost inductor current down slope at zero amps. Assuming the programmed ramp is zero under light load, the off time will be terminated once the inductor current reaches zero. Subsequently, the PFC gate drive would be initiated eliminating any necessary deadtime needed for the DCM mode. The problem is resolved by adding an offset voltage to the current sense signal, which forces the duty cycle to zero at light loads. The offset prevents the PFC from operating in the Discontinous Conduction Mode (DCM) and forces pulse skipping from Continuous Conduction Mode (CCM) to no duty, avoiding the DCM problem altogether. External filtering of the current sense signal helps to smooth out the signal, expanding the operating range somewhat into the DCM range. This should be done carefully as the filtering reduces the bandwidth of the signal feeding the pulse-by-pulse current limit information.

Figure 7 displays the circuit used to provide offset to the I_{SENSE} pin under light load conditions. It adds a negative offset to the I_{SENSE} pin that is inversely proportional to the PFC pulse width, preventing excessive input current under light load conditions. Components C23 and CR16 offset the PFC gate drive by –15V, while the subsequent low-pass network averages the offset square wave. The net effect is a negative voltage summed with the input current sense that increases as the PFC pulse width decreases. Figure 8 illustrates how I_{LIMIT} vs. duty cycle varies with the PFC gate drive offset signal. The 120Hz component of the PFC gate drive is attenuated by more than –50dB at the I_{SENSE} pin. Because this 120Hz component added to the I_{SENSE} input will increase the harmonic distortion in the input AC current, it should kept to a minimum by this low-pass network.

To select the PFC R_{SENSE} value, use a peak current that is 120% of that found in Equation 5.

$$R3 = \frac{V_{LIMIT}}{120\% \times I_{PK}} = \quad (9)$$

$$\frac{1V}{1.2 \times 5.3A} = 0.15\Omega$$

PFC and PWM Gate Drive

The peak current rating of the PFC and PWM gate drive outputs is 1A. A 36Ω gate drive resistor is used to drive two MOSFETs in parallel and limit the gate drive peak current to less than 1A. The charge required to elevate the gate of the IRF840 to 15V is taken from the manufacturer's data sheet in order to estimate the gate drive turn-on time. Estimating the current as a constant allows the approximate time to be derived from Equation 10. Given the switching frequency, the average gate current drawn from V_{CC} can be calculated from Equation 11. Since a typical carbon film resistor is only capable of a peak power of 4 times its average, rated power, a ¼W resistor is limited to 1W peak. With a peak current of 0.416A in a 36Ω resistor, the peak power is 6.23W, well in excess of the 1W limitation. For this reason carbon composition resistors are typically used for gate drive applications.

$$t \approx \frac{Q_{GATE}}{I_{PK}} = \frac{Q_{GATE}}{\frac{V_{CC}}{R_{GATE}}} = \quad (10)$$

$$\frac{60nC}{\frac{15V}{36\Omega}} = \frac{60nC}{0.416A} = 144ns$$

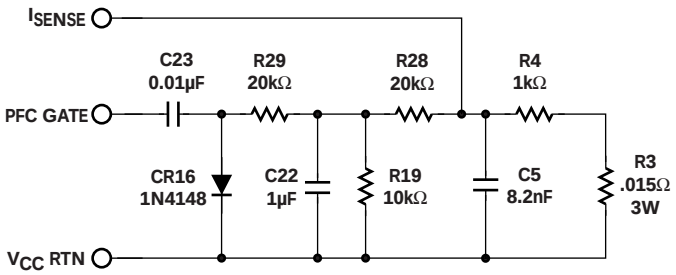

Figure 7. I_{SENSE} Offset Circuit

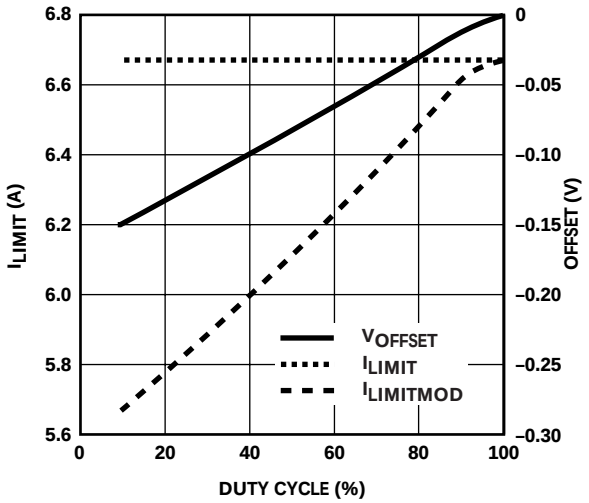

Figure 8. I_{SENSE} and V_{OFFSET} Over Duty Cycle

PFC POWER STAGE DESIGN (Continued)

$$I_{CC_{DRIVE}} = Q_{GATE} \times f_S = \quad (11)$$

$$60nC \times 70kHz = 4.2mA$$

The high-side gate drive transformer magnetizing current can be estimated from Equation 12.

$$I_{AVG} = \frac{V_{CC}}{8 \times f_S \times L_{MAG}} = \quad (12)$$

$$\frac{15V}{8 \times 70kHz \times 450\mu H} = 60mA$$

The total I_{CC} due to gate drive can now be estimated from the sum of all of the above.

PWM POWER STAGE DESIGN

Output Filter

The output inductor value is selected so that the PWM converter can transition into the CCM at roughly 10% of full load and provide sufficient ramp slope for peak current mode operation. With a turns ratio of 0.083 (see Equation 17) and an input voltage of 400V, the steady state duty cycle can be calculated from Equation 13. Given the steady state duty cycle the output filter inductance can be calculated from Equation 14.

$$D = \frac{V_{OUT} + V_D}{V_{BOOST} \times N} = \quad (13)$$

$$\frac{12V + 0.5V}{400V \times 0.083} = 0.376$$

$$L_{OUT} = \frac{(V_{OUT} + V_D) \times (1 - D)}{I_{OUT} \times 20\% \times f_S} = \quad (14)$$

$$\frac{(12V + 0.5V) \times (1 - 0.376)}{20 \times 0.2 \times 70kHZ} = 28\mu H$$

The output capacitor ripple current can be estimated from Equation 15, while the RMS output voltage ripple is calculated from Equation 16.

$$I_{CAP_{RMS}} = \sqrt{\frac{I_{PP}^2}{12}} = \quad (15)$$

$$\sqrt{\frac{(20A \times 0.2)^2}{12}} = 1.15A_{RMS}$$

$$V_{OUT_{RMS}} = I_{CAP_{RMS}} \times ESR = \quad (16)$$

$$1.15A_{RMS} \times 0.03\Omega = 35mV_{RMS}$$

Transformer

The transformer turns-ratio is set by the holdup voltage available at the boost output in the case of a missing cycle in the AC line. With a 50% maximum duty cycle, a holdup voltage of 320V (Equation 8), and a transformer coupling coefficient of 0.9, the transformer turns ratio required is 0.087. The actual transformer used in this example has a turns ratio of 0.083.

$$N = \frac{N_{SEC}}{N_{PRI}} \quad (17)$$

$$N = \frac{V_{OUT} + V_D}{V_{HU} \times D_{MAX} \times k} = \quad (18)$$

$$N = \frac{12V + 0.5V}{320V \times 0.5 \times 0.9} = 0.087$$

The primary magnetizing inductance of the main transformer is selected so that the magnetizing current is roughly equal to the reflected output inductor ripple current.

$$L_{PRI} = \frac{V_{OUT} \times D}{I_{PP} \times N \times f_S} = \quad (19)$$

$$\frac{400V \times 0.376}{(20A \times 0.2) \times 0.083 \times 70kHz} = 6.5mH$$

Current Sense Resistor

The peak current seen at the primary is the sum of the reflected load current and the primary magnetizing current. The trip level for the PWM current limit is 1.65V. The k_{MAG} term in Equation 20 accounts for the magnetizing current in the primary and the ripple current in the secondary. The 1.1 factor sets the current limit at 110% of rated full load.

$$R_{SENSE} = \frac{VI_{LIMIT}}{I_{OUT} \times k_{MAG} \times 110\% xN} = \quad (20)$$

$$\frac{1.65V}{20A \times 1.2 \times 1.1 \times 0.083} = 0.75\Omega$$

V_{CC}OVP and V_{CC}

Full-load to no-load transients at low input voltages can cause excessive overshoot in the PFC output voltage. The V_{CC}OVP is designed to limit the PFC output voltage under a large transient at load off. However, when generating V_{CC} via a winding off the main PWM transformer, the winding will not generate sufficient voltage to trip the V_{CC}OVP during a load off transient. This is due to the fact that the PWM duty approaches zero under the load off transient, thus removing the drive necessary to raise the V_{CC} rail high enough to trip the V_{CC}OVP. By generating the V_{CC} from the boost choke, as shown on the reference schematic, this problem can be eliminated.

In the design example V_{CC} is generated from a winding of the PFC choke. The turns ratio of the auxiliary winding vs. the primary winding is 102:4. V_{CC} should be set as high as possible while guaranteeing the V_{CC}OVP does not trip under normal steady state operating conditions. The output

PWM POWER STAGE DESIGN (Continued)

voltage will range from 377V to 426V, as discussed in the "one-pin error amp" section. Given this variation, the minimum V_{CC}OVP trip level must be guaranteed to occur at a voltage greater than 426V while the maximum OVP trip level must be less than the output capacitor's rated voltage (450V). The spread on the V_{CC}OVP is ±0.5V for a maximum of 16.5V and a minimum of 15.5V. Given the specified PFC choke winding turns ratio, one can calculate the required additional series drop required to limit the minimum OVP trip level to greater than 426V. This additional drop can be achieved by selecting an appropriate value for resistor R31. The maximum V_{CC}OVP trip level can then be checked.

$$N2 = \frac{N_{AUX}}{N_{PRI}} = \frac{4}{102} = 0.039 \quad (21)$$

$$V_{SERIES} = (V_{OUTMIN} \times N2 \times k) - V_{CCOVP_{MIN}} = \quad (22)$$

$$(426V \times 0.039 \times 0.95) - 15.5V = 0.283V$$

$$V_{OUTMAX} = \frac{V_{CCOVP_{MAX}} + V_{SERIES}}{N2 \times k} = \quad (23)$$

$$\frac{16.5V + 0.283V}{0.039 \times 0.95} = 450V$$

In general, the V_{CC}OVP trip level should not interfere with the normal steady-state operation of the PFC, and at the same time should be guaranteed to trip at a level below the maximum rating of the 450V output capacitor.

The maximum voltage at V_{CC} is limited internally by a low current (<10mA) zener clamp ranging from 16.7V to 18.3V. This will limit the V_{CC} voltage applied to the IC during conditions where V_{CC} is applied through the high impedance start up resistors R26 and R27. During normal operation, when the V_{CC} voltage is supplied by way of the boost choke bootstrap winding, V_{CC} will be limited by the V_{CC}OVP protection circuitry (<16.5V). In the case where V_{CC} is supplied by a low impedance source other than a bootstrap winding, the zener minimum voltage (16.7V) must not be exceeded.

RESULTS AND CONCLUSIONS

Table 1 displays the IEC input current harmonic content requirements. A summary of the power supply performance is shown in Table 2. Figures 9 through 14 display input current under various operating conditions, load transients, and turn-on overshoot.

This design shows that the ML4803 provides an effective, inexpensive solution for a power factor corrected 240W switching power supply. Higher power levels can be achieved with proper buffering of the gate drive outputs and detailed attention paid to printed circuit board (PCB) layout. The design has also shown that proper layout can be achieved with a single-sided PCB layout. Applications include desktop PCs, servers, monitors, and distributed power systems.

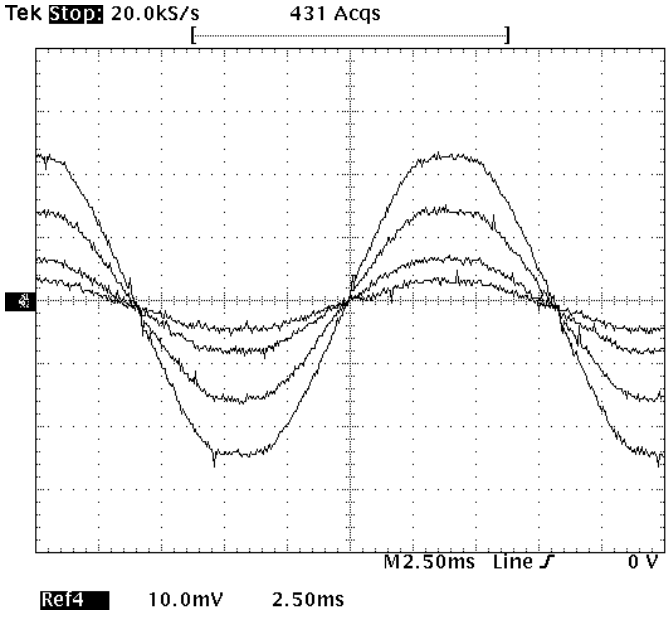

Figure 9. Input AC Current @ 85 V AC. 50W, 100W, 200W, 300W Input Power. 2 A/div.

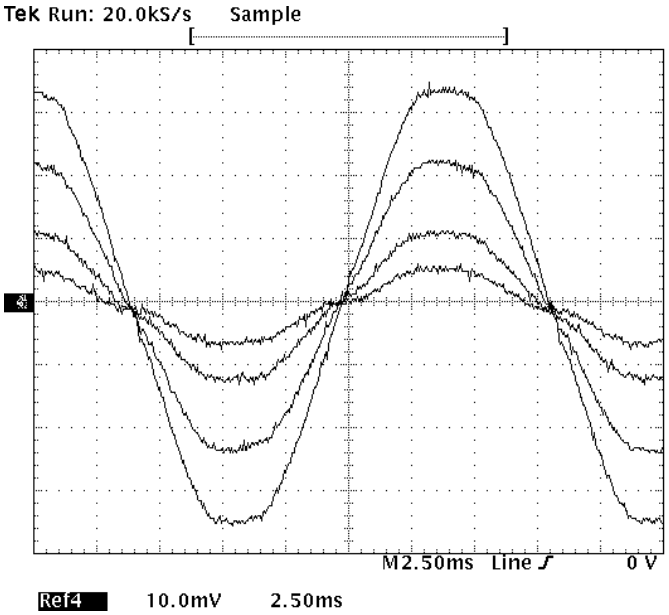

Figure 10. Input AC Current @ 115 V AC. 50W, 100W, 200W, 300W Input Power. 1 A/div.

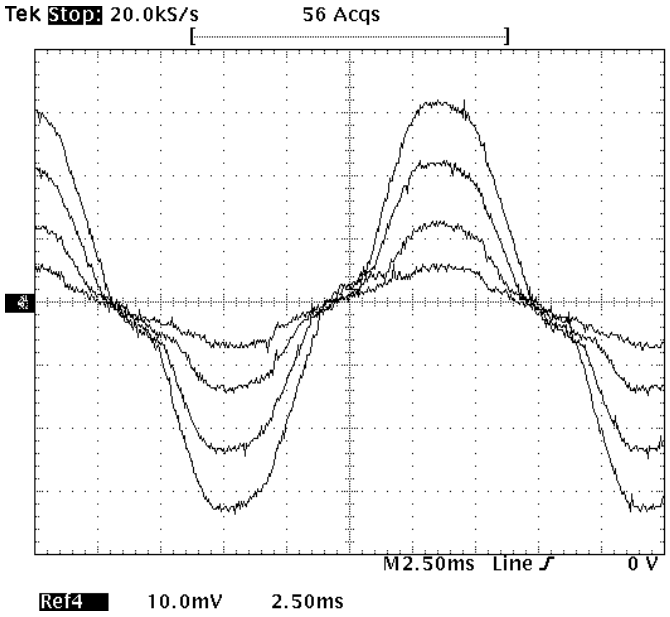

**Figure 11. Input AC Current @ 230 V AC.
50W, 100W, 200W, 300W Input Power.
0.5 A/div.**

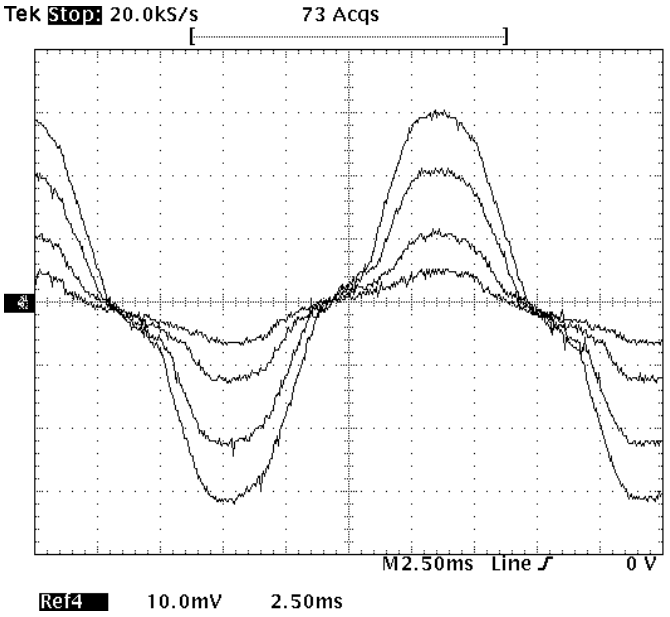

**Figure 12. Input AC Current @ 265 V AC.
50W, 100W, 200W, 300W Input Power.
0.5 A/div.**

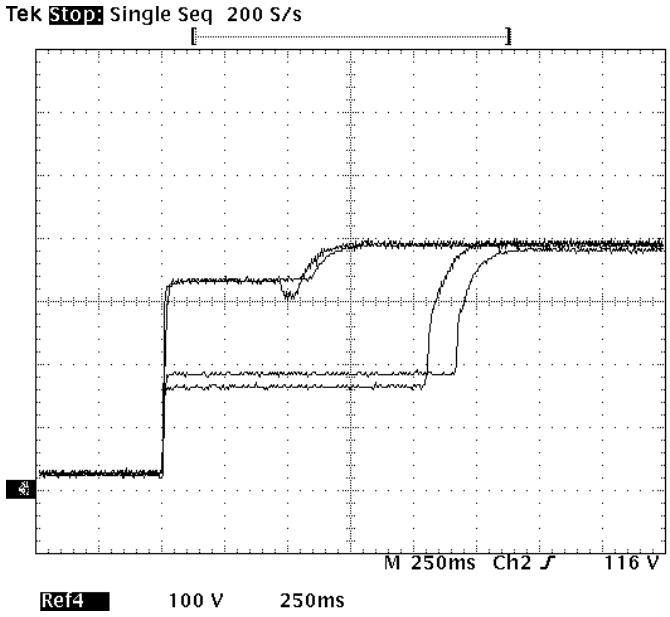

**Figure 13. Boost Output Voltage Turn-On Overshoot @
115 V AC Full Load and No Load
230 V AC Full Load and No Load**

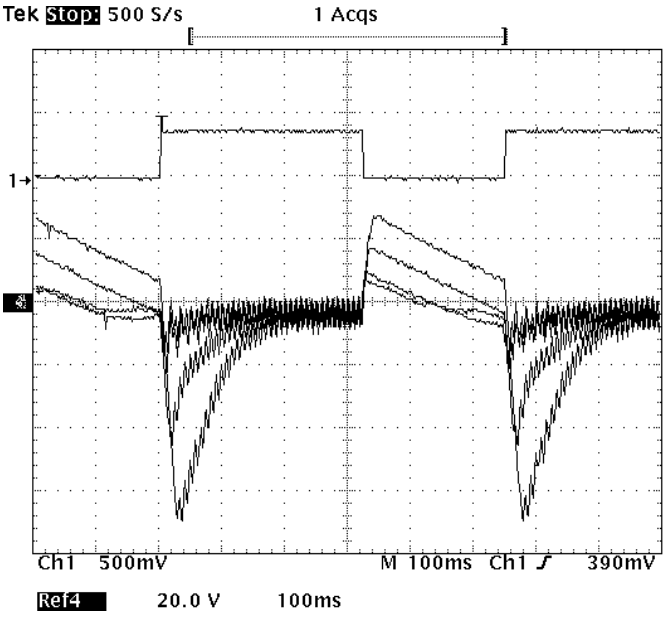

**Figure 14. Boost Output Voltage Load Transient Responce
Top Trace: Load Current Step No Load to 15A
Bottom Traces: Boost Output Voltage Transient Responce
@ 85 V AC, 115 V AC, and 265 V AC Input Voltage**

HARMONIC ORDER	MAXIMUM PERMISSABLE harmonic current per Watt	INPUT POWER				
n	mA/W	50	100	200	300	W
3	3.4	170	340	680	1020	mA
5	1.9	95	190	380	570	mA
7	1	50	100	200	300	mA
9	0.5	25	50	100	150	mA
11	0.35	17.5	35	70	105	mA
13<= n => 39 odd harmonics only	3.85/n	192.5/n	385/n	770/n	1155/n	mA

Table 1 . IEC 1000-3-2
Input Current Harmonic Distortion Limits

HARMONIC DISTORTION SUMMARY

PF	FREQUENCY (Hz)	LINE (V)	POWER (W)	THD (%)	3RD (mA)	5TH (mA)	7TH (mA)	9TH (mA)	11TH (mA)	L_{OUT} (A)	V_{OUT} (V)	EFFICIENCY (%)
0.997	60	85	50.04	5	27	8.6	1.8	2.2	3.3	2.64	12.112	64
0.986	60	120	52.9	13.3	56	19.1	6	3	2.5	2.85	12.112	65
0.966	60	230	47.9	18.8	40.7	11.8	4.3	1.35	3	2.89	12.112	73
0.936	60	265	49.86	22	41.4	10.9	3.2	1.4	2	2.89	12.112	70
0.996	60	120	105	7.2	56	19	11.9	5.3	2.1	6.56	12.116	76
0.973	60	230	101.4	18.8	81	12.9	15.3	1.2	7.8	6.56	12.116	78
0.959	60	265	101	22.9	85.8	9.4	8.2	4.2	2.6	6.56	12.118	79
0.978	60	230	202	17.2	148	36	7.4	4.5	6.27	13.64	12.122	82
0.970	60	265	199.5	20.2	149	18	13.5	13.5	3.8	13.64	12.122	83
0.983	60	230	293	15.5	182	59	25	13.6	3.5	19.81	12.125	82
0.975	60	265	290	18.8	200	46	9	6.9	8.03	19.81	12.125	83

Table 2. ML4803 Performance Summary

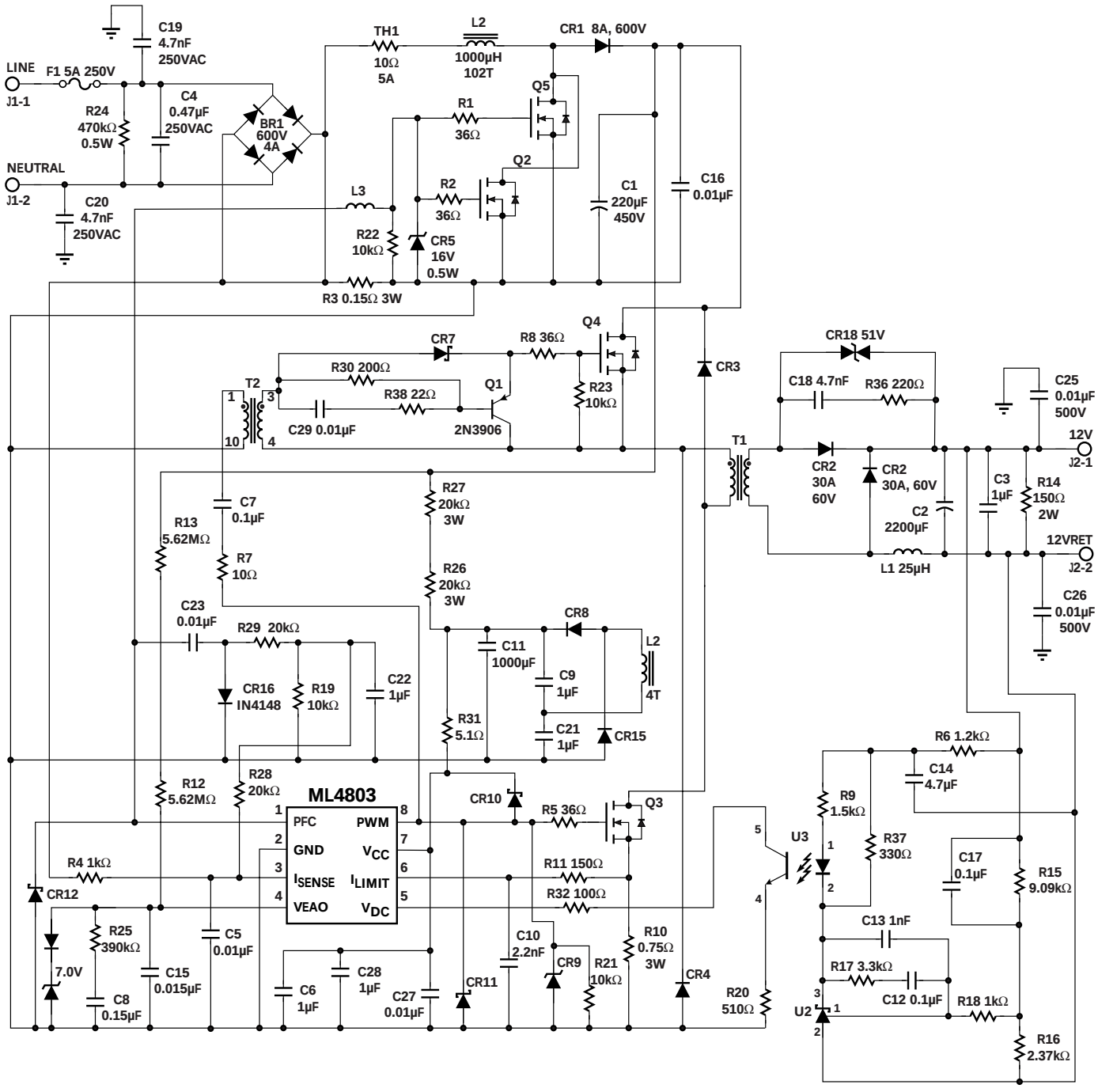

Figure 15. Application Schematic

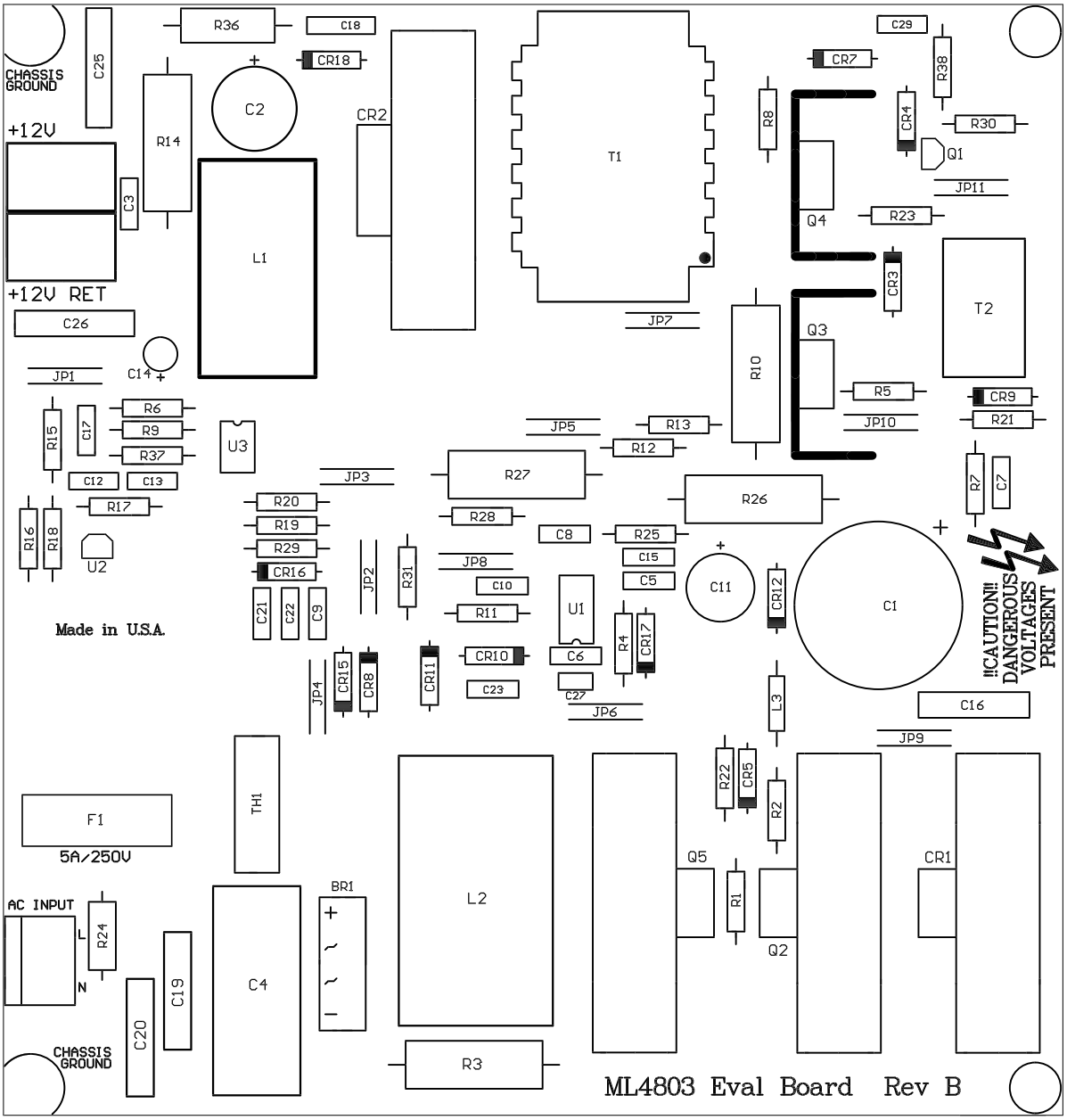

Figure 16. Top Silkscreen

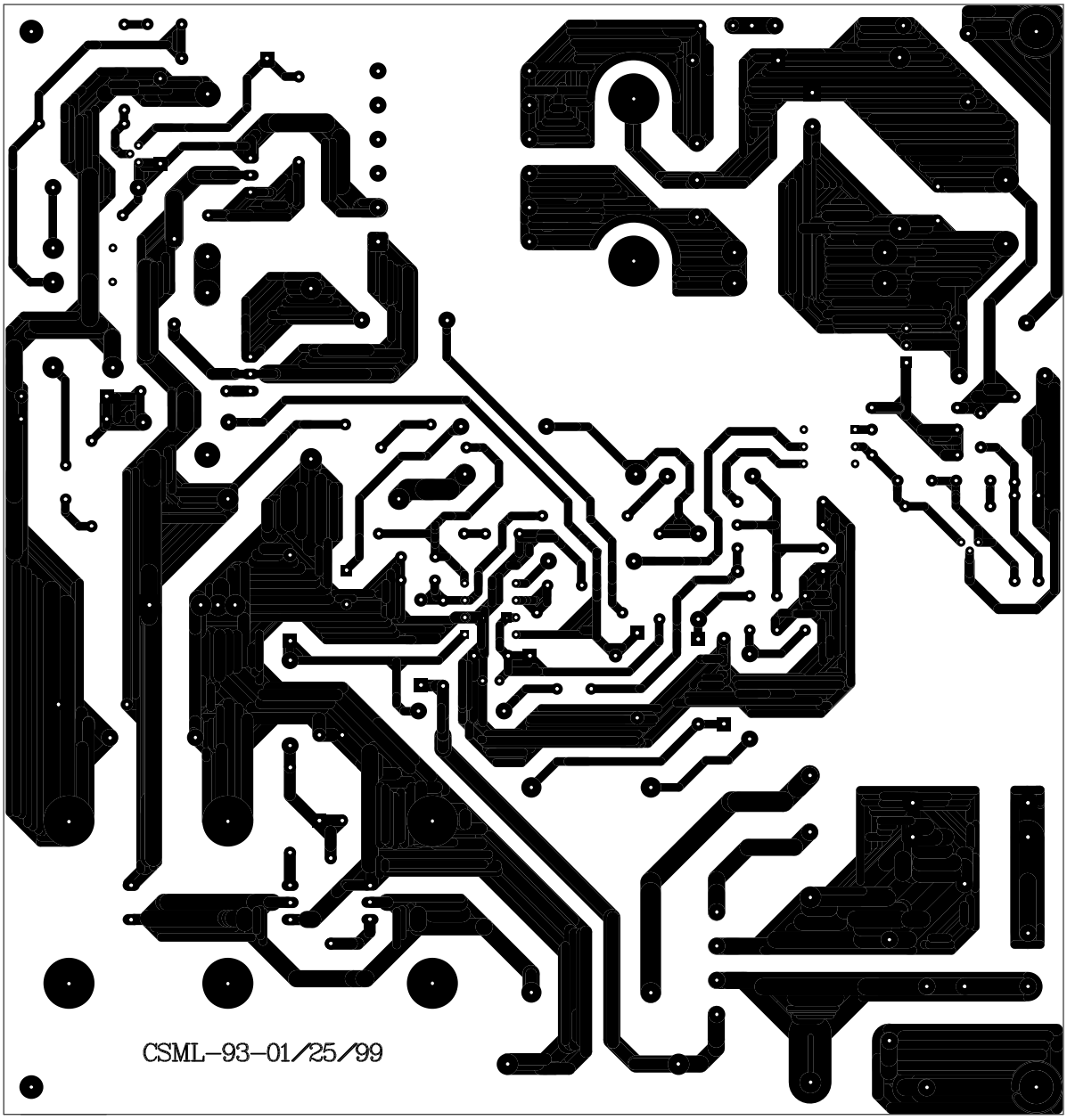

Figure 17. Bottom Plane

PARTS LIST

QUANTITY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER
4	R1, R2, R5, R8	36Ω ¼W 5% Carbon Comp. resistor	Mouser	30BJ250-36
1	R3	0.15Ω 3W 1% Wirewound resistor	Huntington Electric Digi Key	ALSR3F-0.15 ALSR3F-0.15-ND
1	R32	100Ω ¼W 5% Carbon Film	Mouser	29SJ250-100
2	R7	10Ω ¼W 5% Carbon Comp resistor	Mouser	30BJ250-10
1	R6	1.2kΩ ¼W 5% Carbon Film resistor	Mouser	29SJ250-1.2k
1	R9	1.5kΩ ¼W 5% Carbon Film resistor	Mouser	29SJ250-1.5k
1	R10	0.75Ω 3W 1% Wirewound resistor	Huntington Electric Digi Key	ALSR3F-0.75 ALSR3F-0.75-ND
1	R11	150Ω ¼W 5% Carbon Film resistor	Mouser	29SJ250-150
2	R12, R13	5.62MΩ ¼W 1% Metal Film resistor	Dale	CMF-55-5.62MΩ
1	R14	150Ω 2W 5% Metal Oxide Film resistor	Digi Key	150W-2-ND
2	R15	9.09kΩ ¼W 1% Metal Film resistor	Mouser	29MF250-9.09k
1	R16	2.37kΩ ¼W 1% Metal Film resistor	Mouser	29MF250-2.37k
1	R17	3.3kΩ ¼W 5% Carbon Film resistor	Mouser	29SJ250-3.3k
2	R18,R4	1kΩ ¼W 5% Carbon Film resistor	Mouser	29SJ250-1k
1	R30	200Ω ¼W 5% Carbon Film resistor	Mouser	29SJ250-200
1	R20	510Ω ¼W 5% Carbon Film resistor	Mouser	29SJ250-510
4	R19, R21, R22, R23	10kΩ ¼W 5% Carbon Film resistor	Mouser	29SJ250-10k
1	R24	470kΩ ½W 5% Carbon Film resistor	Mouser	29SJ250-470k
1	R25	390kΩ ¼W 5% Carbon Film resistor	Mouser	29SJ250-390k
2	R26, R27	20kΩ 3W 5% Metal Oxide Film resistor	Digi Key	P20kW-3BK-ND
2	R28, R29	20kΩ ¼W 5% Carbon Film resistor	Mouser	30BJ250-20k
1	R31	5.1Ω ¼W 5% Carbon Film resistor	Mouser	30BJ250-5.1
1	R36	220Ω 1W 5% Metal Oxide Film resistor	Digi Key	220W-1-ND
1	R37	330Ω ¼W 5% Carbon Film resistor	Mouser	29SJ250-330
1	R38	22Ω ¼W 5% Carbon Film resistor	Mouser	30BJ250-22
1	C1	220µF 450V 25mm x 50mm TSHB Series capacitor	Panasonic Digi Key	ECO-S2WB221CA P10163-ND
1	C2	2200µF 16V 12.5mm x 30mm capacitor	Panasonic Digi Key	ECA-1CFQ222 P5681-ND
5	C3, C6, C9, C21, C22	1µF 50V 20% Z5U capacitor	Panasonic Digi Key	ECU-S1H105MEB P4968-ND
1	C4	0.47µF 250V capacitor	Panasonic Digi Key	ECQ-E2A474MW P4607-ND
3	C7, C12, C17	0.1µF 50V 20% Z5U capacitor	Panasonic Digi Key	ECU-S1H104MEB P4924-ND
1	C8	0.15µF 100V 10% X7R capacitor	Panasonic Digi Key	ECU-S1H154KBB P4957-ND
1	C10	2.2nF 100V 10% X7R capacitor	Panasonic Digi Key	ECU-S1H222KBB P4900-ND
1	C11	1000µF 25V 20% capacitor	Panasonic Digi Key	ECA-1EM102 P5156-ND
1	C13	1nF 100V 10% X7R capacitor	Panasonic Digi Key	ECU-S1H102KBB P4898-ND
1	C14	4.7µF 25V 10% capacitor	Panasonic Digi Key	ECS-F1EE475K P2047-ND
1	C15	15nF 100V 10% X7R capacitor	Panasonic Digi Key	ECU-S1H153KBB P4952-ND

PARTS LIST (Continued)

QUANTITY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER
1	C16	0.01µF 500V 10% Y5P capacitor	Panasonic Digi Key	ECK-D2H103KB5 P4198A-ND
1	C18	4.7nF 100V 10% X7R capacitor	Panasonic Digi Key	ECU-S1H472KBB P4902-ND
2	C19, C20	4.7nF 250V capacitor	Panasonic Digi Key	ECQ-U2A472MV P4625-ND
2	C25, C26	0.01µF 500V Ceramic disk capacitor	Panasonic Digi Key	ECK-D2H103KB5 P4198A-ND
1	C27	0.01µF 25V Ceramic Disk capacitor	Panasonic Digi Key	ECK-F1E103ZV P4300A-ND
1	C28	1µF 50V Y5V 20% 1206 capacitor	Panasonic Digi Key	ECJ-3YF1E105Z PCC1903CT-ND
3	C5, C23, C29	0.01µF 50V 20% Z5U capacitor	Panasonic Digi Key	ECU-S1H103MEB P4963-ND
1	Q1	PNP transistor	Liteon	2N3906
4	Q2, Q3, Q4, Q5	500V MOSFET	Int'l Rect.	IRF840
1	BR1	600V 4A Diode bridge	Microsemi	RS405L
1	CR1	8A 600V HEXFRED diode	Int'l Rect.	HFA08TB60
1	CR2	TO247 30 Amp 60 Volt Schottky diode	Int'l Rect.	30CPQ060
2	CR3, CR4	1A 600V diode	Liteon	MUR160
2	CR5, CR9	16V 0.5W Zener diode	Microsemi	1N5246BMSCT-ND
4	CR7, CR10, CR11, CR12	1A 30V Schottky Diode	Liteon	1N5818
3	CR8, CR15, CR16	150mA 75V Diode	Liteon	1N4148DITR
1	CR18	51V Bidirectional Transorb	Microsemi	P6KE51CAMSCT
1	U1	PFC/PWM Combo IC	Micro Linear	ML4803CP-1
1	U2	Three-Terminal Zener Regulator IC	Nat. Semi.	LM431A
1	U3	Opto-isolator IC	Motorola	MOC8112
1	L1	Output Choke inductor	Premier Mag.	TSD-1273
1	L2	Boost Choke inductor	Premier Mag.	TSD-1274
1	L3	Ferrite bead	Panasonic Digi Key	EXC-ELSA38 P98188K-ND
1	T1	67kHz 12V Transformer	XFMRS, Inc.	XF4317-00
1	T2	Gate Drive Transformer	P0584	Pulse
1	F1	5A 250VAC 5 x 20mm Fast Blow Fuse	Littlefuse Digi Key	Series 216 F920-ND
2	Ref. F1	5 x 20mm Fuse Clips	Littlefuse	111501
1	TH1	10Ω 5A RMS Thermistor	Keystone Digi Key	KC006L-ND KC006L-ND
1	J2	20A 2-pin Connector	RDI Mouser	NC6-02 506-NC6-P107-02
1	J1	3-pin 0.156 Header	Molex Digi Key	26-60-4030 WM4621-ND
1	J1	3-pin 0.156 Connector	Molex Digi Key	09-50-3031 WM2101-ND
2	Ref. J1	Terminal for 0.156 Housing	Molex Digi Key	08-50-0106 WM2300-ND
4	Ref. CR1, CR2, Q2, Q5	Heatsinks	AAVID Digi Key	530102B00150 HS152-ND