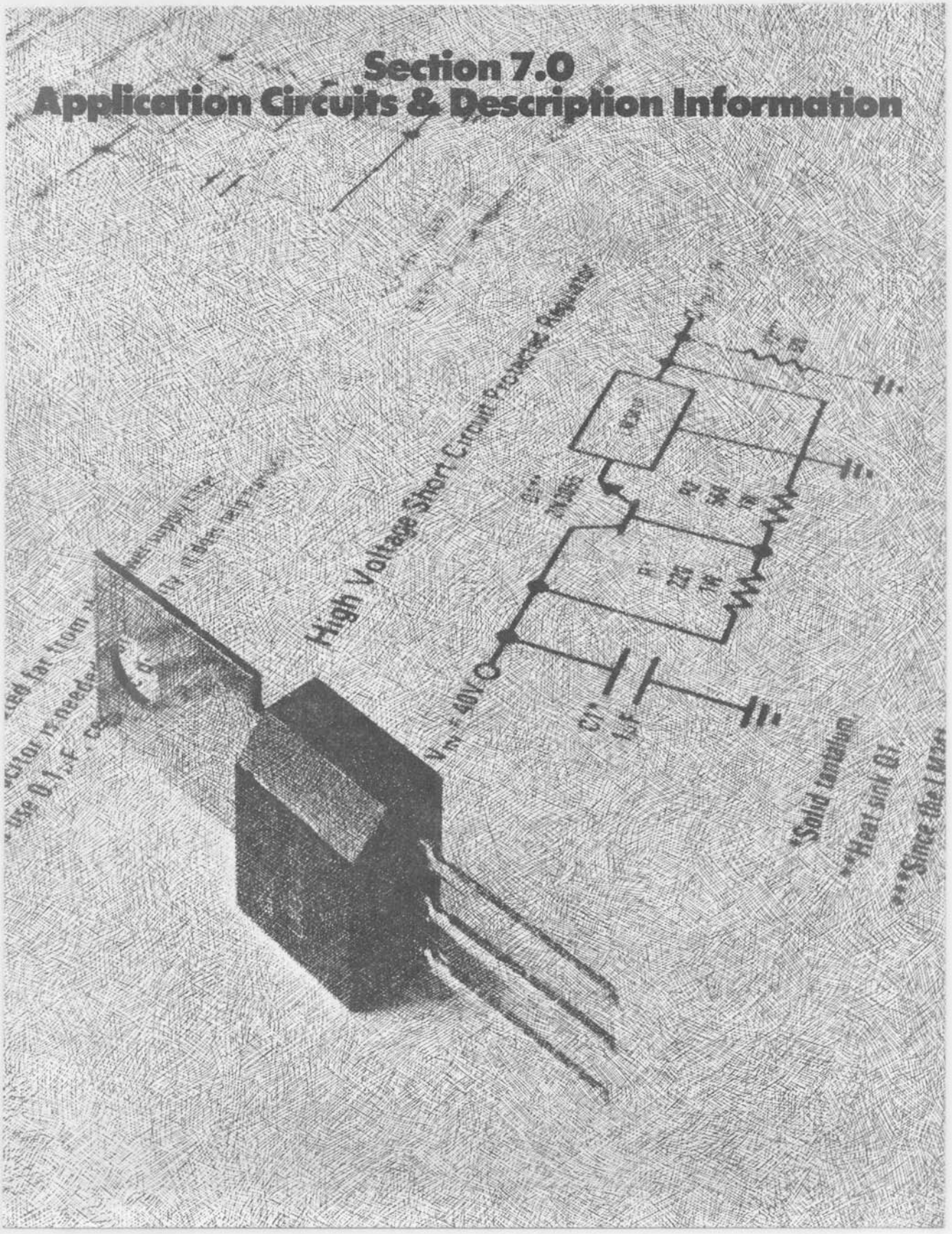
Section 7.0
Application Circuits & Description Information



7.0 APPLICATIONS

Voltage regulator use can be expanded beyond that of the simple three-terminal fixed voltage regulator. Some of the circuits which are practical and useful are described in this section. Pertinent equations are included rather than providing fixed component values as the circuits are equally applicable to all regulators within a family.

7.1 POSITIVE REGULATORS

7.1.1 Basic Regulator

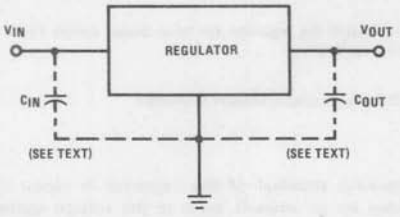


FIGURE 7.1. Basic Regulator Connection

Normal connections are indicated in Figure 7.1. If the regulator is located more than two inches from the supply filter capacitor, a supply bypass capacitor is required to maintain stability (much as is the case with op-amps). This should be an 0.22 μF or larger disc ceramic, 2 μF or larger solid tantalum, or 25 μF or larger aluminum electrolytic capacitor (the LM120 and LM123 series require the solid tantalum or aluminum electrolytics). Progressively larger values are required of ceramic, solid tantalum and aluminum electrolytic capacitors because the effective series resistance ESR increases respectively in each type capacitor. The LM120 series alone of all the group requires an output capacitor to insure stable operation. The others are stable when operating into a resistive load. The LM120 output capacitor should be a 1 μF or larger solid tantalum or 25 μF or larger aluminum electrolytic. Transient response of all the regulators is improved when output capacitors are added. To minimize high-frequency noise, an 0.01 μF output capacitor is recommended on the LM78LXX and LM140L series.

7.1.2 Current Source

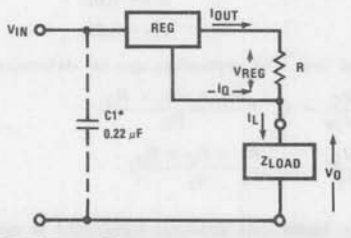


FIGURE 7.2. Current Source

A constant output current I_L is delivered to a variable load impedance Z_L.

$$I_L = \frac{V_{REG}}{R} + I_Q \qquad (7.1)$$

$$\text{for } 0 \leqslant Z_L \leqslant \frac{V_{IN} - (V_{REG} + V_{dropout})}{I_L}$$

The output impedance is:

$$Z_O = \frac{\Delta V_O}{\Delta I_L} = \frac{1}{\frac{\Delta I_Q}{\Delta V_{IN}} + \frac{L'_r}{R}} \qquad (7.2)$$

where: $\frac{\Delta I_Q}{\Delta V_{IN}}$ = quiescent current change per volt of input voltage change of the regulator

$L'_r = \frac{\Delta V_O}{\Delta V_{IN}}$ = line regulation, the change in regulator output per volt of input voltage change at a given I_O

7.1.3 High Current Regulator

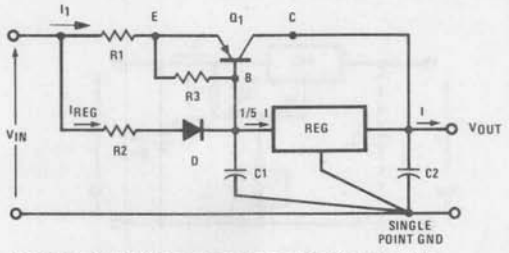


FIGURE 7.3. High Current Regulator with Short Circuit Limit During Output Shorts

This current boost circuit takes advantage of the internal current limiting characteristics of the regulator to provide short-circuit current protection for the booster as well. The regulator and Q_1 share load current in the ratio set between R_2 and R_1 if $V_D = V_{BE(Q1)}$.

$$I_1 = \frac{R_2}{R_1} I_{REG} \qquad (7.3)$$

During output shorts

$$I_{1(SC)} = \frac{R_2}{R_1} I_{REG(SC)} \qquad (7.4)$$

If the regulator and Q_1 have the same thermal resistance θ_{JC} and the pass transistor heat sink has R_2/R_1 times the capacity of the regulator heat sink, the thermal protection (shutdown) of the regulator will also be extended to Q_1. Some suggested transistors are listed below.

Q_1	D	I_1	I_{REG}	R_2/R_1	R_3
2N4398	IN4719	$\geqslant$3 A	1 A	$\geqslant$3	5 - 10 Ω
NSD32	IN4719	2 A	1 A	2	5 - 10 Ω
NSDU51A	IN4003	1 A	0.5 A	2	5 - 10 Ω

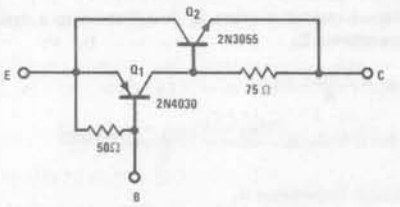


FIGURE 7.4. Equivalent of Power PNP Transistor

The minimum input-to-output voltage differential of the regulator circuit is increased by a diode drop plus the V_{R1} drop. For high current applications a low priced PNP/NPN combination may be used to replace the expensive single PNP 2N4398 as illustrated in Figure 7.4.

7.1.4 Adjustable Output Voltage

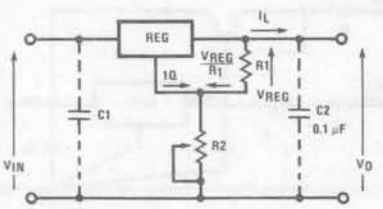


FIGURE 7.5. Adjustable V_{OUT}

A fraction of the regulator current V_{REG}/R_1 is used to raise the ground pin of the regulator and provide, through voltage drop across R_2, an adjustable output voltage.

$$V_O = V_{REG} + R_2(I_Q + \frac{V_{REG}}{R_1}) \tag{7.5}$$

Line regulation is

$$\frac{\Delta V_O}{\Delta V_{IN}} = (L'_r)(\frac{R_1 + R_2}{R_1}) + (\frac{\Delta I_Q}{\Delta V_{IN}})R_2 \tag{7.6}$$

Load regulation is

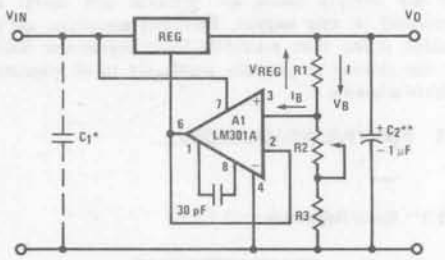
$$\frac{\Delta V_O}{\Delta I_L} = (L_r)(\frac{R_1 + R_2}{R_1}) + (\frac{\Delta I_Q}{\Delta I_O})R_2 \tag{7.7}$$

where: $L_r = \frac{\Delta V_O}{\Delta I_O}$, the regulator load regulation per amp of load change

$\frac{\Delta I_Q}{\Delta I_O}$ = quiescent current change per amp of load current change

$\frac{\Delta I_Q}{\Delta V_{IN}}$ = quiescent current change per volt of input voltage change

7.1.5 Variable Output Voltage



* Required if the regulator far from power supply filter
** Solid tantalum

FIGURE 7.6. Variable Output Regulator

The ground terminal of the regulator is raised above common by an amount equal to the voltage applied at the non-inverting input of the op-amp. For $I >> I_B$, the output voltage is:

$$V_O = (\frac{R_1 + R_2 + R_3}{R_1})V_{REG} \tag{7.8}$$

The minimum output voltage will be determined by the V_{REG} and $V_{B(MIN)}$, where $V_{B(MIN)}$ is the op-amp common-mode voltage lower limit (≈ 2 V for LM301A used with single supply).

$$V_{O(MIN)} = V_{REG} + V_{B(MIN)} \tag{7.9}$$

when $R_2 = 0$, $\frac{R_3}{R_1} = \frac{V_{B(MIN)}}{V_{REG}}$ (7.10a)

$$V_{O(MAX)} = (\frac{R_1 + R_{2(MAX)} + R_3}{R_1})V_{REG} = V_{IN} - V_{dropout} \tag{7.10b}$$

To choose R_1, R_2, R_3 for a specified V_{IN}, start with an arbitrary value for R_1. Determine R_2 and R_3 from Eqn 7.10 and finally check to insure that

$$\frac{V_{O(MIN)}}{R_1 + R_3} >>> I_B, \quad \frac{V_{O(MAX)}}{R_1 + R_2 + R_3} >> I_B$$

Example: V_{IN} = 25 V LM341P-05
V_O = 7-23 V R_1 = 3K
R_2 = 10K
R_3 = 1.2K

The load and line regulation can be determined by:

$$\frac{\Delta V_O}{\Delta V_{IN}} = (L'_r)(\frac{R_1 + R_2 + R_3}{R_1}) \tag{7.11}$$

$$\frac{\Delta V_O}{\Delta I_L} = (L_r)(\frac{R_1 + R_2 + R_3}{R_1}) \tag{7.12}$$

The ΔI_Q factor (see previous paragraph) is neglected because the op-amp output impedance is very low.

7.1.6 Variable Output Voltage with $V_{O(MIN)} \approx 0$

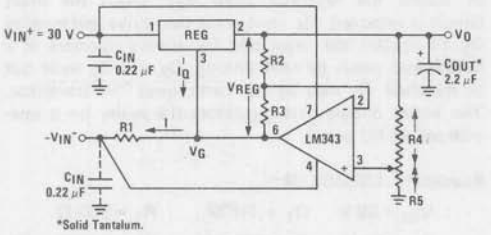


FIGURE 7.7. Variable Output Voltage of 0.5 - 28 V

A wide range of output voltages can be obtained with the circuit of Figure 7.7. A 0- to 20-volt supply can be built using a -7-volt supply and a conventional op-amp. For higher output voltages, a high-voltage op-amp, such as LM143, is required. If

$$R_2 + R_3 = R_4 + R_5 = R, \quad \text{and} \quad R_2/R_3 = 1/10,$$

$$\text{then } V_O = V_{REG}\left(\frac{R_2}{R_4}\right) = V_{REG}\left(\frac{1}{11}\right)\left(\frac{R_4 + R_5}{R_4}\right) \qquad (7.13)$$

Since V_O is inversely proportional to R_4, low output voltages can be very accurately set. The required R_1 is

$$R_1 = \frac{V_{IN}^-}{I_Q}$$

The $V_{O(MAX)}$ is dependent on V_{IN} and $V_{dropout}$, provided that the amplifier can source the current required to raise V_G to $V_O - V_{REG}$.

Example: $V^-_{IN} = -15$ V, $R_1 = 2.1$K
$V^+_{IN} = +30$ V, $R_2 = 910\ \Omega$
$V_O = 0.5$-28 V, $R_3 = 9.1$K
LM340K-05, $R_4 + R_5 = 10$K

7.1.7 High Input Voltage

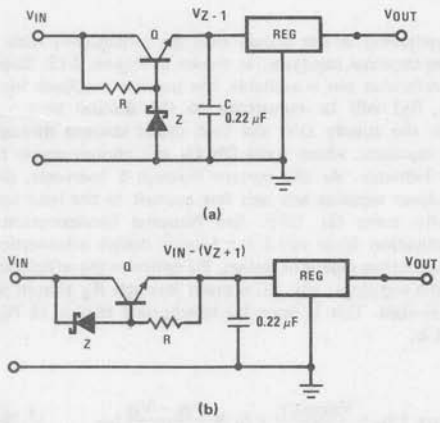


FIGURE 7.8. High Input Voltage

For input voltages higher than $V_{IN(MAX)}$ as specified for the regulator, a transistor/low-power zener combination can be used (instead of an expensive power zener) to reduce the input voltage seen by the regulator. Transistor Q conducts full load current, and therefore requires a power device with adequate heat sink.

Example: In Figure 7.8b

$V_{IN} = 48$ V, LM341P-15
$I_L = 400$ mA, Z = 1N4745 (16 V)

Q would dissipate 7 W, therefore use an NSD31 power transistor. For higher dissipation, use a 2N3055.

7.1.8 High Output Voltage

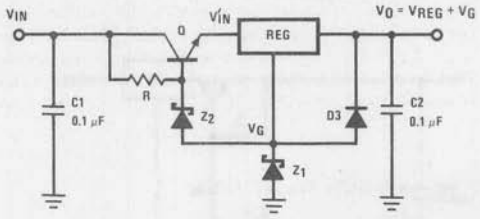


FIGURE 7.9. High-Voltage Regulator

With the circuit of Figure 7.6, one can obtain high output voltages if a high-voltage op-amp is used (LM343). Another approach is to raise the ground terminal with a zener diode as illustrated in Figure 7.9. Transistor Q and Z_2 set $V'_{IN} \approx V_{Z2} + V_{Z1} - 1$ V. D_3 aids full load start-up and also holds V_G to a diode drop above ground during short circuits, thus protecting the regulator from high input-to-output voltage differentials.

Example: LM340T-24, Z_1 = 1N5359 (24 V)
$V_{IN} = 80$ V, Z_2 = 1N5365 (36 V)
$V_O = 48$ V, Q = 2N3055
$R = 600\ \Omega$

Under short-circuit conditions, V'_{IN} reduces to 35 V.

Figure 7.10 illustrates another circuit for a high-voltage regulator with better input voltage limiting under short circuit conditions. In normal operation, Q_2 is OFF and Q_1 conducts full load current. Q_2 saturates when the output is shorted, thus dropping the voltage at Q_1 base and limiting regulator V'_{IN} to a low value. D_1 (1N914) protects Q_2 from base-emitter breakdown. If an output capacitor is used, D_2 protects the regulator from V_{IN}

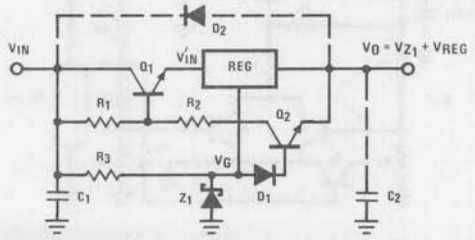


FIGURE 7.10. High-Voltage Regulator

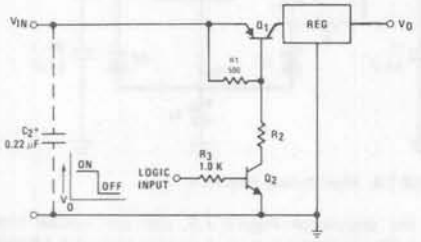
shorts which would temporarily reverse V_{IN} - V_O polarity. A large input capacitor C_1 should be included in the circuit to insure that V_G will rise along with V_{IN} at turn-on. Since Q_1 does not switch OFF under short-circuit load, it must be a power device with heat sink adequate to handle the short circuit dissipation.

Example: LM340T-24

	Z_1 = 1N5359 (24 V)	R_1 = 300 Ω, 10 W
V_{IN} = 60 V	Q_1 = 2N3055	R_2 = 60 Ω, 4 W
V_O = 48 V	Q_2 = 2N3643	R_3 = 1500 Ω, 4 W

Under short circuit conditions V'_{IN} reduces to 9 V.

7.1.9 Electronic Shutdown



* Required if regulator far from power supply filter

FIGURE 7.11. Electronic Shutdown Circuit

Electronic shutdown in three-terminal regulators is done by simply opening the input circuit using a transistor switch. Q_1 operates as the switch which is driven by Q_2. The control voltage V_C can be TTL compatible with the use of R_3 = 1K. R_1 is a biasing resistor, and R_2 can be calculated as

$$R_2 = \frac{V_{IN} - .1\,V}{I_O} \beta_{SAT(Q1)} \qquad (7.14)$$

Figure 7.12 illustrates a short-circuit dependent power shutdown circuit with reduced heat sink requirements under short-circuit conditions.

When the power is first applied, Q_2 turns ON and saturates Q_1. The regulator output ramps up to turn Q_3 ON, which turns Q_2 OFF (V_C should be $> V_A$), thus maintaining Q_1 in the ON state.

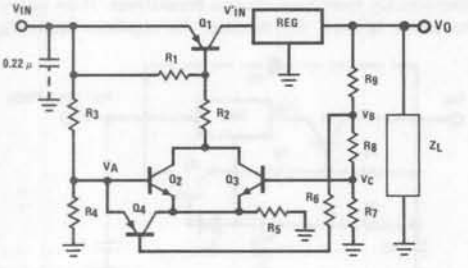


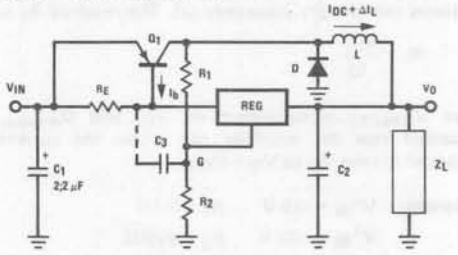
FIGURE 7.12. Output Dependant Electronic Shutdown on High Voltage Regulator

When the output is shorted, Q_3 turns OFF, Q_4 turns ON to clamp Q_2 OFF. Q_1 loses base drive and so opens to isolate the regulator from V_{IN}. When the short circuit is removed, Q_4 loses some base drive and enables Q_2 to re-start the regulator. Q_1 always operates as a switch and needs no heat sinking. Q_2 and Q_3 need not be matched. Q_4 may be any small signal PNP transistor. The entire circuit (less regulator) fits easily on a one-inch square PC board.

Example: LM340K-24

V_{IN} = 36 V	Q_1 = TIP32	R_1 = 500 Ω
V_O = 24 V	Q_2 = 2N4141	R_2 = 250 Ω, 2 W
I_O = 1 A	Q_3 = 2N4141	R_3 = 3300 Ω
V_A = 2.5 V	Q_4 = 2N2906	R_4 = 240 Ω
V_B = 8 V		R_5 = 62 Ω
V_C = 4.8 V		R_6 = 2K
		R_7 = 1K
		R_8 = 680 Ω
		R_9 = 3.3K

7.1.10 Switching Regulator



$$\text{Ripple} \approx V_{IN} \frac{R_2}{R_1 + R_2}$$

FIGURE 7.13. Switching Regulator

A switching power supply may be constructed with a three-terminal regulator, as shown in Figure 7.13. Since no reference pin is available, the positive feedback loop (R_1, R_2) will be connected to the ground terminal. With the supply ON, the load draws current through the regulator, which turns ON Q_1 and applies power to the inductor. As the current through L increases, the regulator supplies less and less current to the load and finally turns Q_1 OFF. See National Semiconductor Application Note AN-2 for further design information on switching regulator design. To optimize the efficiency of the regulator, any DC current through R_E should be minimized. This is done by appropriate choice of R_E, that is:

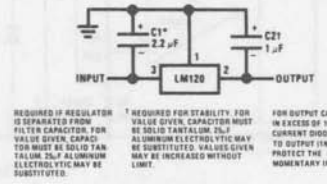
$$I_{RE} + I_b = \frac{V_{BE(SAT)}}{R_E} + I_b \approx \frac{V_{IN} - V_O}{2L} t_{on} \qquad (7.15)$$

Capacitor C_3 improves the waveform at node G to minimize ripple.

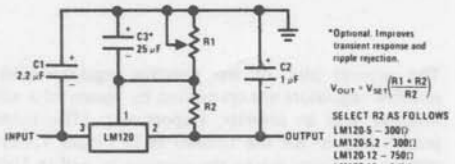
Example: LM341P05 (less heat sink)

$V_O = 5$ V	f = 37 kHz	$R_2 = 1\ \Omega$
$V_{IN} = 10$ V	L = 500 μH	$R_E = 10\ \Omega$
$I_O = 300$ mA	$t_{on} = t_{off}$	$C_2 = 100\ \mu$F
	n = 80%	$C_3 = 0.1\ \mu$F
	Q = 2N2905A	$R_1 = 500\ \Omega$
	D = 1N5807	

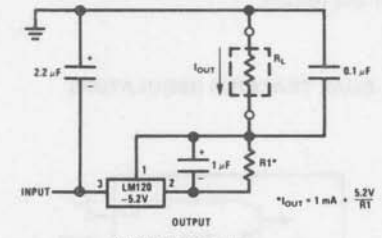
7.2 NEGATIVE REGULATORS



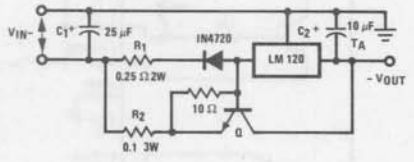
(a) Fixed Regulator



(b) Variable Output



(c) Current Source



(d) High Current Regulator

Q = 2N3055 (for 5 A)
or NSD31 (for less than 2-3 A

FIGURE 7.14. Negative Regulator Circuits

All the applications circuits for positive regulators can be used with the polarities inversed for the negative regulator LM320/345 series (e.g., reverse the sense of the diodes, replace PNP's with NPN's etc., etc.), as shown in Figure 7.14.

7.2.1 Basic Dual Power Supply

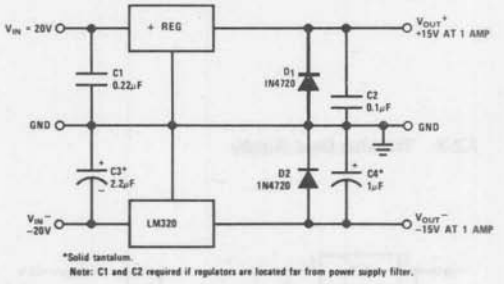


FIGURE 7.15. Dual Power Supply

A positive regulator can be connected with an LM320 to form a non-tracking dual power supply. Each regulator exhibits line and load regulation consistent with their specifications as individual devices. Protective diodes D_1, D_2 allow the regulators to start under common load. They should be rated at the regulator short circuit current.

Examples:

1. ±15 V supply, 1 A common load:
   LM340T-15, LM320T-15, D_1, D_2: IN4720.
2. ±12 V supply, 1 A common load:
   LM340T-12, LM320T-12, D_1, D_2: IN4720.
3. ±15 V supply, 200 mA common load:
   LM342H-15, LM320H-15, D_1, D_2: IN4001.

7.2.2 Trimmed Dual Supply

Figure 7.15 may be modified to obtain a dual supply trimmed to a closer output tolerance. The trimming potentiometers are connected across the outputs so positive or negative trimming currents are available to set the voltage across the $R_1(R_2)$ resistors. R_3, R_5 are included to linearize the adjustment and to prevent shorting the regulator ground pin to opposite polarity output voltages.

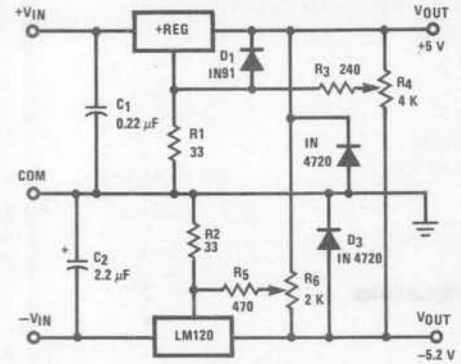
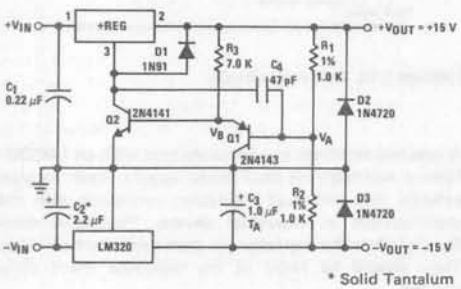


FIGURE 7.16. Trimmed Dual Supply

7.2.3 Tracking Dual Supply



* Solid Tantalum

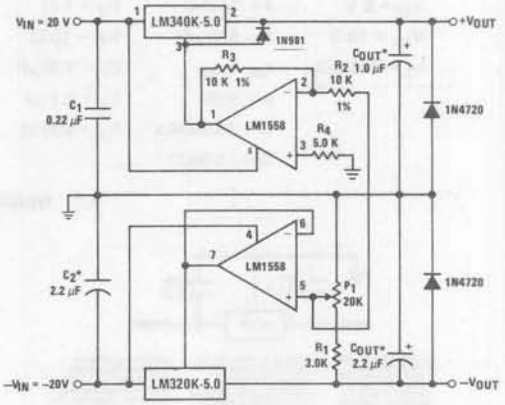
FIGURE 7.17. Tracking Dual Supply

A tracking dual supply can be built as in Figure 7.17 where the positive regulator tracks the negative regulator. V_A is a virtual ground under steady state conditions. Q_2 conducts the quiescent current of the positive regulator.

If $-V_{OUT}$ falls, V_A follows forward biasing collector-base junction of Q_1. V_B falls, thus raising the collector voltage of Q_2 and $+V_{OUT}$ to restore V_A to desired voltage. Germanium diode D_1 may be needed to start the positive regulator with a high differential load.

Example: ±15 V, 1 A tracking dual supply:
LM340T-05, LM320T-15.
The 340 will track the LM320 within 100 mV. D_2, D_3: IN4720.

7.2.4 Variable Tracking Dual Supply ±5.0 to ±18 V @ 1 A

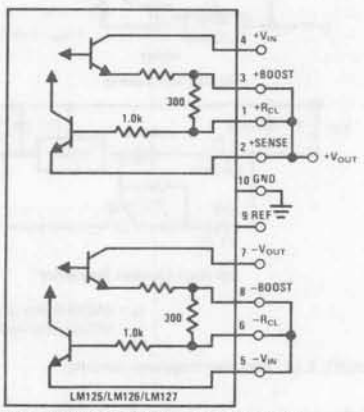


* Solid Tantalum

FIGURE 7.18. Variable Tracking Dual Supply ±5.0 V - ±18 V

The ground pins of the negative regulator and the positive regulators are controlled by means of a voltage follower and an inverter, respectively. (The same approach is used for the LM340 as in Figure 7.18.) The positive regulator tracks the negative to within 100 mV over the entire output range if R_2 is matched to R_3 within one percent.

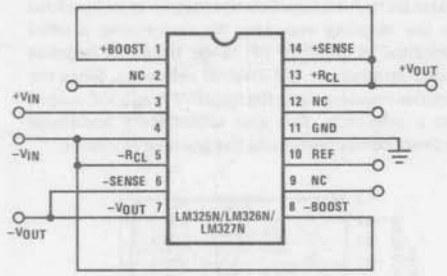
7.3 DUAL TRACKING REGULATORS



NOTE: PIN NUMBERS FOR METAL CAN PACKAGE ONLY.

(a)

FIGURE 7.19 (a). Basic Dual Regulator



(b)

FIGURE 7.19b. Basic Dual Regulator for the 14-Pin Package*

7.3.1 High Current Regulator

The basic dual regulator is shown connected in Figure 7.19. The only connections required other than plus and minus inputs, outputs, and ground are the completion of the output current paths from $+R_{CL}$ to $+V_{OUT}$ and from $-R_{CL}$ to $-V_{IN}$. These may be direct shorts if the internal preset current limit is desired, or resistors may be used to set the maximum current at some level less than the internal current limit. The internal 300 Ω resistors from pins 3 to 1 and pins 8 to 6 should be shorted as shown when no external pass transistors are used. To improve line ripple rejection and transient response, filter capacitors may be added to the inputs, outputs, or both, depending on the unregulated input available. If a very low noise output voltage is desired, a capacitor may be connected from the reference voltage pin to ground, thus shunting noise generated by the reference zener. Figure 7.20 shows the internal current-limiting characteristics for the basic regulator circuit of Figure 7.19.

7.3.1 High Current Regulator

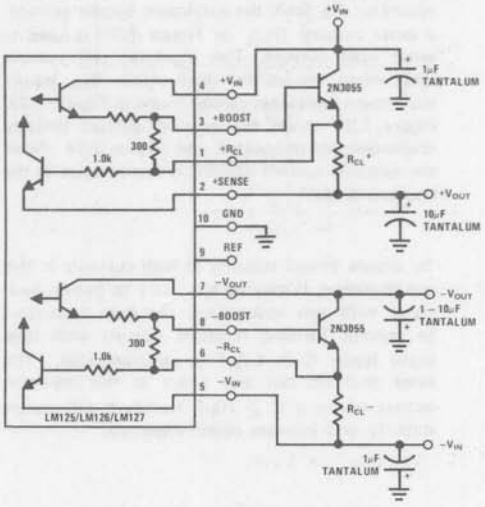
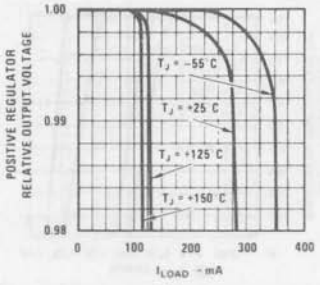


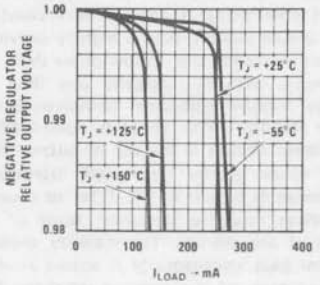
FIGURE 7.21. Boosted High Current Regulator

For applications requiring more output current than can be delivered by the basic regulator, an external NPN pass transistor may be added to each regulator. This will increase the maximum output current by a factor of the external transistor beta. The circuit for current boosted operation is shown in Figure 7.21.

***Note:** In the 14-pin package (N and S packages) the -SENSE pin (pin 6) has been brought out of the chip, and therefore should be connected to the $-V_O$ pin (pin 7). The remaining applications circuits are shown for the TO-5 package. These circuits also apply for the 14-pin N package, provided that the $-V_O$ pin is connected to the -SENSE pin (normally done at the load to eliminate effects of supply line voltage drop).



(A)



(B)

FIGURE 7.20. Internal Current Limiting Characteristics

In the boosted mode, current limiting is often a necessary requirement to insure that the external pass device is not overheated or destroyed. Experience shows this to be the usual cause of IC regulator failure. If the regulator output is grounded the pass device may fail and short, destroying the regulator. To limit the maximum output current, a series resistor (R_{CL} in Figure 7.21) is used to sense load current. The regulator will current limit when the voltage drop across R_{CL} equals the current limit sense voltage found in Figure 7.22. Figure 7.23 shows the external current limiting characteristics unboosted and Figure 7.24 shows the external current limiting characteristics in the boosted mode.

To ensure circuit stability at high currents in this configuration, it may be necessary to bypass each input with low inductance, tantalum capacitors to prevent forming resonant circuits with long input leads; $C \geqslant 1.0\mu F$ is recommended. The same problem can also occur at the regulator output where a $C \geq 10\mu F$ tantalum will ensure stability and increase ripple rejection.

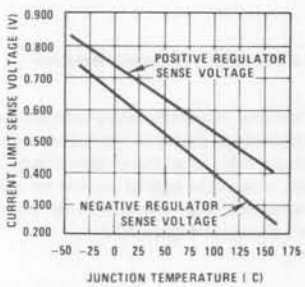


FIGURE 7.22. Current Limit Sense Voltage for a 0.1% Change in Regulated Output Voltage

The 2N3055 pass device is low in cost and maintains a reasonably high beta at collector currents up to several amps. The devices 2N3055 may be of either planar or alloy junction construction. The planar devices, have a high f_T providing more stable operation due to low phase shift. The alloy devices, with f_T typically less than 1.0 MHz, may require additional compensation to guarantee stability. The simplest compensation for the slower devices is the use of output filter capacitor values greater than 50μF (tantalum). An alternative is to use an RC filter to create a leading phase response to cancel some of the phase lag of the devices. The stability problem with slower pass transistors, if it occurs at all, is usually seen only on the negative regulator. This is because the positive regulator output stage is a conventional Darlington while the negative output stage contains three devices in a modified triple Darlington connection giving slightly more internal phase shift. Additional compensation may be added to the negative regulator by connecting a small capacitor in the 100 pF range from the negative boost terminal to the internal reference. Since the positive regulator uses the negative regulator output for a reference, this also offers some additional indirect compensation to the positive regulator.

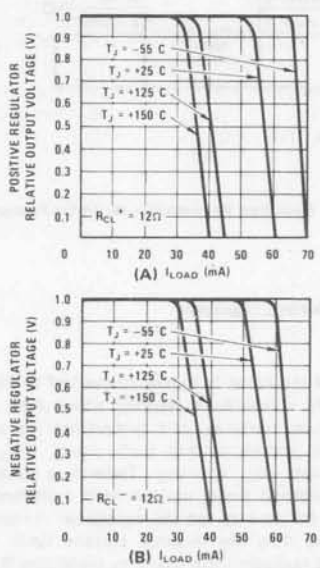


FIGURE 7.23. External Current Limiting Characteristic-Unboosted

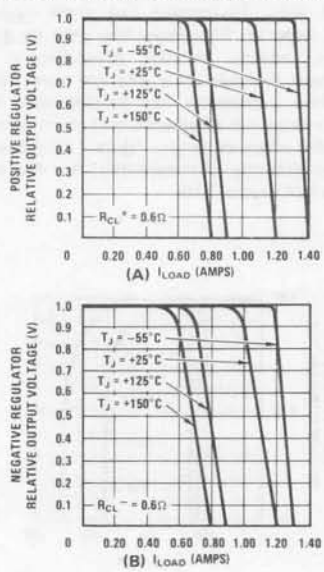


FIGURE 7.24. External Current Limiting Characteristics-Boosted

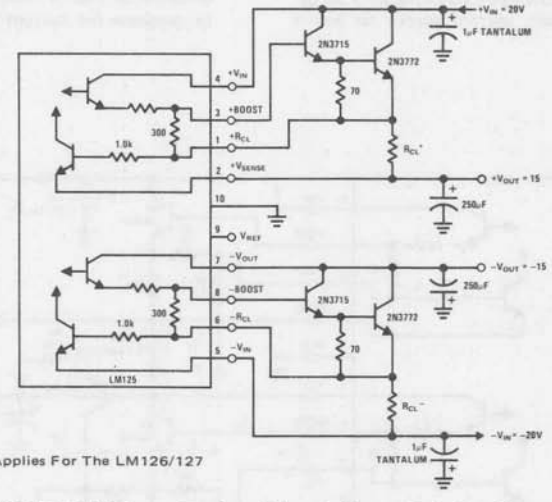
7.3.2 7-Amp Regulator

In Figure 7.25 the single external pass transistor has been replaced by a conventional Darlington using a 2N3715 and a 2N3772. With this configuration the output current can reach values to 10A with very good stability. The external Darlington stage increases the minimum input-output voltage differential to 4.5V. When current limit protection resistor is used, as in Figure 7.25, the maximum output current is limited by power dissipation of the 2N3772 (150W at 25°C). During normal operation this is $(V_{IN}-V_{OUT})\ I_{OUT}$ (W), but it increases to $V_{IN}\ I_{SC}$ (W) under short circuit conditions. The short circuit output current is then:

$$I_{SC} = \frac{P_{MAX}\ (T_C = 25°C)}{V_{IN}}$$

$$= \frac{150W}{20V\ (min)} = 7.5A\ max.$$

I_L could be increased to 10A or more only if $I_{SC} < I_L$. A foldback current limit circuit will accomplish this. The typical load regulation is 40 mV from no load to a full load. (T_j = 25°C, pulsed load with 20 ms t_{ON} and 250 ms t_{OFF}.)



Note: The Same Circuit Applies For The LM126/127

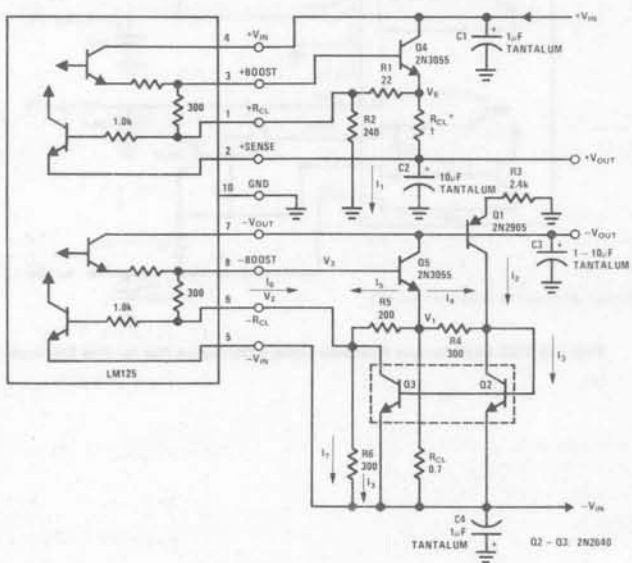
FIGURE 7.25. High Current Regulator Using a Darlington Pair for Pass Elements

7.3.3 Foldback Current Limiting

In many regulator applications, the normal operation power dissipation in the pass device can easily be multiplied by a factor of ten or more when the output is shorted. This may destroy the pass device, and possibly the regulator, unless the heat sink is oversized to handle this fault condition. A foldback current limiting circuit reduces short circuit output current to a fraction of the full load output current thus avoiding the need for larger heat sink. Figure 7.26 shows a foldback current limiting circuit on both positive and negative regulators.

The foldback current limiting, a fraction of the output voltage must be used to oppose the voltage across the current limit sense resistor. Current limiting does not occur until the voltage across the sense resistor is higher than this opposing voltage by the amount shown in Figure 7.22. When the output is grounded, the opposing voltage is no longer present so current limiting occurs at a lower level. This is accomplished in Figure 7.26 by using a programmable current source to give a constant voltage drop across R5 for the negative regulator, and by a simple resistor divider for the positive regulator. The reason for the difference between the two is that the negative regulator current limiting circuit is located between the output pass transistor and the unregulated input while the positive regulator current limiter is between the output pass transistor and the regulated output.

The operation of the positive foldback circuit is similar to that described in NSC application note AN-23. A voltage divider R1 and R2 from V_E to ground creates a fixed voltage drop across R1 opposite in polarity to the drop across R_{CL}^+. When the load current increases to the point where the drop across R_{CL}^+ is equal to the drop across R1 plus the current limit sense voltage given in Figure 7.22, the positive regulator will begin to current limit. As the positive output begins to drop, the voltage across R1 will also decrease so that it now requires less load current to produce the current limit sense voltage. With



Note: For LM126 (127); $V_{IN}^+ = 25\ (20)V$, $V_{IN}^- = 25V$
$R_1 = 20\ (22)$, $R_2 = 180\ (80)$
$R_{CL}^+ = 0.9$
$R_3 = 1.35$ K, $R_6 = 290$; $R_{CL}^- = 0.9$
$I_{FB} = \pm 2A$, $I_{SC} = \pm 0.75A$

FIGURE 7.26. Foldback Current Limiting Circuit

the regulator output fully shorted to ground ($+V_{OUT} = 0$) the current limit will be set by the value of $+R_{CL}$ alone.

If $\frac{I_{FB}}{I_{SC}} \leq 5$

then the following equations can be used for calculating the positive regulator foldback current limiting resistors.

$$R_{CL}{}^{+} \approx \frac{V_{SENSE}}{I_{SC}} \qquad (7.16)$$

where V_{SENSE} is from Figure 7.22.

At the maximum load current foldback point:

$$V_{RCL}{}^{+} = I_{FB}\, R_{CL}{}^{+} \qquad (7.17)$$

$$V_{R1} = V_{RCL}{}^{+} - V_{SENSE} \qquad (7.18)$$

$$V_{R1} = I_{FB}\, R_{CL}{}^{+} - V_{SENSE} \qquad (7.19)$$

Then

$$R1 = \frac{V_{R1}}{I_1} \qquad (7.20)$$

and

$$R2 = \frac{+V_{OUT} + V_{SENSE}}{I_1} \qquad (7.21)$$

The only point of caution is to ensure that the total current (I_1) through R2 is much greater than the current contribution from the internal 300Ω resistor. This can be checked by:

$$\frac{I_{FB}\, R_{CL}{}^{+}}{300} \ll I_1 \qquad (7.22)$$

Note: The current from the internal 300Ω resistor is $V_{3\text{-}1}/300\Omega$, but $V_{3\text{-}1} = V_{BE} + V_{RCL} - V_{SENSE}{}^{+}$ assuming $V_{BE} \approx V_{SENSE}{}^{+}$ at the foldback point, $V_{3\text{-}1} \approx V_{RCL}{}^{+} = I_{FB}\, R_{CL}{}^{+}$.

Example:

Design a 2 amp regulator using LM125 and positive foldback current limiting (see Figure 7.26).

Given:

$I_{FOLDBACK} = 2.0A$

$I_{SHORT\text{-}CIRCUIT} = 500$ mA

V_{SENSE} (see Figure 7.22).

$+V_{IN} = 25V$

$+V_{OUT} = 15V$

$\beta_{PASS\ DEVICE} = 70$

$\theta_{JA} = 150°C/W$

$T_A = 50°C$

With a beta of 70 in the pass device and a maximum output current of 2.0A the regulator must deliver:

$$\frac{2A}{\beta} = \frac{2A}{70} = 29 \text{ mA}$$

The LM125 power dissipation will be calculated ignoring any negative output current for this example.

$$P_{LM125} = (V_{IN} - V_{OUT})\, I_{OUT}$$
$$= (25 - 15)\, 29 \text{ mA}$$
$$= 290 \text{ mW}$$

$T_{RISE} @ \theta_{JA} = 150°C/W = 150°C \times 0.29 = 44°C$

$T_J = T_A + T_{RISE} = 50°C + 44°C = 94°C$

From Figure 7.22

$V_{SENSE} @ (T_J = 94°C) = 520$ mW

From equation (7.17)

$$R_{CL}{}^{+} = \frac{V_{SENSE}}{I_{SC}} = \frac{520 \text{ mV}}{500 \text{ mA}} \cong 1\Omega$$

From equation (7.18)

$$V_{RCL}{}^{+} = I_{FB}\, R_{CL}{}^{+} = 2A \cdot 1\Omega = 2V$$

From equation (7.19)

$$V_{R1} = V_{RCL}{}^{+} - V_{SENSE}$$
$$V_{R1} = 2V - 520 \text{ mV} = 1.480V$$

A value for I_1 can now be found from equation (7.22)

$$\frac{I_{FB}\, R_{CL}{}^{+}}{300} = \frac{2A \cdot 1\Omega}{300\Omega} = 6.6 \text{ mA}$$

So set $I_1 = 10 \times 6.6$ mA = 66 mA

Equating equation (7.28) with equation (7.29) and inserting resistor values shown in Figure 7.26,

$$I_2 + I_4 = I_5 + I_6 - I_7$$

$$I_2 + \frac{I_{FB}\, R_{CL}^- - V_{SENSE}}{300} = I_5 + \frac{I_{FB}\, R_{CL}^-}{300} - \frac{V_{SENSE}}{300} \qquad (7.34)$$

Canceling, we find:

$$I_2 = I_5 \qquad (7.35)$$

This is the key to the negative foldback circuit. Current source Q1 forces current I_2 to flow through resistor R5. The voltage drop across R5 opposes the normal current limit sense voltage so that the regulator will not current limit until the drop across R_{CL}^- due to load current, equals the controlled drop across R5 plus V_{SENSE} (given in Figure 7.22). This can be written as:

$$I_{FB} = \frac{V_{SENSE} + I_2\, R5}{R_{CL}^-}$$

$$I_{FB} = \frac{V_{SENSE} + 200\, I_2}{R_{CL}^-} \qquad (7.36)$$

Example:

Given:

$I_{FOLDBACK} = 2.5A$

$I_{SHORT\text{-}CIRCUIT} = 750\ mA$

V_{SENSE} (See Figure 7.22)

$-V_{IN} = 25V$

$-V_{OUT} = -15V$

$\beta_{PASS\ DEVICE} = 90$

$\theta_{JA} = 150°C/W$

$T_A = 25°C$

The same calculations are used here to figure V_{SENSE} as with the positive regulator foldback example maximum regulator output current is calculated from:

$$I_{OUT} = \frac{2.5\ A}{90} = 28\ mA$$

$$P_{LM125} = (V_{IN} - V_O)\, I_{OUT}$$
$$= 10V \times 28\ mA$$
$$= 280\ mW$$

$$T_{RISE} = 150°C/W \times 0.28W = 42°C$$

$$T_J = T_A + T_{RISE} = 25°C + 42°C = 67°C$$

From Figure 7.22:

$$V_{SENSE} = 500\ mV$$

From equation (7.23):

$$R_{CL}^- = \frac{500\ mV}{750\ mA} = 0.68\Omega$$

From equation (7.36):

$$I_2 = \frac{I_{FB}\, R_{CL}^- - V_{SENSE}}{200\Omega} = 6.0\ mA$$

From equation (7.24):

$$R3 = \frac{V_{OUT} - V_{BEQ1}}{I_2}$$

$$R3 \simeq \frac{14.3}{6.0\ mA} = 2.4k$$

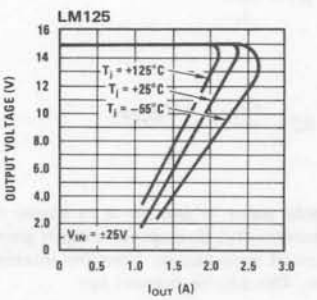


FIGURE 7.28. Negative Regulator Foldback Current Limiting Characteristics

Figure 7.27 and 7.28 show the measured foldback characteristics for the values derived in the design examples. The value of R5 is set low so that the magnitude of I_5 for foldback is greater than I_4 through I_6. This reduces the foldback point sensitivity to the TC of the internal 300Ω resistor and any mismatch in the TC of Q2, Q3 or the pass device.

R6 can be computed from equation (7.33):

$$R6 = \frac{V_{SENSE}^-}{I_7} = \frac{V_{SENSE}^-}{I_5 + I_6 - I_3}$$

combining (7.28) and (7.35).

$$R6 = \frac{V_{SENSE}^-}{I_6 - I_4} = \frac{V_{SENSE}^-}{I_{FB}\, R_{CL}^- \left(\frac{1}{300} - \frac{1}{R4}\right) + \frac{V_{BE}}{R4}} \quad (7.37)$$

Setting $V_{BE} \simeq V_{SENSE}$ and R4 = 300 to match the internal 300Ω (22) becomes:

$$R6 = R4$$

Also setting $\frac{I_4}{I_5} = \frac{2}{3} \rightarrow R5 = 200$

7.3.4 A 10-Amp Regulator

Figure 7.29 illustrates the complete schematic of a 10A regulator with foldback current limiting. The design approach is similar to that of the 2A regulator. However, in this design, the current contribution from the internal 300Ω resistor is greater due to the 2 V_{BE} drop across the Darlington pair. Expression (7.22) becomes:

$$\frac{I_{FB}\, R_{CL}^+ + V_{BE}}{300} \ll I_1 \; ; \quad (7.38)$$

and, for the negative regulator, expression (7.39) becomes:

$$R6 = \frac{V_{SENSE}^-}{I_{FB}\, R_{CL}^- \left[\frac{1}{300} - \frac{1}{R4}\right] + V_{BE}\left[\frac{1}{300} + \frac{1}{R4}\right]} \quad (7.40)$$

The disagreement between the theoretical and experimental values for the negative regulator is not alarming. In fact R_{CL} was based on equation (7.23), which is correct if for zero V_{OUT}, I_5 is zero as well. This implies:

$$V_{SENSE} \text{ (at SC)} = \frac{V_{BEQ4} + V_{BEQ5}}{2} \text{ (at SC)}$$

which is a first order approximation.

Figure 7.30 illustrates the power dissipation in the external power transistor for both sides. Maximum power dissipation occurs between full load and short circuit so the heat sink for the 2N3772 must be designed accordingly, remembering that

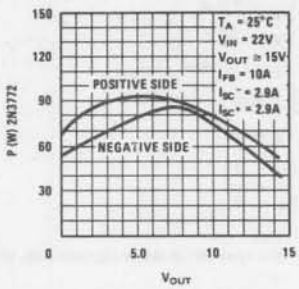


FIGURE 7.30. Power Dissipation in the External Pass Transistor (Q5, Q7)

the 2N3772 must be derated according to 0.86W/°C above 25°C. This corresponds to a thermal resistance junction to case of 1.17°C/W.

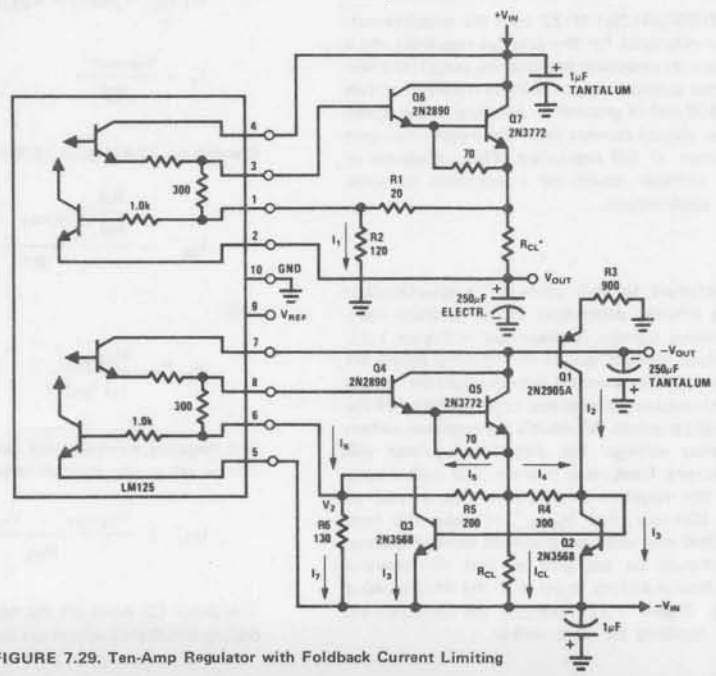


FIGURE 7.29. Ten-Amp Regulator with Foldback Current Limiting

Example

Positive Side	Theoretical Value	Experimental Results
I_{FB} = 10 A	I_{125} = 13 mA	I_{FB} = 9.8 A
I_{SC} = 2.5 A	P_{LM125} = 150 mW	I_{SC} = 2.9 A
V_{IN} = 22V	R_{CL}^+ = 0.26Ω	R_{CL}^+ = 0.26Ω
V_{OUT} = 15V	R1 = 21Ω	R1: adjusted to 20Ω
$\beta = \beta 1\, \beta 2$ = 15 X 50 = 750 min	R2 = 130Ω	R2: adjusted to 120Ω
T_A = 25°C	V_{SENSE}^+ = 650 mV	

Negative Side	Theoretical Value	Experimental Results
I_{FB} = 10 A	R_{CL}^- = 0.22Ω	I_{FB} = 10 A
I_{SC} = 2.5 A	R4 = 300Ω	I_{SC} = 2.9 A
V_{IN} = 22V	R5 = 200Ω	R_{CL}^-: adjusted to 0.3Ω
V_{OUT} = 15V	R6 = 150Ω	R6: adjusted to 130Ω
β = 800	R3 = 1.6 kΩ	R3: adjusted to 900Ω
T_A = 25°	V_{SENSE}^- = 550 mV	
$\frac{I_4}{I_5} = \frac{2}{3}$		

Note: For this example, in designing each side, the power dissipation of the opposite side has not been taken into the account.

7.3.5 Positive Current Dependent Simultaneous Current Limiting

The LM125/LM126/LM127 uses the negative output as a reference for the positive regulator. As a consequence, whenever the negative output current limits, the positive output follows tracks to within 200 – 800 mV of ground. If, however, the positive regulator should current limit the negative output will remain in full regulation. This imbalance in output voltages could be a problem in some supply applications.

As a solution to this problem, a simultaneous limiting scheme, dependent on the positive regulator output current, is presented in Figure 7.31. The output current causes an I-R drop across R1 which brings transistor Q1 into conduction. As the positive load current increases I_1 increases until the voltage drop across R2 equals the negative current limit sense voltage. The negative regulator will then current limit, and positive side will closely follow the negative output down to a level of 700 – 800 mV. For V_{OUT}^+ to drop the final 700 – 800 mV with small output current change, R_{CL}^+ should be adjusted so that the positive current limit is slightly larger than the simultaneous limiting. Figure 7.32 illustrates the simultaneous current limiting of both sides.

The following design equations may be used:

$$R1\, I_{CL}^+ = R3\, I_1 + V_{BEQ1} \tag{7.41}$$

$$I_1 = \frac{V_{SENSE}^-}{R2} \tag{7.42}$$

Combining (7.41) and (7.42)

$$I_{CL}^+ = \frac{\frac{R3}{R2} V_{SENSE}^- + V_{BEQ1}}{R1} \tag{7.43}$$

with

$$R_{CL}^+ = \frac{V_{SENSE}^+}{1.1\, I_{CL}^+} \tag{7.44}$$

The negative current limit (independent of I_{CL}^+) can be set at any desired level.

$$I_{CL}^- = \frac{V_{SENSE}^- + V_{DIODE}}{R_{CL}^-} \tag{7.45}$$

Transistor Q2 turns off the negative pass transistor during simultaneous current limiting.

From equations (7.20) and (7.21)

$$R1 = \frac{V_{R1}}{I_1} = \frac{1.480V}{66\ mA} \cong 22\Omega$$

$$R2 = \frac{+V_{OUT} + V_{SENSE}}{I_1} = \frac{15 + 0.520}{66\ mA}$$

$$\cong 240\Omega$$

The foldback limiting characteristics are shown in Figure 7.27 for the values calculated above at various operating temperatures.

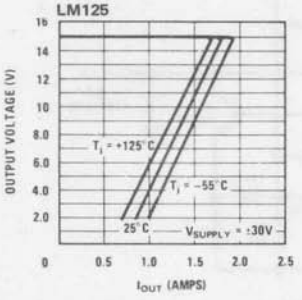


FIGURE 7.27. Positive Regulator Foldback Current Limiting Characteristics

The negative regulator foldback current limiting works essentially the same way as the positive side. Q1 forces a constant current, I_2, determined by $-V_{OUT}$ and R3, through Q2. Transistors Q2 and Q3 are matched so a current identical to I_3 will flow through Q3. With the output short-circuited ($-V_{OUT} = 0$), Q1 will be OFF, setting $I_2 = 0$. The load current will be limited when V_1 increases sufficiently due to load current to make V_2 higher than $-V_{IN}$ by the current limit sense voltage.

The short circuit current is:

$$I_{SC} \simeq \frac{V_{SENSE}}{R_{CL}^-} \qquad (7.23)$$

For calculating the maximum full load current with the output still in regulation, current I_2

$$I_2 = \frac{V_{OUT} - V_{BEQ1}}{R3} \qquad (7.24)$$

At the point of maximum load current, I_{FB}, where the regulator should start folding back:

$$V_1 = -V_{IN} + I_{FB}\ R_{CL}^- \qquad (7.25)$$

and

$$V_2 = -V_{IN} + V_{SENSE} \qquad (7.26)$$

The current through Q2 (and Q3) will have increased from I_2 by the amount of I_4 due to the voltage V_1 increasing above its no-load quiescent value. Since the voltage across Q2 is simply the diode drop of a base-emitter junction:

$$I_4 = \frac{[V_1 - (-V_{IN})] - V_{BE}}{R4}$$

Substituting in equation (7.25) gives:

$$I_4 = \frac{I_{FB}\ R_{CL}^- - V_{BE}}{R4} = \frac{I_{FB}\ R_{CL}^- - V_{BE}}{300\Omega} \qquad (7.27)$$

The current through Q2 is now

$$I_3 = I_2 + I_4 \qquad (7.28)$$

and the current through Q3 is:

$$I_3 = I_5 + I_6 - I_7 \qquad (7.29)$$

The drop accross R5 is found from:

$$V_1 - V_2 = (-V_{IN} + I_{FB}\ R_{CL}^-) - [V_{SENSE} + (-V_{IN})];$$

simplifying,

$$V_1 - V_2 = I_{FB}\ R_{CL}^- - V_{SENSE} \qquad (7.30)$$

Since V_{SENSE} is the base to emitter voltage drop of the internal limiter transistor, the V_{SENSE} in equation (7.30) very nearly equals the V_{BE} in equation (7.27). Therefore the drop across R5 approximately equals the drop across R4. The current through R5, I_5, can now be determined as:

$$I_5 = \frac{I_{FB}\ R_{CL}^- - V_{SENSE}}{R5} \qquad (7.31)$$

Summing the currents through Q3 is now possible assuming the base-emitter drop of the 2N3055 pass device can be given by $V_{BE} \approx V_{SENSE}$:

$$I_6 = \frac{V_3 - V_2}{300} \qquad (7.32)$$

where $V_3 = V_1 + V_{BE} \approx V_1 + V_{SENSE}$

$$I_6 = \frac{V_1 + V_{SENSE} - V_2}{300}$$

Substituting in equation (7.30)

$$I_6 = \frac{I_{FB}\ R_{CL}}{300}$$

$$I_7 = \frac{V_2 - (-V_{IN})}{R6} = \frac{V_{SENSE}}{R6} \qquad (7.33)$$

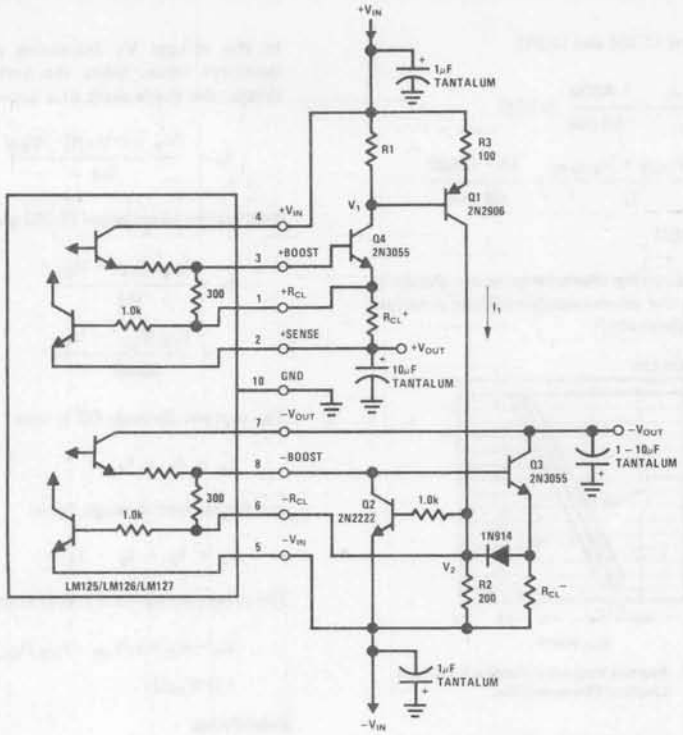


FIGURE 7.31. Positive Current Dependent Simultaneous Current Limiting

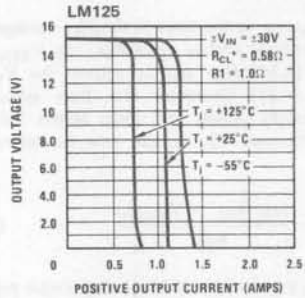


FIGURE 7.32. Positive Current Dependent Simultaneous Shutdown

7.3.6 Electronic Shutdown

In some regulated supply applications it is desirable to shutdown the regulated outputs ($\pm V_O = 0$) without having to shutdown the unregulated inputs (which may be powering additional equipment). Various shutdown methods may be used. The simplest is to insert a relay, a saturated bipolar device, or some other type switch in series with either the regulator inputs or outputs. The switch must be able to open and close under maximum load current which may be several amps.

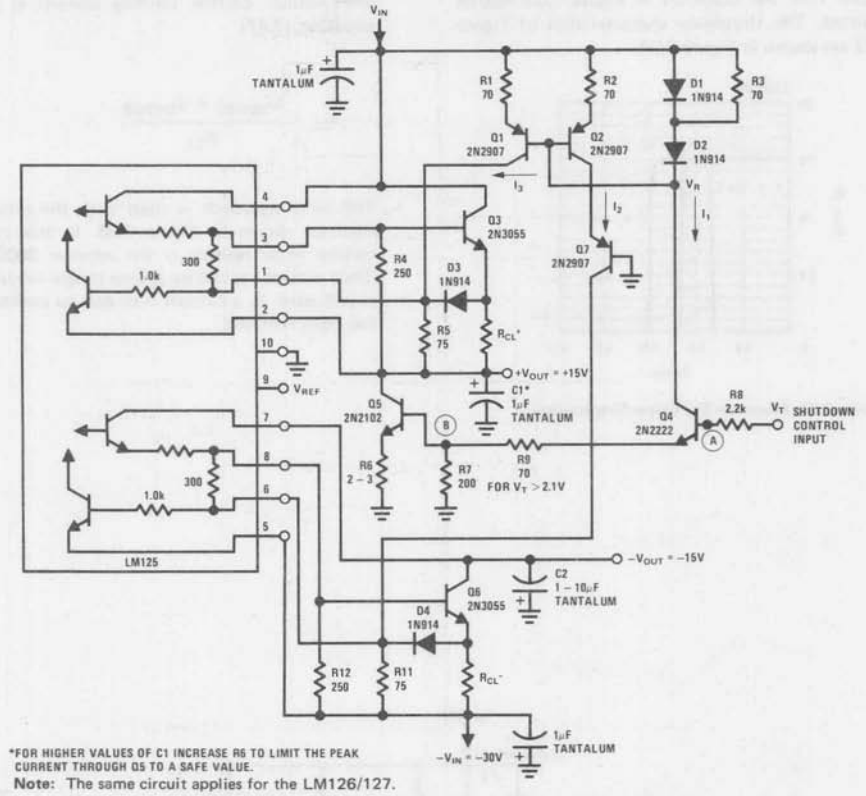
As an alternate solution, the internal reference voltage of the regulator may be shorted to ground. (See Figure 7.37)

This will force the positive and negative outputs to approximately +700 mV and +300 mV respectively. Both outputs are fully active so the full output current can still be supplied into a low impedance load. If this is unacceptable, another solution must be found.

The circuit in Figure 7.33 provides complete electronic shutdown of both regulators. The shutdown control signal is TTL compatible but by adjusting R8 and R9 the regulator may be shutdown at any desired level above 2 V_{BE}, calculated as follows:

$$V_T \simeq \left[\frac{R8}{R3\,\beta\,Q4} + \frac{R9}{R3}\right] V_{BE} + 2\,V_{BE} \quad (7.46)$$

Positive and negative shutdown operations are similar. When a shutdown signal V_T is applied, Q4 draws current through R3 and D2 establishing a voltage V_R which starts the current sources Q1 and Q2. Assuming that Q1 and Q2 are matched, and making R1 = R2 = R3, the currents I_1, I_2, I_3 are equal and both sides of the regulator shutdown simultaneously.



*FOR HIGHER VALUES OF C1 INCREASE R6 TO LIMIT THE PEAK CURRENT THROUGH Q5 TO A SAFE VALUE.

Note: The same circuit applies for the LM126/127.

FIGURE 7.33. Electronic Shutdown for the Boosted Regulator

The current I_3 creates a drop across R5, which equals or exceeds the limit sense voltage of the positive regulator, causing it to shutdown. Since I_3 has no path to ground except through the load, a fixed load is provided by Q5, which is turned on by the variable current source Q4. C1 also discharges through Q5 and current limiting resistor R6. Resistor R4 prevents Q3 turn on during shutdown, which could otherwise occur due to the drop across R5 plus the internal 300Ω resistor. Diode D3 prevents I_3 from being shunted through R_{CL}.

Capacitor C2 discharges through the load. Q7 shares the total supply voltage with Q2, thus limiting power dissipation of Q2. Another power dissipation problem may occur when the design is done for V_T = 2.0V for example, and V_T is increased above the preset threshold value. I_1 is increased and Q4 has to dissipate $(V_{IN} - 3\,V_{BE} - V_T)\,I_1$ (W). The simplest solution is to increase R8. If this is insufficient, a set of diodes may be added between nodes A and B to clamp I_1 to a reasonable value. This is illustrated in Figure 7.34.

$$I_1 = \frac{V_{R9}}{R9} \simeq \frac{V_T - V_{BE} - [V_T - 2\,V_{BE}]}{R9}$$

$$= \frac{V_{BE}}{R9}$$

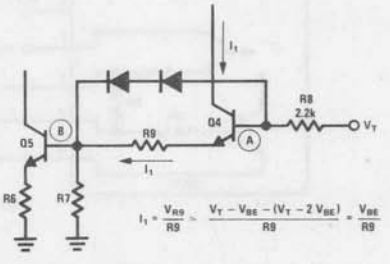


FIGURE 7.34.

So I_1 is made independent of V_T and by setting a minimum value of 10 mA (R9 = 70Ω). The regulator will shutdown at any desired level above 3 V_{BE}, without overheating transistor Q4. Also using

Figure 7.34 the diode D1 in Figure 7.33 may be omitted. The shutdown characteristics of Figure 7.33 are shown in Figure 7.34.

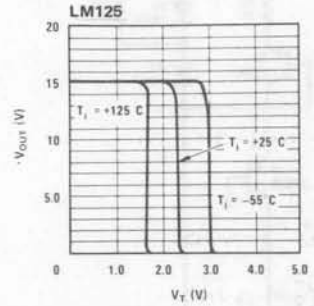
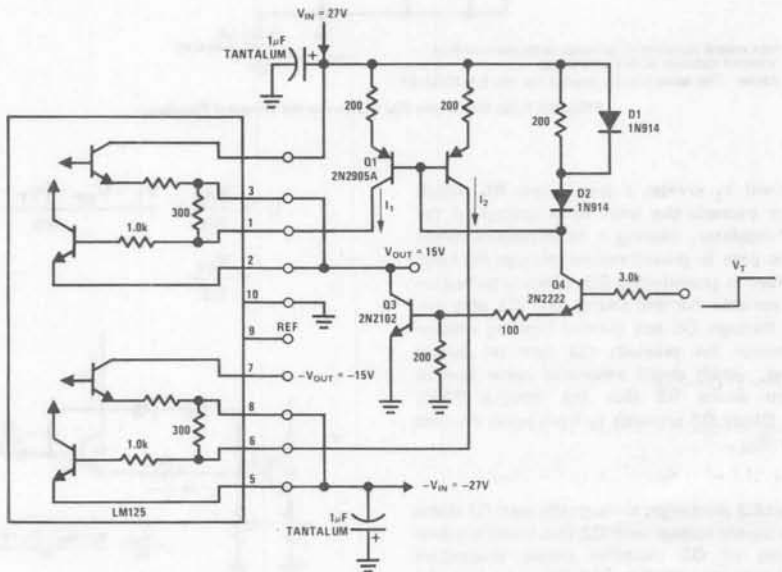


FIGURE 7.35. Electronic Shutdown Characteristics

The normal current limiting current is set by equation (7.47)

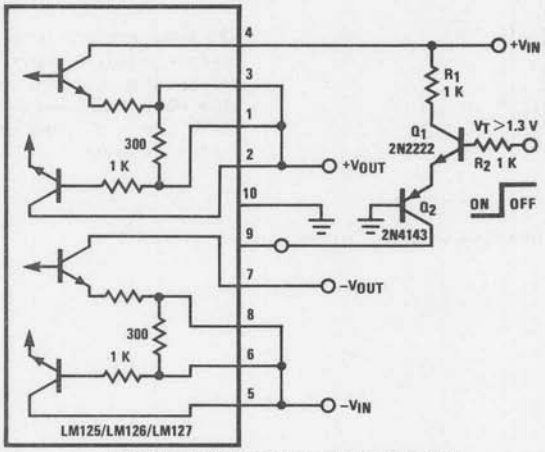
$$I_{CL} = \frac{V_{SENSE} + V_{DIODE}}{R_{CL}} \qquad (7.47)$$

The same approach is used with the unboosted regulator shown in Figure 7.36. In this case the voltage sense resistor is the internal 300Ω one. Since output capacitors are no longer required Q3 is just used as a current sink and its emitter load has been removed.



Note: The Same Circuit Applies For The LM126/127.

FIGURE 7.36. Electronic Shutdown for the Basic Regulator



NOTE: PIN NUMBERS FOR METAL CAN PACKAGE ONLY

FIGURE 7.37. Simplified Shutdown

7.3.7 Power Dissipation

The power dissipation of the LM125 is:

$$P_d = (V_{IN}^+ - V_{OUT}^+)\, I_{OUT}^+ + (V_{IN}^- - V_{OUT}^-)\, I_{OUT}^- + V_{IN}^+ I_S^+ + V_{IN}^- I_S^-$$

where I_S is the standby current.

Example:
±1A regulator using 2N3055 pass transistors. Assuming a β = 100, and ±25V supply,

$$P_d = 400 \text{ mW}.$$

The temperature rise for the TO-5 package will be:

$$T_{RISE} = 0.4 \times 150^\circ C/W = 60^\circ C$$

Therefore the maximum ambient temperature is $T_{AMAX} = T_{JMAX} - T_{RISE} = 90^\circ C$. If the device is to operate at T_A above 90°C then the TO-5 package must have a heat sink. T_{RISE} in this case will be:

$$T_{RISE} = P_d\,(\theta_{J\text{-}C} + \theta_{C\text{-}S} + \theta_{S\text{-}A}).$$