LM340 Series Three Terminal Positive Regulators

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Application Note 103
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INTRODUCTION

The LM340-XX are three terminal 1.0A positive voltage regulators, with preset output voltages of 5.0V or 15V. The LM340 regulators are complete 3-terminal regulators requiring no external components for normal operation. However, by adding a few parts, one may improve the transient response, provide for a variable output voltage, or increase the output current. Included on the chip are all of the functional blocks required of a high stability voltage regulator; these appear in *Figure 1*.

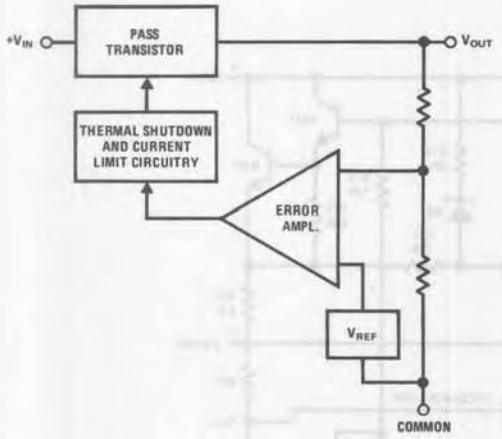

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FIGURE 1. Functional Block of the LM340

The error amplifier is internally compensated; the voltage reference is especially designed for low noise and high predictability; and, as the pass element is included, the regulator contains fixed current limiting and thermal protection. The LM340 is available in either metal can TO-3 or plastic TO-220 package.

1. CIRCUIT DESIGN

Voltage Reference

Usually IC voltage regulators use temperature-compensated zeners as references. Such zeners exhibit BV > 6.0V which sets the minimum supply voltage somewhat above 6.0V. Additionally they tend to be noisy, thus a large bypass capacitor is required.

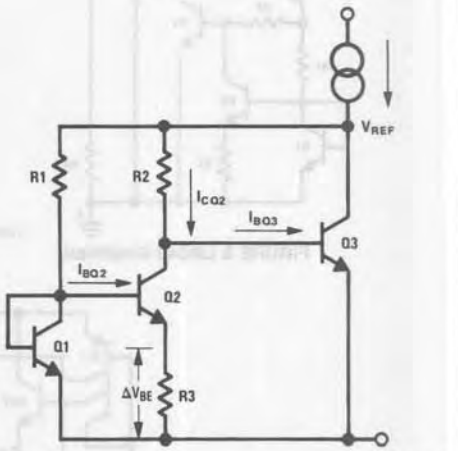

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FIGURE 2. Simplified Volt Reference

Figure 2 illustrates a simplified reference using the predictable temperature, voltage, and current relationship of emitter-base junctions.

Assuming $J_{Q1} > J_{Q2}$, $I_{CQ2} \gg I_{BQ2} = I_{BQ3}$,
Area (emitter Q1) = Area (emitter Q2), and

$$V_{BEQ1} = V_{BEQ3}, \quad (1\text{-}1)$$

then

$$V_{REF} \cong \left(\frac{kT}{q} \ln \frac{R2}{R1}\right)\frac{R2}{R3} + V_{BEQ3} \quad (1\text{-}2)$$

Simplified LM340

In *Figure 3* the voltage reference includes R1–R3 and Q1–Q5. Q3 also acts as an error amplifier and Q6 as a buffer between Q3 and the current source. If the output drops, this drop is fed back, through R4, R5, Q4, Q5, to the base of Q3. Q7 then conducts more current re-establishing the output given by:

$$V_{OUT} = V_{REF}\frac{R4 + R5}{R4}$$

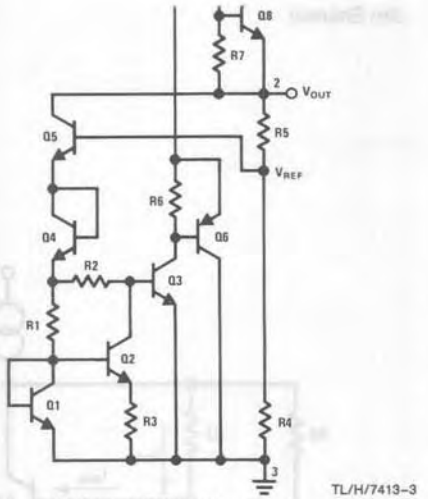

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FIGURE 3. LM340 Simplified

develop the reference voltage. R17 is changed to get the various fixed output voltages.

Short Circuit Protection

A) $V_{IN}-V_{OUT} < 6.0V$: There is no current through D2 and the maximum output current will be given by:

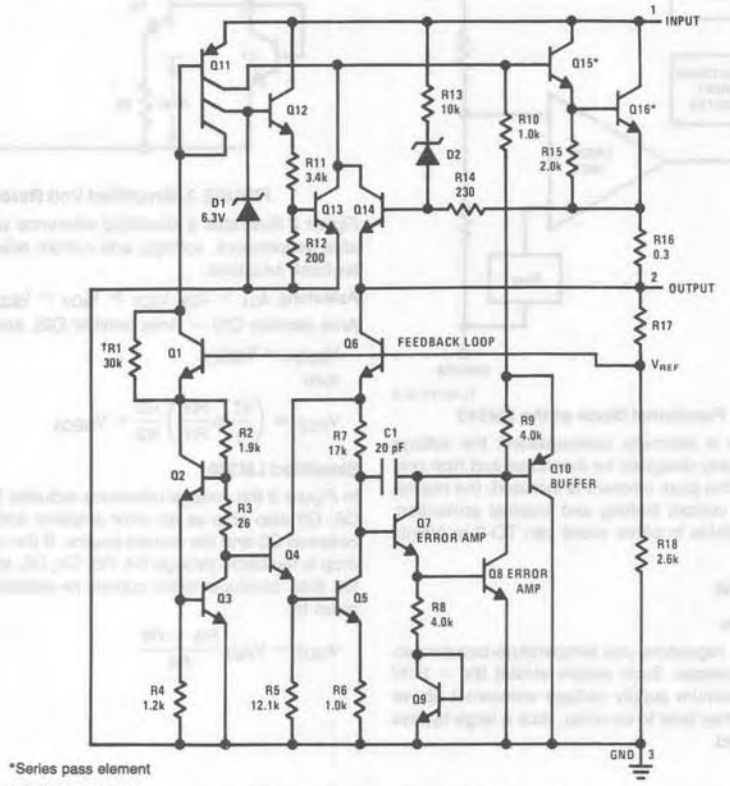
$$I_{OUT\ MAX} = \frac{V_{BEQ14}}{R16} \cong 2.2A\ (T_j = 25°C) \qquad (1\text{-}4)$$

B) $V_{IN}-V_{OUT} > 6.0V$: To keep Q16 operating within its maximum power rating the output current limit must decrease as $V_{IN}-V_{OUT}$ increases. Here D2 conducts and the drop across R16 is less than V_{BE} to turn on Q14. In this case I_{OUT} maximum is:

$$I_{OUT\ MAX} = \int \frac{1}{R16}\left(V_{BEQ14} - \frac{[(V_{IN} - V_{OUT}) - V_{ZD2} - V_{BEQ14}]}{R13} R14\right)$$

$$= 0.077\ [37.2 - (V_{IN} - V_{OUT})]\ (A) \qquad (1\text{-}5)$$

at $T_j = 25°C$



*Series pass element

†Starting up resistor

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FIGURE 4. Complete Circuit of the LM340

Thermal Shut Down

In *Figure 4* the V_{BE} of Q13 is clamped to 0.4V. When the die temperature reaches approximately +175°C the V_{BE} to turn on Q13 is 0.4V. When Q13 turns on it removes all base drive from Q15 which turns off the regulator thus preventing a further increase in die temperature.

Power Dissipation

The maximum power dissipation of the LM340 is given by:

$$P_{D\,MAX} = (V_{IN\,MAX} - V_{OUT})\, I_{OUT\,MAX} + V_{IN\,MAX}\, I_Q \text{ (W)} \quad (1\text{-}6)$$

The maximum junction temperature (assuming that there is no thermal protection) is given by:

$$T_{jM} = \frac{36 - 13\, I_{OUT\,MAX} - (V_{IN} - V_{OUT})}{0.0855} + 25°C \quad (1\text{-}7)$$

Example:

$V_{IN\,MAX}$ = 23V, $I_{OUT\,MAX}$ = 1.0A, LM340T-15.

Equation (1-7) yields: T_{jM} = 200°C. So the T_j max of 150°C specified in the data sheet should be the limiting temperature.

From (1-6) $P_D \cong$ 8.1W. The thermal resistance of the heat sink can be estimated from:

$$\theta_{s\text{-}a} = \frac{T_{jMAX} - T_A}{P_D} - (\theta_{j\text{-}c} + \theta_{c\text{-}s}) \text{ (°C/W)} \quad (1\text{-}8)$$

The thermal resistance $\theta_{j\text{-}c}$ (junction to case) of the TO-220 package is 6°C/W, and assuming a $\theta_{c\text{-}s}$ (case to heat sink) of 0.4, equation (1-8) yields:

$\theta_{s\text{-}a}$ = 8.4°C/W

2. CURRENT SOURCE

The circuit shown on *Figure 5* provides a constant output current (equal to $V_{OUT}/R1$ or 200 mA) for a variable load impedance of 0 to 85Ω. Using the following definitions and the notation shown on *Figure 5*, Z_{OUT} and I_{OUT} are:

Q_{CC}/V = Quiescent current change per volt of input/output (pin 1 to pin 2) voltage change of the LM340

L_r/V = Line regulation per volt: the change in the LM340 output voltage per volt of input/output voltage change at a given I_{OUT}.

$$\Delta I_{OUT} = (Q_{CC}/V)\, \Delta V_{OUT} + \frac{L_r/V}{R1} \Delta V_{OUT} \quad (2\text{-}1)$$

$$Z_{OUT} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \quad (2\text{-}2)$$

$$Z_{OUT} = \frac{\Delta V_{OUT}}{(Q_{CC}/V)\Delta V_{OUT} + \frac{(L_r/V)}{R1}\Delta V_{OUT}} \quad (2\text{-}3)$$

$$Z_{OUT} = \frac{1}{(Q_{CC}/V) + \frac{(L_r/V)}{R1}} \quad (2\text{-}4)$$

The LM340-5.0 data sheet lists maximum quiescent current change of 1.0 mA for a 7.0V to 25V change in input voltage; and a line regulation (interpolated for I_{OUT} = 200 mA) of 35 mV maximum for a 7.0V to 25V change in input voltage:

$$Q_{CC}/V = \frac{1.0\text{ mA}}{15V} = 55\ \mu A/V \quad (2\text{-}5)$$

$$L_r/V = \frac{35\text{ mV}}{18V} \cong 2\text{ mV/V} \quad (2\text{-}6)$$

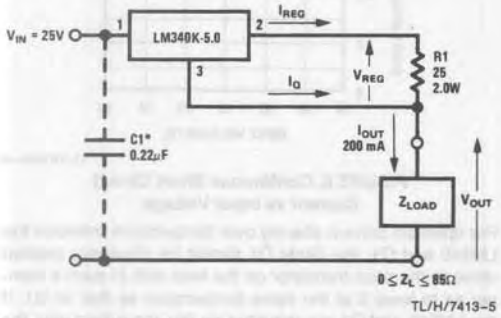
The worst case change in the 200 mA output current for a 1.0V change in output or input voltage using equation 2-1 is:

$$\frac{\Delta I_{OUT}}{1.0V} = 55\ \mu A + \frac{2\text{ mV}}{25\Omega} = 135\ \mu A \quad (2\text{-}7)$$

and the output impedance for a 0 to 85Ω change in Z_L using equation 2-4 is:

$$Z_{OUT} = \frac{1}{55\ \mu A + \frac{2\text{ mV}}{25\Omega}} = 7.4\text{ k}\Omega \quad (2\text{-}8)$$

Typical measured values of Z_{OUT} varied from 10–12.3 kΩ, or 81–100 μA/V change input or output (approximately 0.05%/V).

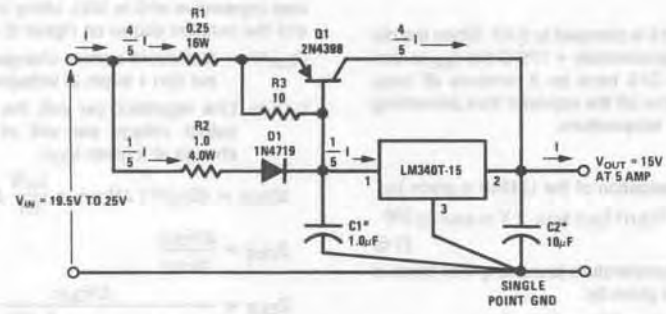


*Required if regulator is located far from power supply filter

FIGURE 5. Current Source

3. HIGH CURRENT REGULATOR WITH SHORT CIRCUIT CURRENT LIMIT

The 15V regulator circuit of *Figure 6* includes an external boost transistor to increase output current capability to 5.0A. Unlike the normal boosting methods, it maintains the LM340's ability to provide short circuit current limiting and thermal shut-down without use of additional active components. The extension of these safety features to the external pass transistor Q1 is based on a current sharing scheme



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*Solid tantalum

Note 1: Current sharing between the LM340 and Q1 allows the extension of short circuit current limit, safe operating area protection, and (assuming Q1's heat sink has four or more times the capacity of the LM340 head sink) thermal shutdown protection.

Note 2: $I_{SHORT\ CIRCUIT}$ is approximately 5.5 amp.

Note 3: $I_{OUT\ MAX}$ at V_{OUT} = 15V is approximately 9.5 amp.

FIGURE 6. 15V 5.0A Regulator with Short Circuit Current Limit

using R1, R2, and D1. Assuming the base-to-emitter voltage of Q1 and the voltage drop across D1 are equal, the voltage drops across R1 and R2 are equal. The currents through R1 and R2 will then be inversely proportional to their resistances. For the example shown on *Figure 6*, resistor R1 will have four times the current flow of R2. For reasonable values of Q1 beta, the current through R1 is approximately equal to the collector current of Q1; and the current through R2 is equal to the current flowing through the LM340. Therefore, under overload or short circuit conditions the protection circuitry of the LM340 will limit its own output current and, because of the R1/R2 current sharing scheme, the output current of Q1 as well. Thermal overload protection also extends Q1 when its heat sink has four or more times the capacity of the LM340 heat sink. This follows from the fact that both devices have approximately the same input/output voltage and share the load current in a ratio of four to one.

The circuit shown on *Figure 6* normally operates at up to 5.0A of output current. This means up to 1.0A of current flows through the LM340 and up to 4.0A flows through Q1. For short term overload conditions the curve of *Figure 7* shows the maximum instantaneous output current versus temperature for the boosted regulator. This curve reflects the approximately 2.0A current limit of the LM340 causing an 8.0A current limit in the pass transistor, or 10A, total.

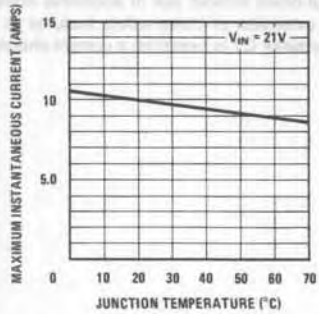

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FIGURE 7. Maximum Instantaneous Current vs Junction Temperature

Under continuous short circuit conditions the LM340 will heat up and limit to a steady total state short circuit current of 4.0A to 6.0A as shown in *Figure 8*. This curve was taken using a Wakefield 680-75 heat sink (approximately 7.5°C/W) at a 25°C ambient temperature.

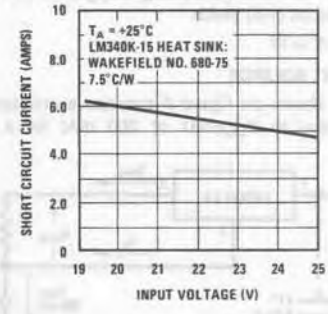

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FIGURE 8. Continuous Short Circuit Current vs Input Voltage

For optimum current sharing over temperature between the LM340 and Q1, the diode D1 should be physically located close to the pass transistor on the heat sink in such a manner as to keep it at the same temperature as that of Q1. If the LM340 and Q1 are mounted on the same heat sink the LM340 should be electrically isolated from the heat sink since its case (pin 3) is at ground potential and the case of Q1 (its collector) is at the output potential of the regulator. Capacitors C1 and C2 are required to prevent oscillations and improve the output impedance respectively. Resistor R3 provides a path to unload excessive base charge from the base of Q1 when the regulator goes suddenly from full load to no load. The single point ground system shown on *Figure 6* allows the sense pins (2 and 3) of the LM340 to monitor the voltage directly at the load rather than at some point along a (possibly) resistive ground return line carrying up to 5.0A of load current. *Figure 9* shows the typical variation of load regulation versus load current for the boosted regulator. The insertion of the external pass transistor increases the input/output differential voltage from 2.0V to

approximately 4.5V. For an output current less than 5.0A, the R2/R1 ratio can be set lower than 4:1. Therefore, a less expensive PNP transistor may be used.

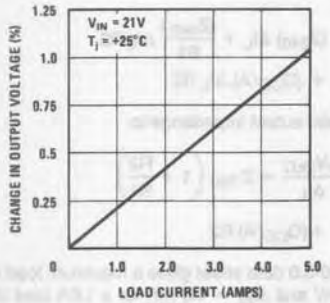

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FIGURE 9. Load Regulation

4. 5.0V, 5.0A VOLTAGE REGULATOR FOR TTL

The high current 5.0V regulator for TTL shown in *Figure 10* uses a relatively inexpensive NPN pass transistor with a lower power PNP device to replace the single, higher cost, power PNP shown in *Figure 6*. This circuit provides a 5.0V output at up to 5.0A of load current with a typical load regulation of 1.8% from no load to full load. The peak instantaneous output current observed was 10.4A at a 25°C junction temperature (pulsed load with a 1.0 ms ON and a 200 ms OFF period) and 8.4A for a continuous short circuit. The typical line regulation is 0.02% of input voltage change (I_{OUT} = 0).

One can easily add an overload indicator using the National's new NSL5027 LED. This is shown with dotted lines in *Figure 10*. With this configuration R2 is not only a current sharing resistor but also an overload sensor. R5 will determine the current through the LED; the diode D2 has been added to match the drop across D1. Once the load current exceeds 5.0A (1.0A through the LM340 assuming perfect current sharing and $V_{D1} = V_{D2}$) Q3 turns ON and the overload indicator lights up.

Example:

$I_{OVERLOAD}$ = 5.0A

I_{LED} = 40 mA (light intensity of 16 mcd)

$$V_{LED} = 1.75,\ R5 \cong \frac{V_{IN} - 2.65}{I_{LED}} \qquad (4\text{-}1)$$

5. ADJUSTABLE OUTPUT VOLTAGE REGULATOR FOR INTERMEDIATE OUTPUT VOLTAGES

The addition of two resistors to an LM340 circuit allows a non-standard output voltage while maintaining the limiting features built into IC. The example shown in *Figure 11* provides a 10V output using an LM340K-5.0 by raising the reference (pin number 3) of the regulator by 5.0V.

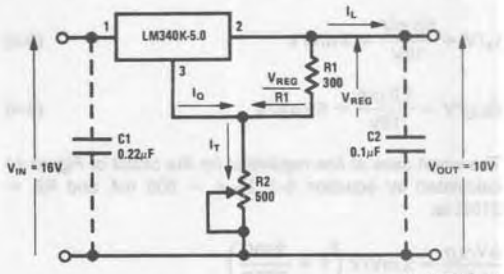

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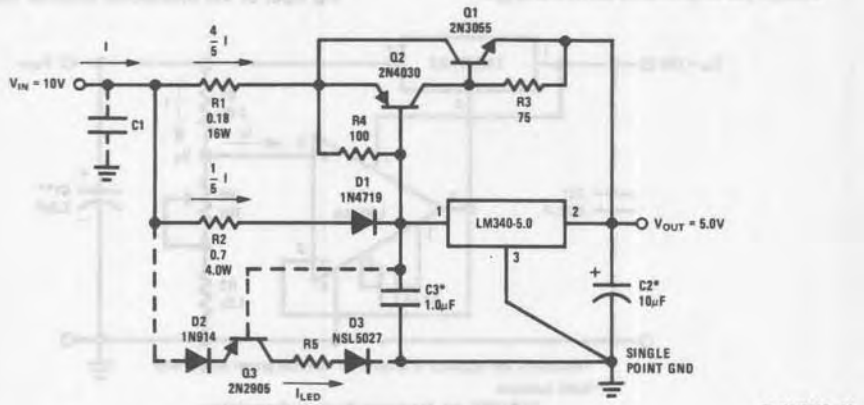
FIGURE 11. 10V Regulator

The 5.0V pedestal results from the sum of regulator quiescent current I_Q and a current equal to $V_{REG}/R1$, flowing through potenteniometer R2 to ground. R2 is made adjustable to compensate for differences in I_Q and V_{REG} output. The circuit is practical because the change in I_Q due to line voltage and load current changes is quite small.

The line regulation for the boosted regulator is the sum of the LM340 line regulation, its effects on the current through



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*Solid tantalum

FIGURE 10. 5.0V, 5.0A Regulator for TTL (with short circuit, thermal shutdown protection, and overload indicator)

R2, and the effects of ΔI_Q in response to input voltage changes. The change in output voltage is:

$$\Delta V_{OUT} = (L_r/V)\,\Delta V_{IN} + \frac{(L_r/V)\,\Delta V_{IN}\,R2}{R1} + (Q_{CC}/V)\,\Delta V_{IN}\,R2 \quad (5\text{-}1)$$

giving a total line regulation of:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = (L_r/V)\left(1 + \frac{R2}{R1}\right) + (Q_{CC}/V)\,R2 \quad (5\text{-}2)$$

The LM340-5.0 data sheet lists $\Delta V_{OUT} < 50$ mV and $\Delta I_Q < 1.0$ mA for $\Delta V_{IN} = 18$V at $I_{OUT} = 500$ mA. This is:

$$L_r/V = \frac{50\text{ mV}}{18\text{V}} \approx 3\text{ mV/V} \quad (5\text{-}3)$$

$$Q_{CC}/V = \frac{1.0\text{ mA}}{18\text{V}} = 55\ \mu\text{A/V} \quad (5\text{-}4)$$

The worst case at line regulation for the circuit of *Figure 11* calculated by equation 5-2, $I_{OUT} = 500$ mA and R2 = 310Ω is:

$$\frac{\Delta V_{OUT}}{1.0\text{V}} = 3\text{ mV/V}\left(1 + \frac{310\Omega}{300\Omega}\right) + (55\ \mu\text{A/V})\,310\Omega \quad (5\text{-}5)$$

$$\frac{\Delta V_{OUT}}{1.0\text{V}} = 6\text{ mV/V} + 17\text{ mV/V} = 23\text{ mV/V} \quad (5\text{-}6)$$

This represents a worst case line regulation value of 0.23%/V.

The load regulation is the sum of the LM340 voltage regulation, its effect on the current through R2, and the effect of ΔI_Q in response to changes in load current. Using the following definitions and the notation shown on *Figure 11* ΔV_{OUT} is:

Z_{OUT} = Regulator output impedance: the change in output voltage per amp of load current change.

Z_{340} = LM340 output impedance

Q_{CC}/A = Quiescent current change per amp of load current change

$$\Delta V_{OUT} = (Z_{340})\,\Delta I_L + \frac{(Z_{340})}{R1}\,\Delta I_L\,R2 + (Q_{CC}/A)\,\Delta I_L\,R2 \quad (5\text{-}7)$$

and the total output impedance is:

$$Z_{OUT} = \frac{\Delta V_{OUT}}{\Delta I_L} = Z_{340}\left(1 + \frac{R2}{R1}\right) + (Q_{CC}/A)\,R2 \quad (5\text{-}8)$$

The LM340-5.0 data sheet gives a maximum load regulation $L_r = 50$ mV and $\Delta I_Q = 1.0$ mA for a 1.0A load change.

$$Z_{340} = \frac{50\text{ mV}}{1.0\text{A}} = 0.05\Omega \quad (5\text{-}9)$$

$$Q_{CC}/A = \frac{1\text{ mA}}{1.0\text{A}} = 100\ \mu\text{A/A} \quad (5\text{-}10)$$

This gives a worst case dc output impedance (ac output impedance being a function of C2) for the 10V regulator using equation 5-8 of:

$$Z_{OUT} = 0.05\Omega\left(1 + \frac{310\Omega}{300\Omega}\right) + (100\ \mu\text{A/A})\,310\Omega \quad (5\text{-}11)$$

$$Z_{OUT} = 0.10\Omega + 0.031\Omega = 0.13\Omega$$

or a worst case change of approximately 1.5% for a 1.0A load change. Typical measured values are about one-third of the worst case value.

6. VARIABLE OUTPUT REGULATOR

In *Figure 12* the ground terminal of the regulator is "lifted" by an amount equal to the voltage applied to the non-inverting input of the operational amplifier LM101A. The output

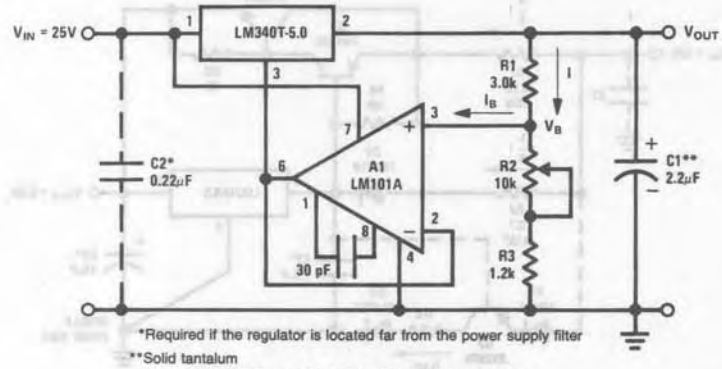

FIGURE 12. Variable Output Regulator

voltage of the regulator is therefore raised to a level set by the value of the resistive divider R1, R2, R3 and limited by the input voltage. With the resistor values shown in *Figure 12*, the output voltage is variable from 7.0V to 23V and the maximum output current (pulsed load) varies from 1.2A to 2.0A (T_j = 25°C) as shown in *Figure 13*.

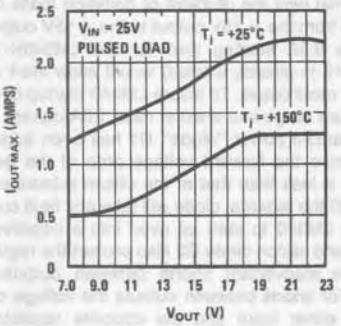

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FIGURE 13. Maximum Output Current

Since the LM101A is operated with a single supply (the negative supply pin is grounded). The common mode voltage V_B must be at least at a 2.0 V_{BE} + V_{SAT} above ground. R3 has been added to insure this when R2 = 0. Furthermore the bias current I_B of the operational amplifier should be negligible compared to the current flowing through the resistive divider.

Example:

V_{IN} = 25V

$V_{OUT\ MIN}$ = 5 + V_B, (R2 = 0),

V_B = R3 (I − I_B) = 2.0V

R1 = 2.5 R3

$V_{OUT\ MAX}$ = V_{IN} − dropout volt.

(R2 = $R2_{MAX}$)

$R2_{MAX}$ = 3.3 R1

So setting R3, the values of R1 and R2 can be determined.

If the LM324 is used instead of the LM101A, R3 can be omitted since its common mode voltage range includes the ground, and then the output will be adjustable from 5 to a certain upper value defined by the parameters of the system.

The circuit exhibits the short-circuit protection and thermal shutdown properties of the LM340 over the full output range.

The load regulation can be predicted as:

$$\Delta V_{OUT} = \frac{R1 + R2 + R3}{R1} \Delta V_{340} \qquad (6\text{-}1)$$

where ΔV_{340} is the load regulation of the device given in the data sheet. To insure that the regulator will start up under full load a reverse biased small signal germanium diode, 1N91, can be added between pins 2 and 3.

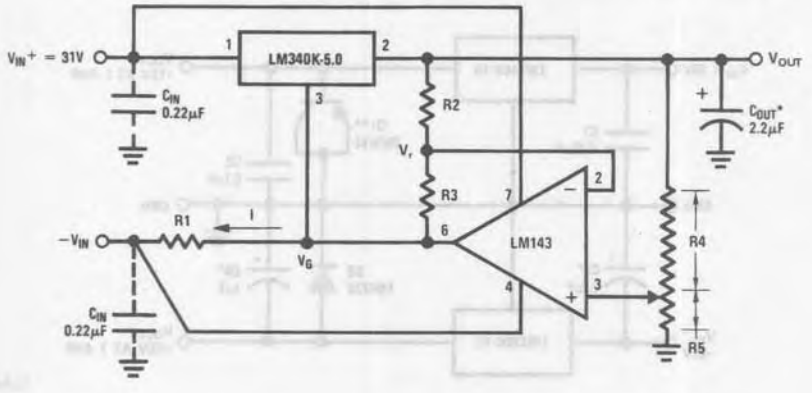
7. VARIABLE OUTPUT REGULATOR 0.5V–29V

When a negative supply is available an approach equivalent to that outlined in section 6 may be used to lower the minimum output voltage of the regulator below the nominal voltage that of the LM340 regulator device. In *Figure 14* the voltage V_G at the ground pin of the regulator is determined by the drop across R1 and the gain of the amplifier. The current I may be determined by the following relation:

$$I = \frac{V_{340}}{R1} \frac{R2\ R5 - R3\ R4}{R4\ (R2 + R3)} + \frac{V_{IN}^-}{R1} \qquad (7\text{-}1)$$

or if R2 + R3 = R4 + R5 = R

$$I = \frac{V_{340}\ R2}{R1\ R4} + \frac{1}{R1} (V_{IN}^- - V_{340}) \qquad (7\text{-}2)$$



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*Solid tantalum

FIGURE 14. Variable Output Voltage 0.5V − 30V

considering that the output is given by:

$$V_{OUT} = V_G + V_{340} \quad (7\text{-}3)$$

and

$$V_G = R1\,I - V_{IN}^- \quad (7\text{-}4)$$

combining 7-2, 7-3, 7-4 an expression for the output voltage is:

$$V_{OUT} = V_{340}\frac{R2}{R4} \quad (7\text{-}5)$$

Notice that the output voltage is inversely proportional to R4 so the output voltage may be adjusted very accurately for low values. A minimum output of 0.5V has been set. This implies that

$$\frac{R2}{R4} = 0.1\frac{R3}{R4} = 0.9\frac{R3}{R2} = 9 \quad (7\text{-}6)$$

An absolute zero output voltage will require R4 = ∞ or R2 = 0, neither being practical in this circuit. The maximum output voltage as shown in *Figure 14* is 30V if the high voltage operational amplifier LM143 is used. If only low values of V_{OUT} are sought, then an LM101 may be used. R1 can be computed from:

$$R1 = \frac{V_{IN}^-}{I_{Q340}} \quad (7\text{-}7)$$

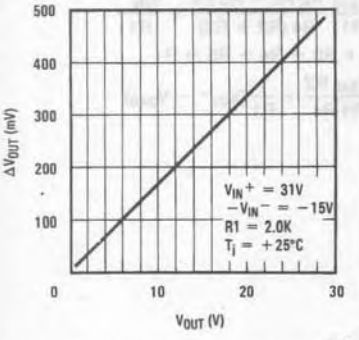

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FIGURE 15. Typical Load Regulation for a 0.5V−30V Regulator (ΔI_{OUT} = 1.0A)

Figure 15 illustrates the load regulation as a function of the output voltage.

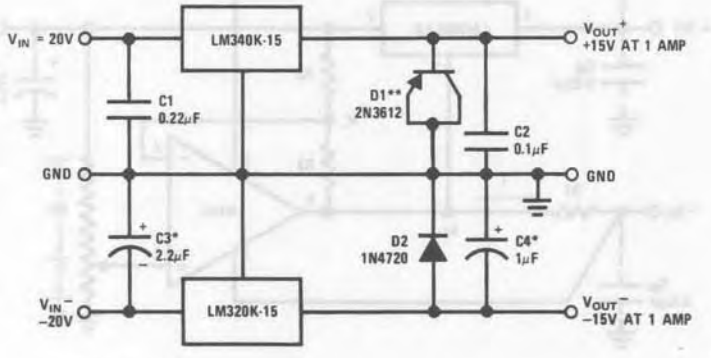
8. DUAL POWER SUPPLY

The plus and minus regulators shown in *Figure 16* will exhibit line and load regulations consistent with their specifications as individual regulators. In fact, operation will be entirely normal until the problem of common loads occurs. A 30Ω load from the +15V output to the −15V output (representing a 0.5A starting load for the LM340K-15 if the LM320K-15 is already started) would allow start up of the LM340 in most cases. To insure LM340 startup over the full temperature range into a worst case 1.0A current sink load the germanium power "diode" D1 has been added to the circuit. Since the forward voltage drop of the germanium diode D1 is less than that of the silicon substrate diode of the LM340 the external diode will take any fault current and allow the LM340 to start up even into a negative voltage load. D1 and silicon diode D2 also protect the regulator outputs from inadvertant shorts between outputs and to ground. For shorts between outputs the voltage difference between either input and the opposite regulator output should not exceed the maximum rating of the device.

The example shown in *Figure 16* is a symmetrical ±15V supply for linear circuits. The same principle applies to nonsymmetrical supplies such as a +5.0V and −12V regulator for applications such as registers.

9. TRACKING DUAL REGULATORS

In *Figure 17*, a fraction of the negative output voltage "lifts" the ground pins of the negative LM320K-15 voltage regulator and the LM340K-15 through a voltage follower and an inverter respectively. The dual operational amplifier LM1558 is used for this application and since its supply voltage may go as high as ±22V the regulator outputs may be set between 5.0V and 20V. Because of the tighter output tolerance and the better drift of the LM320, the positive regulator is made to track the negative. The best tracking action is achieved by matching the gain of both operational amplifiers, that is, the resistors R2 and R3 must be matched as closely as possible.



TL/H/7413–16

*Solid tantalum

**Germanium diode (using a PNP germanium transistor with the collector shorted to the emitter)

Note: C1 and C2 required if regulators are located far from power supply filter.

FIGURE 16. Dual Power Supply

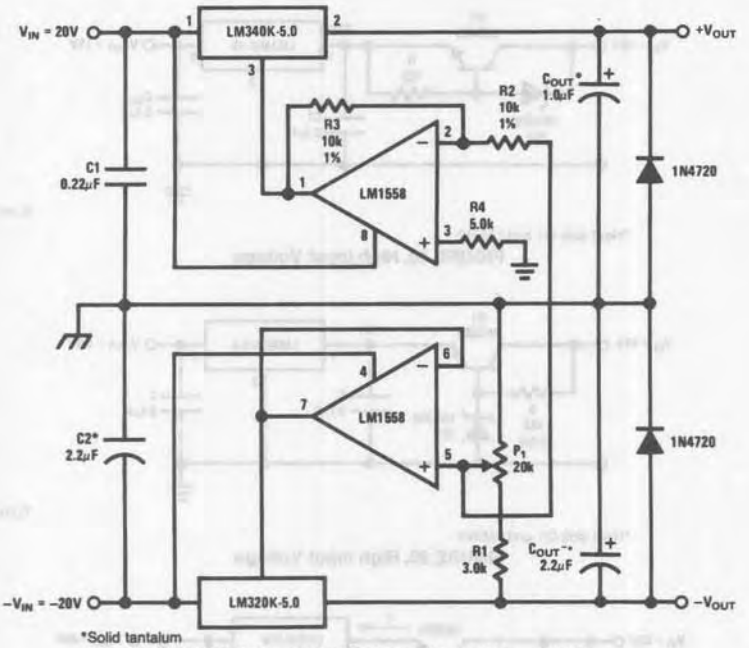


FIGURE 17. Tracking Dual Supply ±5.0V − ±18V

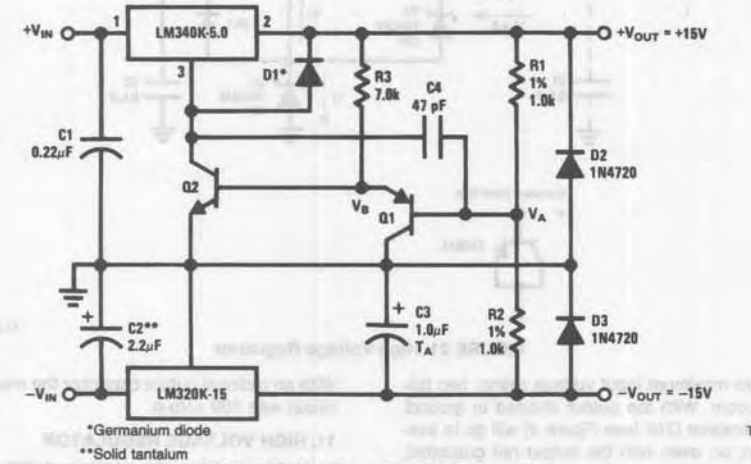


FIGURE 18. Tracking Dual Supply ±15V

Indeed, with R2 and R3 matched to better than 1%, the LM340 tracks the LM320 within 40–50 mV over the entire output range. The typical load regulation at V_{OUT} = ±15V for the positive regulator is 40 mV from a 0 to 1.0A pulsed load and 80 mV for the negative.

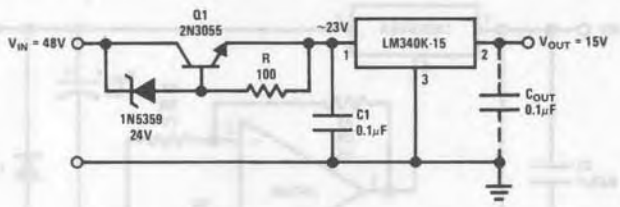
Figure 18 illustrates ±15V tracking regulator, where again the positive regulator tracks the negative. Under steady state conditions V_A is at a virtual ground and V_B at a V_{BE} above ground. Q2 then conducts the quiescent current of the LM340. If $-V_{OUT}$ becomes more negative the collector base junction of Q1 is forward biased thus lowering V_B and raising the collector voltage of Q2. As a result $+V_{OUT}$ rises and the voltage V_A again reaches ground potential.

Assuming Q1 and Q2 to be perfectly matched, the tracking action remains unchanged over the full operating temperature range.

With R1 and R2 matched to 1%, the positive regulator tracks the negative within 100 mV (less than 1%). The capacitor C4 has been added to improve stability. Typical load regulations for the positive and negative sides from a 0 to 1.0A pulsed load (t_{ON} = 1.0 ms, t_{OFF} = 200 ms) are 10 mV and 45 mV respectively.

10. HIGH INPUT VOLTAGE

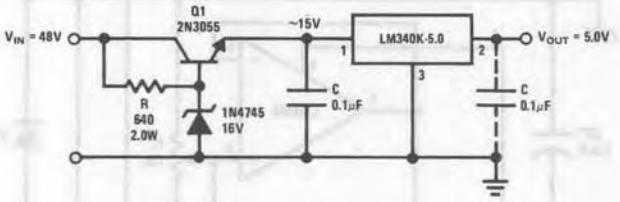
The input voltage of the LM340 must be kept within the limits specified in the data sheet. If the device is operated



TL/H/7413–19

*Heat sink Q1 and LM340

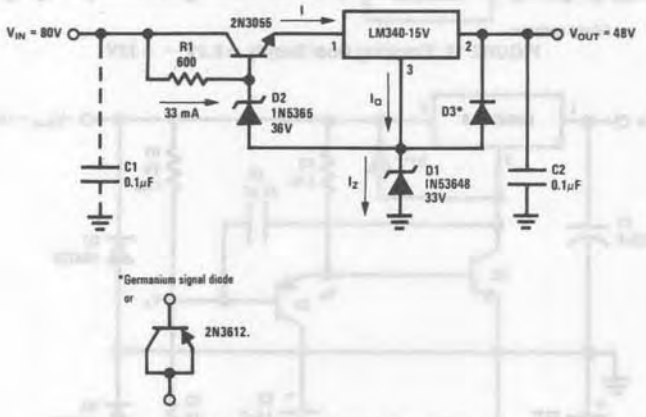
FIGURE 19. High Input Voltage



TL/H/7413–20

*Heat sink Q1 and LM340

FIGURE 20. High Input Voltage



TL/H/7413–21

FIGURE 21. High Voltage Regulator

above the absolute maximum input voltage rating, two failure modes may occur. With the output shorted to ground, the series pass transistor Q16 (see *Figure 4*) will go to avalanche breakdown; or, even with the output not grounded, the transistor Q1 may fail since it is operated with a collector-emitter voltage approximately 4.0V below the input.

If the only available supply runs at a voltage higher than the maximum specified, one of the simplest ways to protect the regulator is to connect a zener diode in series with the input of the device to level shift the input voltage. The drawback to this approach is obvious. The zener must dissipate ($V_{SUPPLY} - V_{IN\ MAX}$ LM340). (I_{OUTMAX}) which may be several watts. Another way to overcome the over voltage problem is illustrated in *Figure 19* where an inexpensive, NPN-zener-resistor, combination may be considered as an equivalent to the power zener. The typical load regulation of this circuit is 40 mV from 0 to 1.0A pulsed load (T_j = 25°C) and the line regulation is 2.0 mV for 1.0V variation in the input voltage (I_{OUT} = 0). A similar alternate approach is shown in *Figure 20*.

With an optional output capacitor the measured noise of the circuit was 700 μVp-p.

11. HIGH VOLTAGE REGULATOR

In previous sections the principle of "lifting the ground terminal" of the LM340, using a resistor divider or an operational amplifier, has been illustrated. One can also raise the output voltage by using a zener diode connected to the ground pin as illustrated in the *Figure 21* to obtain an output level increased by the breakdown voltage of the zener. Since the input voltage of the regulator has been allowed to go as high as 80V a level shifting transistor-zener (D2)—resistor combination has been added to keep the voltage across the LM340 under permissible values. The disadvantage of the system is the increased output noise and output voltage drift due to the added diodes.

Indeed it can be seen that, from no load to full load conditions, the ΔI_Z will be approximately the current through R1 (≅ 35 mA) and therefore the degraded regulation caused by D1 will be V_Z (at 35 mA + I_Q) − V_Z (at I_Q).

The measured load regulation was 60 mV for ΔI_{OUT} of 5.0 mA to 1.0A (pulsed load), and the line regulation is 0.01%V of input voltage change (I_{OUT} = 500 mA) and the typical output noise 2.0 mVp-p (C2 = 0.1 μF). The value of R1 is calculated as:

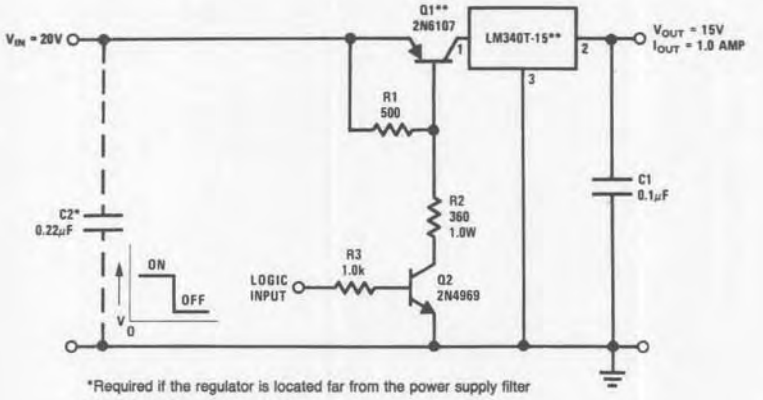
$$R1 \cong \beta\left[\frac{V_{IN} - (V_{Z1} + V_{Z2})}{I\ \text{full load}}\right] \qquad (11\text{-}1)$$

12. ELECTRONIC SHUTDOWN

Figure 22 shows a practical method of shutting down the LM340 under the control of a TTL or DTL logic gate. The pass transistor Q1 operates either as a saturated transistor or as an open switch. With the logic input high (2.4V specified minimum for TTL logic) transistor Q2 turns on and pulls 50 mA down through R2. This provides sufficient base drive to maintain Q1 in saturation during the ON condition of the switch. When the logic input is low (0.4V specified maximum for TTL logic) Q2 is held off, as is Q1; and the switch is in the OFF condition. The observed turn-on time was 7.0 μs for resistive loads from 15Ω to infinity and the turn-off time varied from approximately 3.0 μs for a 15Ω load to 3.0 ms for a no-load condition. Turn-off time is controlled primarily by the time constant of R_{LOAD} and C1.

13. VARIABLE HIGH VOLTAGE REGULATOR WITH OVERVOLTAGE SHUTDOWN

A high voltage variable-output regulator may be constructed using the LM340 after the idea illustrated in section 7 and drawn in *Figure 23*. The principal inconvenience is that the voltage across the regulator must be limited to maximum

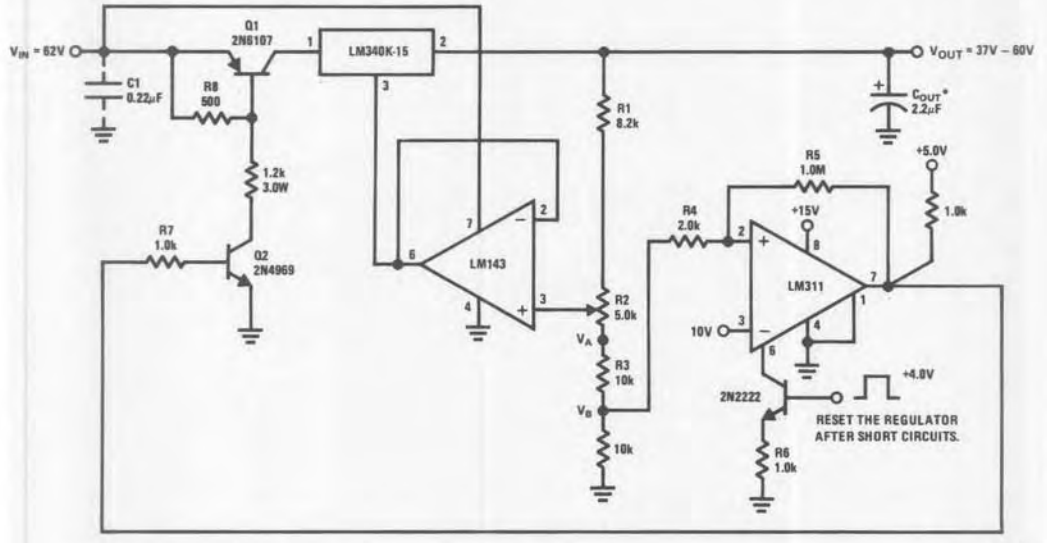


*Required if the regulator is located far from the power supply filter

**Head sink Q1 and the LM340

TL/H/7413–22

FIGURE 22. Electronic Shutdown Circuit



*Solid tantalum

TL/H/7413–23

FIGURE 23. Variable High Voltage Regulator with Shortcircuit and Overvoltage Protection

rating of the device, the higher the applied input voltage the higher must be lifted the ground pin of the LM340. Therefore the range of the variable output is limited by the supply voltage limit of the operational amplifier and the maximum voltage allowed across the regulator. An estimation of this range is given by:

$$V_{OUT\ MAX} - V_{OUT\ MIN} = V_{SUPPLY\ MAX340} - V_{NOMINAL340} - 2.0V \quad (13\text{-}1)$$

Examples:

LM340-15: $V_{OUTMAX} - V_{OUTMIN} = 35 - 15 - 2 = 18V$

Figure 23 illustrates the above considerations. Even though the LM340 is by itself short circuit protected, when the output drops, also V_A drops and the voltage difference across the device increases. If it exceeds 35V the pass transistor internal to the regulator will breakdown, as explained in section 11. To remedy this, an over-voltage shutdown is included in the circuit. When the output drops the comparator switches low, pulls down the base Q2 thus opening the switch Q1, and shutting down the LM340. Once the short circuit has been removed the LM311 must be activated through the strobe to switch high and close Q1, which will start the regulator again. The additional voltages required to operate the comparator may be taken from the 62V since the LM311 has a certain ripple rejection and the reference voltage (pin 3) may have a superimposed small ac signal. The typical load regulation can be computed from equation 6-1.

BIBLIOGRAPHY

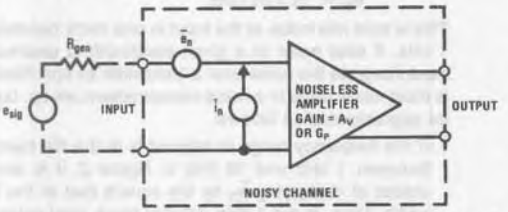
1. AN-42: *"IC Provides on Card Regulation for Logic Circuits."*

2. Carl T. Nelson: *"Power distribution and regulation can be simple, cheap and rugged."* EDN, February 20, 1973.

It's really all very simple—once you understand it. Then, here's the inside story on noise for those of us who haven't been designing low noise amplifiers for ten years.

You hear all sorts of terms like signal-to-noise ratio, noise figure, noise factor, noise voltage, noise current, noise power, noise spectral density, noise per root Hertz, broadband noise, spot noise, shot noise, flicker noise, excess noise, 1/F noise, fluctuation noise, thermal noise, white noise, pink noise, popcorn noise, bipolar spike noise, low noise, no noise, and loud noise. No wonder not everyone understands noise specifications.

In a case like noise, it is probably best to sort it all out from the beginning. So, in the beginning, there was noise; and then there was signal. The whole idea is to have the noise very small compared to the signal; or, conversely, we desire a high signal-to-noise ratio S/N. Now it happens that S/N is related to noise figure NF, noise factor F, noise power, noise voltage $\bar{e}_n$, and noise current $\bar{i}_n$. To simplify matters, it also happens that any noisy channel or amplifier can be completely specified for noise in terms of two noise generators $\bar{e}_n$ and $\bar{i}_n$ as shown in *Figure 1*.



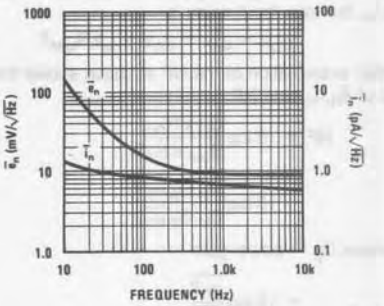
TL/H/7414–1

FIGURE 1. Noise Characterization of Amplifier

All we really need to understand are NF, $\bar{e}_n$, and $\bar{i}_n$. So here is a rundown on these three.

NOISE VOLTAGE, $\bar{e}_n$, or more properly, EQUIVALENT SHORT-CIRCUIT INPUT RMS NOISE VOLTAGE is simply that noise voltage which would appear to originate at the input of the noiseless amplifier if the input terminals were shorted. It is expressed in nanovolts per root Hertz nV/$\sqrt{\text{Hz}}$ at a specified frequency, or in microvolts in a given frequency band. It is determined or measured by shorting the input terminals, measuring the output rms noise, dividing by amplifier gain, and referencing to the input. Hence the term, equivalent noise voltage. An output bandpass filter of known characteristic is used in measurements, and the measured value is divided by the square root of the bandwidth $\sqrt{B}$ if data is to be expressed per unit bandwidth or per root Hertz. The level of $\bar{e}_n$ is not constant over the frequency band; typically it increases at lower frequencies as shown in *Figure 2*. This increase is 1/f NOISE.

NOISE CURRENT, $\bar{i}_n$, or more properly, EQUIVALENT OPEN-CIRCUIT RMS NOISE CURRENT is that noise which



TL/H/7414–2

FIGURE 2. Noise Voltage and Current for an Op Amp

occurs apparently at the input of the noiseless amplifier due only to noise currents. It is expressed in picoamps per root Hertz pA/$\sqrt{\text{Hz}}$ at a specified frequency or in nanoamps in a given frequency band. It is measured by shunting a capacitor or resistor across the input terminals such that the noise current will give rise to an additional noise voltage which is $\bar{i}_n \times R_{in}$ (or X_{cin}). The output is measured, divided by amplifier gain, referenced to input, and that contribution known to be due to $\bar{e}_n$ and resistor noise is appropriately subtracted from the total measured noise. If a capacitor is used at the input, there is only $\bar{e}_n$ and $\bar{i}_n X_{cin}$. The $\bar{i}_n$ is measured with a bandpass filter and converted to pA$\sqrt{\text{Hz}}$ if appropriate; typically it increases at lower frequencies for op amps and bipolar transistors, but increases at higher frequencies for field-effect transistors.

NOISE FIGURE, NF is the logarithm of the ratio of input signal-to-noise and output signal-to-noise.

$$NF = 10 \text{ Log } \frac{(S/N)_{in}}{(S/N)_{out}} \quad (1)$$

where: S and N are power or (voltage)^2 levels

This is measured by determining the S/N at the input with no amplifier present, and then dividing by the measured S/N at the output with signal source present.

The values of R_{gen} and any X_{gen} as well as frequency must be known to properly express NF in meaningful terms. This is because the amplifier $\bar{i}_n \times Z_{gen}$ as well as R_{gen} itself produces input noise. The signal source in *Figure 1* contains some noise. However e_{sig} is generally considered to be noise free and input noise is present as the THERMAL NOISE of the resistive component of the signal generator impedance R_{gen}. This thermal noise is WHITE in nature as it contains constant NOISE POWER DENSITY per unit bandwidth. It is easily seen from Equation 2 that the $\overline{e_n^2}$ has the units V^2/Hz and that ($\bar{e}_n$) has the units V/$\sqrt{\text{Hz}}$

$$\overline{e_R^2} = 4kTRB \quad (2)$$

where: T is the temperature in °K

R is resistor value in Ω

B is bandwidth in Hz

k is Boltzman's constant

RELATION BETWEEN $\bar{e}_n$, $\bar{i}_n$, NF

Now we can examine the relationship between $\bar{e}_n$ and $\bar{i}_n$ at the amplifier input. When the signal source is connected, the $\bar{e}_n$ appears in series with the e_{sig} and $\bar{e}_R$. The $\bar{i}_n$ flows through R_{gen} thus producing another noise voltage of value $\bar{i}_n \times R_{gen}$. This noise voltage is clearly dependent upon the value of R_{gen}. All of these noise voltages add at the input in rms fashion; that is, as the square root of the sum of the squares. Thus, neglecting possible correlation between $\bar{e}_n$ and $\bar{i}_n$, the total input noise is

$$\overline{e_N^2} = \overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2} R_{gen}^2 \qquad (3)$$

Further examination of the NF equation shows the relationship of $\bar{e}_N$, $\bar{i}_n$, and NF.

$$NF = 10 \log \frac{S_{in} \times N_{out}}{S_{out} \times N_{in}}$$

$$= 10 \log \frac{S_{in}\, G_p\, \overline{e_N^2}}{S_{in}\, G_p\, \overline{e_R^2}}$$

where: G_p = power gain

$$= 10 \log \frac{\overline{e_N^2}}{\overline{e_R^2}}$$

$$= 10 \log \frac{\overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2} R_{gen}^2}{\overline{e_R^2}}$$

$$NF = 10 \log \left(1 + \frac{\overline{e_n^2} + \overline{i_n^2} R_{gen}^2}{\overline{e_R^2}}\right) \qquad (4)$$

Thus, for small R_{gen}, noise voltage dominates; and for large R_{gen}, noise current becomes important. A clear advantage accrues to FET input amplifiers, especially at high values of R_{gen}, as the FET has essentially zero $\bar{i}_n$. Note, that for an NF value to have meaning, it must be accompanied by a value for R_{gen} as well as frequency.

CALCULATING TOTAL NOISE, $\bar{e}_N$

We can generate a plot of $\bar{e}_N$ for various values of R_{gen} if noise voltage and current are known vs frequency. Such a graph is shown in *Figure 3* drawn from *Figure 2*. To make this plot, the thermal noise $\bar{e}_R$ of the input resistance must be calculated from Equation 2 or taken from the graph of *Figure 4*. Remember that each term in Equation 3 must be squared prior to addition, so the data from *Figure 4* and from *Figure 2* is squared. A sample of this calculation follows:

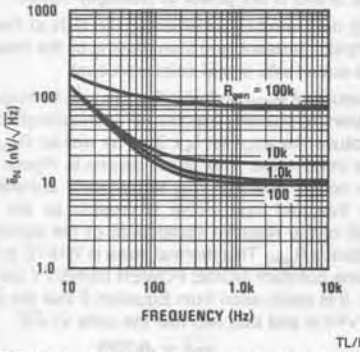


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FIGURE 3. Total Noise for the Op Amp of *Figure 2*

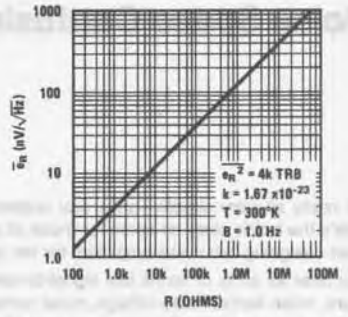

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FIGURE 4. Thermal Noise of Resistor

Example 1: Determine total equivalent input noise per unit bandwidth for an amplifier operating at 1 kHz from a source resistance of 10 kΩ. Use the data from *Figures 2* and *4*.

1. Read $\bar{e}_R$ from *Figure 4* at 10 kΩ; the value is 12 nV/$\sqrt{Hz}$.
2. Read $\bar{e}_n$ from *Figure 2* at 1 kHz; the value is 9.5 nV/$\sqrt{Hz}$.
3. Read $\bar{i}_n$ from *Figure 2* at 1 kHz; the value is 0.68 pA/$\sqrt{Hz}$. Multiply by 10 kΩ to obtain 6.8 nV/$\sqrt{Hz}$.
4. Square each term individually, and enter into Equation 3.

$$\bar{e}_N = \sqrt{\overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2} R_{gen}^2}$$

$$= \sqrt{9.5^2 + 12^2 + 6.8^2} \quad = \sqrt{279}$$

$$\bar{e}_N = 16.7 \text{ nV}/\sqrt{Hz}$$

This is total rms noise at the input in one Hertz bandwidth at 1 kHz. If total noise in a given bandwidth is desired, one must integrate the noise over a bandwidth as specified. This is most easily done in a noise measurement set-up, but may be approximated as follows:

1. If the frequency range of interest is in the flat band; i.e., between 1 kHz and 10 kHz in *Figure 2*, it is simply a matter of multiplying $\bar{e}_N$ by the square root of the bandwidth. Then, in the 1 kHz–10 kHz band, total noise is

$$\bar{e}_N = 16.7\sqrt{9000}$$

$$= 1.59\ \mu V$$

2. If the frequency band of interest is not in the flat band of *Figure 2*, one must break the band into sections, calculating average noise in each section, squaring, multiplying by section bandwidth, summing all sections, and finally taking square root of the sum as follows:

$$\bar{e}_N = \sqrt{\overline{e_R^2} B + \sum_1^i (\overline{e_n^2} + \overline{i_n^2} R_{gen}^2)_i B_i} \qquad (5)$$

where: i is the total number of sub-blocks.

For most purposes a sub-block may be one or two octaves. Example 2 details such a calculation.

Example 2: Determine the rms noise level in the frequency band 50 Hz to 10 kHz for the amplifier of *Figure 2* operating from R_{gen} = 2k.

1. Read $\bar{e}_R$ from *Figure 4* at 2k, square the value, and multiply by the entire bandwidth. Easiest way is to construct a table as shown on the next page.
2. Read the median value of $\bar{e}_n$ in a relatively small frequency band, say 50 Hz–100 Hz, from *Figure 2*, square it and enter into the table.

3. Read the median value of $\bar{i}_n$ in the 50 Hz–100 Hz band from *Figure 2*, multiply by R_{gen} = 2k, square the result and enter in the table.
4. Sum the squared results from steps 2 and 3, multiply the sum by Δf = 100–50 = 50 Hz, and enter in the table.
5. Repeat steps 2–4 for band sections of 100 Hz–300 Hz, 300 Hz–1000 Hz and 1 kHz–10 kHz. Enter results in the table.
6. Sum all entires in the last column, and finally take the square root of this sum for the total rms noise in the 50 Hz–10,000 Hz band.
7. Total $\bar{e}_n$ is 1.62 μV in the 50 Hz–10,000 Hz band.

CALCULATING S/N and NF

Signal-to-noise ratio can be easily calculated from known signal levels once total rms noise in the band is determined. Example 3 shows this rather simple calculation from Equation 6 for the data of Example 2.

$$S/N = 20 \log \frac{e_{sig}}{\bar{e}_N} \qquad (6)$$

Example 3: Determine S/N for an rms e_{sig} = 4 mV at the input to the amplifier operated in Example 2.

1. RMS signal is e_{sig} = 4 mV
2. RMS noise from Example 2 is 1.62 μV
3. Calculate S/N from Equation 6

$$S/N = 20 \log \frac{4\ mV}{1.62\ \mu V}$$

$$= 20 \log (2.47 \times 10^3)$$

$$= 20 (\log 10^3 + \log 2.47)$$

$$= 20 (3 + 0.393)$$

$$S/N = 68\ dB$$

It is also possible to plot NF vs frequency at various R_{gen} for any given plot of $\bar{e}_n$ and $\bar{i}_n$. However there is no specific all-purpose conversion plot relating NF, $\bar{e}_n$, $\bar{i}_n$, R_{gen} and f. If either $\bar{e}_n$ or $\bar{i}_n$ is neglected, a reference chart can be constructed. *Figure 5* is such a plot when only $\bar{e}_n$ is considered. It is useful for most op amps when R_{gen} is less than about 200Ω and for FETs at any R_{gen} (because there is no significant $\bar{i}_n$ for FETs), however actual NF for op amps with R_{gen} > 200Ω is higher than indicated on the chart. The graph of *Figure 5* can be used to find spot NF if $\bar{e}_n$ and R_{gen} are known, or to find $\bar{e}_n$ if NF and R_{gen} are known. It can also be used to find max R_{gen} allowed for a given max NF when $\bar{e}_n$ is known. In any case, values are only valid if $\bar{i}_n$ is negligible and at the specific frequency of interest for NF and $\bar{e}_n$, and for 1 Hz bandwidth. If bandwidth increases, the plot is valid so long as $\bar{e}_n$ is multiplied by $\sqrt{B}$.

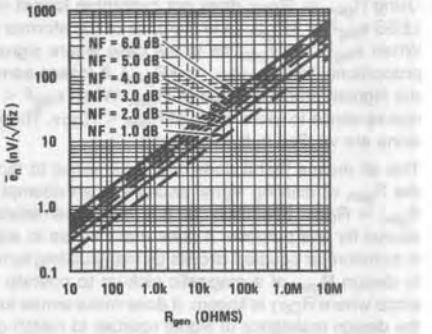

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FIGURE 5. Spot NF vs R_{gen} when Considering *Only* $\bar{e}_n$ and $\bar{e}_R$ (not valid when $\bar{i}_n$ R_{gen} is significant)

THE NOISE FIGURE MYTH

Noise figure is easy to calculate because the signal level need not be specified (note that e_{sig} drops out of Equation 4). Because NF is so easy to handle in calculations, many designers tend to lose sight of the fact that signal-to-noise ratio $(S/N)_{out}$ is what is important in the final analysis, be it an audio, video, or digital data system. One can, in fact, choose a high R_{gen} to reduce NF to near zero if $\bar{i}_n$ is very small. In this case $\bar{e}_R$ is the major source of noise, overshadowing $\bar{e}_n$ completely. The result is very low NF, but very low S/N as well because of very high noise. Don't be fooled into believing that low NF means low noise *per se*!

Another term is worth considering, that is optimum source resistance R_{OPT}. This is a value of R_{gen} which produces the lowest NF in a given system. It is calculated as

$$R_{OPT} = \frac{\bar{e}_n}{\bar{i}_n} \qquad (7)$$

This has been arrived at by differentiating Equation 4 with respect to R_{gen} and equating it to zero (see Appendix). *Note that this does not mean lowest noise.*

For example, using *Figure 2* to calculate R_{OPT} at say 600 Hz,

$$R_{OPT} = \frac{10\ nV}{0.7\ pA} = 14\ k\Omega$$

TABLE I. Noise Calculations for Example 2

B (Hz)	Δf (Hz)	$\bar{e}_n^2$ (nV/Hz)	$+ \bar{i}_n^2 R_{gen}^2$			SUM x Δf	=	(nV^2)
50–100	50	$(20)^2 = 400$	$(8.7 \times 2.0k)^2$	=	302	702* x 50		35,000
100–300	200	$(13)^2 = 169$	$(8 \times 2.0k)^2$	=	256	425 x 200		85,000
300–1000	700	$(10)^2 = 100$	$(7 \times 2.0k)^2$	=	196	296 x 700		207,000
1.0k–10k	9000	$(9)^2 = 81$	$(6 \times 2.0k)^2$	=	144	225 x 9000		2,020,000
50–10,000	9950	$\bar{e}_R^2 = (5.3)^2 = 28$				28 x 9950		279,000

Total $\bar{e}_N = \sqrt{2{,}626{,}000}$ = 1620 nV = 1.62 μV

*The units are as follows: $(20\ nV/\sqrt{Hz})^2$ = 400 $(nV)^2/Hz$

$(8.7\ pA/\sqrt{Hz} \times 2.0\ k\Omega)^2 = (17.4\ nA/\sqrt{Hz})^2$ = 302 $(nV)^2/Hz$

Sum = 702 $(nV)^2/Hz$ x 50 Hz = 35,000 $(nV)^2$

Then note in *Figure 3*, that $\bar{e}_N$ is in the neighborhood of 20 nV/$\sqrt{Hz}$ for R_{gen} of 14k, while $\bar{e}_N$ = 10 nV/$\sqrt{Hz}$ for R_{gen} = 0–100Ω. STOP! Do not pass GO. Do not be fooled. Using $R_{gen} = R_{OPT}$ does not guarantee lowest noise UNLESS $e_{sig}^2 = kR_{gen}$ as in the case of transformer coupling. When $e_{sig}^2 > kR_{gen}$, as is the case where signal level is proportional to R_{gen} ($e_{sig} = kR_{gen}$), it makes sense to use the highest practical value of R_{gen}. When $e_{sig}^2 < kR_{gen}$, it makes sense to use a value of $R_{gen} < R_{OPT}$. These conclusions are verified in the Appendix.

This all means that it does not make sense to tamper with the R_{gen} of existing signal sources in an attempt to make $R_{gen} = R_{OPT}$. Especially, do not add series resistance to a source for this purpose. It does make sense to adjust R_{gen} in transformer coupled circuits by manipulating turns ratio or to design R_{gen} of a magnetic pick-up to operate with preamps where R_{OPT} is known. It does make sense to increase the design resistance of signal sources to match or exceed R_{OPT} so long as the signal voltage increases with R_{gen} in at least the ratio $e_{sig}^2 \propto R_{gen}$. It does not necessarily make sense to select an amplifier with R_{OPT} to match R_{gen} because one amplifier operating at $R_{gen} = R_{OPT}$ may produce lower S/N than another (quieter) amplifier operating with $R_{gen} \neq R_{OPT}$.

With some amplifiers it is possible to adjust R_{OPT} over a limited range by adjusting the first stage operating current (the National LM121 and LM381 for example). With these, one might increase operating current, varying R_{OPT}, to find a condition of minimum S/N. Increasing input stage current decreases R_{OPT} as $\bar{e}_n$ is decreased and $\bar{i}_n$ is simultaneously increased.

Let us consider one additional case of a fairly complex nature just as a practical example which will point up some factors often overlooked.

Example 4: Determine the S/N *apparent to the ear* of the amplifier of *Figure 2* operating over 50-12,800 Hz when driven by a phonograph cartridge exhibiting R_{gen} = 1350Ω, L_{gen} = 0.5H, and average e_{sig} = 4.0 mVrms. The cartridge is to be loaded by 47k as in *Figure 6*. This is equivalent to using a Shure V15, Type 3 for average level recorded music.

1. Choose sectional bandwidths of 1 octave each, these are listed in the following table.
2. Read $\bar{e}_n$ from *Figure 2* as average for each octave and enter in the table.
3. Read $\bar{i}_n$ from *Figure 2* as average for each octave and enter in the table.
4. Read $\bar{e}_R$ for the R_{gen} = 1350Ω from *Figure 4* and enter in the table.
5. Determine the values of Z_{gen} at the midpoint of each octave and enter in the table.
6. Determine the amount of $\bar{e}_R$ which reaches the amplifier input; this is

$$\bar{e}_R \frac{R1}{R1 + Z_{gen}}$$

7. Read the noise contribution $\bar{e}_{47k}$ of R1 = 47k from *Figure 4*.
8. Determine the amount of $\bar{e}_{47K}$ which reaches the amplifier input; this is

$$\bar{e}_{47k} \frac{Z_{gen}}{R1 + Z_{gen}}$$

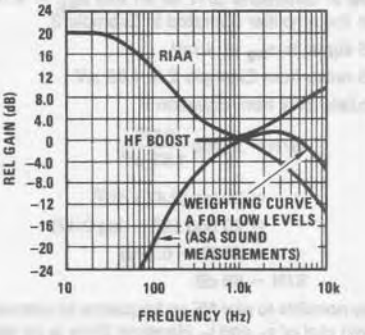

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FIGURE 7. Relative Gain for RIAA, ASA Weighting A, and H-F Boost Curves

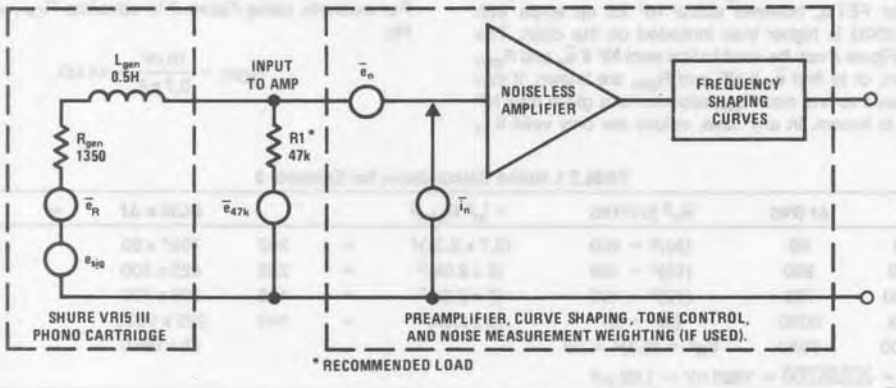

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FIGURE 6. Phono Preamp Noise Sources

9. Determine the effective noise contributed by $\bar{i}_n$ flowing through the parallel combination of R1 and Z_{gen}. This is
$$\bar{i}_n \frac{Z_{gen}\,R1}{Z_{gen} + R1}$$
10. Square all noise voltage values resulting from steps 2, 6, 8 and 9; and sum the squares.
11. Determine the relative gain at the midpoint of each octave from the RIAA playback response curve of *Figure 7*.
12. Determine the relative gain at these same midpoints from the A weighted response curve of *Figure 7* for sound level meters (this roughly accounts for variations in human hearing).
13. Assume a tone control high frequency boost of 10 dB at 10 kHz from *Figure 7*. Again determine relative response of octave midpoints.
14. Multiply all relative gain values of steps 11-13 and square the result.
15. Multiply the sum of the squared values from step 10 by the resultant relative gain of step 14 and by the bandwidth in each octave.
16. Sum all the values resultant from step 15, and find the square root of the sum. This is the total audible rms noise apparent in the band.
17. Divide e_{sig} = 4 mV by the total noise to find S/N = 6.95 dB.

STEPS FOR EXAMPLE

1	Frequency Band (Hz)	50–100	100–200	200–400	400–800	800–1600	1.6–3.2k	3.2–6.4k	6.4–12.8k
	Bandwidth, B (Hz)	50	100	200	400	800	1600	3200	6400
	Bandcenter, f (Hz)	75	150	300	600	1200	2400	4800	9600
5	Z_{gen} at f (Ω)	1355	1425	1665	2400	4220	8100	16k	32k
	Z_{gen} R1 (Ω)	1300	1360	1600	2270	3900	6900	11.9k	19k
	$Z_{gen}/R1 + Z_{gen})$	0.028	0.030	0.034	0.485	0.082	0.145	0.255	0.400
	$R1/(R1 + Z_{gen})$	0.97	0.97	0.97	0.95	0.92	0.86	0.74	0.60
11	RIAA Gain, A_{RIAA}	5.6	3.1	2.0	1.4	1	0.7	0.45	0.316
12	Corr for Hearing, A_A	0.08	0.18	0.45	0.80	1	1.26	1	0.5
13	H-F Boost, A_{boost}	1	1	1	1	1.12	1.46	2.3	3.1
14	Product of Gains, A	0.45	0.55	0.9	1.12	1.12	1.28	1.03	0.49
	A^2	0.204	0.304	0.81	1.26	1.26	1.65	1.06	0.241
4	$\bar{e}_R$ (nV/√Hz)	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5
7	$\bar{e}_{47k}$ (nV/√Hz)	29	29	29	29	29	29	29	29
3	$\bar{i}_n$ (pA/√Hz)	0.85	0.80	0.77	0.72	0.65	0.62	0.60	0.60
2	$\bar{e}_n$ (nV/√Hz)	19	14	11	10	9.5	9	9	9
9	$\bar{e}_1 = \bar{i}_n (Z_{gen}\,R1)$	1.1	1.09	1.23	1.63	2.55	4.3	7.1	11.4
6	$\bar{e}_2 = \bar{e}_R\,R1/(R1 + Z_{gen})$	4.35	4.35	4.35	4.25	4.15	3.86	3.33	2.7
8	$\bar{e}_3 = \bar{e}_{47k}\,Z_{gen}/(R1 + Z_{gen})$	0.81	0.87	0.98	1.4	2.4	4.2	7.4	11.6
10	$\overline{e_n^2}$	360	195	121	100	90	81	81	81
	$\overline{e_1^2}$ (from $\bar{i}_n$)	1.21	1.2	1.5	2.65	6.5	18.5	50	150
	$\overline{e_2^2}$ (from $\bar{e}_R$)	19	19	19	18	17	15	11	7.2
	$\overline{e_3^2}$ (from $\bar{e}_{47k}$)	0.65	0.76	0.96	2	5.8	18	55	135
	$\Sigma\overline{e_n^2}$ (nV²/Hz)	381	216	142	122	120	133	147	373
15	BA^2 (Hz)	10.2	30.4	162	504	1010	2640	3400	1550
	$BA^2\Sigma\overline{e2}$ (nV²)	3880	6550	23000	61500	121000	350000	670000	580000

16 $\Sigma(\overline{e_{n_i}^2} + \overline{e_{1_i}^2} + \overline{e_{2_i}^2} + \overline{e_{3_i}^2})\,B_iA_i^2 = 1{,}815{,}930\ nV^2$

$\bar{e}_N = \sqrt{\Sigma} = 1.35\ \mu V$

17 $S/N = 20 \log (4.0\ mV/1.35\ \mu V) = 69.5\ dB$

ployed in the example. If it were not for the A curve attenuation at low frequencies, the $\overline{e}_n$ would add a very important contribution below 200 Hz. This would be due to the RIAA boost at low frequency. As it stands, 97% of the 1.35 μV would occur in the 800–12.8 kHz band alone, principally because of the high frequency boost and the A measurement curve. If the measurement were made without either the high frequency boost or the A curve, the $\overline{e}_n$ would be 1.25 μV. In this case, 76% of the total noise would arise in the 50 Hz–400 Hz band alone. If the A curve were used, but the high-frequency boost were deleted, $\overline{e}_n$ would be 0.91 μV; and 94% would arise in the 800–12, 800 Hz band alone.

The three different methods of measuring would only produce a difference of +3.5 dB in overall S/N, however the prime sources of the largest part of the noise and the frequency character of the noise can vary greatly with the test or measurement conditions. It is, then, quite important to know the method of measurement in order to know which individual noise sources in *Figure 6* must be reduced in order to significantly improve S/N.

2. Select on the basis of low values of $\overline{e}_n$ and especially $\overline{i}_n$ if R_{gen} is over about a thousand Ω.
3. Don't select on the basis of NF or R_{OPT} in most cases. NF specs are all right so long as you know precisely how to use them and so long as they are valid over the frequency band for the R_{gen} or Z_{gen} with which you must work.
4. Be sure to (root) sum all the noise sources $\overline{e}_n$, $\overline{i}_n$ and $\overline{e}_R$ in your system over appropriate bandwidth.
5. The higher frequencies are often the most important unless there is low frequency boost or high frequency attenuation in the system.
6. Don't forget the filtering effect of the human ear in audio systems. Know the eventual frequency emphasis or filtering to be employed.

APPENDIX I

Derivation of R_{OPT}:

$$NF = 10 \log \frac{\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R_{gen}^2}{\overline{e_R^2}}$$

$$10 \log \left(1 + \frac{\overline{e_n^2} + \overline{i_n^2} R_{gen}^2}{\overline{e_R^2}}\right)$$

$$\frac{\delta NF}{\delta R} = \frac{0.435}{(4\ kTRB)^2} \frac{4\ kTRB\ (2R\ \overline{i_n^2}) - (\overline{e_n^2} + \overline{i_n^2} R^2) 4\ kTB}{1 + (\overline{e_n^2} + \overline{i_n^2} R^2)/4\ kTRB}$$

where: $R = R_{gen}$

Set this = 0, and

$$4\ kTRB(2R\ \overline{i_n^2}) = 4\ kTB\ (\overline{e_n^2} + \overline{i_n^2} R^2)$$

$$2\ \overline{i_n^2} R^2 = \overline{e_n^2} + \overline{i_n^2} R^2$$

$$\overline{i_n^2} R^2 = \overline{e_n^2}$$

$$R^2 = \overline{e_n^2}/\overline{i_n^2}$$

$$R_{OPT} = \frac{\overline{e}_n}{\overline{i}_n}$$

APPENDIX II

Selecting R_{gen} for highest S/N.

$$S/N = \frac{e_{sig}^2}{B(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2)}$$

For S/N to increase with R,

$$\frac{\delta S/N}{\delta R} > 0$$

$$\frac{\delta S/N}{\delta R} = \frac{2e_{sig}\ (\delta e_{sig}/\delta R)\ (\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2) - e_{sig}^2\ (4\ kT + 2\ \overline{i_n^2} R)}{B(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2)^2}$$

APPENDIX II (Continued)

If we set > 0, then

$$2\,(\delta e_{sig}/\delta\,R)\,(\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\,R^2) > e_{sig}\,(4\,kT + 2\,\overline{i_n{}^2}\,R)$$

For $e_{sig} = k_1\sqrt{R}$, $\delta e_{sig}/\delta R = \dfrac{k_1}{2\sqrt{R}}$

$$(2\,k_1/2\sqrt{R})\,(\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\,R^2) > k_1\sqrt{R}\,(4\,kT + 2\,\overline{i_n{}^2}\,R)$$

$$\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\,R^2 > 4\,kTR + 2\,\overline{i_n{}^2}\,R^2$$

$$\overline{e_n{}^2} > \overline{i_n{}^2}\,R^2$$

$$R < \overline{e}_n/\overline{i}_n$$

Therefore S/N increases with R_{gen} so long as $R_{gen} \leq R_{OPT}$

For $e_{sig} = k_1 R$, $\delta e_{sig}/\delta R = k_1$

$$2\,k_1\,(\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\,R^2) > k_1 R\,(4\,kT + 2\,\overline{i_n{}^2}\,R)$$

$$2\,\overline{e_R{}^2} + 2\,\overline{e_n{}^2} + 2\,\overline{i_n{}^2}\,R^2 > 4\,kTR + 2\,\overline{i_n{}^2}\,R^2$$

$$\overline{e_R{}^2} + 2\,\overline{e_n{}^2} > 0$$

Then S/N increases with R_{gen} for any amplifier.

For any $e_{sig} < k_1\sqrt{R}$, an optimum R_{gen} may be determined. Take, for example, $e_{sig} = k_1 R^{0.4}$, $\delta e_{sig}/\delta R = 0.4 k_1 R^{-0.6}$

$$(0.8\,k_1/R^{0.6})\,(\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\,R^2) > k_1\,R^{0.4}\,(4\,kT + 2\,\overline{i_n{}^2}\,R)$$

$$0.8\,\overline{e_R{}^2} + 0.8\,\overline{e_n{}^2} + 0.8\,\overline{i_n{}^2}\,R^2 > 4\,kTR + 2\,\overline{i_n{}^2}\,R^2$$

$$0.8\,\overline{e_n{}^2} > 0.2\,\overline{e_R{}^2} + 1.2\,\overline{i_n{}^2}\,R^2$$

Then S/N increases with R_{gen} until

$$0.25\,\overline{e_R{}^2} + 1.5\,\overline{i_n{}^2}\,R^2 = \overline{e_n{}^2}$$