

1. Major Characteristics and Features of the Fairchild Power Switch (FPS) IC

- Current mode control
- Universal input voltage
- Latch up or auto restart shutdown options
- Matched gate driver
- Low power consumption : low I_{start} and I_{op}
- Over voltage protection (OVP) built-in
- Over current protection (OCP) built-in
- Over load protection (OLP) built-in
- Over temperature protection (TSD) built in
- Minimization of manufacturing defects through V_{CC} surge protection and built in diode reinforcement

1.1 Starting resistance design and UVLO

For a universal input supply the input voltage range is 85 to 265V_{AC}. When V_{ac} is a minimum, the maximum value for the start up resistor is calculated as follows:

The value calculated is the limit value. i.e. at minimum V_{ac} , V_{cc} it will only just reach 15V.

$$R_{start} = \frac{85\sqrt{2} - 15}{170\mu A} = 600k\Omega$$

The starting current through the start up resistor charges the capacitor on the Fairchild Power Switch(FPS) V_{cc} terminal. When V_{cc} becomes greater than the starting voltage the Fairchild Power Switch(FPS) built in MOSFET starts to switch, at which point the current in the Fairchild Power Switch (FPS) control IC abruptly increases to 7mA. The start up resistor cannot supply this current and therefore, after the start, the auxiliary winding of the transformer supplies most of the power to the Fairchild Power Switch(FPS). The size of the power capacitor on the V_{cc} terminal is important and not totally arbitrary: if the capacitor is too large, the starting time can be delayed. Generally, 10mF is about right. Figure 2 describes this operation. Although V_{cc} needs to be set above 9V only during operation, be careful to set it so that the over voltage protection (OVP) does not trigger during an over load condition. An appropriate value for V_{cc} at full load is about 18 - 20V and 13 - 14V at no load.

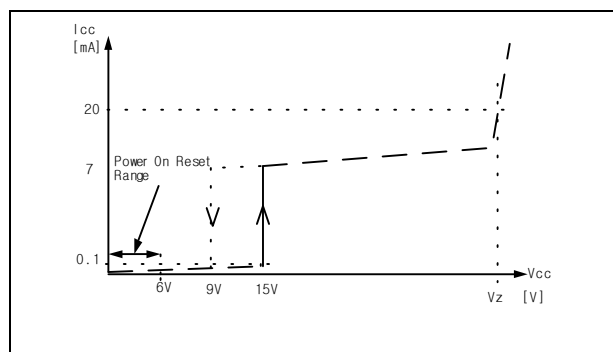


Figure 2. Start up waveform.

1.2 Fairchild Power Switch(FPS) protection circuitry

The Fairchild Power Switch(FPS) has several self protection circuits that operate without additional external components. This increases reliability without increasing cost. Note that when a protection circuit comes on it can completely stop the SMPS until the mains power is removed and reconnected. This is (latch mode protection), or it can make the SMPS operate above the under voltage lockout level (UVLO) by unlatching the control voltage below the ULVO (i.e., auto restart mode protection). Fairchild power Switch(FPS) provides the whole line up of the devices, which have either auto restart mode or latch mode, so user can select either mode. Devices, which have auto restart mode, can be converted into latch mode by changing the value of external components.

1.2.1 Overload protection (OLP)

In the hierarchy of possible failures in an SMPS, an overload is different to a short circuited load. An overload is defined as a load that during normal operation exceeds some pre set load value. In this case the Fairchild Power Switch (FPS) overload protection circuit will stop the device. However, it is necessary to prevent the protection circuit from operating during a transient state. Hence, in determining whether the condition is a transient one or a true overload, the Fairchild Power Switch (FPS)'s protection circuit operates only after a specified interval. Overload shutdown is delayed. The operation is described as follows. Because the Fairchild Power Switch (FPS) uses current mode control, there is a set maximum current that limits maximum input power for a fixed input voltage. Now see the circuit diagram in Figure 3. If the output loading tries to go higher than the maximum allowed, V_o becomes less than the set voltage, and only a minimum current can flow through the LM431 reference. As a result, the secondary current of the opto coupler becomes almost zero. If all the current from the Fairchild Power Switch(FPS) 0.9mA current source flows through the

internal resistors ($2.5R + R = 3.5R$) connected to it through diode D2, V_{fb} becomes approximately 3V, and the 4mA current source starts to charge C_{fb} . Because the opto coupler secondary current is almost zero, V_{fb} continues to increase until it reaches 7.5V, at which time the Fairchild Power Switch(FPS) shuts down. The time delay to shutdown is dominated by the time required for the 4uA source to increase the C_{fb} voltage by a further 4.5V and is easily set when C_{fb} is 0.01uF, t_2 is about 11.2ms. when C_{fb} is 0.1uF, it is about 120ms. When this delay time is set, the Fairchild Power Switch(FPS) does not shutdown for most transient states. However, simply increasing C_{fb} to obtain a longer delay time can cause a problem, because C_{fb} is important in determining the response speed (dynamic response) of the SMPS.

Again, when V_{fb} exceeds 3V and the 4uA current starts to charge C_{fb} , V_{fb} will continue to increase until it reaches 7.5V. A resistor added between the Fairchild Power Switch (FPS) feedback pin (pin 4) and ground will lengthen the time to shutdown by allowing part of the delay current to pass through it. Our tests show that the shutdown time delay for the Fairchild Power Switch(FPS) with a 470pF C_{fb} and a 3.9MΩ resistor is about twice as longer than with C_{fb} alone. When V_{fb} is 7.5V, the current flowing through the 3.9MΩ resistor is approximately 1.9mA. The same results can be obtained using a Zener diode of about 3.9 - 4.7V in series with a capacitor, with these series-connected components shunted across C_{fb} as shown in Figure 3; the capacitor sets the shutdown time.

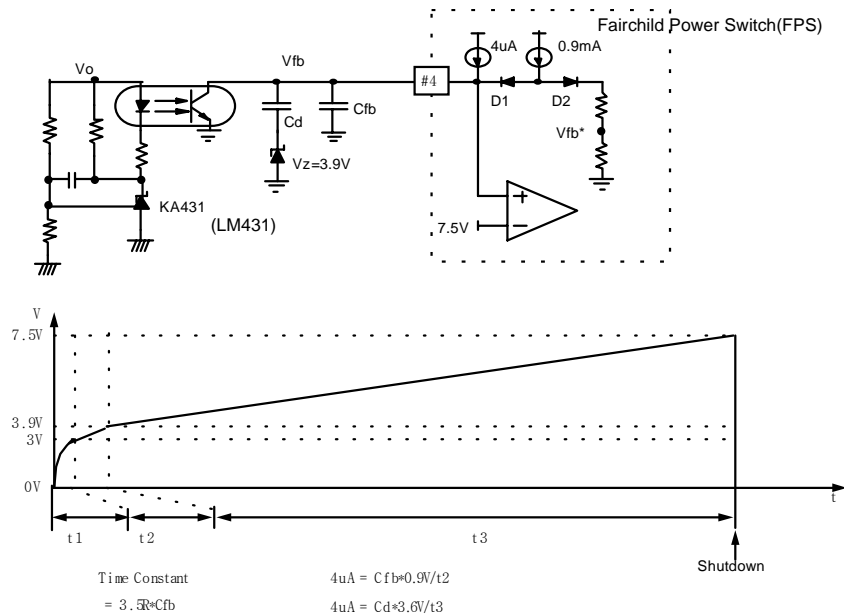


Figure 3. Fairchild Power Switch(FPS) delayed shutdown operation.

1.2.2 Over voltage protection (OVP)

The Fairchild Power Switch(FPS) has built-in self protection against feedback loop open and short circuits. When the feedback terminal shorts, as seen from the primary side, the feedback terminal voltage goes to zero, preventing switching from starting. If the feedback terminal opens, however, due to a malfunction in the secondary side feedback circuit such as a dry joint, the primary side would continue to switch with the set maximum current until the protection circuit came on. In such a case, the secondary side voltage would become much greater than the rated voltage. If

there were no protection against such a condition, the fuse could blow or, more seriously, a fire could start. Fire aside, however, any ICs connected to an unregulated secondary could be destroyed. To guard against such failures, the Fairchild Power Switch(FPS) contains an over voltage protection circuit. The Fairchild Power Switch(FPS), V_{cc} voltage is proportional to the output voltage. Therefore if the output voltage increases, so will the V_{cc} voltage. If V_{cc} tries to exceed 24V, the over voltage protection circuit operates. Therefore, it is appropriate to keep V_{cc} below 24V during normal operation.

1.2.3 Over current protection (OCP)

The I_{peak} control concept does not go beyond limiting the magnitude of the current during normal operation. The overcurrent protection feature (OCP) can prevent the destruction of the Fairchild Power Switch(FPS) in the event of a malfunction like a shorted secondary side rectifier diode or a load short. If not prevented from doing so, in such failure conditions a large current would flow through the Fairchild Power Switch(FPS) SenseFET. Tens of amperes would flow for the minimum turn on time of 600ns and destroy the Fairchild Power Switch(FPS). Instead, however, the OCP block senses this instantaneous current and latches, operating as follows. At the point when the SenseFet is switched on, the OCP block senses I_{peak}

through the sense resistor for $1\mu s$. After the OCP block turns on, the voltage across the sense resistor is compared to the preset voltage in the comparator. If the measured value of I_{peak} is greater than the threshold for longer than 200ns within the allowed comparison time of $1\mu s$, the comparator outputs a high signal, which latches the OCP. Figure 4 shows the OCP latch waveform. When there is a diode or load short, the Fairchild Power Switch(FPS) turns on for the minimum turn on time. In Figure 4, the 100ns delay after the 200ns maximum comparison period is the delay time to SenseFET gate off and is generated from the comparison of the voltage across the sense resistor.

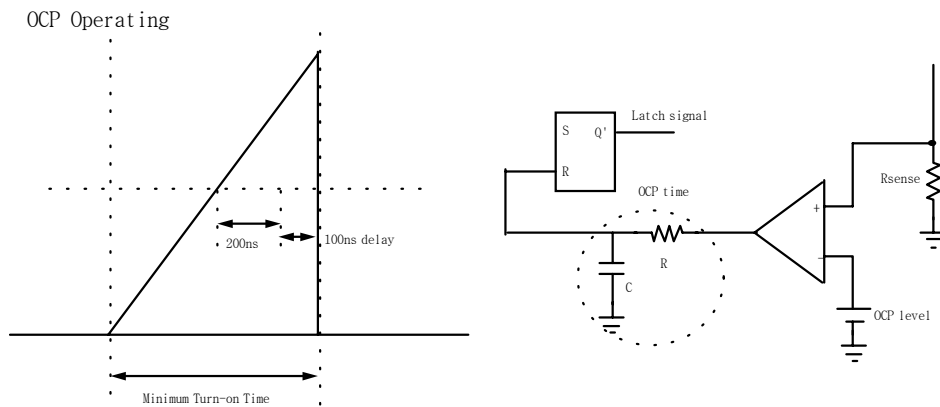


Figure 4. Operation of the over current protection block.

2. Multi output Flyback Converter Using a Fairchild Power Switch(FPS)

Most SMPSs have multiple outputs to accommodate the analog and digital sections of equipment such as TVs, monitors, VCRs, DVDs, and set top boxes. Design considerations for multi output SMPSs are described in the following sections. Their basic topology is shown in Figure 5. The output voltage and regulation are the most important parameters.

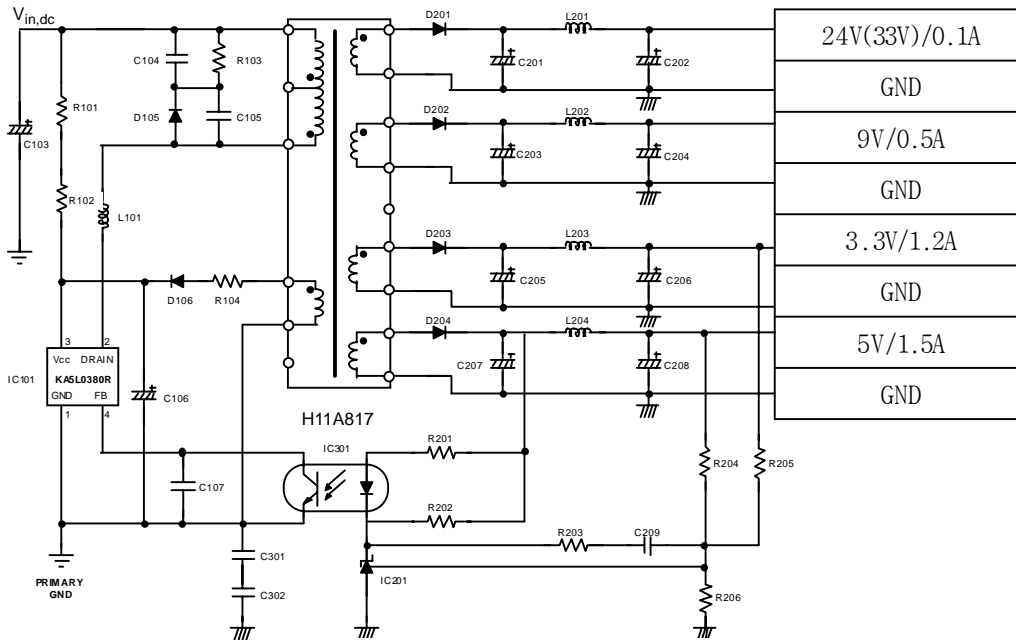


Figure 5. Basic SMPS topology.

2.1 Primary side feedback control

Figure 6 shows an SMPS using primary side feedback control. Note the absence of an opto coupler and shunt regulator

reference. The missing components lower the cost of the SMPS, but do so at the expense of output regulation, which, at more than $\pm 10\%$, is poor.

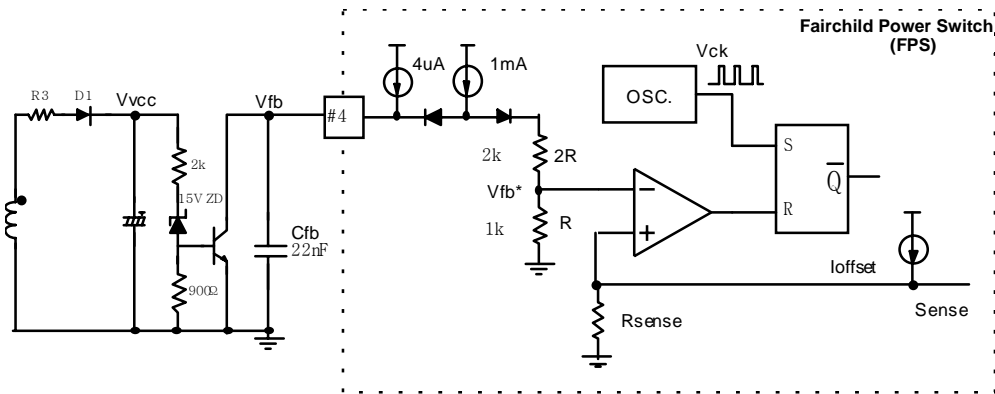


Figure 6. Primary side feedback control.

2.2 Secondary side feedback control

In Figure 7 the feedback loop is formed using a Zener diode on the secondary side. When the secondary side is so controlled, a system controlled output terminal has about a $\pm 5\%$ voltage tolerance; uncontrolled outputs have about a

$\pm 10\%$ tolerance, similar to that of the primary side feedback method. The Zener diode gives the control side voltage about a $\pm 2\%$ tolerance.

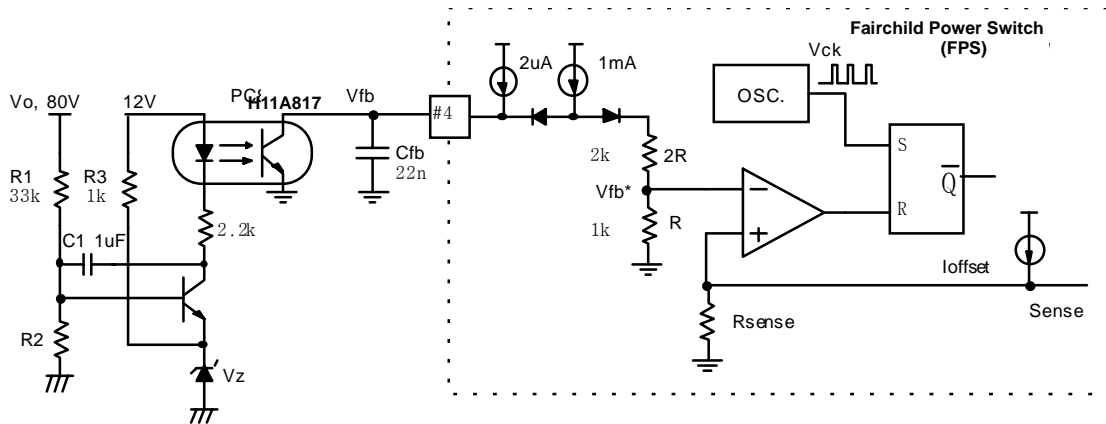


Figure 7. Feedback loop using a Zener diode in the secondary side control.

2.3 Opto coupler and shunt regulator

Current shunt regulators offer very good reference voltage with deviations of less than 1%. The system in Figure 8 uses

a shunt regulator; controlled voltages have less than $\pm 5\%$ tolerance while the other outputs have about $\pm 10\%$ tolerance.

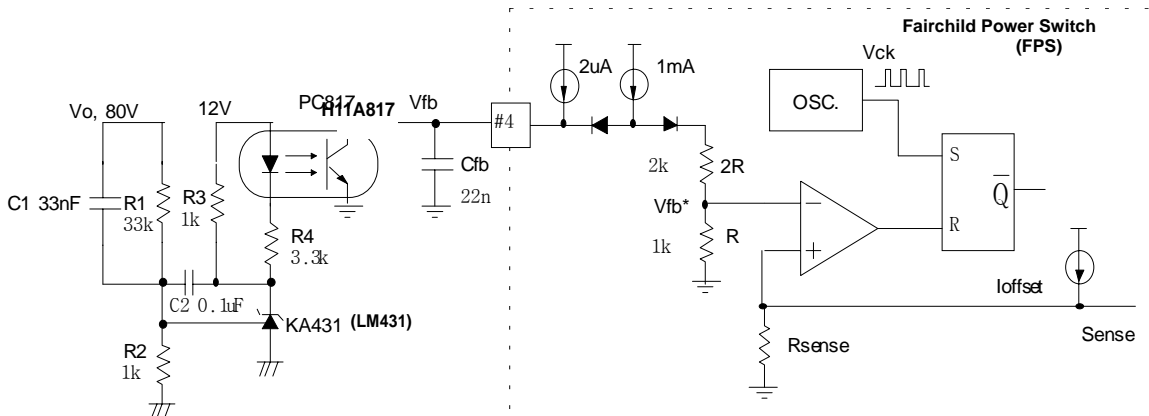


Figure 8. Feedback loop using a KA431(LM431) shunt regulator for tighter output regulation.

2.4 Two output control

Figure 9 shows a two output (5V and 3.3V) control circuit. Theoretically, this type of control should be able to precisely regulate two voltages, but the controlled voltages can interfere with one another according to their loading. The reference voltage must be calculated as follows:

First set the value for $I_1 + I_2$. When using the KA431(LM431) this is recommended to be around 2mA. Then calculate R3 from $R_3 = V_{ref} / (I_1 + I_2)$.

It is recommended to ensure that both voltage outputs have equal control over the loop make $I_1 = I_2 = I_3/2$.

Now calculate R1 from $R_1 = (V_5 - V_{ref}) / I_1$ and $R_2 = (V_{3.3} - V_{ref}) / I_2$.

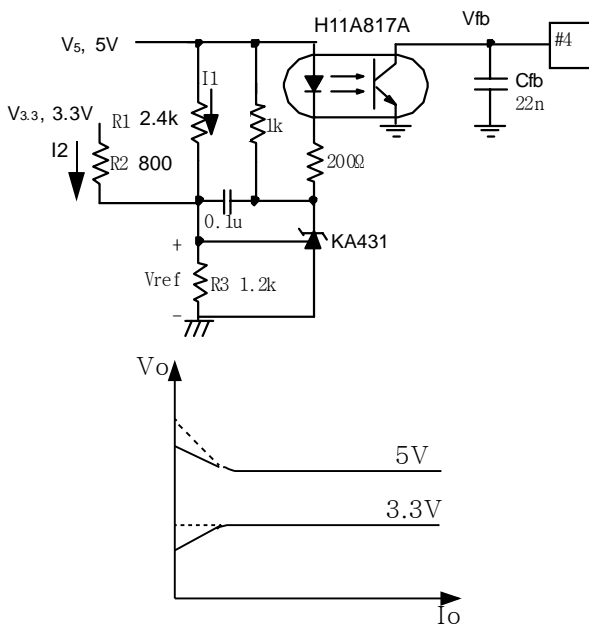


Figure 9. Two output control using a LM431.

3. Example Transformer Design for a Set Top Box SMPS

The transformer of a multiple output SMPS has multiple windings. The example SMPS for a set top box, the circuit for which is shown on Figure. 11, has four outputs: 24V, 9V, 5V, and 3.3V. The latter two voltages power micro controller, CPU, and memory, while the 9V and 24V outputs power audio, HDD, DVD-ROM, CD-ROM, and tuner circuits. The transformer design proceeds as follows.

3.1. Define system specifications:

Output Power, $P_o = 19W$
 (24V @ 0.1A; 9V @ 0.5A; 3.3V, 1.2A @ 5V, 1.5A)
 Input voltage, 85 to 265V_{ac} (universal input); $f_s = 60Hz$
 SMPS efficiency, $\eta = 75\%$

3.2. Determine minimum input voltage, V_{min} :

When the SMPS operates with the same output power at all ac inputs, maximum peak drain current occurs at the minimum input voltage, V_{min} . V_{min} also has its largest ripple at that time. C_{in} , the dc link capacitor, charges and discharges at twice the line frequency, or 120 Hz.

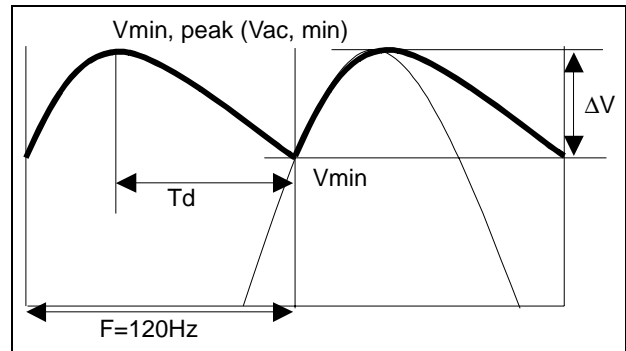


Figure. 10

2a. Now calculate energy discharge time, T_d as

$$T_d = \frac{1}{f_s} \times \frac{1}{4} \times \left(1 + \frac{\arcsin \frac{V_{min}}{V_{min,peak}}}{\frac{\pi}{2}} \right)$$

2b. It is possible to calculate C_{in} , the dc link capacitor, from the input energy during discharge time;

$$W_{in} = P_{in} \cdot T_d \quad (W_{in}=\text{input energy, } P_{in}=\text{input power})$$

$$W_{in} = \frac{1}{2} \cdot C_{in} \cdot (V_{min,peak}^2 - V_{min}^2)$$

2c. Now, for the SMPS example here,

$$T_d = 6.42ms$$

$$W_{in} = \frac{P_{out}}{\eta} \cdot T_d = 25.33 \times 6.773ms = 162.5mJ$$

2d. Assume 30V_{ac} ripple, and solve for C_{in} from the earlier equation, substituting in it $W_{in} = 162.5 mJ$:

$$C_{in} = \frac{2W}{V_{min,peak}^2 - V_{min}^2} = \frac{2 \times 162.5m}{(\sqrt{2} \times 85)^2 - (\sqrt{2} \times 85 - 30)^2} = 52\mu F$$

Since 52μF is not a standard value, use 47μF and, using the earlier equation, solve for $V_{min} = 87V$.

3.3. Set the maximum duty, D_{max}

A typical current-mode SMPS has a D_{max} under 50%. Since a D_{max} over 50% can cause sub harmonic instabilities, it is recommended that D_{max} should be designed to 45%.

3.4. Calculate primary inductance (L_p) and select the Fairchild Power Switch(FPS):

$$P_{in} = I_{in} \cdot V_{min}, I_{in} = \frac{1}{2} D_{max} I_{peak}$$

$P_{in} = 25.33W$ (from P_o/h) and $V_{min} = 87V$, hence calculate $I_{in} = 291.1mA$ and $I_{peak} = 1.294A$ in discontinuous current mode (DCM). $L_p = 600\mu H$.

$$L_p = \frac{D_{max} \cdot V_{in,min}}{I_{peak} \cdot f_{switch}}$$

Using the value of I_{peak} , select the KA5L0380R, Fairchild Power Switch(FPS); this is an 800V, 3A device that switches at 50kHz and has an auto restart mode.

3.5. Choose ferrite core:

The output power dictates the ferrite core. For this SMPS with an output power under 20W, choose an EI2820 core, for which, according to the TDK core

databook:

EI2820: PC40EI28-Z

A_e (effective cross sectional area) = 86.0mm²

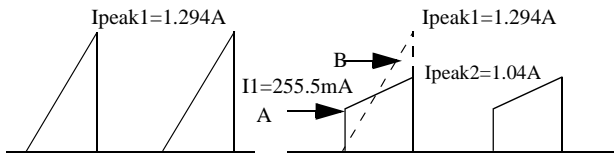
A_L (inductance/turn²) = 4300 ±25% nH/turn²

B_s (flux density at saturation) = 340 - 370mT at 100°C

$$A_{min} = \frac{(I_{peak} - I_1) \sqrt{A_L \cdot L_p}}{\Delta B_{max}}$$

For a design margin, let $\Delta B_{max} = 250mT$ and A_{min} (minimum required effective core area) = 70mm² (i.e., < 86.0mm²). Also, to improve temperature and EMI characteristics, increase L_p to 1.0mH from the 600μH calculated value. This decrease I_{peak} to 1.04A from 1.294A. Because the SMPS operating mode is changed to continuous current mode (CCM) at turn on, drain current $I_1 = 255.5mA$. Therefore, the value of A_L can now be calculated by solving for it from the preceding equation: $A_L = 500nH/turn^2$.

1. Average current will be the same in DCM and CCM if the output has the same value for the same input.



2. Determine $L_p = 1.0mH$, slope of the drain current can be changed as follows.

$$\frac{V_{min}}{L_p} = \frac{I_{peak1}}{T_{on}} D_{CM}$$

$$\frac{V_{min}}{L_p} = \frac{I_{peak2} - I_1}{T_{on}} C_{CM}$$

$$I_{peak2} = I_{peak1} - I_1$$

core gap L_g is as follows.

$$L_g = \frac{N_p^2 \mu_o A_e}{L_p} \times 10^3 = \frac{44^2 \times 4\pi \times 10^{-7} \times 70 \times 10^{-6}}{1 \times 10^{-3}} \times 10^3 = 0.170mm$$

3. Calculate I_1 in CCM.

$$I_{peak2} = 1.294A - I_1$$

$$\frac{87V}{1m} = \frac{1.04A - 2 \times I_1}{9\mu s}$$

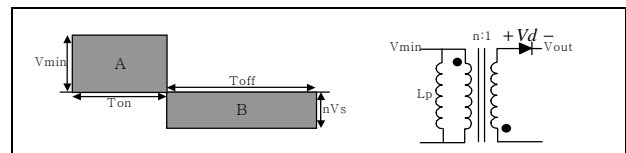
Therefore, I_1 becomes 255.5mA and I_{peak2} becomes 1.04A.

3.6. Determine primary turns, $N_p = 44$ turns, from

$$N_p = \sqrt{\frac{L_p}{A_L}} \quad \text{or} \quad N_p = \frac{L_p \cdot (I_{peak} - I_1)}{A_{min} \cdot \Delta B_{max}}$$

3.7. Determine secondary turns, N_s , for the 3.3V, 5V, 9V, and 24V windings,

The figure immediately below shows a portion of the flyback converter. With the energy of the core L_p totally discharged, area A for charging will be the same as area B for discharging; that is, $(V_{min})(T_{on}) = (nV_s)(T_{off})$, and $V_s = V_{out} + V_d$.



Since the switch is operating at maximum duty, $D_{max} = 45\%$, $V_{MIN} = 87V$ from an earlier calculation, and $V_s = 5.5V$ (controlled voltage), n is calculated at 12.942. From $n = N_p/N_s$ with $N_p = 44$ turns, $N_s = 3.4$. Therefore set $N_s = 3$ turns. The other secondary turns can be calculated by voltage ratio.

$$\frac{N_{V_{CC}}}{N_{5V}(3T)} = \frac{14V}{5.5V}$$

(Fast recovery diode: $V_d = 0.7V$, schottky diode: $V_d = 0.5V$)

From which $N_{3.3V} = 2$ turns, $N_{9V} = 5$ turns, $N_{24V} = 14$ turns.

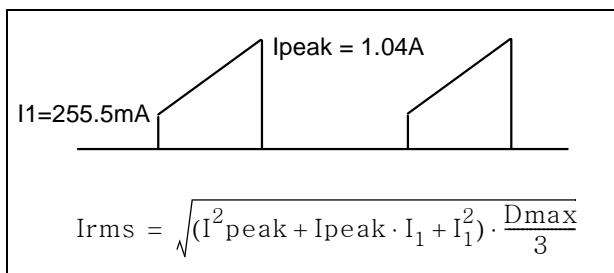
3.8. Determine IC bias turns (N_{V_{CC}})

The Fairchild Power Switch (FPS) will work properly at a V_{CC} from 9V to 25V. For the design example here, set V_{CC} = 14V at no load. Hence,

$$\frac{N_{V_{CC}}}{N_{5V}(3T)} = \frac{14V}{5.5V} \quad N_{V_{CC}} = 8\text{Turns}$$

3.9. Determine wire thickness:

The copper wire's current capability is 5A/mm². The rms current through primary N_p is 461mA in the example as calculated below.



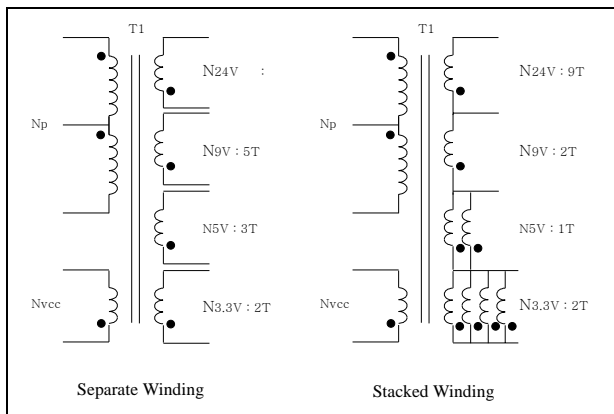
Use a current capacity of 5A/mm² and Using the formula below, calculate the wire diameter:

The wire diameter of N_p is 0.35mm:

by

$$\pi\left(\frac{\phi}{2}\right)^2 = I_{rms}/5A$$

Obtain the secondary wire diameter, N_s, in the same way. Considering the core window and leakage inductance, use bifilar or Litz wire.



3.10. Transformer construction:

While there are many winding methods, the figure above illustrates two ways: separate winding, and stacked winding. (The primary coil winding is constructed sandwich style.) Each winding technique has advantages and disadvantages. For the separate winding technique the disadvantages are poor regulation when lightly loaded and a requirement for more pins on the bobbin. Its advantage is a minimal energy loss from the leakage inductance. The disadvantages of the stacked winding are that the highest voltage winding must be placed closest to the primary winding and the common coil (the 3.3V winding, in the example) carries the larger current (0.1 + 0.5 + 1.2 + 1.5A). Its advantage is an improved cross regulation.

4. SMPS Design for a Set Top Box

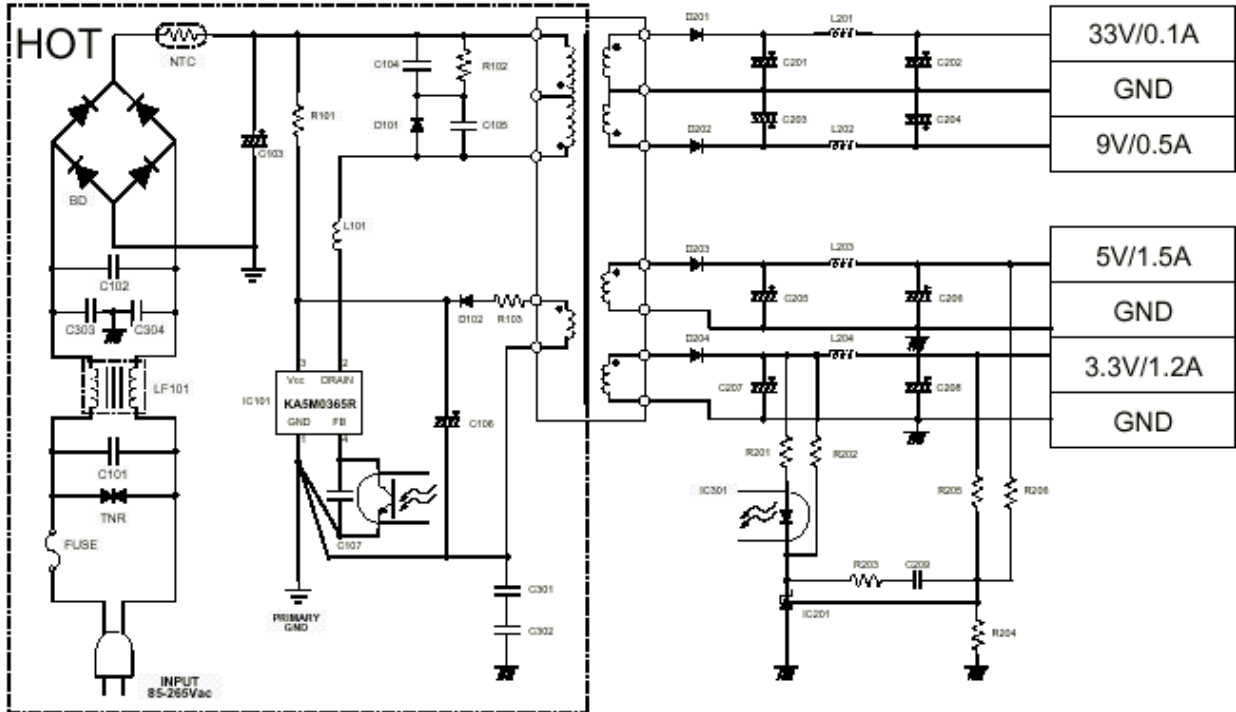
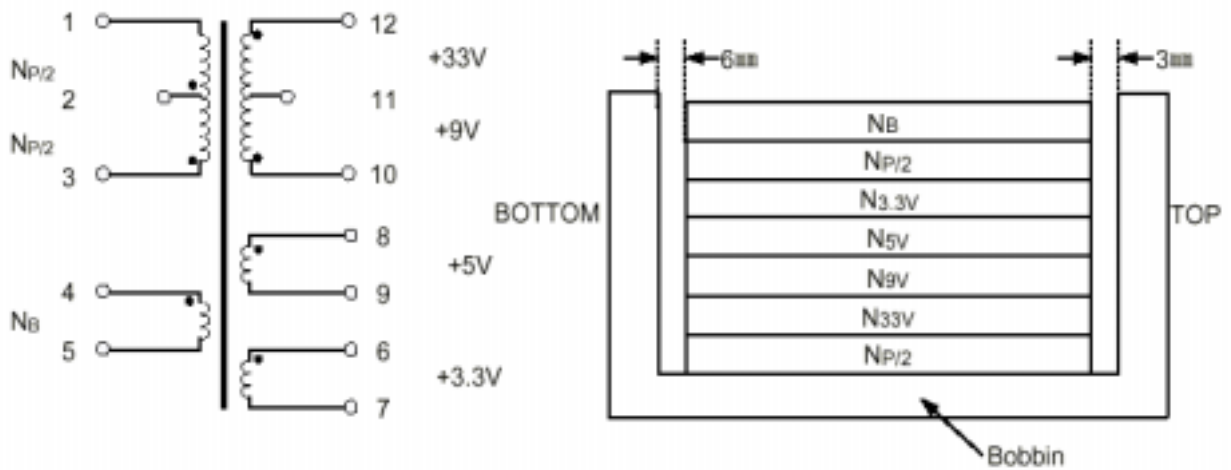


Figure. 11

4.1 Transformer Specification for the Set Top Box SMPS

4.1.1 Schematic diagram (top view)



* THE '•' MARKS ARE START POINT.

4.1.2 Winding specification

No.	Pin (S-F)	Wire	Turns	Insulation	Remarks
NP/2	3 - 2	0.25φ	22	PS TAPE, t=0.05mm, 3T	SOLENOID WINDING
N33V	12 - 11	0.3φ	18	PS TAPE, t=0.05mm, 2T	SPACE WINDING
N9V	10 - 11	0.4φ	5	PS TAPE, t=0.05mm, 2T	SPACE WINDING
N5V	8 - 9	0.4φ × 3	3	PS TAPE, t=0.05mm, 2T	SPACE WINDING
N3.3V	6 - 7	0.4φ × 2	2	PS TAPE, t=0.05mm, 2T	SPACE WINDING
NP/2	2 - 1	0.25φ	22	PS TAPE, t=0.05mm, 2T	SOLENOID WINDING
NB	4 - 5	0.25φ	9	PS TAPE, t=0.05mm, 3T	SPACE WINDING

4.1.3 Electrical characteristics

Closure	Pin	Spec.	Remarks
Inductance	3 - 1	900μH ± 5%	1 kHz, 1V
Leakage L	3 - 1	20 μH MAX.	2nd all short

4.1.4 Core and bobbin

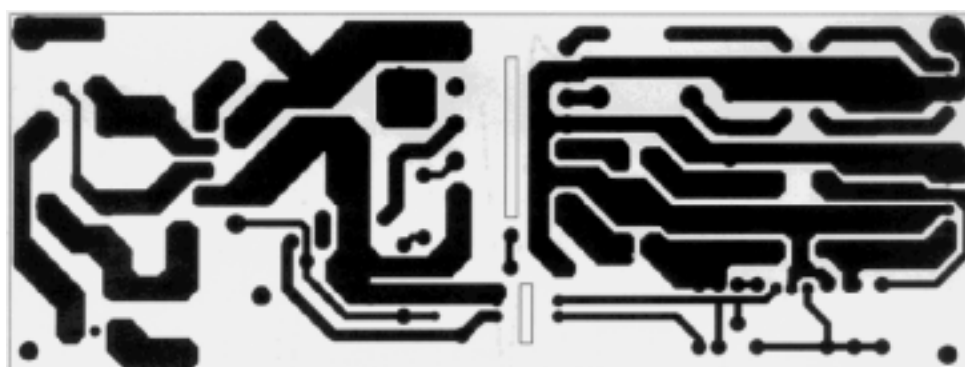
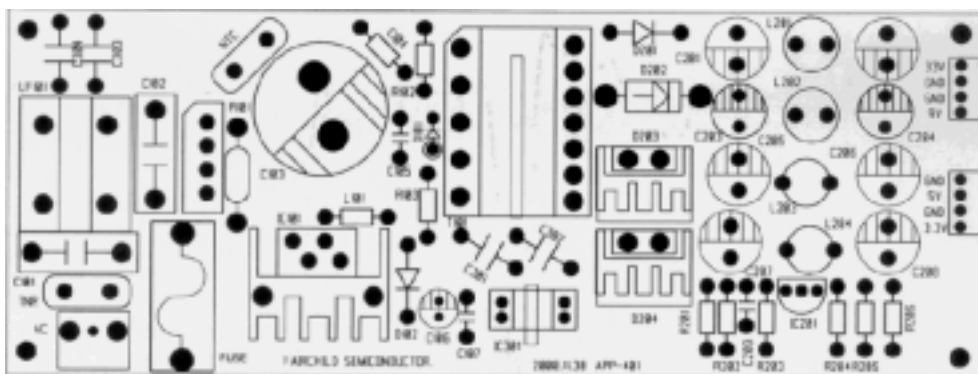
Core: EER2828

Bobbin: EER2828

Parts List

Part No.	Value	Note	Part No.	Value	Note
FUSE			C205	1000μF, 10V	Electrolytic capacitor
FUSE	250V, 2A	-	C206	1000μF, 10V	Electrolytic capacitor
NTC			C207	1000μF, 10V	Electrolytic capacitor
NTC	10D-9	-	C208	1000μF, 10V	Electrolytic capacitor
VARISTOR			C209	0.1μF	Film capacitor
TNR	7D471	TNR	C301	3.3nF	AC coupling capacitor
RESISTOR			C302	3.3nF	AC coupling capacitor
R101	500kΩ	1/4W	INDUCTOR (1kH, 1.0V)		
R102	56kΩ	2W	L101	BEAD	-
R103	10kΩ	1/4W	L201	4μF	-
R201	330Ω	1/4W	L202	4μF	-
R202	1kΩ	1/4W	L203	8μF	-
R203	1.2kΩ	1/4W	L204	8μF	-
R204	1.2kΩ	1/4W	DIODE		
R205	800Ω	1/4W	BD	KBP206	Bridge Diode
R206	2.7kΩ	1/4W	D105	UF4007	FAIRCHILD
CAPACITORS			D106	UF4004	FAIRCHILD
C101	0.1μF, 275VAC	Box Capacitor	D201	UF4007	FAIRCHILD
C102	0.1μF, 275VAC	Box Capacitor	D202	UF5402	-

Part No.	Value	Note	Part No.	Value	Note
C103	68μF/450V	Electrolytic Capacitor	D203	D5S4M	5A, 40V
C104	10nF/1kV	Ceramic Capacitor	D204	D5S4M	5A, 40V
C105	-	-	-	-	-
C106	10μF/ 50V	Electrolytic Capacitor	IC		
C107	22nF	Film Capacitor	IC101	KA5M0365R	FAIRCHILD
C201	47μF/100V	Electrolytic Capacitor	IC201	KA431AZ	FAIRCHILD
C202	47μF/100V	Electrolytic Capacitor	OPT	Q817A	FAIRCHILD
C203	470μF/35V	Electrolytic Capacitor	LINE FILTER		
C204	470μF/35V	Electrolytic Capacitor	LF101	40mH	-



DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICODUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.