Add an auxiliary voltage to a buck regulator

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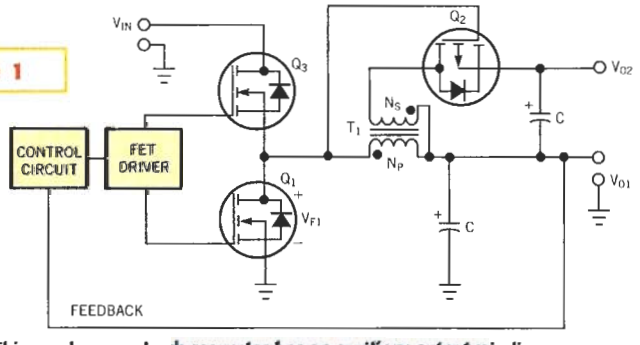
YOU OFTEN NEED more than one regulated output voltage in a system. A frequently used and reasonably simple way to create this auxiliary output voltage is to add a second winding to the output inductor, creating a coupled inductor or a transformer, followed by a diode to rectify (peak-detect) this output voltage. The biggest drawback of this approach is that the diode's voltage drop varies with temperature and load current and can have a 2-to-1 variation, resulting in poor output-voltage regulation. This problem becomes more critical as output voltages decrease and may require the addition of a linear regulator. The circuit shown in **Figure 1** is an alternative approach that replaces this diode with Q_2, a p-channel FET. The circuit works as follows:

Figure 1



This synchronous buck converter has an auxiliary-output winding.

During the conduction time of FET Q_1, the voltage across the primary winding of transformer T_1 clamps to the voltage, $V_{OUT}+V_{F1}$, where V_{F1} is the voltage drop across FET Q_1. Through transformer action, the voltage on the secondary winding of inductor L_1 is equal to the turns ratio between the windings times the voltage across the primary winding. The output capacitor on the auxiliary output, V_{02}, then charges to the peak of the secondary-winding voltage. FET Q_2 turns off when Q_3 turns back on to prevent the output capacitor from discharging. The secondary voltage floats; you can add it to the main output voltage by tying one end of the secondary winding to the main output. You can also tie it to ground for an output voltage lower than V_{01}, if desired. The equation that defines the auxiliary-output voltage for the circuit in **Figure 1** is:

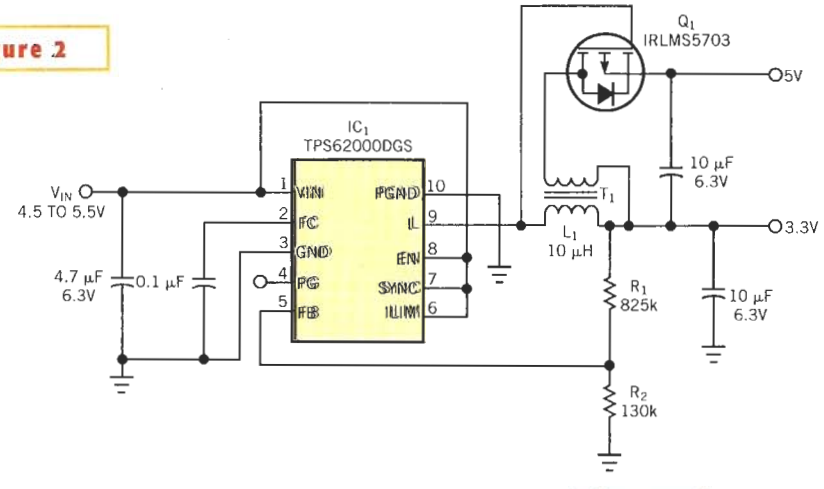
$$V_{02}=V_{01}\left(1+\frac{N_S}{N_P}\right)+\left(V_{F1}\times\frac{N_S}{N_P}-V_{F2}\right).$$

The second half of this equation represents a voltage-error term between FETs Q_1 and Q_2. To cancel out the error attributable to the FET voltage drops, you need to make the voltage drop of FET Q_2 equal to $V_{F2}=V_{F1}\times(N_S/N_P)$, where N_S/N_P is the transformer's turns ratio. Because these FET voltages are a function of the output currents and the on-resistance of the FETs, you can select the on-resistance of FET Q_2 by using the following equation:

$$R_{Q2}=R_{Q1}\times\frac{N_S}{N_P}\times\left[(1-d)\left(1+\frac{I_{01}}{I_{02}}\right)-d\times\frac{N_S}{N_P}\right],\ \text{where}\ d=\frac{V_{01}}{V_{IN}}.$$

In **Figure 2**, the main output voltage is 3.3V, yielding an inductor primary voltage when Q_1 is conducting equal to only 3.44V, because of the low voltage drop across FET Q_1. Thus, if you wanted a 5V output, the secondary winding would need to develop an additional 1.7V, necessitating a 2-to-1 step-down turns ratio. The desired on-resistance of the FET internal to IC_1 from the above equation should be 0.16Ω to cancel the voltage drop across Q_1 at maximum loads and while operating from a 5V input voltage. This example uses a 0.20Ω FET with a voltage drop equal to only 88 mV. This choice allows for good voltage matching between FETs Q_1 and the FET internal to IC_1, resulting in excellent error cancellation, less power loss, and better overall output-voltage regulation than diode rectification provide. An added benefit of this approach is that you can use it with controllers that have integrated switching FETs, because you don't need access to Q_1 and Q_3 gate drives. Measured results, although varying both outputs' loads over their full operational range, showed less than a ±3% variation in the

Figure 2



This circuit is similar to the one in Figure 1, but uses an integrated buck-converter IC.

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placing the input capacitor between V_{IN} and V_{OUT} is equivalent to placing it between the IC's V_{IN} and ground pins (**Figure 1**). The other, commonly accepted method of placing the bulk input capacitor between V_{IN} and ground (**Figure 2**) significantly increases the output-voltage ripple (**figures 3** and **4**). To make matters worse, this configuration requires an additional high-frequency bypass capacitor between the V_{IN} and ground pins of the IC.

In simple positive-to-negative converters, such as those in **figures 1** and **2**, the output-voltage ripple is

$$\Delta V_{OUT(P-P)} = ESR_{COUT} \times \Delta I_{COUT(P-P)}.$$

Low-ESR output capacitors, such as ceramics, help to minimize the output-voltage ripple in dc/dc converters. For a given output-capacitor ESR, you can further reduce the output-voltage ripple by minimizing the current ripple that the output capacitor is forced to absorb. In **Figure 2**, the output capacitor is part of the high-di/dt switching-current path, making the output voltage ripple proportionately larger. With the bulk input capacitor placed as shown in **Figure 1**, the peak-to-peak ripple current in the output capacitor is equal to the peak-to-peak ripple current in the inductor: $\Delta I_{COUT(P-P)} = \Delta I_{L(P-P)} = (V_{IN} \times$ duty cycle$)/(f_{SW} \times L)$, where $\Delta I_{COUT(P-P)}$ = output ripple current, $\Delta I_{L(P-P)}$ = inductor ripple current, and f_{SW} = switching frequency.

When the bulk input capacitor is placed as shown in **Figure 2**, the peak-to-peak ripple current in the output capacitor is much higher than the inductor's ripple current alone; it is almost equal to the inductor's ripple current plus the input capacitor's ripple current: $\Delta I_{CIN(P-P)} = I_{L(P)} = I_{OUT} + I_{IN} + \Delta I_{L(P-P)}/2$, and $\Delta I_{COUT\ (P-P)} \sim \Delta I_{L(P-P)} + \Delta I_{CIN(P-P)}$. With much lower output-capacitor ripple current, the output capacitor in the circuit in **Figure 1** can be much smaller than that of the circuit in **Figure 2**. Also, it needs to handle much less rms ripple current (approximately equal to peak-to-peak ripple current divided by the square root of 12). Another advantage of removing the output capacitor from the high-di/dt switching loop (by judicious placement of the input capacitor) is a greatly simplified layout. You must place the high-di/dt components in **Figure 1** in the smallest loop possible to minimize trace inductance and the resulting voltage (noise) spikes. With one fewer component to worry about in the layout, you can more easily create a noise-free circuit using the layout in **Figure 1** than it is using the one in **Figure 2**.

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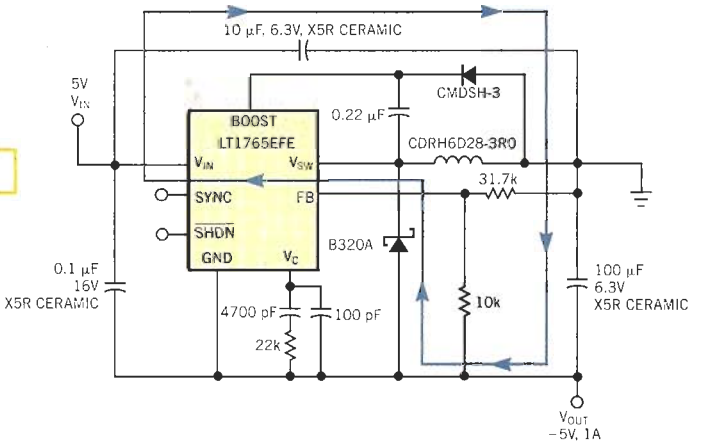
Figure 2



This +5-to-−5V converter with the bulk capacitor between V_{IN} and ground has much higher output ripple than the circuit in Figure 1. The high-di/dt path, indicated here with blue lines, includes the output capacitor, thus increasing output ripple.

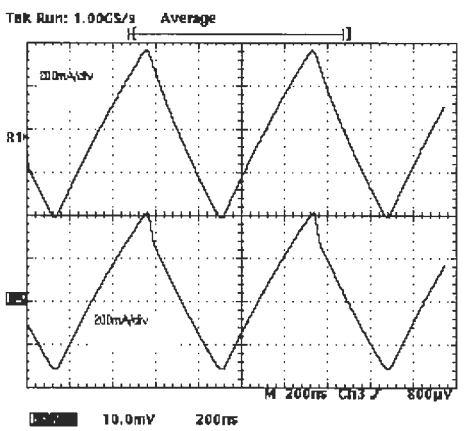


Figure 3

In the circuit in Figure 1, the output capacitor's peak-to-peak current ripple is equal to the inductor's peak-to-peak ripple with 1A output.

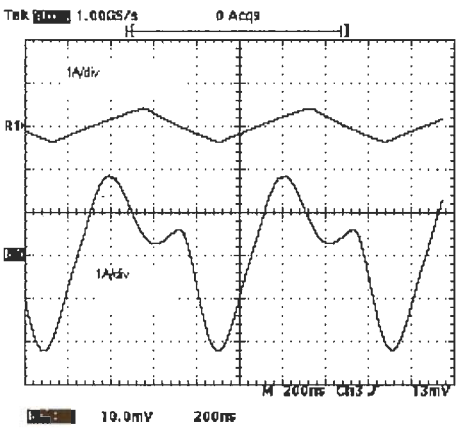


Figure 4

In the circuit in Figure 2, the output capacitor's peak-to-peak current ripple is five times as high as the inductor's peak-to-peak ripple and, therefore, five times as high as the current ripple shown in Figure 3 with 1A output.

Figure 3 is an I/O and core-voltage-sequencing circuit. Instead of using an RC charge voltage to control the turn-on, IC_3 of the core regulator compares the output of the I/O during turn-on and matches the core voltage until it reaches the regulation voltage. **Figure 4** shows the I/O and core voltages during the power-on cycle. Equally important is the power-down cycle. The I/O voltage must never reach 0.6V below the core voltage. This condition can forward-bias the substrate diode, damaging the processor. D_2, a Schottky diode with a forward voltage drop of 0.4V, keeps the I/O voltage from dropping 0.6V below the core voltage during the power-down cycle (**Figure 5**).

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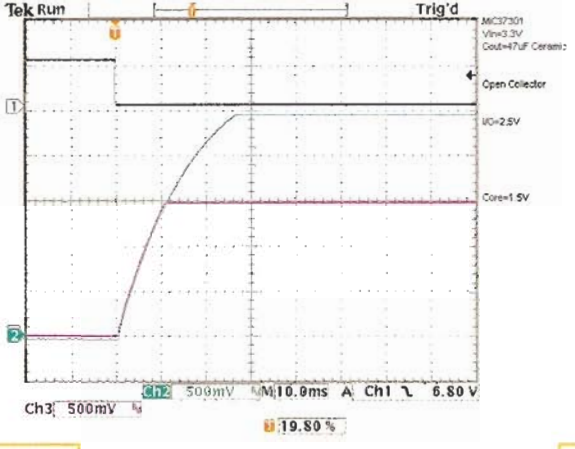

Figure 4

The I/O and core voltages have controlled rise times during the power-on phase.

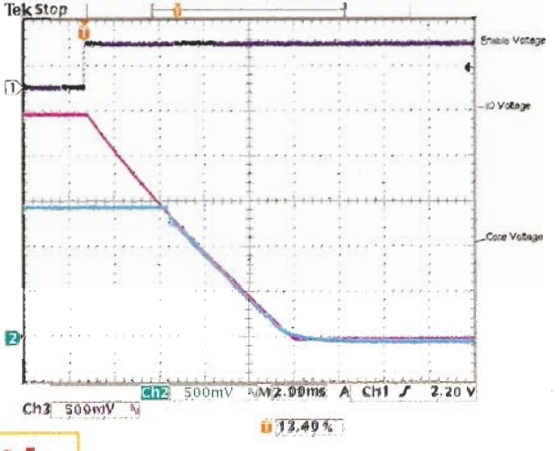

Figure 5

A Schottky diode keeps the I/O voltage from dropping 0.6V below the core voltage.