Power Supply Design Seminar

Choosing the Right Fixed Frequency Buck Regulator Control Strategy

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Choosing the Right Fixed Frequency Buck Regulator Control Strategy

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Topic 1

ABSTRACT

The choice of using a non-isolated buck converter topology to reduce a distribution voltage to a lower one for point-of-load applications is an easy one. The buck is simple, has relatively few components and may be configured for a wide variety of applications. The choice of how to manage the control of the converter is not quite as straightforward a decision. In this topic, the operation and basic design considerations of a buck converter are reviewed. The topic then examines the trade-offs between two fixed-frequency control strategies and some enhancements to extend their capabilities. Basic voltage mode control is adapted with input voltage feed-forward and current mode control is enhanced with emulated current mode control. The highlights and challenges for each technique are discussed and select design examples are presented. In a follow-on topic, "Choosing the Right Variable Frequency Buck Regulator Control Strategy", constant on-time control and its variants are presented.

I. INTRODUCTION

A buck converter operates by applying a pulse width modulated (PWM) waveform of a controlled duty cycle to a low pass L-C filter, thus converting one voltage to a lower one. One side of a switch is connected to an input voltage and the other to an inductor. The switch when turned on connects the input voltage to the inductor of the filter and disconnects it when off. The ratio of the on-time of the switch to the switching period is called the "duty cycle". The low-pass filter averages the switching voltage, resulting in a relatively constant DC voltage at the converter output. A "catch" diode allows the inductor current to decay when the switch opens, clamping the voltage at the "switching" node (SW) to just below ground and allows the net average inductor current to remain at a constant level.

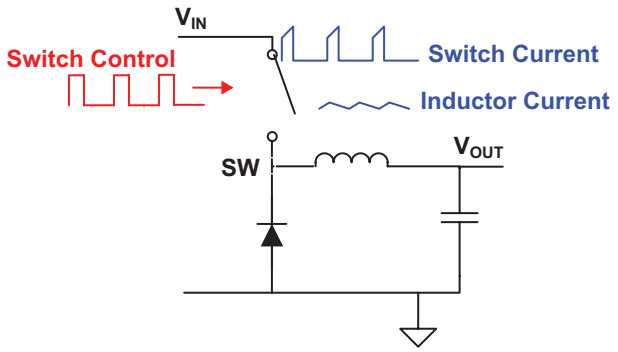


Figure 1 – Buck converter fundamental operation.

The input voltage and the duty cycle of the switch determine the output voltage. Equation 1 shows the V_{OUT} to V_{IN} relationship for an ideal (loss-less) buck converter.

$$V_{OUT} = D \cdot V_{IN} = \frac{t_{ON}}{T_S} \cdot V_{IN} \quad (1)$$

The duty cycle is defined as the ratio of the main switch on-time to the total switching period. This relationship holds as long as there is continuous current flowing in the inductor, or in Continuous Conduction Mode (CCM). Another mode, called Discontinuous Conduction Mode (DCM), is discussed later in this paper.

In this topic, the equations given are simplified and the effects of circuit losses are omitted. For now, it is understood that circuit losses tend to increase the duty cycle slightly in order to maintain a regulated output voltage. For those interested, the materials listed at the end of this topic provide more detail.

A variation on a simple buck replaces the diode with a controlled switch, or synchronous rectifier (SR). A synchronous rectifier generally has lower losses than a conventional or Schottky diode and so its use is quite popular in DC/DC converters. In operation, the drive of the synchronous rectifier is complementary to that of the upper switch, less a small dead time to prevent both switches being on at the same time. In this

configuration, the inductor circulating current flows through the FET channel, $R_{DS(ON)}$, rather than a diode. This configuration is termed a synchronous buck converter. Figure 2 shows an example of a synchronous buck converter. Accompanying waveforms are presented in following sections.

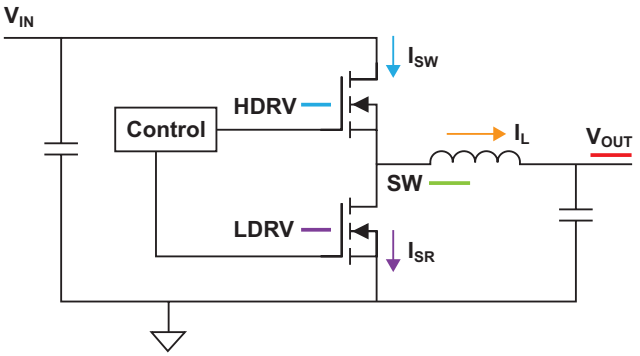


Figure 2 – Synchronous buck converter.

A. Control Variations

From Equation 1 above, given an input voltage (assume for this discussion it is not controlled) there are two variables remaining that are controllable: period (T_S) of the switching and/or on-time (t_{ON}) of the switch. Deciding which variable to control to regulate the output voltage of the converter has an impact on the design of the converter and may have system-level implications as well. For example, if there are multiple DC/DC converters in a system, each operating at approximately the same switching frequency, it may be necessary to synchronize them to a common frequency to avoid sub-harmonic noise. In this case, a control technique that relies on modulating the on-time of the switch with a fixed period would be the best choice. Voltage mode control (VMC) and current mode control (CMC) enable this.

Conversely, if fast response to load current variations is most important, then a variable frequency control technique is best. This is because, with fixed frequency control, the duty cycle cannot be changed after a PWM pulse has been delivered to the LC filter. There is a time lag, or latency, of up to a period, from when the load changes to when the next pulse of energy is sent to the inductor. With a variable frequency control technique the period is variable so that when a demand for increased or decreased energy occurs the controller responds with minimal latency.

B. CCM Operation

No matter which control approach is ultimately decided upon, a thorough understanding of the fundamental operating characteristics of the buck topology is necessary. The next step in this discussion is to follow the operation of the circuit for one switching cycle.

i. Turn ON of the Upper Switch

- At some time just prior to turn ON of the upper switch (HDRV), a signal from the control IC turns OFF the synchronous rectifier (LDRV), driving the current in the synchronous rectifier body diode I_{SR} to zero.
- When the PWM signal turns ON the upper switch (HDRV), the SW node is pulled towards the input voltage. In the plot here, the input voltage is 5 volts.
- As the SW node voltage rises above the output voltage level (V_{OUT}) the inductor current, I_L, begins to increase.
- The current in the upper switch, I_{SW}, has a step increase due to the DC bias of the inductor current and increases with the same slope as inductor current.

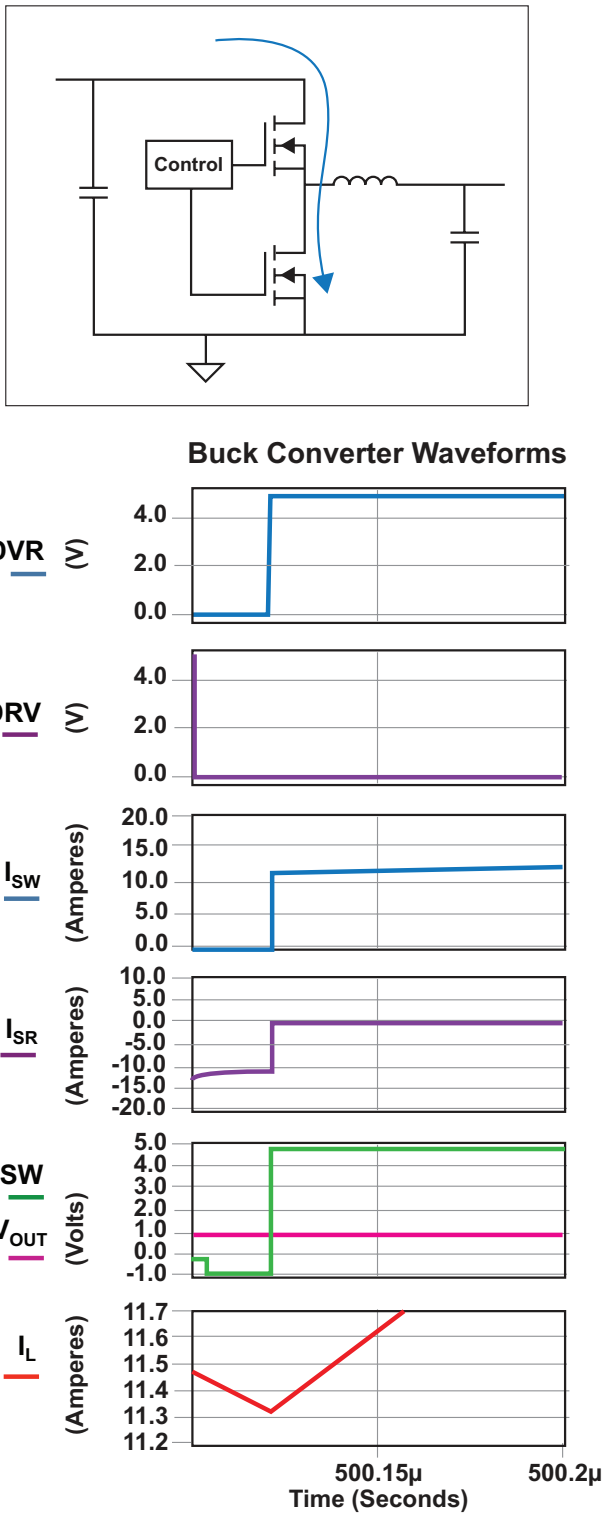


Figure 3 – Turn ON of upper switch.

ii. Steady-State Interval of Upper Switch ON

- The switching transition is complete.
- Current continues to increase in both the upper switch and inductor according to:

$$\Delta IL_{ON} = V\frac{S_{IN} - V_{OUT}}{L} \cdot t_{ON}$$

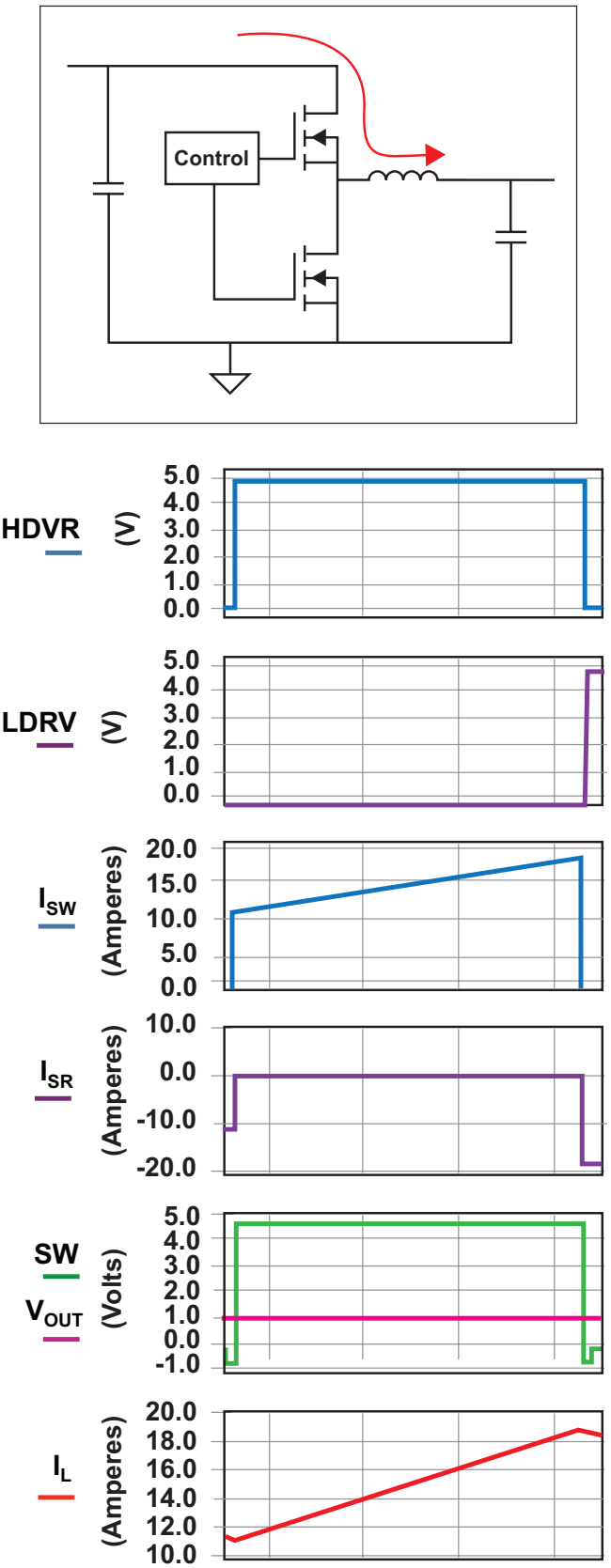


Figure 4 – Steady-state interval of upper switch ON.

iii. Turn OFF of Upper Switch and Transition to Turn ON of Lower Switch

- In this interval, the PWM signal turns OFF the upper switch. Then as the inductor current continues to flow, the SW node voltage falls and is clamped below ground by the synchronous rectifier body diode.
- The inductor current transitions to the body diode of the SR.
- The upper switch current falls to zero.
- After the transition is complete, the SR MOSFET is turned ON and the current transitions from the body diode to its channel. Evidence of this is the SW node voltage going closer to GND than the body diode voltage of the MOSFET allowed.
- The current in the inductor begins to decrease according to:

$$\Delta IL_{OFF} = \frac{V_{OUT} + V_{SR}}{L} \cdot t_{OFF}$$

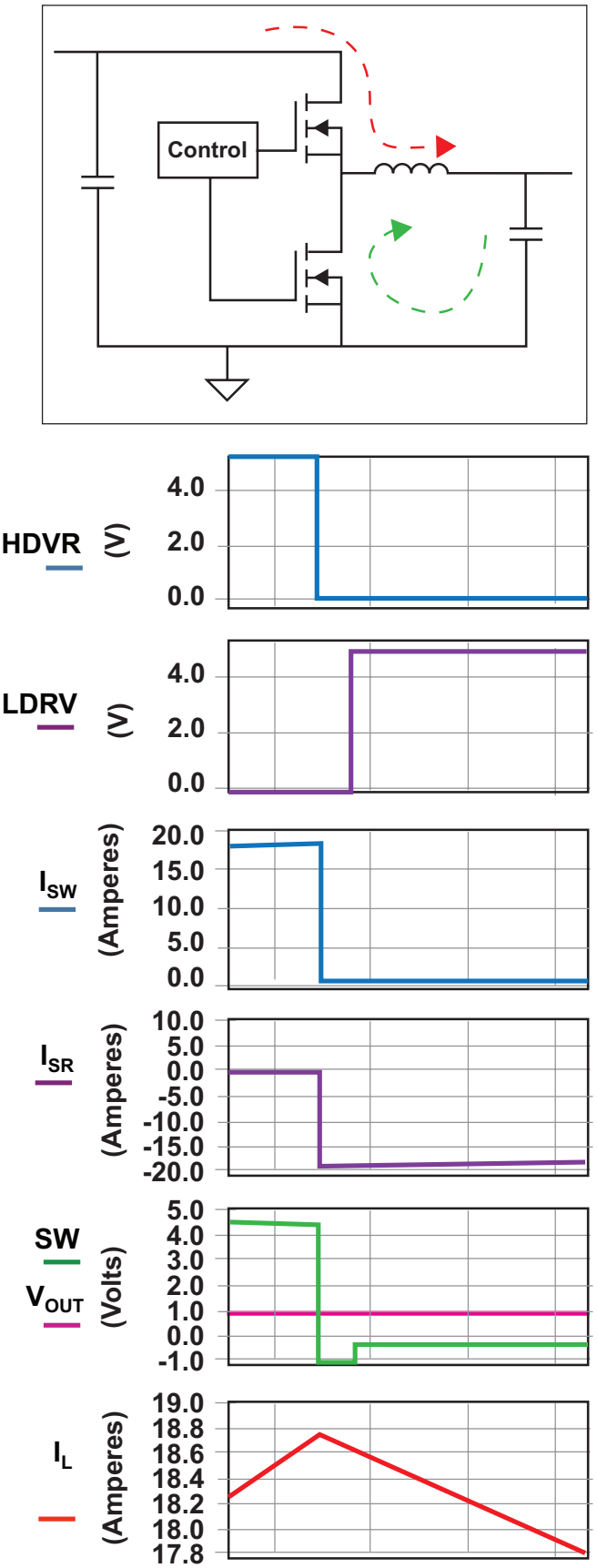


Figure 5 – Turn OFF of upper switch and transition to turn ON of lower switch.

iv. Operation with the Lower Switch ON

- In this freewheeling interval the inductor current flows through the synchronous rectifier.
- During this interval, the voltage across the Rds_{ON} of the SR (SW) decays because of the decay of the current in the inductor.
- At the end of this interval, the SR gate signal LDRV turns OFF the SR and the inductor current transitions from the channel back to its body diode.
- The cycle starts again with the PWM signal turning on the main switch MOSFET.

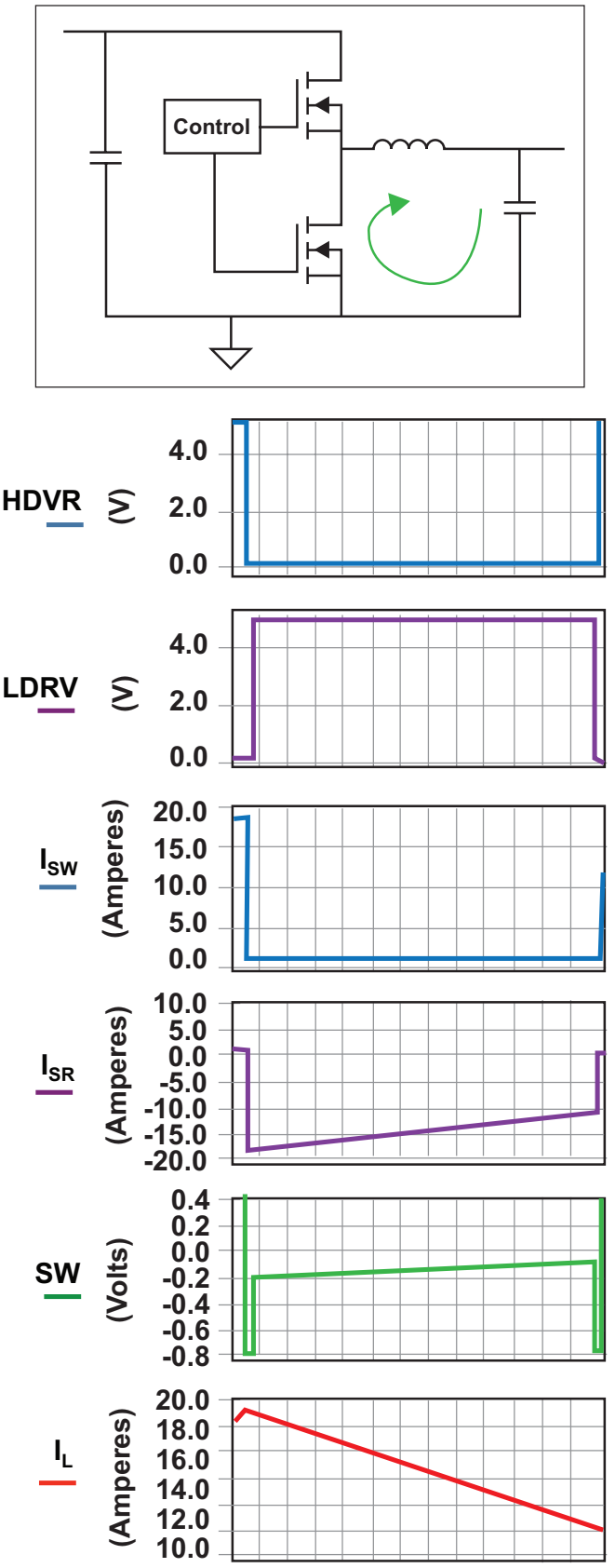


Figure 6 – Operation with the lower switch ON.

C. Discontinuous Current Operation

One of the key differences in circuit operation between a synchronous and a non-synchronous converter occurs at light loads when the converter's DC load current is less than half the magnitude of the peak-to-peak ripple current in the output inductor. In a non-synchronous buck converter, when the DC inductor current attempts to go below zero, current no longer flows due to the rectifier diode's blocking effect. In this condition, the inductor is running "discontinuous" because current flow is interrupted. When this occurs, the SW node rings up to the output voltage and settles at that level until the next switching cycle begins. This low energy ringing is generated by the energy in the inductor resonating with MOSFET parasitic capacitance. Figure 7 shows operating waveforms of a buck converter in DCM.

When the inductor goes discontinuous, the duty cycle required to maintain output voltage regulation is no longer simply the ratio of the output voltage to the input voltage. Equation 2 shows the relationship of the duty cycle to the circuit parameters.

$$\text{Duty Cycle}_{DCM} = \sqrt{\frac{2 \cdot L \cdot I_{OUT}}{T_S \cdot V_{IN}} \cdot \frac{V_{OUT}}{V_{IN} - V_{OUT}}} \qquad (2)$$

Notice that the input to output ratio is no longer a linear function of the duty cycle. This is because the inductor acts as a current source feeding the output impedance of the converter. The issue that arises from this effect is that the closed loop gain of the converter is reduced and is no longer a linear function. Care should be taken to verify loop stability and response characteristics under both CCM and DCM conditions.

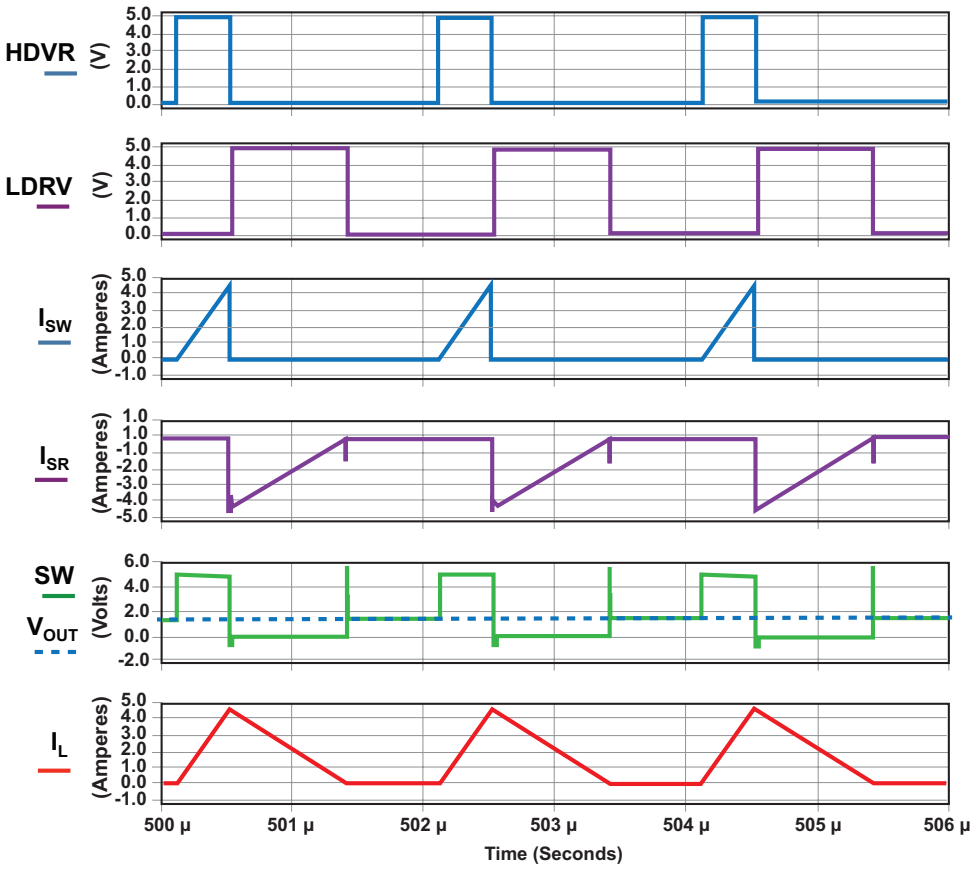


Figure 7 – Operating waveforms with discontinuous inductor current.

In a synchronous converter, the synchronous rectifier is controlled such that it either allows current to flow in only one direction as in a non-synchronous converter or, by allowing the synchronous rectifier to remain ON for the entire freewheeling interval, operates so that current flows in the reverse direction. The clear advantage is that if current is continuous in the output inductor, then the output voltage will remain a linear function of the duty cycle, and the loop response will be constant over the entire load current range. A disadvantage is that, under light loads, there is now power dissipated in the channel of the SR MOSFET and in the inductor as current flows in the reverse direction.

D. Filter Inductor Determination

The inductor and capacitor form a low pass filter, converting a switching waveform into its averaged equivalent (DC) plus a small amount of output noise. The ripple current in the inductor creates the fundamental portion of the noise. The peak to peak current during CCM operation is:

$$\Delta I_L\,(\text{peak to peak}) = \frac{\left(V_{IN} - V_{OUT}\cdot D\cdot T_S\right)}{L} \qquad (3)$$

$$= \frac{\left(V_{OUT} + V_R\right)\cdot(1-D)\cdot T_S}{L}$$

The voltage impressed across the inductor (V_{IN} - V_{OUT}) when the upper switch is on induces current to build in the inductor. During the time when the upper switch is off, the inductor current decays at a rate determined by the output voltage plus the drop across the rectifier (V_R). With fixed frequency operation, the design of the inductor is straightforward. The ripple current is chosen to be 10% to 30% of the full load output current, per Equation 3 above.

With a variable frequency control approach, the filter is also a contributor to the basic function of the converter. Consider a hysteretic control technique: the on-time of the switch is terminated when the output voltage reaches an upper regulation threshold and the output voltage reaches a lower threshold terminating the off-time. Knowledge of the impedance characteristics of the output capacitor is necessary to determine the ripple current necessary to meet the regulation requirements and determine the operating frequency.

A variation of hysteretic control fixes the on-time of the switch (called constant on-time or COT control) and requires the off-time to vary to maintain regulation. Similar to the hysteretic converter, the output capacitor impedance characteristics must be known to ensure the inductor current rise time is consistent with the on-time for the desired operating frequency and regulation voltage.

Notice that if the input voltage were to vary, the fixed frequency controlled converter would experience a change in duty cycle and a change in the peak to peak ripple. The variable frequency control technique maintains a fixed amount of ripple and results in a change in operating frequency.

When losses increase due to an increase in the load current, the resulting duty cycle increase to maintain output voltage regulation causes a slight increase in the peak-to-peak ripple due to the increased duty cycle for the fixed frequency converter. For a constant on-time converter, the increase in losses due to a load increase tends to increase the operating frequency.

E. Output Capacitor Determination

The output capacitors perform multiple functions, and so their selection, both type and value, are important to the performance of the converter. The “parasitic” components associated with a capacitor, equivalent series inductance (ESL) and resistance (ESR), have as much impact on the operation of a converter as the capacitance value itself.

One function of the capacitors is to filter the current from the inductor to a DC voltage. The minimum capacitance is found by:

$$C_{MIN} = \frac{IC_{P-P}}{8\cdot F_S\cdot V_{OUT_{P-P}}}$$

A word of caution here: the equation above refers only to the voltage across the capacitance portion of the capacitors. The total ripple and noise is due to this voltage drop plus the drops across the ESL and ESR.

The ripple across the ESR is found by multiplying the ripple current in the inductor by the ESR.

$$Vpeak\_ripple_{ESR} = \cdot R_{ESR} \cdot \Delta I_L$$

The total ripple is the sum of the two components

$$Vpeak\_ripple_{TOTAL} = \cdot Vpeak\_ripple_C + Vpeak\_ripple_{ESR}$$

A third component of output noise, spikes, is due to the ESL of the output capacitors. Refer to the References section of this paper for further detail, as the spikes are beyond the scope of this topic.

F. LC Filter for Transient Response

Another function of the output capacitors is to act as a "reservoir" for energy during load current transients. For example, during a step load increase, inductor current needs to build from one level to a higher level. If the increase in current is faster than the inductor can support in a single switching cycle, then the remaining energy must come from the output capacitors until the current in the inductor builds to the required level. This means that in an application that requires fast current build up, the ripple current needs to be higher than it otherwise would need to be. With higher ripple current comes the need for more capacitance to keep the ripple low and to support the output voltage during a load transient. Figure 8 show a pictorial description of a step up load transient event.

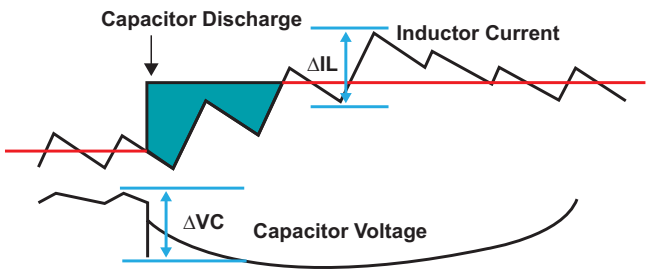


Figure 8 – Step up load transient event.

To determine the capacitance value based on the need to support the output voltage during a load transient:

$$\Delta VC = \frac{\Delta I_{STEP}^2}{2 \cdot (V_{IN} - V_{OUT})} \cdot \frac{L}{C}$$

In a later section it will be shown that the loop bandwidth also plays a part in capacitor selection for good transient response.

II. Fixed Frequency Control Techniques

A. Voltage Mode Control

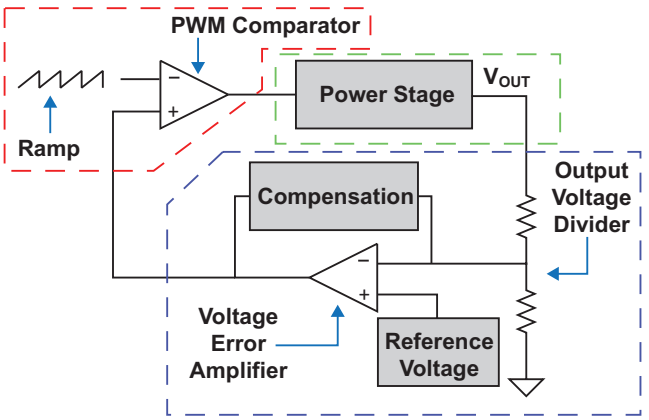


Figure 9 – Voltage mode control block diagram.

Figure 9 shows a block diagram of the three main components of a closed loop voltage mode control (VMC) system. The power stage consists of the power switches and output filter. The compensation block includes the output voltage divider, error amplifier, voltage reference and compensation components. The pulse width modulator (PWM) uses a comparator to compare the error signal to a fixed ramp, creating an output pulse train that has a width controllable by the level of the error signal. This output is fed into gate drivers that, in turn, control the power switches.

The next few sections go through each of the blocks in the block diagram. Since the control loop is a closed loop system, it does not really matter where on the loop the designer starts. This example starts with the output filter.

B. Voltage Mode Control Output Filter

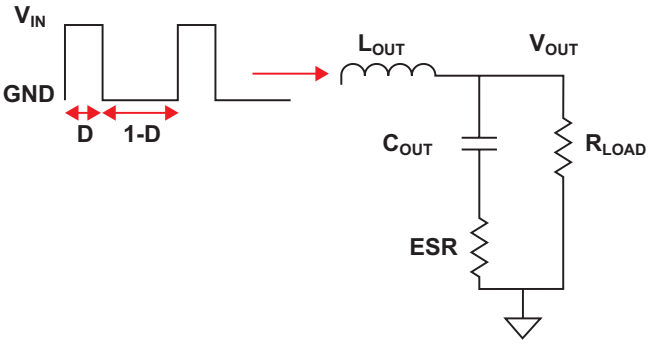


Figure 10 – Output filter for a buck converter.

Figure 10 shows the output filter for a buck converter. The simplified output filter consists of the output inductor, output capacitor, equivalent series resistance of the output capacitor and the load (represented by a resistor). This circuit is a second order system; this means that in the "s" domain it has a polynomial that is represented by a quadratic. Equation 4 describes the system. A graphical representation of the Bode plot gain and phase is shown in Figure 11.

The inductor and output capacitor form a double pole at the resonant frequency of the two components. The output capacitance and the ESR create a zero. Below the LC double pole frequency, the gain is flat and equal to 0 dB. Above the LC double pole frequency, the gain changes at a slope of -40 dB per decade. At the resonant frequency the phase also shifts -180 degrees. Beyond the ESR zero frequency, the gain slope changes to -20 dB per decade. There is also a +90 degree phase shift due to the ESR zero.

$$H_{PS}(s) = \frac{1 + \left(C_{OUT} \cdot R_{esr}\right)s}{1 + \left(\frac{L_{OUT}}{R_{OUT}} + R_{esr} \cdot C_{OUT}\right)s + \left(\frac{R_{OUT} + R_{esr}}{R_{OUT}}\right) L_{OUT} \cdot C_{OUT} \cdot s^2} \quad (4)$$

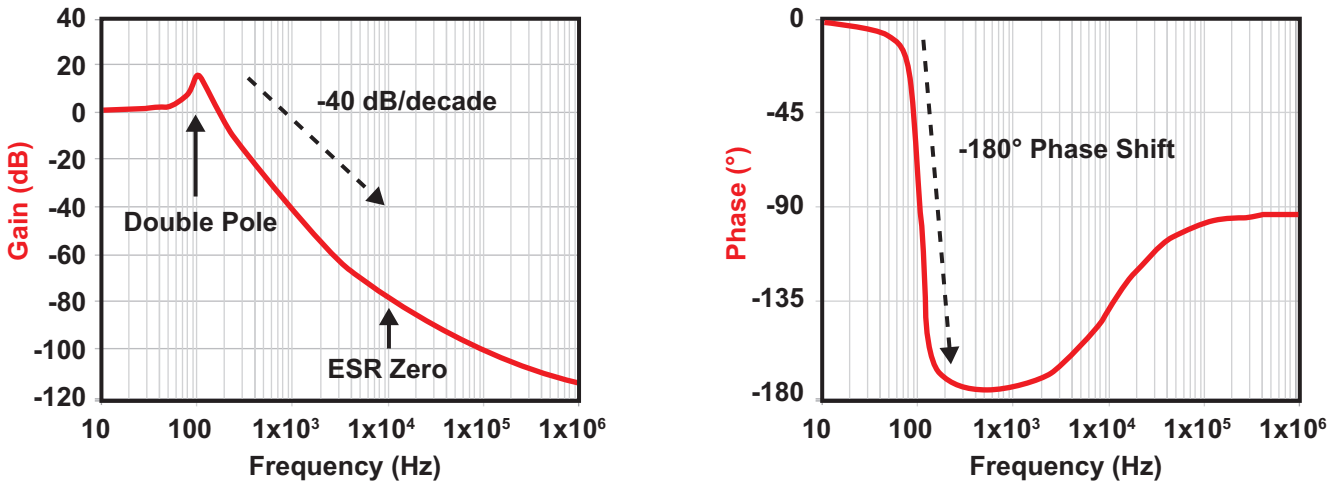


Figure 11 – Voltage mode output filter plot.

C. Voltage Mode Control Modulator Gain

The pulse width modulator portion of the loop adds a gain factor shown in Equation 5.

$$H_{Mod} = \frac{V_{IN}}{V_{Ramp}} \quad (5)$$

The gain due to the PWM is proportional to V_{IN}. If the converter has to operate over a wide range of input voltages, this could cause a problem. If the gain changes over input operating conditions, it makes it difficult to optimize the control loop. The loop response has to be lowered to accommodate all conditions. Many controllers that are designed to operate over a wide range use voltage feed forward. This increases the ramp signal proportionally to the input voltage. Figure 12 shows an example of the ramp changing with input voltage.

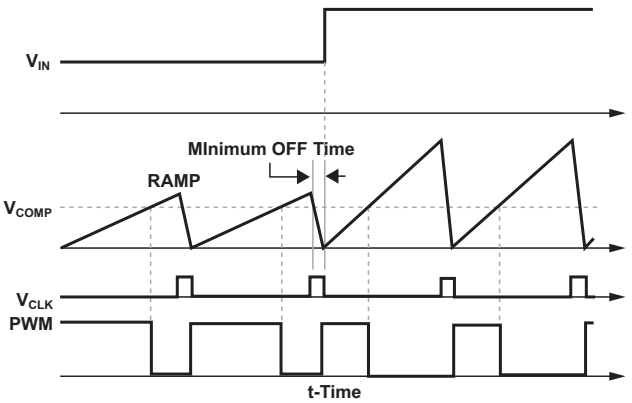


Figure 12 – Voltage feed forward.

D. Error Amplifier and Compensation

The compensator includes an error amplifier, voltage reference, output voltage divider and compensation components. The purpose of the compensator, as the name suggests, is to compensate for the drop in phase from the power stage and PWM. The goal of the compensator is to adjust the gain of the PWM and power stage so the Bode response maintains a -20 dB per decade slope and a phase margin of at least 45 degrees at the crossover frequency. The output voltage of the power supply is compared to a reference voltage through a resistor divider. This generates an error signal that feeds the PWM comparator. The three most common compensator networks are discussed here.

A Type 1 compensator, also referred to as dominant-pole compensation is shown in Figure 13. This compensator uses a large integrating capacitor across the error amplifier. The response of this amplifier configuration is a -20 dB per decade slope with -90 degrees of phase shift. The pole is located at the origin.

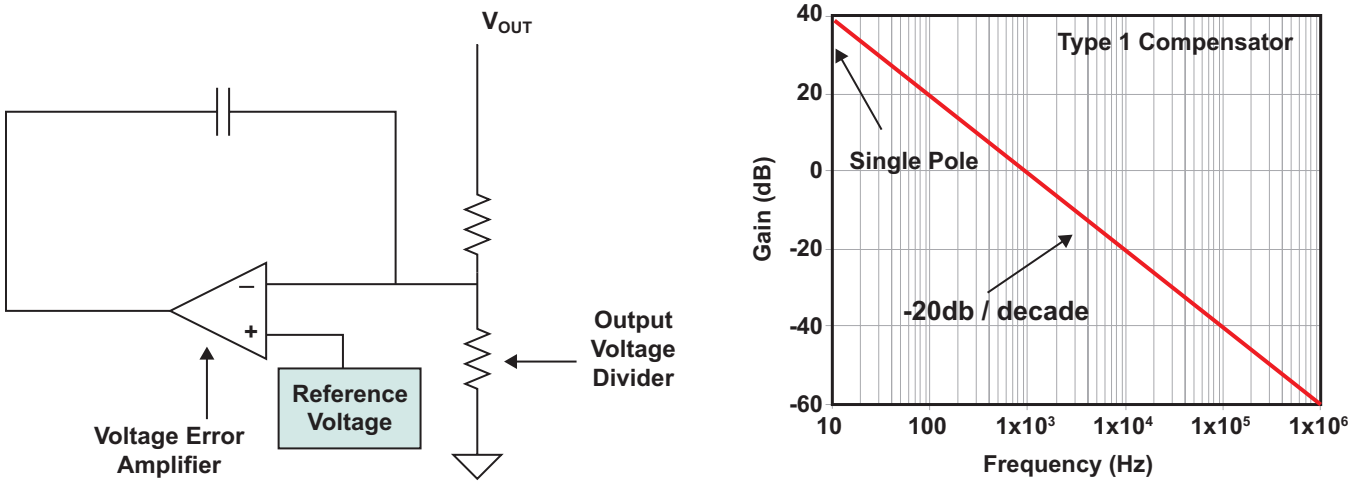


Figure 13 – Simplified type 1 compensator.

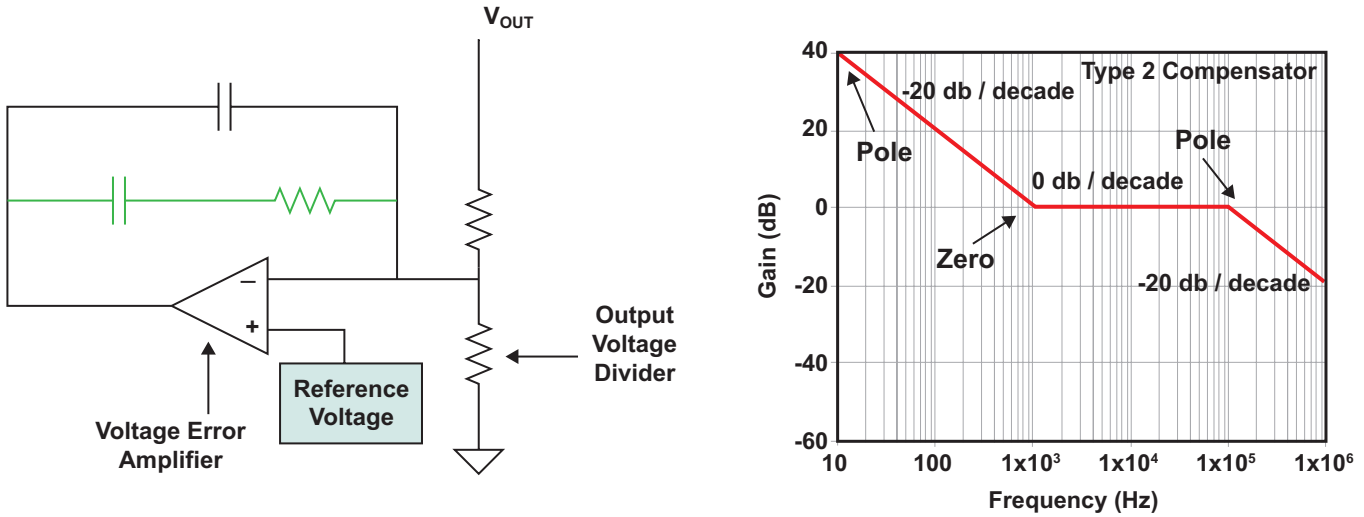


Figure 14 – Simplified type 2 compensator.

Figure 14 shows a type 2 compensator. This adds a resistor and a high frequency capacitor to the type 1 compensator. The type 2 compensator has two poles and one zero. This yields a phase shift of 0 degrees.

A Type 3 compensator is shown in Figure 15. The compensator builds on the type 2 compensator by adding an additional zero and pole combination. The additional components are a resistor and capacitor put in parallel with the high side resistor of the output voltage divider. The type 3 compensator has 3 poles and two zeros. This yields a phase shift of +90 degrees.

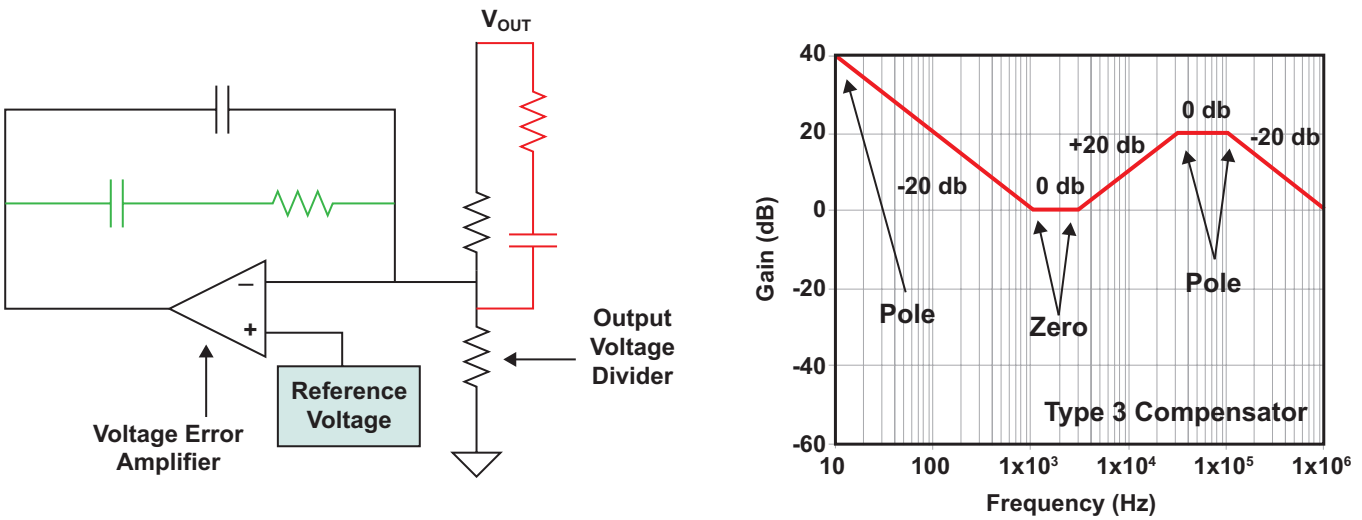


Figure 15 – Simplified type 3 compensator.

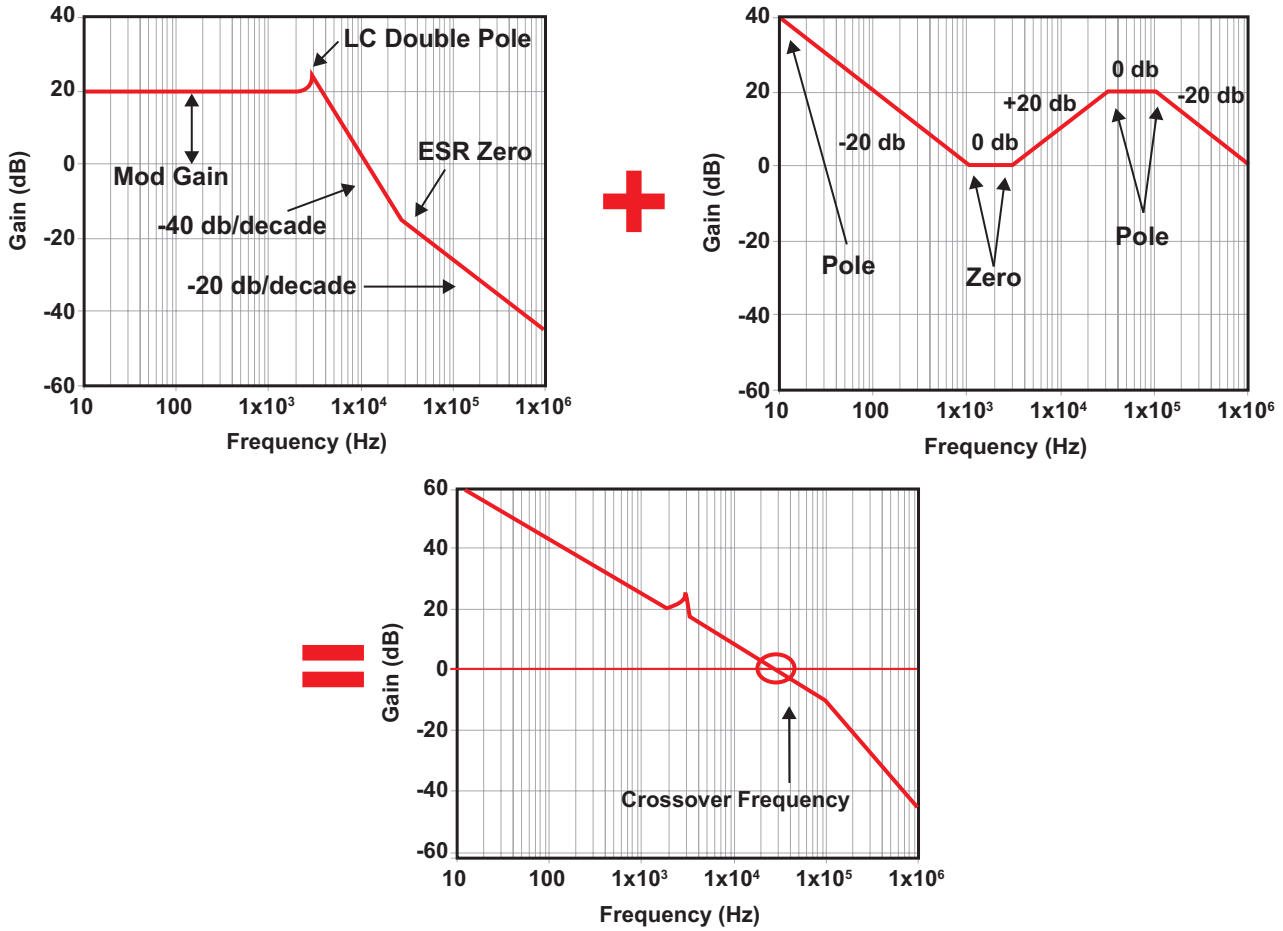


Figure 16 – Full loop response for voltage mode control.

E. VMC Control Loop

Taking the three parts of the voltage mode controlled power supply and adding them all together yields the full control loop. Figure 16 shows how all of the parts come together. The goal of the loop analysis is to provide sufficient bandwidth to handle the load and line transients. The loop must crossover 0 dB with a -20 dB/decade slope, also termed a minus 1 slope, and maintain at least 45 degrees of phase margin.

F. Pulse Width Limitations

Minimum controllable on-time is an issue seen in fixed frequency converters. There are fixed propagation delays that limit how fast a pulse to the gate drivers can be terminated. Equation 6 shows how the minimum pulse width is calculated for a given buck converter.

$$T_{on_{min}} \leq \frac{V_{OUT}}{V_{in\,max} \cdot f_{max}} \qquad (6)$$

If the calculated value for the on-time is less than the specification for the IC then pulse skipping occurs to maintain the output voltage. This leads to abnormal and increased output voltage ripple patterns. In order to prevent pulse skipping, the frequency is reduced.

G. Closed Loop Transient Performance

Earlier, transient response was briefly discussed in relation to choosing the L and C for the output filter. The equations described there balanced the energy in the inductor versus the charge in the output capacitor. In reality, it is not that simple. The bandwidth of the control loop also plays a role in the response time and voltage deviation of the output. Figure 17 shows a graphical depiction of the two terms.

The loop bandwidth is directly proportional to voltage deviation and the speed of recovery. The higher the crossover frequency, the lower the voltage deviation and faster the recovery. Closing the control loop decreases the output impedance

of the power stage. For a buck converter, the output filter dominates the output impedance. A simple way to estimate the voltage deviation is to multiply the load step amplitude by the impedance of the output filter at the crossover frequency, as shown in Equation 7. More information can be found in the references.

$$\Delta V_P + \Delta I_{step} \cdot Z_{OUT@fc0} \quad (7)$$

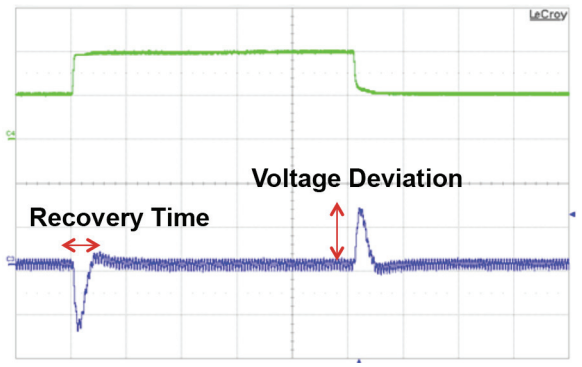


Figure 17 – Output voltage response to a load step.

H. VMC Summary

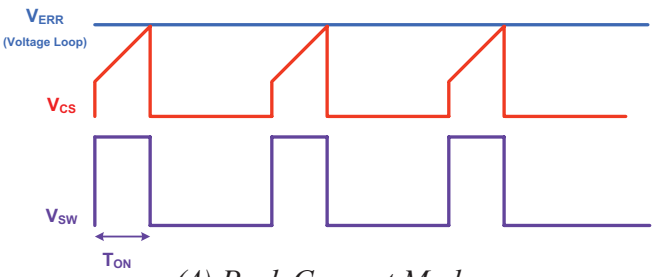
Voltage mode control offers a lot of advantages and a few challenges to overcome. Table 1 lists a few of the advantages and disadvantages of the VMC technique.

Advantages	Disadvantages
Fixed frequency operation	High bandwidth error amplifier required
Easy to synchronize	Double pole compensation is more difficult
Voltage regulation is independent of load	Inductor value affects the compensation
Single feedback loop	Vin affects loop gain (unless using feed forward)
Less susceptible to noise	Difficult to control light load efficiency modes
Good load regulation	Multiphase operation requires an extra current sharing loop

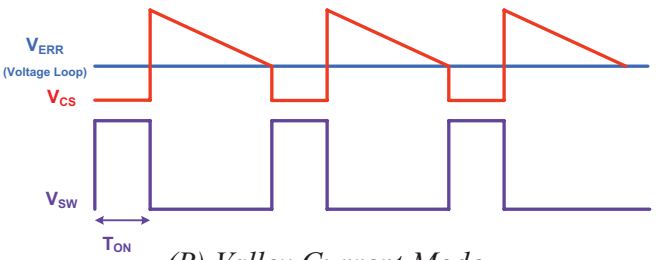
Table 1 – Voltage mode control.

III. Current Mode Control

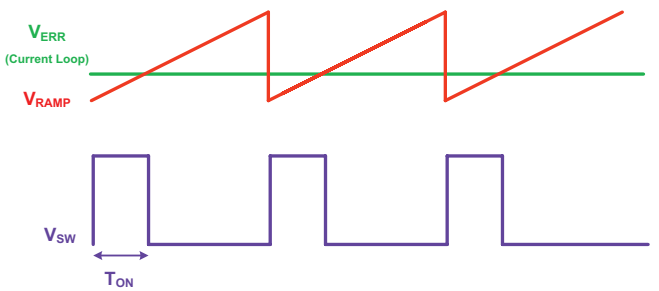
In current mode control, a buck converter controls the inductor current in order to regulate the output voltage. Current mode control can be categorized in two ways: 1) peak (or valley) measured current mode control and 2) average current mode control. In peak current mode, an inner loop regulates the peak inductor current. With valley current mode, the inductor's valley current is regulated. By regulating average inductor current, noise sensitivity issues are eliminated, as compared with peak or valley current mode control methods.



(A) Peak Current Mode



(B) Valley Current Mode



(C) Average Current Mode

Figure 18 – Current mode control PWM methods.

The most popular current mode control scheme is peak current mode. Figure 19 shows a block diagram for the peak current mode control. An inner loop controls the converter duty cycle so that the feedback current is equal to a control voltage. The inner current control loop is a sampled data

loop. Peak inductor current feedback is sampled and held until the next switching cycle. The control voltage is generated by the outer loop to maintain output voltage regulation. In this way, the outer loop determines the level of current necessary to deliver the proper output voltage for any load condition.

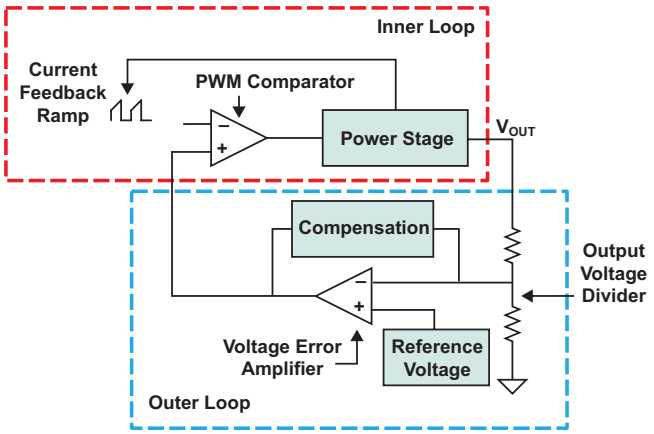
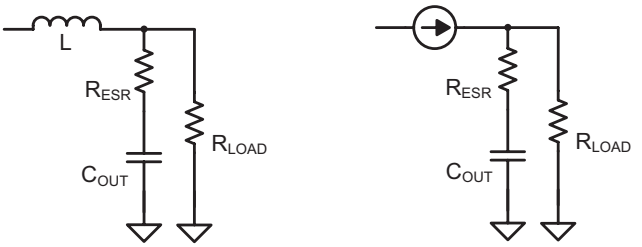


Figure 19 – Peak current mode control block diagram.

A. Current Mode Control vs. Voltage Mode Control

While voltage mode control regulates duty cycle to control output voltage directly, current mode control regulates duty cycle to deliver the inductor current required to control the output voltage. Because the inductor current is regulated, the LC resonance in the output filter is avoided and the inductor can be modeled as an ideal current source.



(A) Voltage Mode *(B) Current Mode*

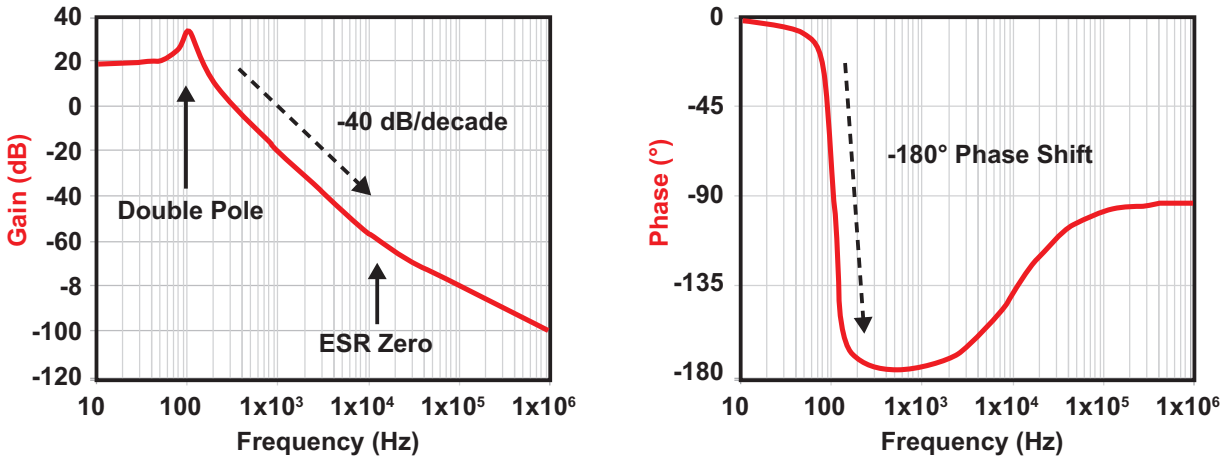
Figure 20 – Output filter model.

By replacing the inductor with a current source in the current-sampled system, the LC double pole in the control-to-output transfer function is split. One pole moves to a lower frequency and becomes a single load pole, which is easily compensated by the type 2 compensator. The other pole moves higher to one half of the switching frequency.

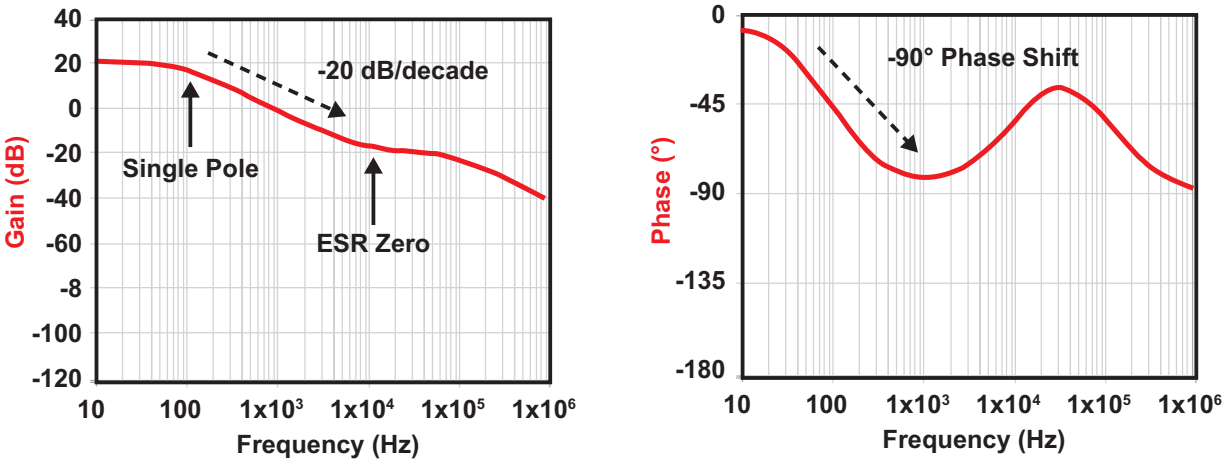
Figure 21 compares the control-to-output transfer functions between voltage mode and current mode control. In current mode control, the gain drops at 20 dB per decade after a single load pole and the phase shifts 90°, while the gain drops at 40 dB per decade after the LC double pole and the phase shifts 180° in voltage mode control. Equation 8 shows how to calculate the load pole in current mode control. ESR zero frequency is determined per Equation 9 in both voltage and current mode control.

$$F_{load\ pole} = \frac{1}{2\pi R_{LOAD} C_{OUT}} [Hz] \quad (8)$$

$$F_{ESR\ zero} = \frac{1}{2\pi R_{ESR} C_{OUT}} [Hz] \quad (9)$$



(A) Voltage Mode

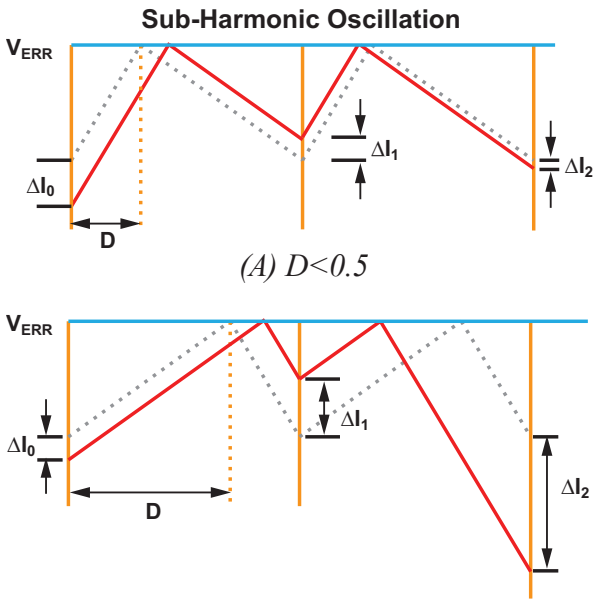


(B) Current Mode

Figure 21 – Control-to-output transfer function.

B. Sub-Harmonic Oscillation and Slope Compensation

Sub-harmonic oscillation is alternation of wide and narrow pulses at the switching node. Figure 22 compares inductor current waveforms in peak current mode control when the duty cycle is less than 50% and greater than 50%. Assuming, for this example, the output voltage has no ripple and the error amplifier output is constant, a perturbation ΔI_0 at the start of the first switching cycle becomes larger at the next switching cycle if the duty cycle is greater than 50%. This instability results in the sub-harmonic oscillation.



(A) D<0.5

(B) D>0.5

Figure 22 – Inductor current after a perturbation.

Additional slope dampens the sub-harmonic oscillation in current mode control. Figure 23 shows waveforms at the input of the PWM comparator with additional slope on top of the sensed inductor current. Because the rising slope, including the additional slope, is greater than the falling slope at the input of PWM comparator as shown in Figure 23, the perturbation ΔI_0 at the start of the first switching cycle is effectively damped and is attenuated at the next switching cycle. Ideally, the sub-harmonic oscillation occurs when the duty cycle is greater than 50% (D>0.5) in peak current mode control.

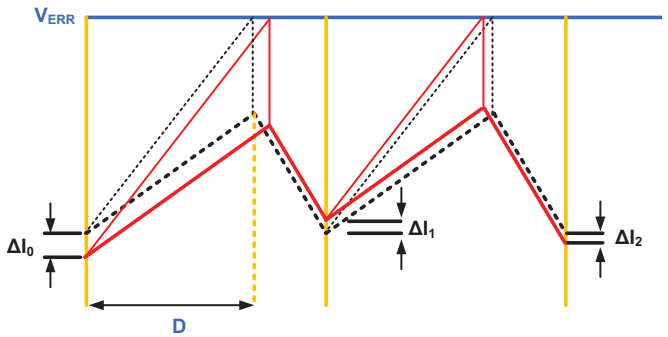


Figure 23 – Slope compensation.

C. Type 2 Loop Compensation

The type 2 compensator is widely used in the current mode buck converter.

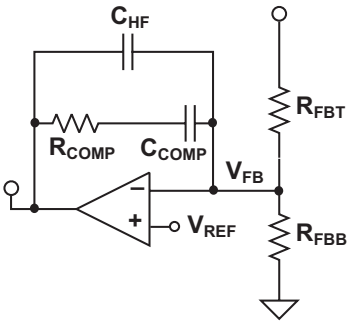
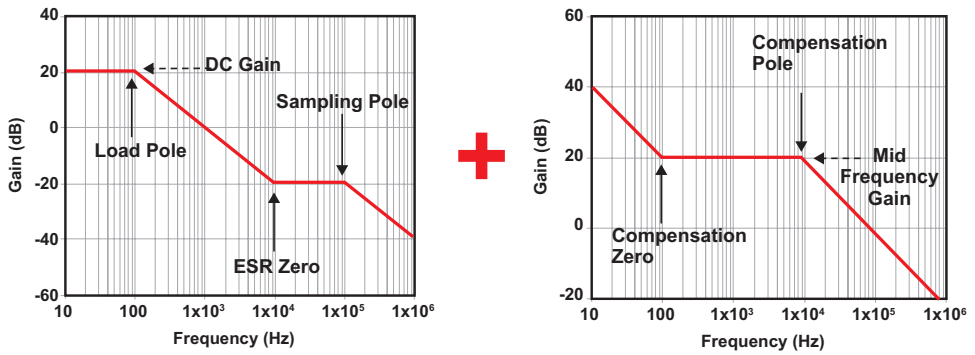
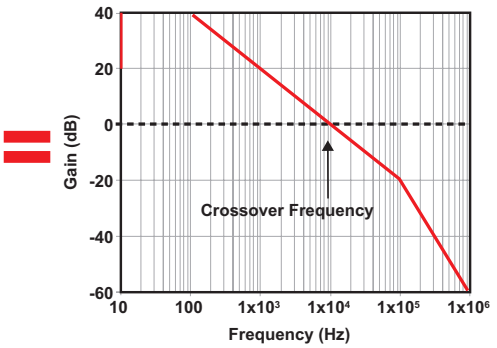


Figure 24 – Type 2 compensation.

This configuration places a pole at DC, a mid-frequency zero and a high frequency pole as shown in Figure 25 (B). The pole at DC minimizes steady state output error. By placing the mid-frequency zero at the power stage load pole and the high frequency pole at the ESR zero, the poles and zeros of the power stage and the compensation tend to cancel, yielding a straight-line frequency response curve. As a result, the open loop response crosses over 0 dB (unity-gain) with a single pole response and 90 degree phase shift as shown in Figure 25 (B).



(A) Control-to-output + output-to-control responses



(B) Full loop response for current mode control

Figure 25 – Current mode control loop responses.

D. Leading Edge Spike and Blanking

The inner loop monitors inductor current at every cycle and may be sensitive to current sensing noise. Figure 26 shows a way to sense the rising slope of the inductor current in the peak current mode control.

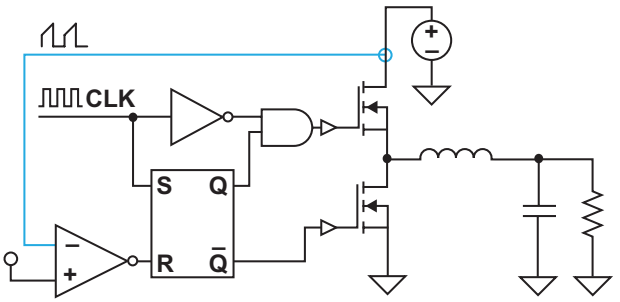


Figure 26 – Peak current mode current sensing.

When the high-side switch turns on and the body diode of the low-side MOSFET turns off, a large reverse recovery current flows, creating a leading edge spike as shown in Figure 27. This spike should be filtered or blanked to prevent a false trip of the PWM comparator.

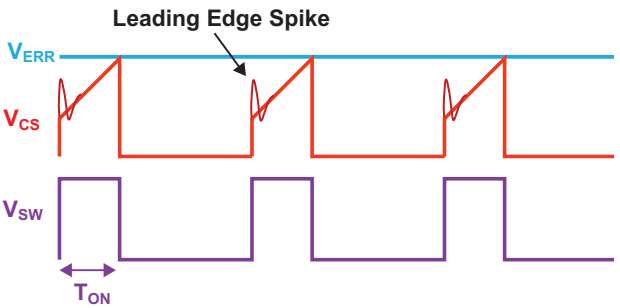


Figure 27 – Peak current mode leading-edge spike.

E. Summary of Peak Current Mode Control

Advantages	Disadvantages
Single-pole system allows simple Type 2 compensation	Need for slope compensation to eliminate sub-harmonic oscillation
Inherent feed forward improves line transient performance	Noise sensitivity at leading edge spike
Easy implementation of cycle-by-cycle current limit	Need for relatively long minimum on-time (peak current mode)
Easy current share across multiple converters	

Table 2 – Peak-current mode control advantages and disadvantages.

F. Current Mode vs. Emulated Current Mode

Emulated current mode control is intended to mitigate issues caused by a leading edge spike, such as distortion of the sensed inductor current by an RC filter, or a limitation of minimum controllable on-time by blanking the leading edge of the sensed waveform.

Figure 28 shows a block diagram for emulated peak current mode control. The roles of the inner and outer loops are the same as conventional peak current mode control, however now the inner loop sensing of the load current is achieved differently.

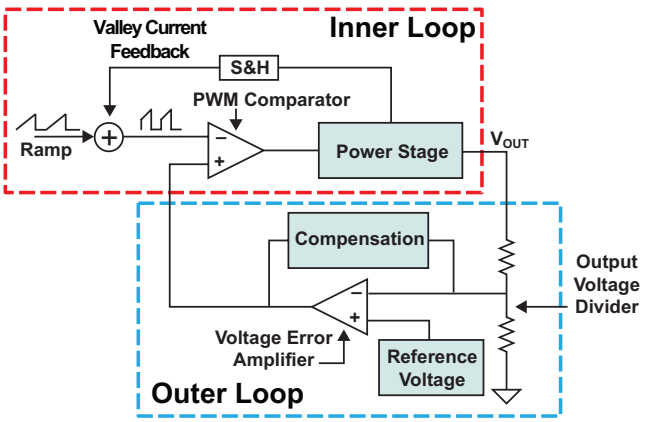


Figure 28 – Emulated current mode control diagram.

Emulated current mode control does not actually measure the high-side switch current but, rather, reconstructs an equivalent signal using low-side current sensing and summing an "emulated ramp".

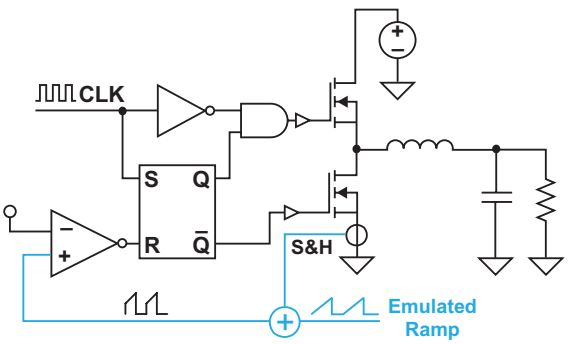


Figure 29 – Emulated peak current mode current sensing.

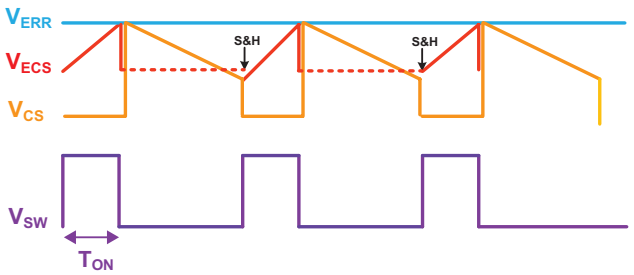


Figure 30 – Emulated peak current mode PWM input.

G. Emulated Current Mode Ramp Reconstruction

The reconstruction of the sensed inductor current consists of a sample-and-hold, to provide the DC level, summed with a saw-tooth waveform providing an emulated inductor current ramp. The sample-and-hold builds the DC level, which is derived from the low-side current sensing. The voltage across the sense resistor is sampled just before the high-side switch turn-on and held until the next switching cycle.

The positive ramp signal of conventional peak current mode control is emulated by C_{RAMP} and two current sources within the controller. During the high-side switch on-time, a current source proportional to V_{IN} - V_{OUT} emulates inductor current positive slope. By selecting C_{RAMP} according to Equation (10), a 25 µA source generates an additional ramp for slope compensation.

$$R_S \times A_S = \frac{5\mu \times L}{C_{RAMP}} \qquad (10)$$

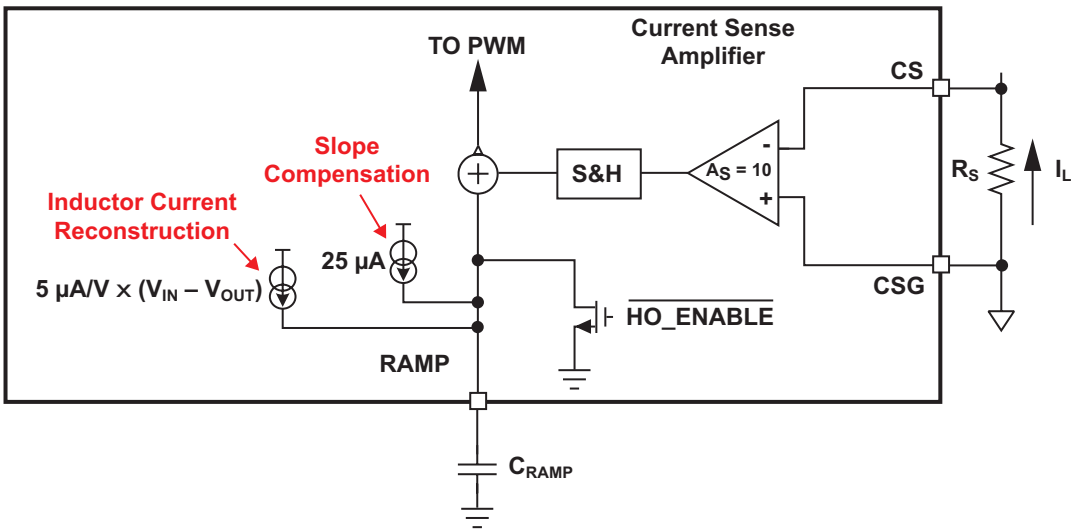


Figure 31 – Ramp generation block.

$$RAMP = \left(5\ \mu A / V \times (V_{IN} - V_{OUT}) + 25\ \mu A\right) \times \frac{t_{ON}}{C_{RAMP}}$$

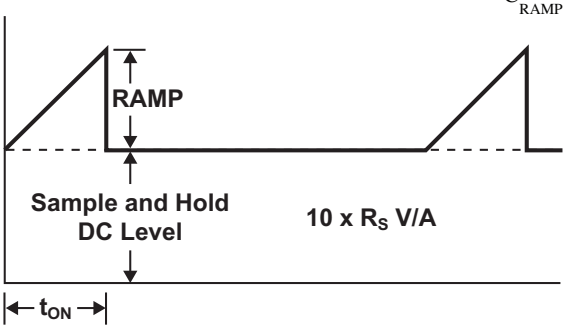


Figure 32 – Ramp reconstruction.

H. Comparison of Peak Current Mode and Emulated Current Mode Control

Table 3 shows the comparisons of emulated current mode and peak-current mode control.

Advantages	Disadvantages
Noise immunity at leading edge spike	Requires relatively long minimum off-time vs. peak current mode
Enables relatively short minimum on-time vs. peak current mode	

Table 3 – Emulated current mode control advantages and disadvantages.

IV. Summary

While this topic has only covered the fixed frequency control portion of the whole picture, Table 4 below outlines the fundamental differences between both fixed frequency and variable frequency control for comparison. Both offer good output regulation though, with a variable frequency approach, an amplifier is a necessary addition to the basic control approach as will be seen in Topic 2 "Choosing the Right Variable Frequency Buck Regulator Control Strategy".

	Fixed Frequency Control	Variable Frequency Control
Output voltage regulation	Yes	Yes
Synchronize to system clock	Yes	No
Fast transient response	Latency of at least one period	Low latency
EMI spectrum	High peaks, low average	Low peaks, higher average
Minimum controllable pulse width	An issue with high frequency and high conversion ratios	May be fixed (COT)
Loop compensation	Relatively fixed to an application circuit	May be used in multiple applications with little "tuning"

Table 4 – Summary of fixed frequency versus variable frequency control.

V. References

[1] Lynch, Brian, "Under the Hood of Low Voltage DC/DC Converters," SEM-1500 Power Supply Design Seminar, Texas Instruments, 2004.

[2] Lynch, Brian, "Feedback in the Fast Lane," SEM-1700 Power Supply Design Seminar, Texas Instruments, 2006.

[3] Dixon, Lloyd H., "Current-Mode Control of Switching Power Supplies," slup075, Texas Instruments.

[4] Dixon, Lloyd H., "Average Current Mode Control of Switching Power Supplies," slup091, Texas Instruments.

[5] Sheehan, Robert, "Current-Mode Modeling For Peak, Valley and Emulated Control Methods," Texas Instruments.

[6] Erickson, Robert W., "Fundamentals of Power Electronics."

[7] Ridley, Ray, "A More Accurate Current-Mode Control Model," slup122, Texas Instruments.

[8] Betten, John and Kollman, Robert, "Easy Calculation Yields Load Transient Response," Power Electronics Technology, February 2005.

[9] Li, J. and Lee, F. C., "Modeling of V2 Current-Mode Control," IEEE Trans. Circuit and Systems: Part I, vol. 57, no. 9, pp. 2552-2563, Sept. 2010.

Note: Design examples are located at the end of Topic #2.

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