ANALOG edge℠

Minimizing FET Losses for a High-Input Rail Buck Converter

Application Note AN-1628

William Stokes, Applications Engineer

Engineers often face the challenge of choosing the input voltage rail that works best for the DC-DC converter at the Point-of-Load (POL). High voltage rails, above 12V, usually demand intermediate regulation stages that reduce overall efficiency and add to cost. However, the new generation of regulator and controller ICs afford POL regulation from these high input rails directly. Typically the buck regulator is employed as the POL workhorse but its efficiency is highly dependent on the optimization of the High-Side (HS) and Low-Side (LS) MOSFET (FET) combinations. At lower input voltages it is often possible to use the same HS and LS FETs, yet for higher input voltages the selection criteria for these FETs are different, and will be the subject of this application note.

Buck Converter Loss Mechanisms

The schematic in ***Figure 1*** shows the basic architecture for a DC-DC buck (or step-down) voltage regulator circuit that employs the LM5116 as the Pulse Width Modulator (PWM) switch controller. The critical current path is from V_{IN} through the HS FET to the output via the inductor; and alternately, from ground through R_S and the LS FET to the output. Power losses due to the FETs along this path tend to dominate all other losses.

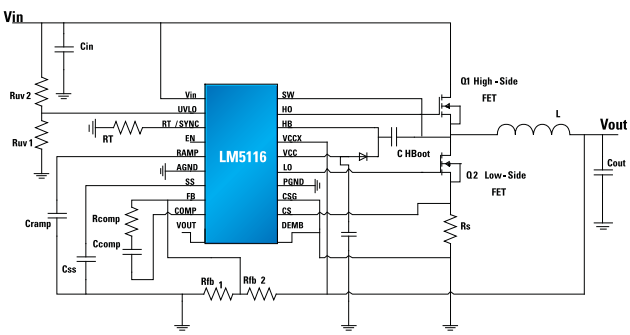

Figure 1. Synchronous Buck Regulator Schematic

Losses occurring in the FETs are a combination of conduction losses in the channel of the FET and switching losses during the turn-on and turn-off transitions. Conductive losses are proportional to the RMS current through each FET, and ignoring the ripple current in the output inductor, are often approximated (for the HS and LS respectively) by the following:

$$P_{QHS} = I_{OUT}^2 \cdot R_{DHS} \cdot D \text{ and}$$
$$P_{QLS} = I_{OUT}^2 \cdot R_{DLS} \cdot (1-D) \quad \text{(Eq. 1)}$$

In these equations I_{OUT} is the output current, R_{DHS} and R_{DLS} are respectively the on-resistances of the HS and LS FETs, D is the duty cycle of the HS FET and $(1-D)$ is the duty cycle of the LS FET.

The duty cycle, D, is given by $D = \frac{V_{IN}}{V_{OUT}}$ **(Eq. 2)**

The switching behaviors of the HS and LS FETs in the buck regulator differ from each other and this difference can be understood with the aid of ***Figure 2.***

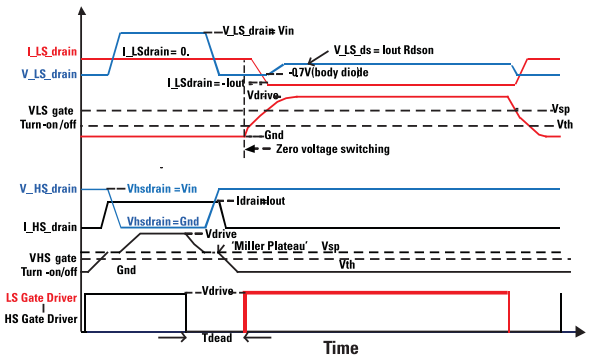

Figure 2. Basic Switching Characteristics (not to scale) for HS and LS FET Operating in a DC-DC Converter Application

The LS FET exhibits zero-voltage switching. First of all, the gate voltage, V_{LSgate}, turns the FET on while the FET's body diode is conducting. Then, when the gate turns the FET off, the load current will continue to flow in the same direction but now through the body diodes, such that the drain voltage stays near zero. Thus the attendant switching losses are negligible in both cases.

The main switching loss caused by the LS FET occur in the gate driver due to the charging and discharging of its gate capacitance. At higher frequencies in high power systems this can impose an upper limit on the number of LS FETs that can be used in parallel to reduce the on-resistance. The increase in gate drive power required as more FETs are used in parallel can exceed the reduction in conduction losses.

Switching losses are significant in the HS FET because its drain-source voltage is equal to V_{IN} and its drain current is approximately equal to I_{OUT} at both turn on and

turn off, leading to large overlap losses. The switching losses are approximated by

$$Psw_{Q1} = \frac{1}{2} \cdot V_{in} \cdot I_{out} \cdot f_{sw} \cdot (tsw_{HS\_rise} + tsw_{HS\_fall}) + Q_{gs} \cdot V_{GH} \cdot f_{sw} + \frac{1}{2} \cdot C_{oss} \cdot V_{in}^2 \cdot f_{sw}$$

(Eq. 3)

where f_{SW} is the switching frequency; tsw_{HS_rise} is the time it takes the gate voltage to rise from its threshold value to the end of the plateau interval; tsw_{HS_fall} is the time it takes the gate voltage to fall from the beginning of the plateau interval to the threshold value; Q_{gs} is the total gate charge of the FET; C_{oss} is the FET's drain-source capacitance; and V_{GH} is its gate drive voltage. The determination of the fall and rise times is beyond the scope of this article, but the relevant equations can be found in the web-published application notes of various MOSFET vendors.

The first term on the right hand side in ***Eq. 3*** is the power lost in the FET due to the simultaneous high drain current and drain-source voltage at turn on and off already mentioned. The second term is the power required by the FET's gate, (which is dissipated in the gate driver). The third term is the power dissipated in charging the parallel combination of the LS and HS FETs' output capacitance.

Another switching loss that occurs in the HS FET is due to the reverse recovery of the LS FET's body diode. This loss can be virtually eliminated at low currents (<5A) by paralleling a schottky diode with the LS FET.

Design Lessons

The following generalizations are based on the above equations and should give further insight into FET selection:

1) Switching losses increase for larger gate and drain capacitance and these capacitance are inversely proportional to the on-resistance. FETs with the lowest on-resistance inevitably have the higher capacitance hindering HS switching speed.
2) Reducing the switching clock frequency reduces switching losses; that is, at lower frequencies the losses during on/off transitions become a diminishing proportion of the total on-time of the FET causing conduction losses to increasingly dominate.
3) For higher input voltages relative to the output voltage the duty cycle of the HS FET decreases causing the switching losses to increasingly dominate.
4) In order to further reduce conduction losses, multiple, parallel, LS FETs are often employed. The number of parallel FETs is determined ultimately by cost, the gate driver's ability to drive them, and the point of diminishing returns.

The engineer should be aware that in most POL applications, especially for input voltages higher than 12V, the switching losses will likely dominate all other losses. ***Equation 3*** shows that under these circumstances the lowest overall losses in the HS FET are not necessarily achieved by using a device with the lowest on-resistance. The FET must be selected to minimize the sum of all the losses. The FET's on-resistance must be optimized at a higher value to achieve reduced capacitance and so reduce the switching losses. The major MOSFET vendors now provide "reduced charge, fast switching " MOSFETs which are optimized in this way for high-side buck applications.

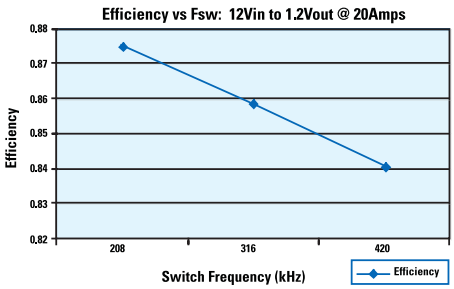

Figure 3. DC-DC Converter Measured Data Showing the Efficiency as a Function of the Switching Frequency

If optimizing the FETs does not enable high enough efficiency in a system, the switching frequency can be reduced to decrease the switching losses and improve the efficiency. This, however, can result in a physically larger system. ***Figure 3*** is an example of measured data from a generic evaluation board. The efficiency of this board was measured at various switching frequencies without changing any components on it except for the frequency-setting resistor. Though the conduction losses increased as the switching frequency was reduced (due to increased ripple currents), the overall efficiency went up because the switching losses in the HS FET decreased. The graph shows that changing the switching frequency has a dramatic effect on the switching losses.

The foregoing discussions have made clear that to achieve maximum efficiency in a high input voltage buck converter, the high side MOSFET must be carefully selected to minimize the sum of the switching and conduction losses. ■

The author wishes to acknowledge Haachitaba Mweene for his help with writing this article.

National Semiconductor
2900 Semiconductor Drive
Santa Clara, CA 95051
1 800 272 9959

Mailing Address:
PO Box 58090
Santa Clara, CA 95052

National Semiconductor
The Sight & Sound of Information