Eliminate the Guesswork in Selecting Crossover Frequency

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Rather than arbitrarily choosing a converter's crossover based on the switching frequency, you can analytically determine the relationship between its crossover and its undershoot in response to a load step.

In most power-supply design examples it is common to arbitrarily place the crossover frequency at one-fifth or one-tenth the switching frequency. However, the crossover frequency actually affects the converter's output impedance and there is a true relationship between these two parameters. Therefore, once a designer selects the output capacitor based on its operating parameters such as rms current, temperature or acceptable voltage ripple, the designer can analytically select the crossover frequency to match the desired output undershoot.

This discussion shows how to derive the relationship that links crossover frequency and undershoot and describes how to tailor the bandwidth to fit exactly the converter's design requirements.

Simplified Buck Converter

Fig. 1 shows a simplified buck converter represented by a square-wave generator driving a low-pass filter. Both the inductor and the capacitor have ohmic losses. The output impedance of such a network can be derived with the input source shorted:

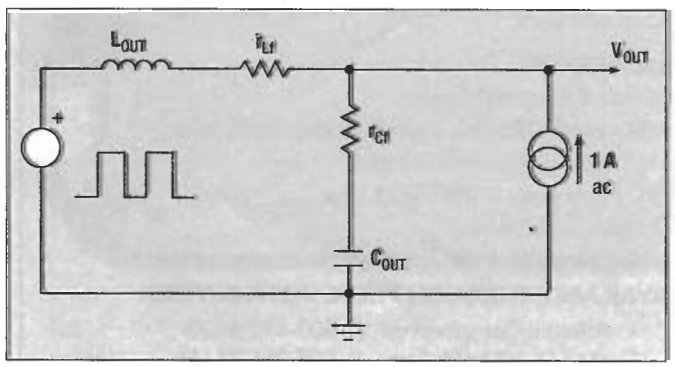

Fig. 1. *A current source ac sweeps the output impedance of a simplified buck converter represented by an output inductor and capacitor, plus parasitics.*

$$Z_{OUT}(s) = (sL_{OUT} + r_{Lf}) \| \left(r_{Cf} + \frac{1}{sC_{OUT}} \right), \quad \text{(Eq. 1)}$$

where Z_{OUT} equals the output impedance in ohms, L_{OUT} equals the output inductance in henrys, C_{OUT} equals the output capacitance in farads, r_{Lf} equals the inductor resistance in ohms and r_{Cf} equals the C_{OUT} equivalent series resistance (ESR) in ohms.

Through inspection, the designer can see that the inductor's resistance dominates the output impedance at dc (L_{OUT} is shorted and C_{OUT} is open) and that its inductance dominates as the frequency increases. Then the capacitor impedance starts to take over until it becomes a short circuit and leaves the impedance value to its series loss r_{Cf}.

By connecting a 1-A ac source to the output, the designer has the ability to quickly plot the output impedance versus frequency using a SPICE simulator. Fig. 2 portrays the obtained results. As can be seen, a peaking occurs at the resonant frequency (f_0). The maximum of this peaking can be analytically derived[1]:

$$Z_{OUT_{MAX}} = \frac{Z_0^2}{R_{Lf}} \sqrt{1 + \left(\frac{R_{Lf}}{Z_0} \right)^2}, \quad \text{(Eq. 2)}$$

where $Z_{OUT_{MAX}}$ equals the maximum output impedance in ohms and $Z_0 = \sqrt{L_{OUT}/C_{OUT}}$ equals the characteristic impedance of the filter in ohms.

Such peaking is typical of a buck output impedance behavior where the LC filter has been optimized to minimize the losses. This situation induces a high-quality coefficient, hence a severe peaking in the impedance graph. One of the feedback aims is to minimize the output impedance to reduce as much as possible the voltage drop due to a load step. On an amplitude versus frequency plot, the natural output impedance of the filter dramatically peaks at the resonant frequency. Therefore, if a crossover frequency below the LC filter resonance is selected, there will not be enough of a gain

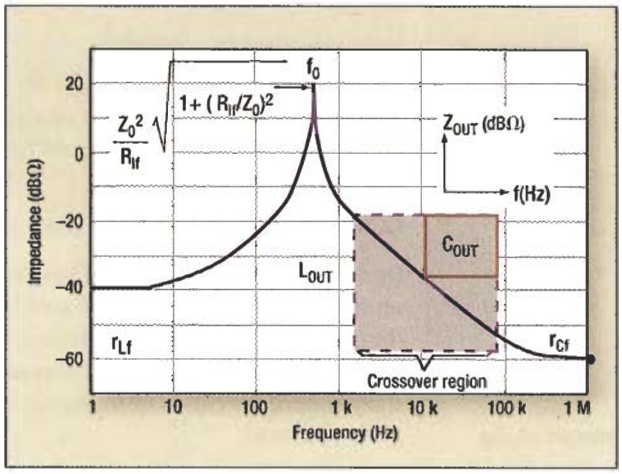

Fig. 2. *As shown by Eq. 1, a converter's ohmic losses dominate its output impedance at both extremes of the plot (f = 0 and f = ∞) of amplitude versus frequency; a peaking occurs at the resonant frequency (f_0).*

to get rid of the resonance and, despite a good phase margin, the system will oscillate. If the designer wants to obtain a good transient response, he or she has to make sure the loop gain remains high enough to tame the peaking when it occurs. In other words, the crossover frequency (f_C) must be selected at least three to five times above f_0.

In Fig. 2, if a crossover region is selected beyond the resonance, the designer can see an impedance graph dominated by the output capacitor impedance (C_{OUT}). At the crossover frequency, this impedance is:

$$Z_{OUT_{OL}}(f_C) \approx \frac{1}{2\pi f_C C_{OUT}}, \quad \text{(Eq. 3)}$$

where f_C equals the crossover frequency and $Z_{OUT_{OL}}$ equals the open-loop output impedance.

Above the crossover frequency, the capacitor's ohmic losses dominate the network's output impedance. To ensure Eq. 3 rules the output impedance alone at the crossover point, the capacitor ESR must be much smaller than the output impedance at the crossover frequency. Mathematically, the following condition must be met:

$$r_{Cf} \ll \frac{1}{2\pi f_C C_{OUT}}. \quad \text{(Eq. 4)}$$

In choosing the final capacitor, besides ripple current and temperature considerations, the designer must also consider the capacitor ESR at the selected crossover frequency.

Closing the Loop

Picture any voltage generator with an equivalent circuit associating a dc source V_{TH} and an output resistor R_{TH}. According to Thévenin's theorem, V_{TH} is evaluated by measuring the output voltage on an unloaded converter and R_{TH}

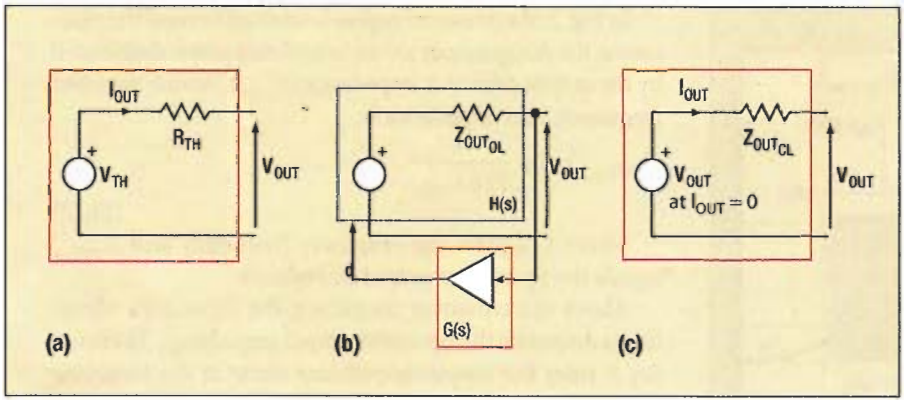

Fig. 3. *Implementing loop control on a converter improves several parameters along with the output impedance: (a) open-loop buck converter produces V_{OUT} for a given V_{IN}, (b) open-loop impedance for a given V_{IN} with Z_{OUT} open loop ($Z_{OUT_{OL}}$) and (c) closed-loop output impedance obeys Eq. 5 with Z_{OUT} closed loop ($Z_{OUT_{CL}}$).*

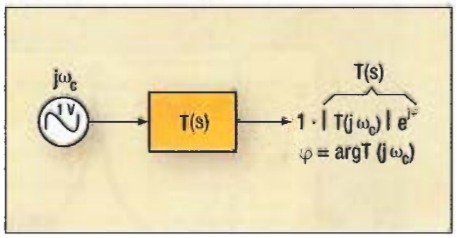

Fig. 5. *Sinusoidal signal also can be represented by a rotating vector expressed by the Euler notation, where φ represents the phase lag brought by the total chain when stimulated at the crossover frequency for a 1-V modulation.*

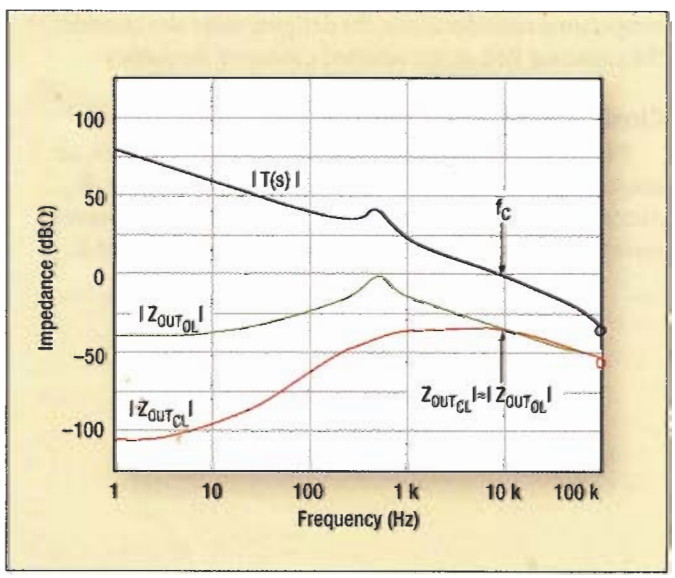

Fig. 4. *The open-loop output impedance ($Z_{OUT_{OL}}$) and the closed-loop output impedance ($Z_{OUT_{CL}}$) are both low at dc but rise with frequency. At low frequencies with a high open-loop gain, the output impedance remains extremely small. As the frequency increases, inductive behavior is seen.*

is found by measuring the output-voltage difference in two loading current conditions. Imagine that Fig. 3a depicts an open-loop buck converter using the Fig. 1 approach. Once loop control is installed through a compensator, bringing gain and phase boost as in Fig. 3b, the open-loop impedance transforms into a closed-loop output impedance that now obeys Eq. 5 (Fig. 3c):

$$Z_{OUT_{CL}}(s) \approx Z_{OUT_{OL}}(s)\frac{1}{1+T(s)}, \qquad \text{(Eq. 5)}$$

where $Z_{OUT_{CL}}(s)$ equals closed-loop output impedance for a loop gain of $T(s) = H(s)G(s)$.

The designer now has an output impedance whose value depends on the open-loop gain. At dc, for $s = 0$, assume a large loop gain to ensure good dc regulation. In other words, the feedback brings the open-loop impedance to a very low value. On the contrary, when the frequency increases, the gain reduces and when the crossover point is reached, the gain no longer acts upon the output impedance. Mathematically, this is:

$$\lim_{s\to 0}\left|Z_{OUT_{CL}}(s)\right| \approx 0 \qquad \text{(Eq. 6)}$$

$$\lim_{s\to s_C}\left|Z_{OUT_{CL}}(s)\right| \approx \left|Z_{OUT_{OL}}(s)\right|. \qquad \text{(Eq. 7)}$$

If a SPICE average model is used and a voltage-mode buck converter is compensated, there is the possibility to ac sweep its output impedance as was done in Fig. 2. The output impedance in Fig. 4 shows what Eqs. 5 and 6 predicted: Thanks to a high open-loop gain in the low-frequency domain, the output impedance remains extremely small, $(r_{Lf}/|T_0|)$. But as the frequency increases, inductive behavior can start to be seen. Then, at the crossover point, the loop gain reaches 0 dB and both the open-loop and closed-loop impedances are almost equal to the output capacitor impedance given by Eq. 3.

Approximate Output Impedance

Previously, the term "almost" has been used to compare the open- and closed-loop output impedances at the crossover frequency. However, try to see how close they are in the vicinity of the crossover point. There are several methods to calculate the module of Eq. 5's right term, $1/(1+T(s))$. One method applies a sinusoidal modulation to the complete chain made of the converter transfer function H(s) followed by the compensator transfer function G(s).

This is exactly what would be done in the laboratory to explore the true open-loop response of the compensated converter. However, in this particular case, rather than expressing the modulation signal through a classical form of $\hat{A}\sin(\omega t + \varphi)$, a phasor notation will be used where φ represents the phase lag brought by the total chain when stimulated at the crossover frequency. Following is what details for a 1-V modulation.

The phasor notation can be update using Euler's formula:

$$T(s)=|T(s)|e^{j\varphi}=|T(s)|[\cos(\varphi)+j\sin(\varphi)]. \quad \text{(Eq. 8)}$$

In this equation, the term φ relates to the phase difference between the output signal and the input modulation. A design criteria here is not φ but φ_m, the phase margin. To help link both, Fig. 5 shows the contribution of the loop to the total phase lag.

Based on the figure, it can be written:

$$-180=\arg T(j\omega_c)-\varphi_m. \quad \text{(Eq. 9)}$$

Solving for φ, we have:

$$\varphi=\arg T(j\omega_c)=\varphi_m-180. \quad \text{(Eq. 10)}$$

Based on Eq. 10, Eq. 8 can be updated as:

$$|T(j\omega_c)|e^{j\varphi}=|T(j\omega_c)|[\cos(\varphi_m-180)+j\sin(\varphi_m-180)]=$$
$$|T(j\omega_c)|[-\cos(\varphi_m)-j\sin(\varphi_m)]. \quad \text{(Eq. 11)}$$

Knowing that the loop gain module at crossover is 1, T(s) can be approximated as:

$$T(s)=-\cos(\varphi_m)-j\sin(\varphi_m). \quad \text{(Eq. 12)}$$

Based on this result, Eq. 5 can now be updated as:

$$|Z_{OUT_{CL}}(s)|=|Z_{OUT_{OL}}(s)|\left|\frac{1}{1+T(s)}\right|=$$
$$|Z_{OUT_{OL}}(s)|\left|\frac{1}{1-\cos(\varphi_m)-j\sin(\varphi_m)}\right|. \quad \text{(Eq. 13)}$$

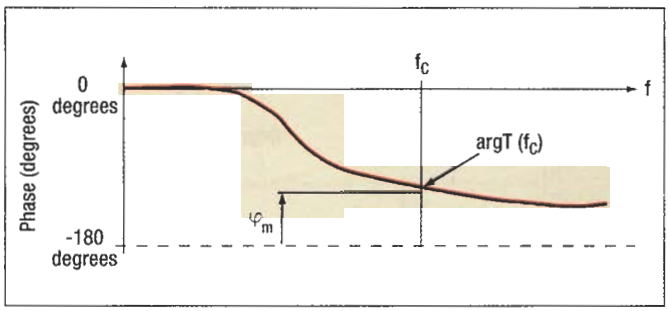

Fig. 6. *Contribution of the loop to the total phase lag, φ, relates to the phase difference between the output signal and the input modulation. Design criteria do not consider φ — but rather φ_M — the phase margin, which is the distance between φ and the -180-degree axis.*

Solving this equation yields:

$$|Z_{OUT_{CL}}(s)|\approx\frac{1}{2\pi f_C C_{OUT}}\frac{1}{\sqrt{2-2\cos(\varphi_m)}}. \quad \text{(Eq. 14)}$$

As can be seen, the module of the capacitor impedance is now affected by a term dependent on the phase margin. The variations of this term can now be plotted versus the phase margin as proposed by Fig. 6.

As observed, a phase margin below 60 degrees degrades

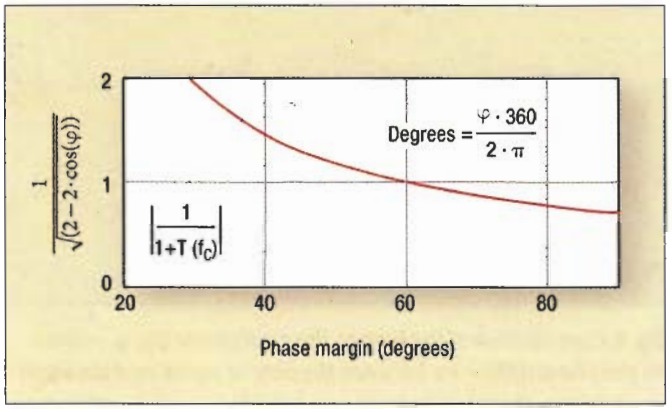

Fig. 7. *A phase margin below 60 degrees degrades the converter's output impedance, whereas it slightly improves it for a phase margin above 60 degrees.*

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Design Example

Assuming a power supply with an output capacitor of 1000 µF, the designer needs to make a choice considering the output-voltage ripple conditions and the corresponding rms current circulating in the capacitor. The specification here notes that there should be a maximum voltage drop of 80 mV when the converter undergoes a current step ΔI_{OUT} of 2 A. What bandwidth is needed to reach this parameter? If Eq. 3 is used and a 2-A step is applied, the voltage drop can be predicted:

$$\Delta V_{OUT} \approx \frac{\Delta I_{OUT}}{2\pi f_C C_{OUT}}. \quad \text{(Eq. 15)}$$

From this equation, it is easy to extract the minimum crossover point:

$$f_C \approx \frac{\Delta I_{OUT}}{\Delta V_{OUT} C_{OUT} 2\pi} = \frac{2}{80\times10^{-3}\times1\times10^{-3}\times2\pi} = 4 \text{ kHz}$$

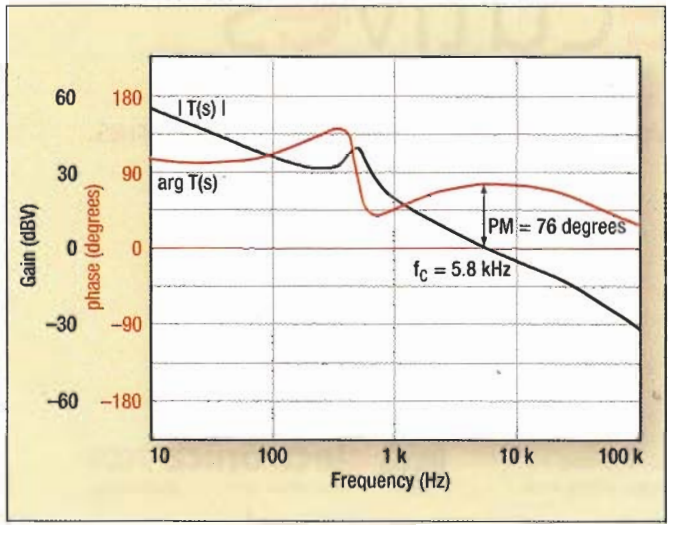

Fig. 8. *Voltage-mode buck converter's loop gain Bode plot SPICE simulation shows a crossover frequency of 5.8 kHz with a phase margin of 76 degrees.*

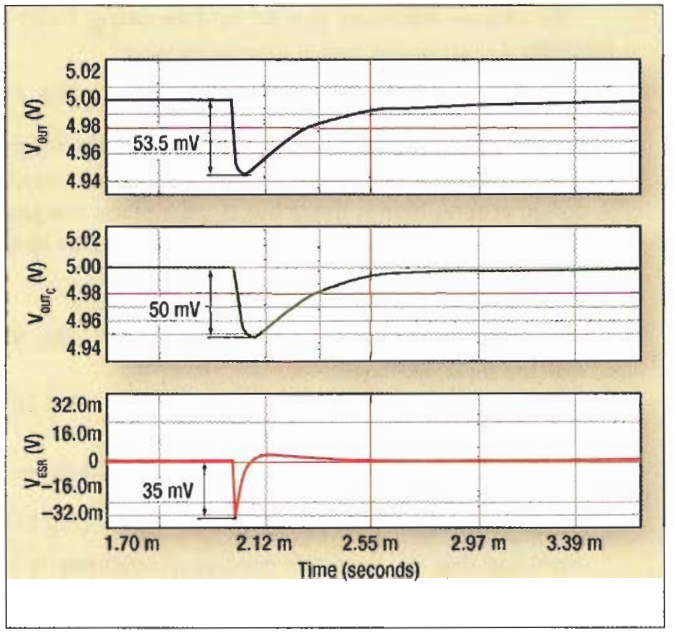

Fig. 9. *A step load ranging from 100 mA to 2.1 A in 10 µs produces a well-controlled undershoot, primarily due to the output capacitor's 35-mV ESR spike, and lasts only during the output current circulation in the capacitor.*

$$\frac{2}{80\times10^{-6}\times2\pi} = 4 \text{ kHz}. \quad \text{(Eq. 16)}$$

Based on this result, the designer must check that the capacitor ESR is lower than:

$$Z_{C_{OUT}} \text{at 4 kHz} = \frac{1}{2\pi\times4\times10^{3}\times10^{-3}} = 40 \text{ m}\Omega. \quad \text{(Eq. 17)}$$

A 1000-µF capacitor from the Panasonic FM series could be the right choice. From the manufacturer's data sheet, the capacitor has an ESR of 19 mΩ at 100 kHz. This ESR alone will contribute to a drop of $19 \times 10^{-3} \times 2 =$ 38 mV, which is 47% of the specification. To offer some margin in this design, increase the crossover frequency to 6 kHz and purposely compensate the converter to meet this goal.

Once compensated, the 5-V voltage-mode buck converter loop-gain Bode plot SPICE simulation appears in Fig. 7. It shows a crossover frequency of 5.8 kHz together with a rather comfortable phase margin of 76 degrees. The output-voltage drop is now going to split between the capacitor and its ESR term. Based on a 76 degree phase margin, the capacitive contribution can be approximated using Eq. 14:

$$\Delta V_{OUT_C} \approx \frac{2}{6.28\times5.8\times1\times10^{-3}} \frac{1}{\sqrt{2-2\cos(76)}} =$$

$$2\times27.4\times10^{-3}\times0.812 = 44.5 \text{ mV}. \quad \text{(Eq. 18)}$$

Now step load the output by a current source ranging from 100 mA to 2.1 A in 10 µs. Fig. 8 shows the simulation results. It can be seen that the total output undershoot is

well within the design goals with a theoretical 53.5-mV deviation. The ESR spike is 35 mV and lasts only during the output-current circulation in the capacitor. The capacitive contribution reaches 50 mV, which is a fairly good agreement with the Eq. 14 predictions.

As can be seen, the ESR term amplitude depends on the output-current step. When the load change is slow enough, the loop has a means to attenuate the ESR contribution. However, usually the transient loading conditions are so fast that all the current step translates into a voltage spike over the ESR. Given its steepness, the loop cannot fight it.

The situation degrades further if the output-current rate of change reaches high values, like in motherboard applications for instance. In that case, the inductive term called the capacitor's equivalent series inductance (ESL) starts to enter the picture and the situation worsens. In these extreme cases, the capacitor selection is almost solely based on the contribution of its parasitic terms and no longer on its capacitive value.

Therefore, the designer can analytically select a crossover frequency rather than arbitrarily choosing it based on the switching frequency. If the capacitor impedance plays a role in relationship with the selected crossover frequency, there are other terms whose contribution is out of control, such as the ESR and ESL of the output capacitor. They are respectively sensitive to the output-current step and the current slope. As loop control has almost no influence on their contributions, it is the designer's task to make sure these parasitic terms stay low enough to keep the overall transient response within the original specifications. **PETech**

References

1. Basso, Christophe, *Switch Mode Power Supplies: SPICE Simulations and Practical Designs*, McGraw-Hill, 2008.