

Single C-MOS IC forms pulse-width modulator

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A pulse-width modulator can be constructed with a single complementary-metal-oxide-semiconductor integrated circuit if the IC's field-effect transistors control the duty cycle of a free-running oscillator. The output resistance of the FET varies almost linearly with input voltage over portions of its characteristic curve, permitting the circuit to be used for applications in switching power supplies and analog conversion in data-communications systems.

This circuit uses a CD4007 dual complementary pair plus an inverter device, which comprises three n-channel and three p-channel enhancement-type MOS transistors. As shown in the figure, inverters I_1 and I_2 , each formed by two gates in the 4007, themselves form an astable multivibrator in conjunction with resistor R and capacitor C . The frequency of oscillation of the multivibrator is given by:

$$f = 1/1.4 RC$$

The 1-megohm resistor, left in the figure, limits the feedback current into I_1 . This prevents the input circuit from burnout and the inverter from switching prematurely and affecting the desired frequency of operation.

The two remaining gates in the 4007, one n-channel and one p-channel gate, are connected across the output of I_1 and R . This network is designed to modify R and

Single IC modulator. Pulse-width modulation is achieved by varying duty cycle of free-running oscillator in accordance with input voltage V_c . Output impedance of FETs shunts switching-time element R , permitting adjustable duty cycle.

thus control switching times t_1 and t_2 .

The oscillation (switching) times for this device may be expressed by two equations:

$$t_1 = RC \ln [(V_{dd} - V_{tr})V_{dd}]$$

and

$$t_2 = RC \ln (V_{tr}/V_{dd})$$

where t_1 is the on time and t_2 is the off time of the oscillator, V_{tr} is the threshold voltage at the gate's input, and V_{dd} is the supply voltage.

When the oscillator's output is high, diode D_1 may conduct. The p-channel output resistance will be in parallel with R , neglecting the diode's forward resistance. The p-channel gate's output resistance will decrease as V_c decreases.

Similarly, when the oscillator's output is low, D_2 may conduct, and the n-channel output is placed in parallel with R . The n-channel's resistance will decrease as V_c increases. The duty cycle of the oscillations (in other words, control of the on and off times) is variable from 1% to 99% of the operating frequency. The duty cycle is directly proportional to the amplitude of the control voltage V_c .

The component values in the figure yield an oscillation frequency of 1 kilohertz. The change in oscillation frequency as a function of duty cycle is minimal; although the basic frequency of oscillation is modified by the FETs across I_1 , the output impedance of one always increases, and the other's decreases proportionately, for any value of control voltage V_c . Thus, the average resistance shunted across R during a cycle is constant. □

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