High Performance Narrowband Receiver Design Simplified by IF Digitizing Subsystem in LQFP

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INTRODUCTION

Mobile radios are used for public safety and emergency services—police, fire and ambulances—as well as for private services such as fleet management. Increasingly, in order to provide enhanced services, along with improved spectral efficiency and coverage, the design of these radios has moved from traditional analog-based modulation schemes, such as FM and PM, to digital modulation approaches.

Receivers for these radios must be capable of accurately digitizing a low-level, high-frequency signal in the presence of large interfering signals. In radios using some narrowband land mobile standards, interfering signals can be 70 dB greater than the desired channel, with frequency offsets as little as 25 kHz. Since these systems usually are not cellular, the geographical coverage range of mobile radios is also an important feature—they must possess excellent sensitivity to recover low-level signals originating from subscribers at the fringe of the coverage range. As a further complication, these radios are often portable with high rates of usage; they demand low power consumption using smaller, longer-lived batteries.

As an aid to equipment designers, Analog Devices has made available the AD9870 IF Digitizing Subsystem, an IC designed to meet the demanding requirements of land mobile radio, and similar narrowband radio applications, with superheterodyne architectures employing analog and/or digital modulation schemes. The AD9870 integrates the entire IF strip with minimal external components. It can accept an IF signal at frequencies as high as 300 MHz, with bandwidths up to 150 kHz, and provides a serial data output containing 16-bit I and Q data, which can then be demodulated with a host processor. The AD9870 is intended for both base stations and subscriber units, combining the dynamic range required by base stations with the low power consumption needed by portable radios.

The big problem in all receivers is dynamic range

The dynamic range of a receiver determines its ability to recover low-level signals in the presence of larger signals, known as *blockers* and *interferers*. Figure 1 shows the various sources that can reduce the effective dynamic range of any radio receiver.

Assume for the moment that the only signal present in the spectrum is the "small target signal." The minimum detectable signal or sensitivity will be determined by the signal bandwidth (B), the receiver's detection threshold (SNR_{MIN}), the receiver's noise figure (NF), and inherent thermal noise limitations (kTB). At a temperature of 290 K, the sensitivity can be estimated with the following equation:

$$\textit{Sensitivity} = SNR_{MIN} + 10 \log(B) + NF + (-174 \text{ dBm/Hz})$$

Following are some of the potential noise sources:

Low-frequency 1/f noise becomes an issue if insufficient gain is applied to the target signal prior to down-conversion to frequencies below the 1/f corner of the process technology. DC components caused by offsets and second order distortion can also be problematic.

Large interferers can have their energy spread over a broad range of frequencies by the phase noise of the receiver's LO through a process known as "reciprocal mixing." The larger the interferer and the closer it is to the target signal, the more likely the target signal will be corrupted by the noise transfer mechanism. Also, if this interferer is large enough to induce nonlinearities in the receiver's front-end circuitry, it is possible for a spurious component to mix back into the target signal's passband. The "half-IF" problem is a specific case afflicting receivers with poor second-order linearity—in which an interferer falling halfway between the LO and the target signal generates a second order component that mixes with the LO's second harmonic to generate a spur falling on the target signal. The IIP2 specification of a receiver allows a receiver designer to quantify the "half-IF" spur. The difference, or Δ, between the interferer level, P_{IN}, and the resulting second-order spur is $IIP2 - P_{IN}$. With an IIP2 of 45 dBm, the AD9870 is mostly immune to this "half-IF" problem.
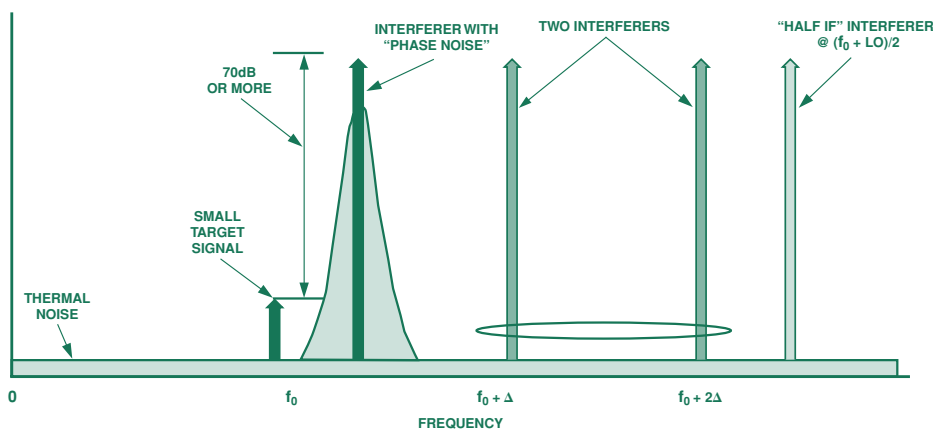

Figure 1. The "Big Problem" in all receivers is dynamic range.

Two large interferers at equally spaced frequency offsets (i.e., $f_0 + \Delta$ and $f_0 + 2\Delta$) from the target signal will result in a spurious component falling on top of the target signal through a process of intemodulation. The linearity of a receiver in this scenario is captured in its IIP3 specification with higher numbers representing a higher tolerance to third-order intermodulation. The difference, or Δ, between the two equal interferers, P_{IN}, and the resulting third-order intermodulation component is $2 \times (IIP3 - P_{IN})$. The AD9870 has a respectable IIP3 performance of –1 dBm, thus tolerating interferers as high as –45 dBm before degrading the receivers sensitivity.

Superheterodyne Architecture

To cope with large interferers that would otherwise degrade the receiver's ability to recover a target low-level signal, a superheterodyne architecture is used to translate an RF signal down to one or more intermediate (IF) frequencies where filtering of the adjacent interferer signals as well as amplification and gain control of the target signal is more practical. The superheterodyne scheme has been employed since World War I and is to this day the most popular of radio receiver architectures. A generic version employing this architecture, common among narrowband digital receivers, is shown by the signal-chain in Figure 2.

Prior to RF-to-IF down-conversion, a band-select filter (duplexer) and/or image reject filter selects the entire RF band within which the target signal operates. The low-noise amplifier (LNA), which provides amplification of the intended RF band prior to down-conversion, is critical in determining the receiver's sensitivity. The down-converted IF spectrum following the RF mixer often contains an array of signals of varying strengths in addition to the target signal. Channel selection and amplification occurs at IF: the target signal is selected from among the other signals via one or more crystal or SAW-type passive filters. After filtering, the target signal undergoes further amplification, with its signal strength stabilized at a preset level by an AGC loop to optimize the quadrature demodulation process. In many digital receivers, an IF analog quadrature modulator separates the IF signal into its quadrature baseband I and Q components, which are then digitized by a dual ADC. In such cases, the modulation accuracy of the demodulated signal is quite sensitive to analog offsets, quadrature LO mismatch, and I/Q gain mismatch in the quadrature modulator and dual ADC.

AD9870 Architecture

The AD9870 IF digitizing subsystem reduces the complexity of a typical superheterodyne receiver by integrating most of the IF, baseband, and some digital post processing functional blocks as shown in Figure 3.
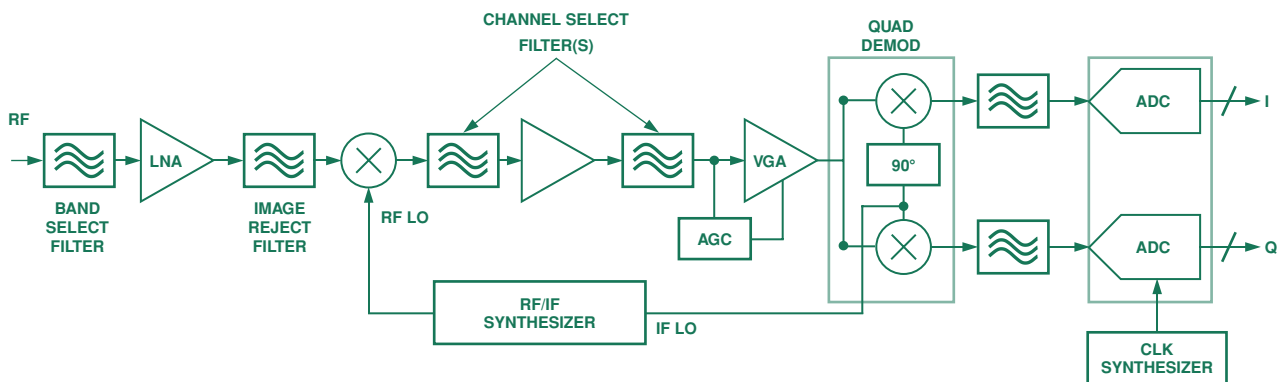

Figure 2. Typical superheterodyne architecture for a digital receiver.
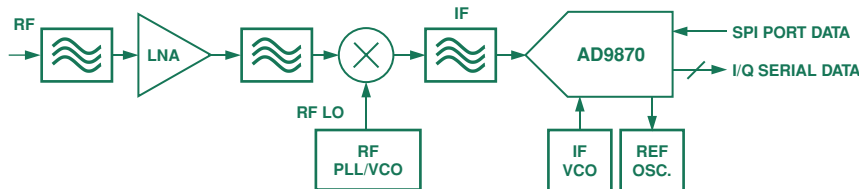

Figure 3. The AD9870 simplifies the digital receiver while enhancing performance.
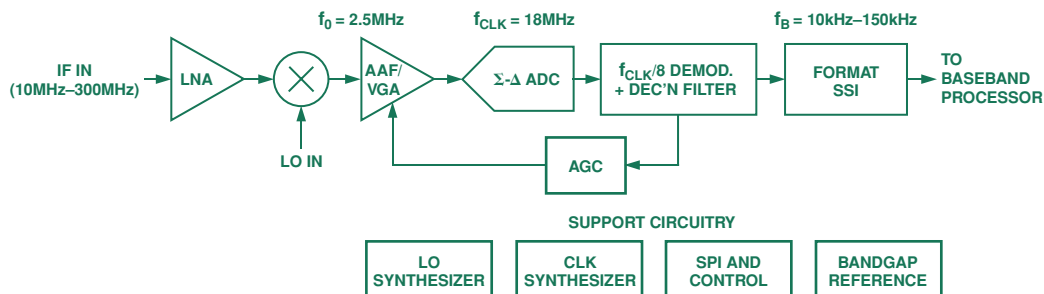

Figure 4. Functional block diagram of the AD9870 shows the level of integration.

The AD9870 differs from the typical superheterodyne architecture by employing a wide-dynamic-range *bandpass sigma-delta ADC* to sample a second-IF signal, along with any neighboring interferers. The demodulation of the target IF signal is performed with digital accuracy and stability, while the intrusive nearby interferers can be suppressed via digital filtering.

Figure 4 shows a functional block diagram of the AD9870. Functioning similarly to the RF portion of the superheterodyne architecture, an *LNA and mixer* are used to amplify and down-convert the target signal centered at the first-IF frequency to a lower second-IF frequency suitable for digitization by the bandpass ADC.

The LNA and mixer provide approximately 10.5 dB of gain, while preserving system dynamic range with an input noise figure of 9 dB and third-order intercept of 0 dBm. The high input impedance (360 Ω) simplifies interfacing to crystal or SAW filters. An *on-chip LO PLL synthesizer* can be used in conjunction with an external loop filter and VCO to generate a tunable LO frequency.

The second-IF signal is centered at exactly $1/8^{th}$ the bandpass ADC sample rate (i.e., $IF2 = f_{CLK}/8$) to allow for a simple $f_S/8$ digital quadrature demodulation scheme. Upon down-conversion to the second-IF, the signal is processed by a tunable (and programmable) *active third-order anti-alias filter (AAF)* to suppress signals which could appear within alias bands of the sampling ADC (i.e., $N \times f_{CLK}/8 \pm f_{CLK}/8$. The AAF tuning circuitry can support ADC sample rates between 13 and 18 MHz, with the 3 dB cut-off frequency typically set and tuned to slightly beyond the second-IF (i.e., $f_{-3dB} = f_{CLK}/3.2$).

Embedded in the AAF is a *variable-gain amplifier (VGA)* that provides up to 26 dB of gain range (Figure 5). The VGA gain, which extends the dynamic range of the AD9870, can either be programmed directly or controlled by an automatic gain-control (AGC) loop. The AGC loop is typically invoked under strong signal conditions to prevent "overloading" or clipping of the A/D converter by maintaining a programmable fixed-signal level at the ADC input. The AD9870 implements the AGC function with a highly effective hybrid approach, as shown in Figure 5: the analog and digital domains work together in signal estimation and control.
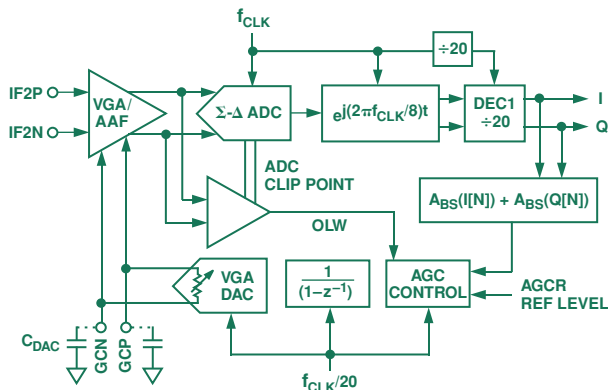

Figure 5. A "hybrid" AGC control loop extends the dynamic range of the AD9870.

In situations where a strong target signal or interferer falls within the bandwidth of the first-stage decimate-by-20 digital filter, the signal is estimated digitally and compared to a programmed reference level (AGCR). The difference between the two levels is fed to a digital integrator, which updates a control DAC to adjust the analog voltage of the VGA. Since a strong interferer falling outside of the passband of the first-stage digital filter can not be accurately estimated, an analog loop based on a simple differential comparator monitors the input to the ADC and assumes control of the loop during any overrange condition, to reduce the VGA gain.

An external capacitor is used to "smooth" the transitions of the DAC, with a time constant established by its capacitance and the internal source resistance of the DAC. The R-C cutoff frequency is typically set well outside the control system's loop bandwidth to ensure continual digital control of the loop dynamics. The control loop bandwidth is digitally programmable with attack and decay times variable over a wide range and ability to react to any overload condition.

The instantaneous dynamic range of any narrowband receiver signal chain containing a VGA is dependent on the particular gain setting of the VGA, since the noise contributed by each stage in the signal path to the "overall" input-referred noise decreases as the gain of the preceding stage increases. This implies that input noise described by its noise figure, NF, is typically dominated by the first few stages (i.e., LNA and mixer); noise sources at the end of the signal chain (i.e., the ADC) have minimal effect upon the system's NF, *provided* that there is sufficient gain between these blocks.
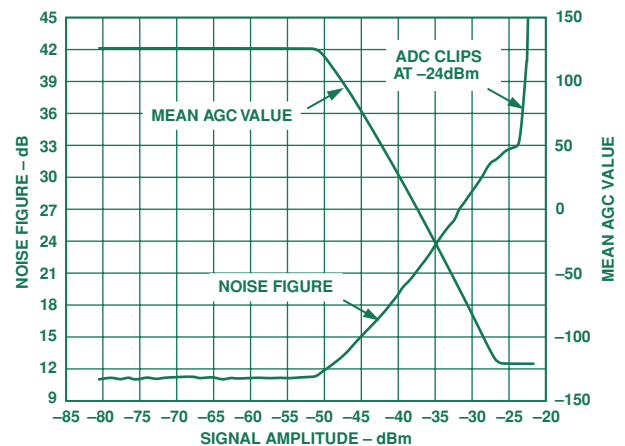

Figure 6. Dynamic range of AD9870 depends on VGA setting.

In the case of the AD9870, the VGA's gain is nominally adjustable over a 25 dB range. Figure 6 shows how the AD9870's noise figure is impacted by the VGA gain setting as a target signal's (or interferer's) input power is increased from –85 dBm to –23 dBm. Under small-signal conditions, the VGA is set to max gain; the AD9870's noise figure is set by the LNA/Mixer as well as the VGA's input noise. However, as the signal power is increased, a point is reached (depending on the AGC reference level) at which the VGA's gain begins to decrease to prevent ADC clipping. At this
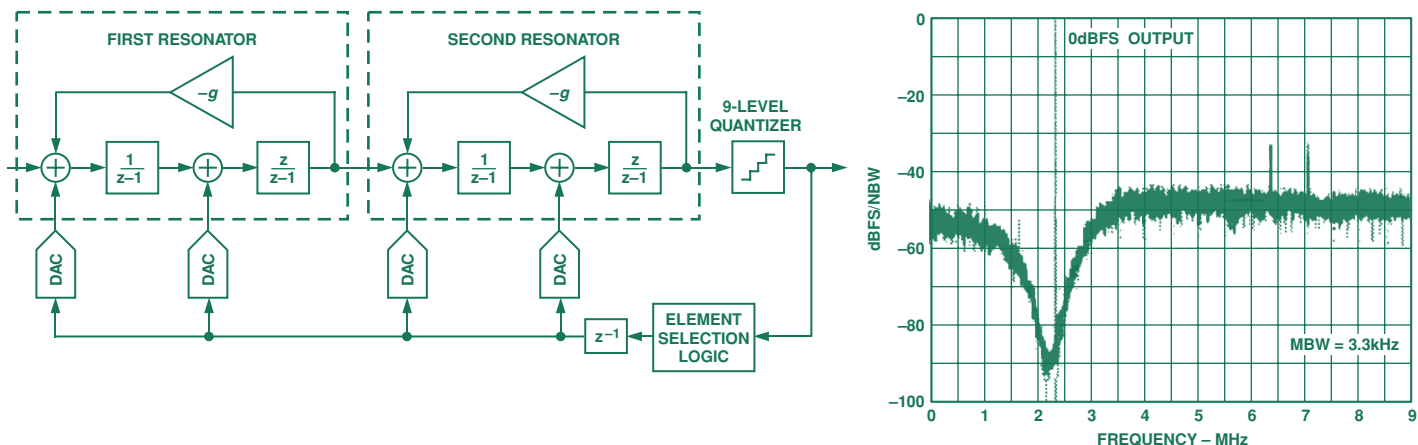
Figure 7. Multibit fourth-order bandpass Σ-Δ ADC results in deep notch at $f_{CLK}/8$.
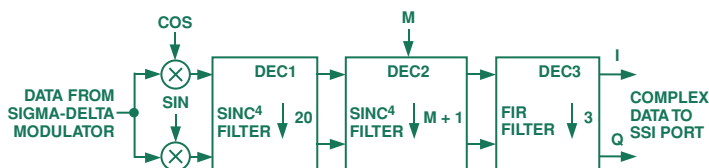

Figure 8. Digital quadrature demodulation, followed by programmable decimation filters, provides baseband I/Q data.

point, the VGA gain is reduced dB for dB as the signal power is further increased. Also, in this region, the input signal level to the ADC remains constant and the noise of the ADC begins to dominate such that the system's NF degrades also at a 1 dB per dB rate. As the signal power continues to increase, a point is reached (i.e., –26 dBm) at which the gain of the VGA is set to its absolute minimum and further increases in signal level are seen at the ADC input until clipping occurs (i.e., –24 dBm).

The bandpass sigma-delta ADC (Figure 7) is the "heart" of the AD9870 that makes a low second-IF digitization approach feasible and practical in an IC intended for radio systems requiring high dynamic range with minimal power consumption. This ADC, together with the back-end digital decimation filters, achieves nearly 14.5-ENOB performance within a 10-kHz bandwidth, while sampling a signal centered at frequencies as high as 2.25 MHz. It achieves these specifications while drawing a mere 13 mA from a 3.0 V power supply.

The sigma-delta ADC is based on a fourth-order switched-capacitor, multi-bit modulator consisting of two cascaded resonators that provide two complex pairs of zeros in the noise transfer function (NTF) falling near $f_{CLK}/8$. The location of these complex zeros at the second-IF frequency, along with the multibit feedback path, help ensure a low noise floor in a narrow region ($\pm73.3\%$ of $f_{CLK}/8$) around the second-IF frequency.

The digital output data from the ADC is fed into the digital signal processing section of the AD9870 (Figure 8). This section consists of an $f_{CLK}/8$ complex (or quadrature) demodulator followed by

three linear-phase FIR filters. The complex demodulator separates the target second-IF signal centered at $f_{CLK}/8$ into its I/Q components prior to filtering.

The output spectrum of the complex demodulator consists of the target signal, now centered at "dc," along with any undesirable interferers and/or noise not sufficiently filtered in the analog domain. A series of decimation filters are used to remove these undesirable components, while simultaneously reducing the data rate in accordance to the target channel's bandwidth. Depending on the modulation scheme, the complex data rate (hence decimation factor) is set to be at least a factor of two greater than the channel bandwidth to allow for further post-processing. Both DEC1 and DEC2 use a cascaded fourth-order comb filter topology; DEC2's decimation factor is user programmable to accommodate different channel bandwidths. DEC3 is a decimate-by-3 FIR filter; it sets the close-in transition-band characteristics of the composite filter. The 16-bit I-and-Q output of DEC3 is fed into the synchronous serial-interface (SSI) function, which formats the data into a serial bit stream and embeds other optional information — AGC, signal strength, and synchronization—into the bit stream.

AVAILABILITY
The AD9870 was released to production in winter 2001. It is available in a 48-lead LQFP package for $16.96 in 1K volume.* The AD9870 datasheet is available on Analog Device's website (www.analog.com). An evaluation board and the associated software are also available.   ▶

*Recommended resale price USD. Prices are subject to change without notice. For specific price quotations, get in touch with our sales offices or distributors.