

Watching the currents flow



It was late Sunday evening, and we were still trying to trace why the embedded DSL modem was feeding a strange 50-MHz carrier into the network—much stronger than -40-dB noise allows. And no 50-MHz signal existed on the design! Jeremy, the board designer, did his best to lay out a six-layer board and placed many bypass capacitors as numerous reviews suggest. He also kept power and ground planes everywhere on separate layers and kept the analog traces

as far from noisy digital parts as he could. We had a faint hope that the board was picking up a spur from a clock line 1 in. away; our hope disappeared when the second, improved board revision made things worse.

Building mixed-signal, quiet boards is an art, and textbook recommendations on layout for signal integrity can fail if you take them literally. We could have been dealing with inductive coupling from the currents flowing in the ground plane, but my suggestion to watch the currents flow in internal layers surprised the team. Don't the electrons simply dive into the ground plane?

Unfortunately, physics claims that currents come only in loops. Even in planes, you can find where most of the current flows, such as the Gulf Stream in the ocean. These currents induce the noise in the traces above it, and no way exists to shield the magnetic field on the board. Finding or predicting these loops is part of the art of mixed-signal design.

WHEN WE TINKERED WITH A FEW DEDICATED BYPASS CAPACITORS BETWEEN THE PAIRS—VOILA!—THE NOISE CURRENTS FLOWING OUT OF THE CPU AREA SHRANK.

Once designers find them, they should make the loops as local as possible, and the low-noise signal traces should never run parallel to these currents.

We made a handy ac-current probe, a Magnepick. It is simply a toothpick with three to four turns of a thin wire making a tiny coil on its tip. It picks up the magnetic field parallel to the toothpick. We connected it to a spectrum analyzer (don't forget 50 Ω termination) and, sniffing with it around the board, could—with maximum intensity—map the paths of select frequency components. We also made an improved-resolution version from the head of a floppy drive someone left on the bench.

(Don't follow our lead if you value friendship.) The revelation was striking.

First, the recommendations for a 1- μ F capacitor per digital IC and to not break planes were our biggest enemies. A cluster of chips exists in the corner of the board, with a processor in the center. The cluster of bypass capacitors also happened to be in the corner, and half of the noise current that should have been localized around the CPU rushed all the way to the corner of the board, where the main capacitance was concentrated. This path was the one of least ac impedance, and electrons quickly sensed this opportunity! Our analog trace was right above this path.

Second, not all of the V_{SS} pins on the CPU were equal. Some of them had much greater noise and carried currents of different frequencies! We could identify the pairs of V_{SS}/V_{CC} that apparently belonged to the same unit in the CPU by their noise-spectrum distributions—a secret the chip designers kept to themselves. We also found a 50-MHz clock in the design, internal to the CPU, when our probe was on top of the CPU package and around some pins. When we tinkered with a few dedicated bypass capacitors between the pairs—voila!—the noise currents flowing out of the CPU area shrank.

Although we now marginally meet the specification, Jeremy knows what he has to do next. He will break the V_{CC} plane into islands around the noisiest chips to isolate the currents into much smaller loops. Then, he will put ferrite beads (ac impedance) between them to break long paths of least resistance. He will route the analog traces away from remaining loops and make them orthogonal to reduce the inductive coupling. And he will hook up his bypass capacitors around the CPU close to the pairs we found. **EDN**

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