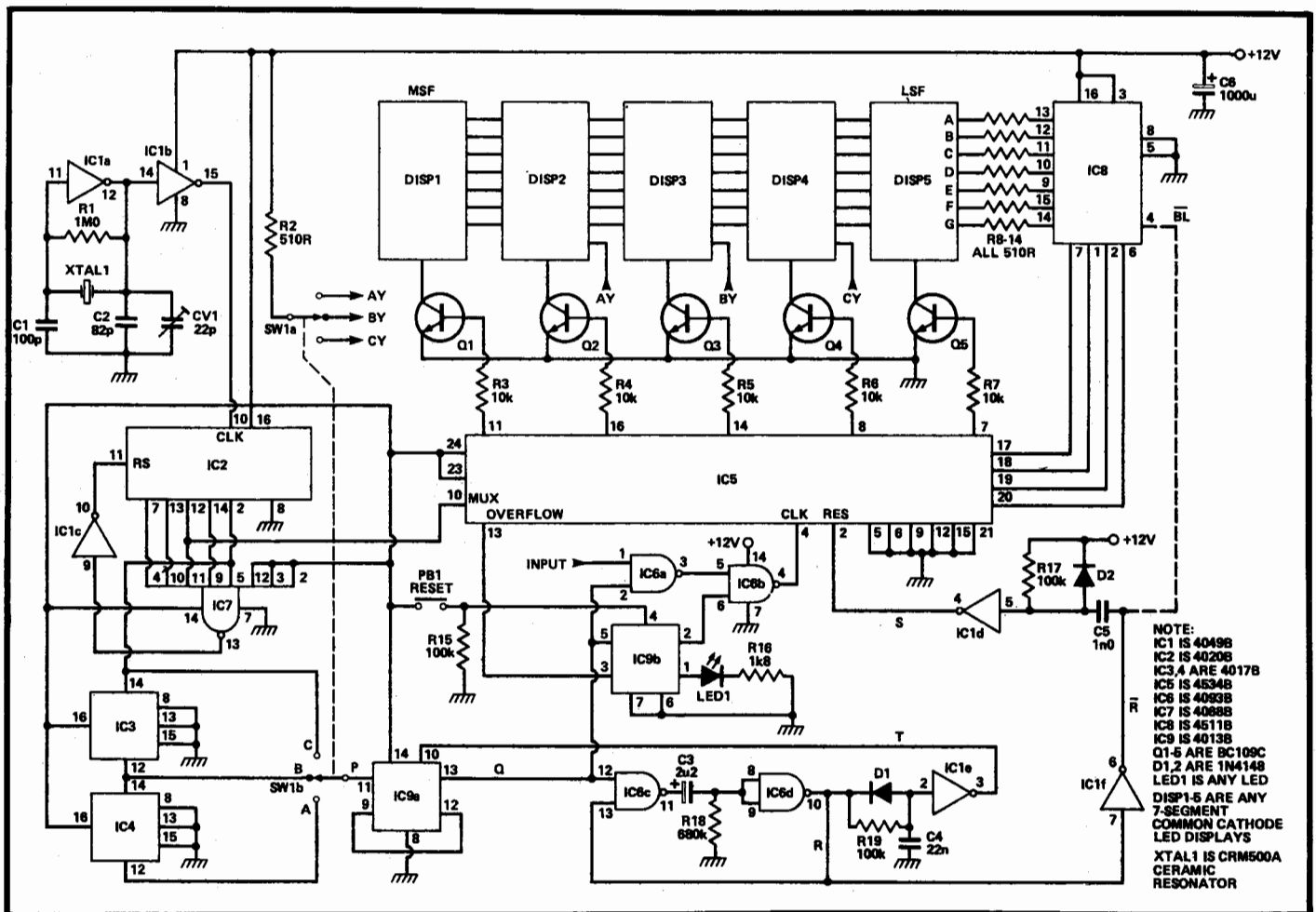

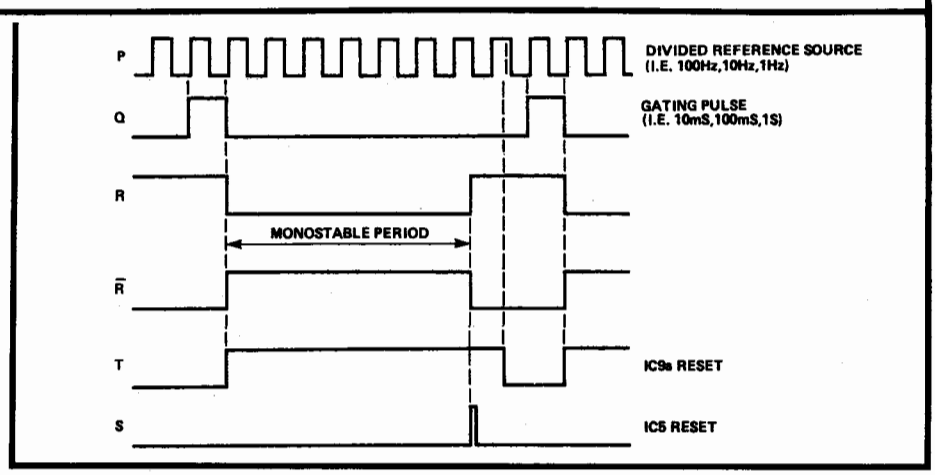

Digital Frequency Meter
William Leung

The design shown is an alternative to those projects for DFMS that utilize one of those new-fangled all-in-one DFM chips. As you can see from the circuit diagram, the only additional circuitry required is an input preamplifier and a suitable regulated 12 V power supply.

IC5 is a real-time five-decade counter incorporating a multiplexed BCD output. With the aid of IC8 (a BCD-to-seven-segment decoder) and transistors Q1-5, the counter and display section of the DFM is formed. The $\overline{\text{BLANK}}$ pin on IC8 is used to extinguish the displays while IC5 is counting, otherwise pin 4 of IC8 should be connected to the positive rail. The frequency reference oscillator is somewhat unique in that a 500 kHz ceramic resonator is used. In practice it offers reasonable accuracy; however, the circuit can be easily modified to use a 1 MHz quartz crystal. In this case, the connections between IC2 and IC7 of the frequency divider section will require the inputs of IC7 to be connected to pins 3, 5, 12, 14 and 15 of IC2. Pin 14 of IC3 should also be connected to IC2 pin 2, and a suitable multiplexing frequency of around 1 kHz should be fed to pin 10 of IC5.

Depending on the position of SW1b, either 1Hz, 10 Hz or 100 Hz will appear at IC9 pin 11 (see Fig. 2, point P), where IC9a is a D-type flip-flop configured to divide by two. Should IC9a be continuously enabled, the output of IC9a will, in fact, be a square wave of half the applied frequency with a mark/space ratio of 1:1. This means that for a 1Hz applied frequency, 0.5 Hz will appear at IC9a pin 13 and the time for which the cycle will be high is, in fact, one second. This is then fed to the gate IC6a. However, only one such gating pulse is produced, after a certain time period set by C3 and R18. The monostable formed round IC6c,d is used to give the reading period of the display, when triggered, by enabling IC8 and disabling IC9a. At the end of the monostable period, a short pulse is produced at S which resets the counter. IC1e is there to ensure that IC9a is not enabled before the reset pulse to the counter is produced (see T), otherwise all hell will break out!

Finally, the D-type flip-flop that remains is used as the basis of the overflow indicator; on the transition of the counter from 99999 to 00000, a pulse is produced at IC5 pin 15 which latches IC9b pin 1 high, thus lighting up the LED. Pressing PB1 resets the whole system.