GERARD ROBIDOUX AND
ROBERT DMITROCA*

LOGIC ANALYZER

Troubleshooting digital circuits is a cinch with this 16-channel, 50-MHz logic analyzer.

A LOGIC ANALYZER IS AN INVALUABLE tool for debugging complex digital circuits. Not only can it sample and store the state of a large number of digital signals, it can perform complex analysis on the signals to determine their timing and state relationships. The acquired data can be displayed on either a waveform screen or a state screen. With four different pull-down menus available, all the controls are right at your fingertips!

The essence of all digital logic circuits is the simultaneous operation of many signal paths. As an example, consider a typical desktop personal computer, such as the IBM PC. In order for the microprocessor to write to a single byte of memory, it must assert 20 address lines, 8 data lines, and over a half-dozen control lines. In total, over 34 signal paths must operate correctly and simultaneously for the computer to function properly.

When a digital circuit fails, it becomes very difficult to debug. Traditional diagnostic tools, such as the oscilloscope, can usually monitor 4 channels at the most. Other tools, such as logic probes, can only display the current state of a signal, and cannot be used to analyze how the signal varies with time.

Those problems led to the development of the logic analyzer. At its most primitive level, the logic analyzer may be considered to be an oscilloscope with a large number of channels, except that only the high-low state of a signal may be seen, rather than a continuous analog waveform. Commercial logic analyzers typically have 16 to 300 channels.

Until now, most logic analyzers have cost well over $1000, which has severely limited their use. Currently, most low-cost logic analyzers consist of cards which plug into personal computers. Those devices require a personal computer to operate and, therefore, are not very portable and tie up the resources of the computer.

Recent advances in CMOS and bipolar technologies, however, make it possible to build a practical, low cost, self-contained logic analyzer. We will show you how you can build a portable, 16 channel, 50-MHz logic analyzer, all for under $700!

Theory

Figure 1 shows a block diagram of the logic analyzer. Connection to the circuit under test is made through an acquisition "pod," or connector array, which contains a set of wires terminated with test clips. The clips are used to attach to the various points in the circuit being tested.

All of the lines contained in the acquisition pod are inputs; the logic analyzer never sends a signal to the device it is connected to. The pod also contains clock and ground inputs as well as data-input lines. More sophisticated units may also contain inputs that qualify the clock, inhibit triggering until certain conditions are met, and so on.

Signals coming in from the acquisition lines enter voltage comparators, which are used to periodically sample the input sig-

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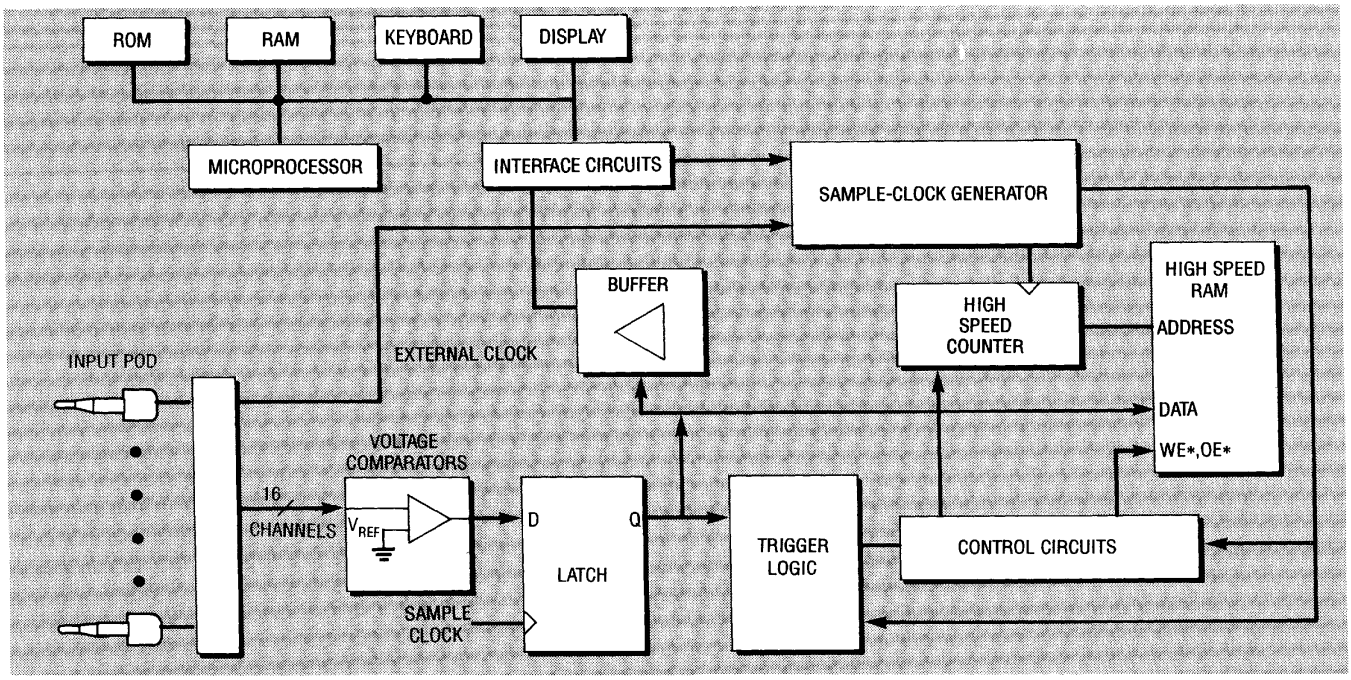
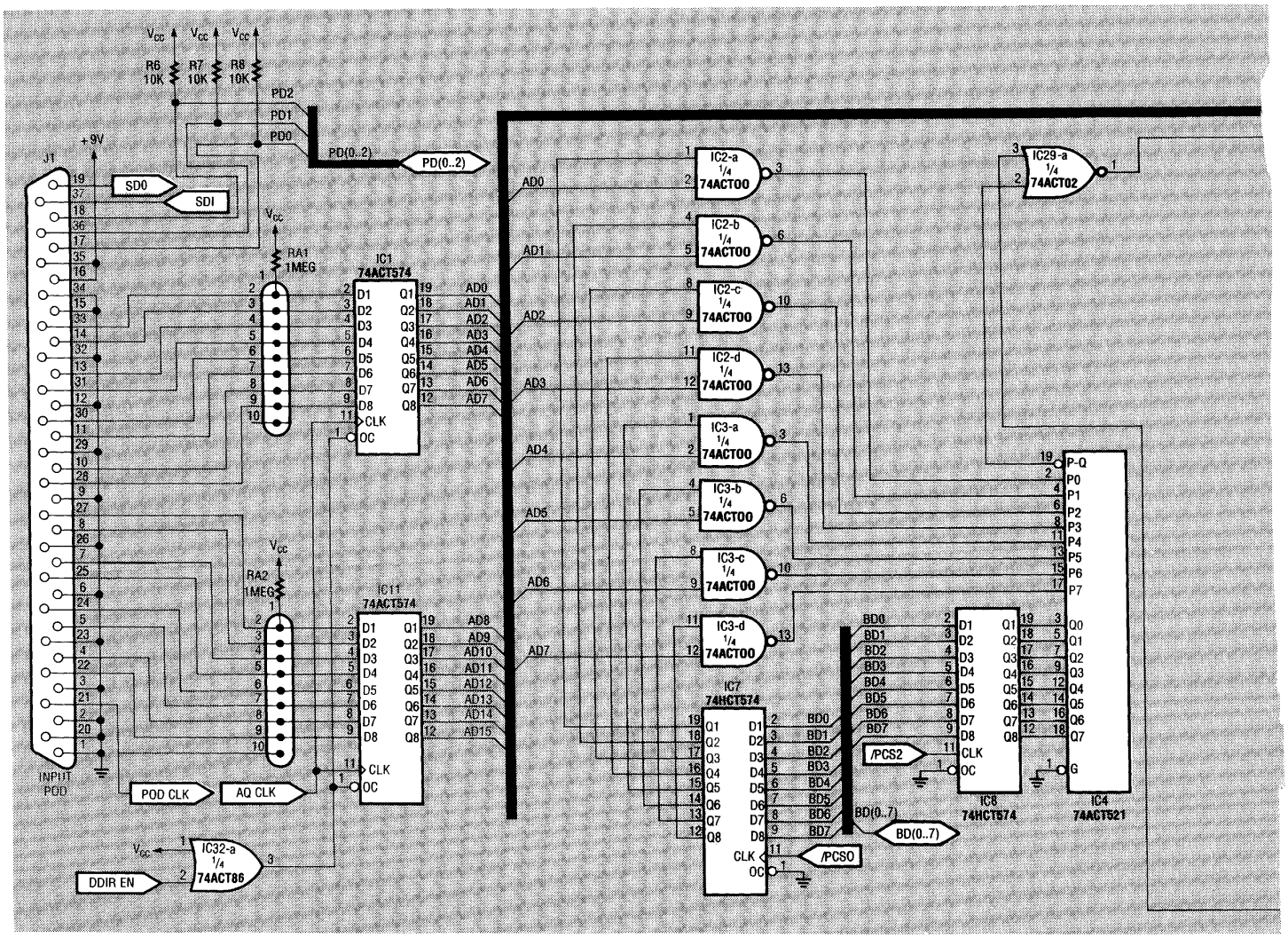


FIG. 1—A BLOCK DIAGRAM OF THE LOGIC ANALYZER. Signals from the acquisition lines enter the voltage comparators and are sampled by the input latches; they then flow into the high-speed RAM and the trigger logic. The final stage is the user interface.



nals and determine their logic level. All logic families have a defined high and low level. For example, the TTL logic family defines a low as a voltage between 0 and 0.8 volts, and a high between 2.4 and 5.0 volts. Some logic analyzers have a variable voltage-threshold, which allows you to define the high and low voltage levels depending on your particular application.

The logic analyzer that we present here recognizes only TTL and 5-volt CMOS levels. Since the vast majority of digital logic is designed with those two families, that's not a serious limitation, and it also eliminates the need for expensive high-speed voltage comparators.

After voltage comparison, the signals entering the logic analyzer are sampled by the input latches. Digital storage scopes (DSO's) use the same sampling technique. The sampling rate is determined by an internal timebase, or from an external clock input. The sampling rate is usually adjustable in a 1-2-5 sequence from a very high frequency to a very low frequency (a few hundred MHz to less than 100 Hz).

With a very fast clock, you can see the operation of the circuit in great detail for a very short period of time. With a slow clock you can see the operation of a circuit for a longer time, but with less accuracy. If you were debugging a high speed digital circuit, such as a microprocessor, you would use a very fast clock. A slower clock would be used to troubleshoot a very slow circuit, such as a 1200-baud serial interface.

The external CLOCK input is used when you want the sampling rate to be controlled by an external circuit. A good example of that is when you attach a logic analyzer to the data and address lines of a microprocessor to trace program execution. The logic analyzer's external CLOCK line is connected to a memory strobe line, such as $\overline{AS}$* (68000 family) or $\overline{ALE}$* (8088 family). The logic analyzer would then capture the status of the processor at each bus cycle.

After being captured by the input latches, the input signal data flows to two places; the high speed RAM and the trigger logic. Let's take a close look at the trigger logic first.

In most digital designs, we're interested in the operation of the circuit at a very specific point. The action of the trigger logic allows us to obtain only that range of data in which we are interested. For each of the signals being monitored, we can specify a trigger pattern of high, low, or "don't care" (either high or low). When the logic analyzer is enabled, it will continuously sample the input data lines until the trigger pattern is recognized. At that point, sampling will either stop, or continue for a preset number of samples. That feature lets us see the state of the signals occurring before, or, perhaps, both after the trigger point.

The high speed static RAM stores the values of the input channels being monitored. That RAM is often known as the acquisition data buffer, since it provides a storage space for the data being acquired from the input data lines.

Notice that a logic analyzer, unlike an oscilloscope, is not a "real-time" device. An oscilloscope can immediately and continuously shows the voltage at the probe. The logic analyzer, on the other hand, stores the signal data until a trigger pattern is recognized. The

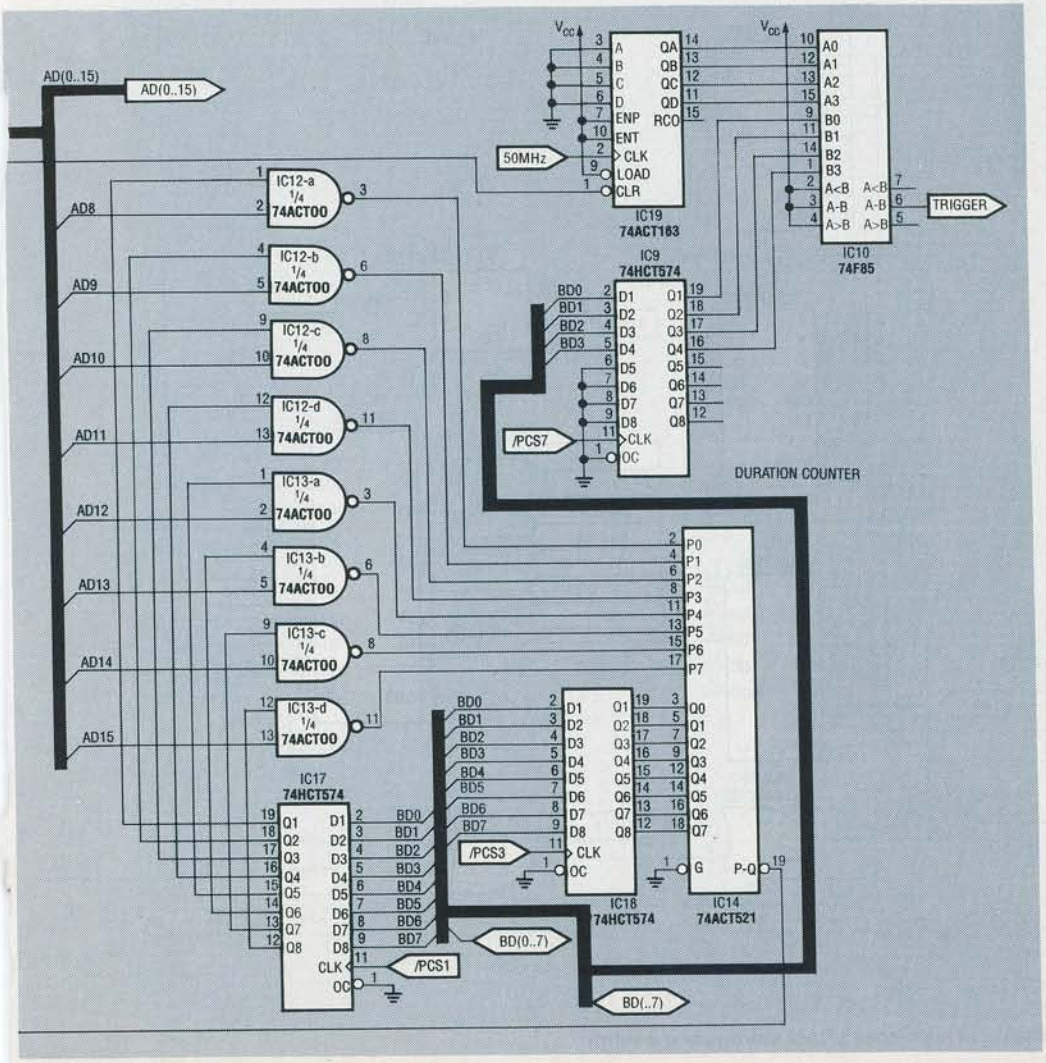


FIG. 2—INPUT BUFFERS AND TRIGGER LOGIC. The input pod contains 16 data-channel inputs, an external clock input and a ground connection. The input data enters resistor arrays RA1 and RA2, and into latches IC1 and IC11. The acquired data is routed into the trigger logic and to the high-speed RAM.

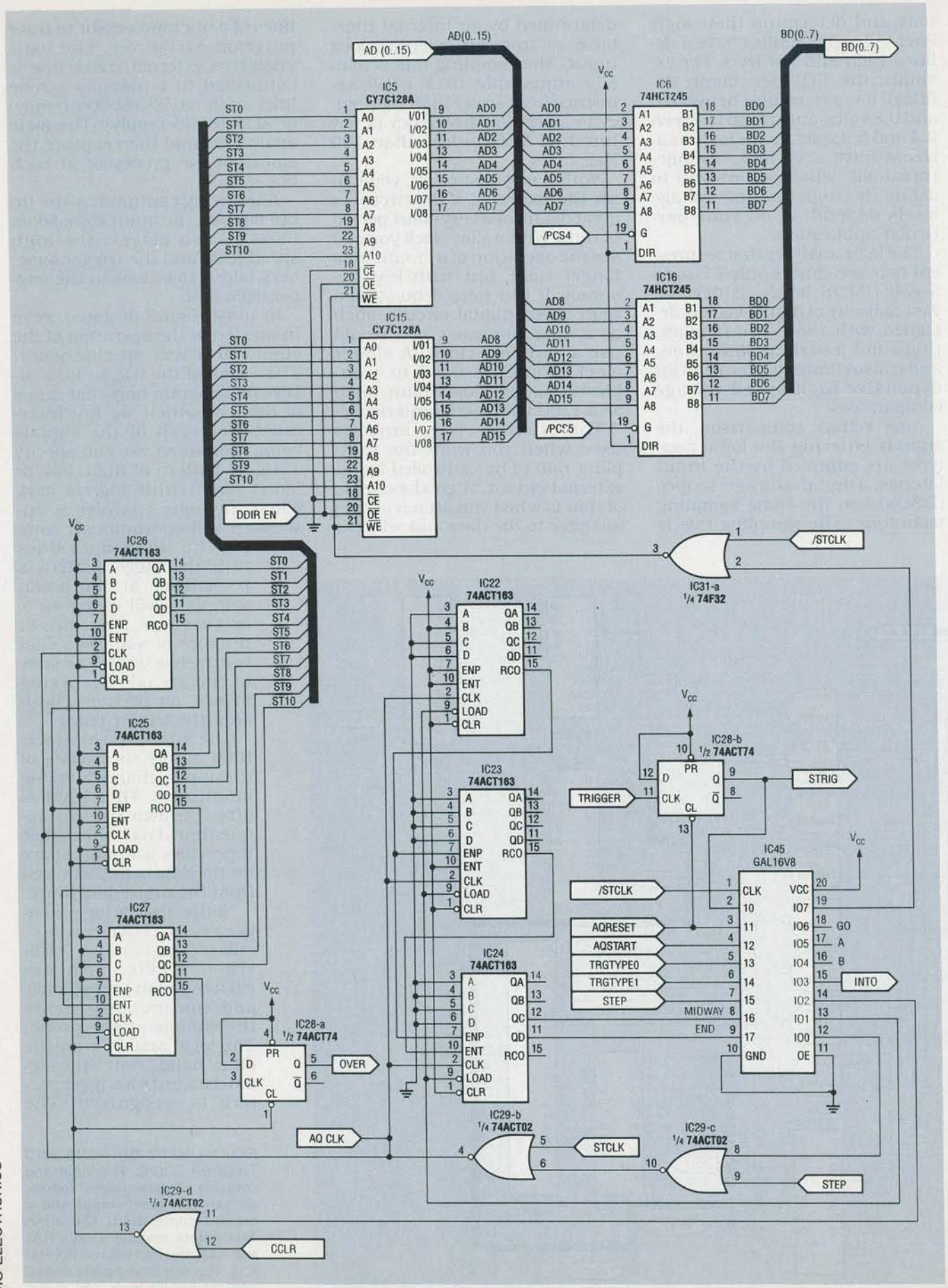


FIG. 3—THE ACQUISITION SECTION, consisting of high-speed RAM storage and control logic, is the heart of the logic analyzer.

signal data is shown only after that has occurred.

The last section of the logic analyzer is the user interface, which consists of a keyboard and display that are built right into the unit.

Circuit description

Now that we've looked at the block diagram of the logic analyzer, we'll turn our attention to how the unit operates. The schematic in Fig. 2 shows the input pod and trigger logic. The input pod connector, J1, contains 16 data-channel inputs, the external clock input and the ground lead connection. It also carries other signals that can be used by external pods.

The data to be sampled goes into J1, through resistor arrays RA1 and RA2, and into latches IC1 and IC11. The level of each channel is latched using the AQ–CLK signal (the sampling clock). Pull-up resistors RA1 and RA2 drive the inputs of the latches high if nothing is connected to the input. The acquired data (AD[0..15]) is routed to the trigger logic and to the high speed RAM storage (Fig. 3).

The trigger condition of the input data may be set to high, low, or "don't care." The "don't care" circuits for the first eight inputs are formed from IC2, IC3, and IC7, and the last eight inputs from IC12, IC13, and IC17. If an input is set to a "don't care" condition, the input of the corresponding NAND gate is set low. That forces the output to be high regardless of the input from the data latch. If the NAND input is set low, the data is simply inverted.

The outputs from the NAND gates are presented to the eight-bit comparators, IC4 and IC14. The output of those IC's (pin 19) goes low whenever the P and Q inputs match.

Masking of IC8 and IC18 latches is performed by the following technique. If the trigger bit to either IC is low, a high is written to the latch. Similarly, if the trigger bit is high, a low is written. For "don't care" conditions, a high value must be written, since we have forced the P input to high (by disabling the NAND gate). The upper and lower trigger outputs of IC29-a forms an active-high trigger output.

PARTS LIST

All resistors are ¼-watt, 5%, unless otherwise indicated.

R1–R8–10,000 ohms
R9—470 ohms
R10—0 ohms, or jumper wire
RA1, RA2—1 megohm, 10-pin bussed SIP resistor array

Capacitors
C1–C11, C13–C20, C23, C25, C27–C38, C40–C49, C58–C60—0.1 µF, ceramic axial
C12, C24—3.3 µF, 10-volt tantalum
C21, C22—10 pF, ceramic disc
C26—100 µF, 25-volt tantalum
C39—50 pF, ceramic disc
C50–C57—22 µF, electrolytic

Semiconductors
IC1, IC11—74ACT574 8-bit latch
IC2, IC3, IC12, IC13—74ACT00 quad 2-input NAND gate
IC4, IC14—74ACT521 8-bit comparator
IC5, IC15—CY7C128A 2K × 8 15-ns static RAM (SRAM)
IC6, IC16—74HCT245 octal transceivers
IC7–IC9, IC17, IC18, IC39—74HCT574 8-bit latch
IC10—74F85 4-bit comparator
IC19, IC22–IC27—74ACT163 4-bit counter
IC20—74HCT138 3-to-8 demultiplexer
IC21—TL7705A voltage supervisor and reset control
IC28—74ACT74 dual D-type flip-flop
IC29—74ACT02 quad 2-input NOR gate
IC30—V25 high-integration microprocessor
IC31—74F32 quad 2-input OR gate
IC32—74ACT86 quad 2-input XOR gate
IC33—74F160 4-bit counter
IC34—74ACT153 dual 4-to-1 mulitplexer
IC35–IC37—74LS390 dual bi-quinary counter
IC38—74ACT151 8-to-1 mutiplexer
IC40—Dallas Semiconductor DS1213C "Smart Socket" and 32K × 8 100-ns SRAM or Dallas Semiconductor DS1235 integrated battery backed RAM
IC41, IC42—MAX232 RS-232 tranceiver and charge pump
IC43—7805 5-volt regulator
IC44—GAL16V8-15LP PLD
IC45—GAL16V8-10LP PLD
IC46—128K × 8 250-ns EPROM
LCD panel—Sharp part no. LM24014W

Other components
XTAL1—16-MHz HC-49 crystal
XTAL2—20-MHz 14-pin DIP package oscillator
XTAL3—50-MHz 14-pin DIP package oscillator
Case—Pactec CM69-120
Key switches (12)—75120-002/0000
AC adapter—9 VDC at 1 amp secondary output

Connectors
J1—Right-angle DB37 connector
P2–P4—3-pin socket strip
J3—Right-angle DB9 connector
J4—20-pin socket strip (2 × 10)
P1—7-pin socket strip (1 × 7)
J2—Power connector (2.3-mm barrel)
Keyboard—7 × 1 row-header
Acquisition clip—DB37 connector with 18 wires and micro-clips.
P1—2 × 10 row-header connector for LCD panel

Sockets
20-pin machined sockets for IC1 and IC11
32-pin socket for IC46
14-pin machined socket for IC32
84-pin PLCC socket for IC30

Hardware
4 ⅜-inch standoffs with 4-40 internal thread
4 ⅝-inch standoffs with 4-40 internal thread
18 4-40 screws with pan head, ¼-inch length
2 4-40 nuts
1 TO-3 heatsink and heatsink grease

The minimum trigger-duration circuit is made from IC9, IC19, and IC10. That circuit ensures that the trigger is present for a minimum amount of time before the trigger pattern is actually recognized, which prevents glitches from causing a false triggering to occur.

The desired trigger-duration count is contained in the latch of IC9. Whenever the trigger pattern occurs, 4-bit counter IC19 is enabled. That counter runs at 50 MHz (20 ns per count). When the desired duration count and the counter value match, the TRIGGER output (pin 6 of IC10) will go high, indicating that a valid trigger pattern has been recognized. If the trigger disappears before the desired duration count has been reached, the counter is cleared. It will start over when the trigger becomes valid again.

The circuit shown in Fig. 3 contains the heart of the logic analyzer: the high speed RAM storage and the control logic. Data for the lower eight channels is stored in IC5, while IC15 stores the data for the upper eight channels. Both IC5 and IC15 are 2K × 8 15-ns SRAMS.

An 11-bit binary counter is formed from IC25, IC26 and IC27. That counter drives the address inputs of the RAM IC's. The

address is incremented by 1 for each cycle of the AQ—CLOCK (acquisition clock) signal.

The TRIG function lets you specify the position of the trigger position within the acquisition data buffer. When PRE is selected, the trigger is set at the start of the buffer. When the trigger condition is met, data is sampled until the entire acquisition buffer is filled. In the MID trigger mode, the trigger point is set at the middle of the data buffer. The first half of the buffer may or may not contain data that was sampled before the trigger point. In the POST trigger mode, storage of data will stop immediately after the trigger condition is recognized.

An 11-bit binary counter is formed from IC22, IC23, and IC24. That counter holds the current position within the acquisition data buffer. The position counter is reset whenever the trigger condition is recognized, after which it is incremented by 1 for each cycle of the AQ—CLOCK signal.

The acquisition section control is formed by IC45, IC29, and portions of IC28 and IC31. The TRIGGER output from IC10 to a constant high level (STRIG) is converted by IC28-*b*. A finite state machine, IC45, coordinates the signals coming in from the microprocessor, trigger logic, and position counters, and generates the appropriate outputs to control the acquisition cycle.

TRGTYPE0 and TRGTYPE1 are used to inform the state machine where the trigger should be positioned in the acquisition buffer (for example, they set the PRE, MID, or POST modes). AQSTART tells the logic analyzer to begin looking for the trigger condition, and to start storing data into the acquisition buffer. The MIDWAY and END signals from the position counters tell the state machine how much buffer has been filled since the trigger.

When a trigger has been recognized and the acquisition buffer filled up, the state machine will assert the INTO line, informing the microprocessor that acquisition data is now available.

The STEP, CCLR, and DDIR—EN

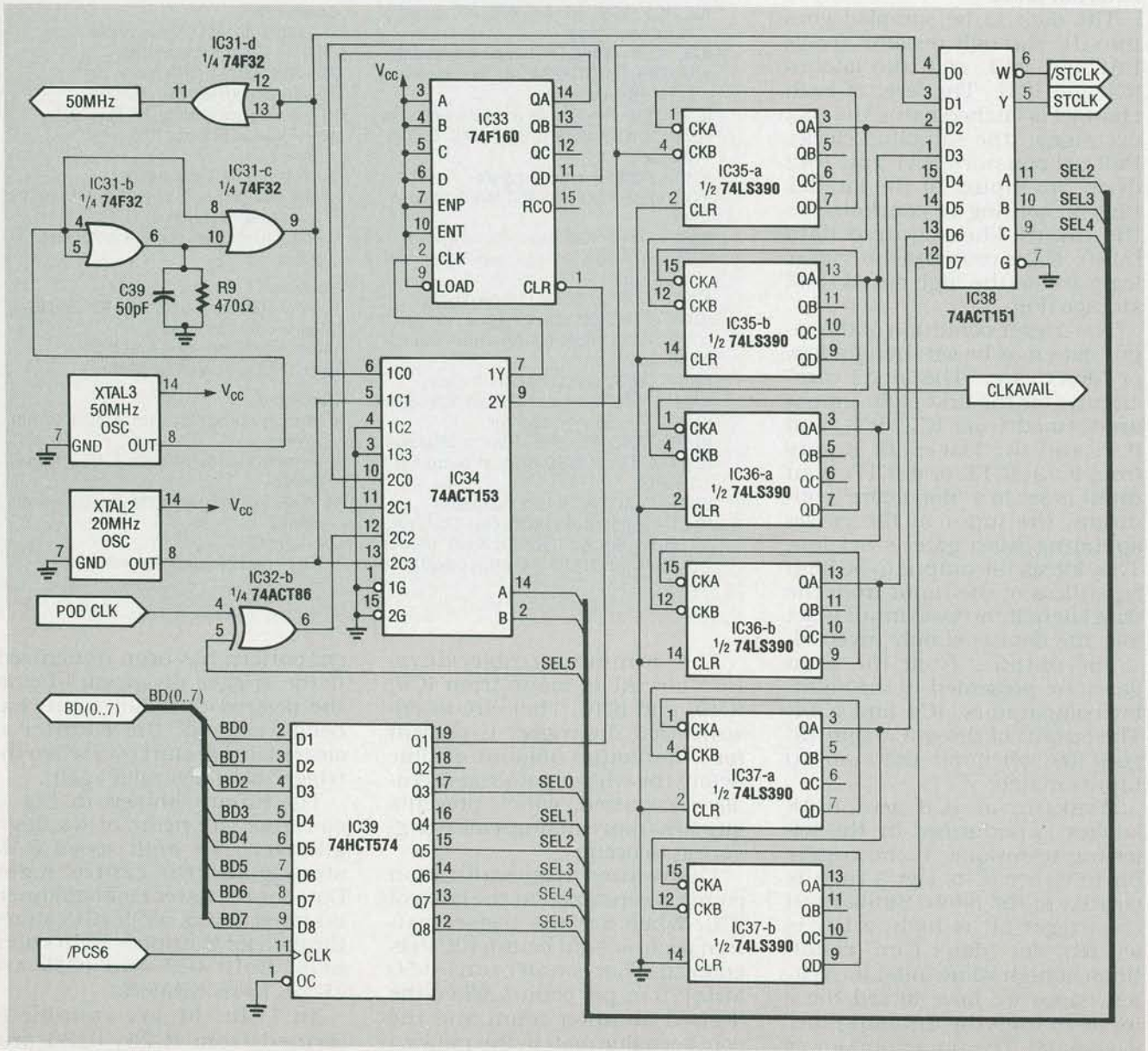


FIG. 4—CLOCK GENERATOR AND TIMING LOGIC. The logic analyzer can generate 22 internal frequencies, ranging from 50 MHz to 5 Hz.

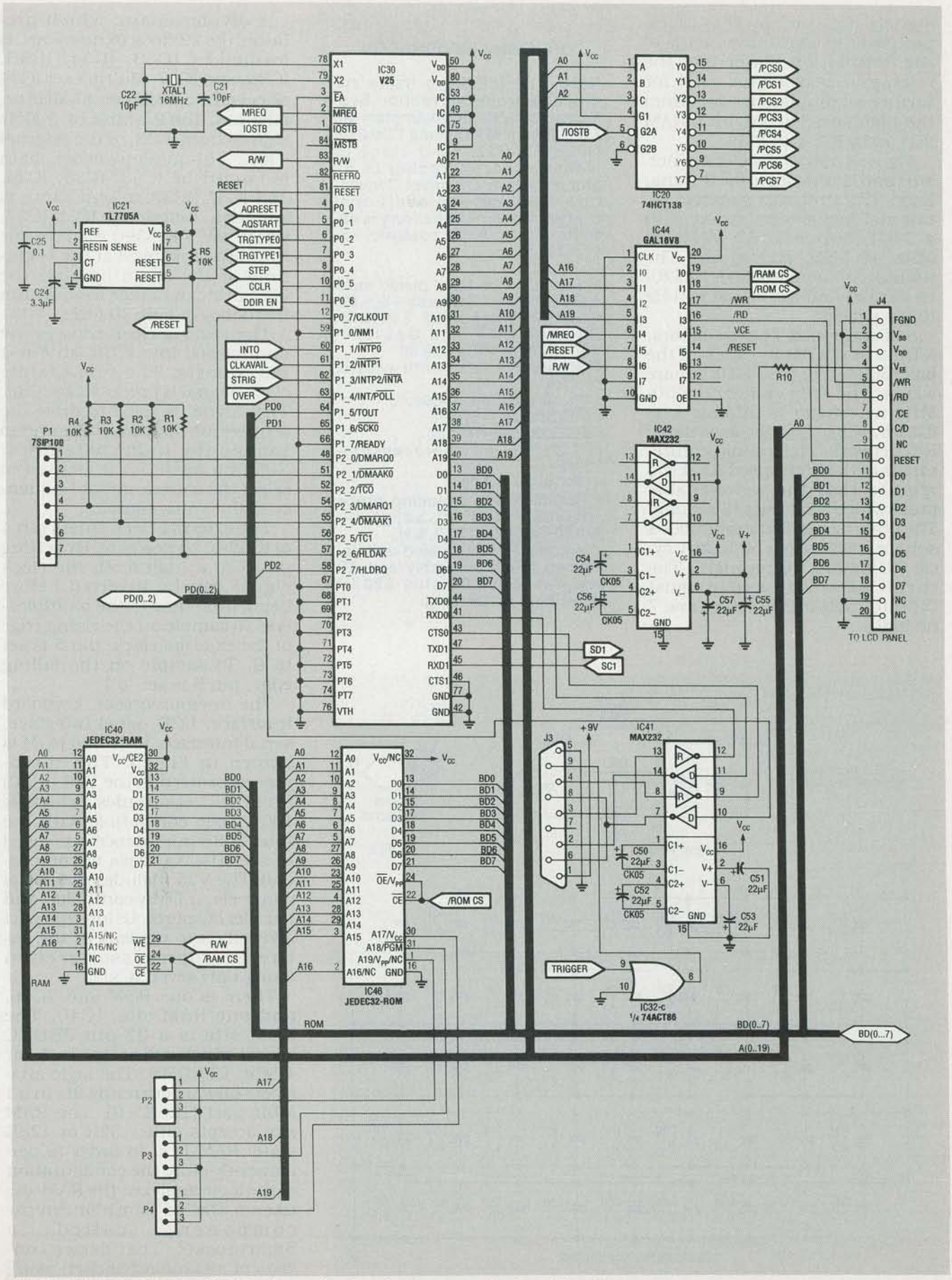


FIG. 5—THE PROCESSOR SECTION contains the microprocessor, keyboard interface, LCD panel interface, serial interface, RAM, and ROM.

signals are used by the microprocessor to copy the contents of the acquisition buffer into the microprocessor's own RAM for further manipulation. Data from the high speed acquisition RAM is read by IC6 and IC16.

Figure 4 shows the clock generator and timing logic for the analyzer. The unit can generate 22 internal frequencies arranged in a 5-2-1 sequence (50 MHz, 20 MHz, 10 MHz, and so on). The highest frequency is 50 MHz (20-ns period) and the lowest is 5 Hz (0.2-s period).

Self-contained TTL oscillators, XTAL2 and XTAL3, generate the base 50-MHz and 20-MHz square waves. The duty cycle of the 50-MHz waveform is adjusted by IC31-b, IC31c and the associated R-C network. The timing requirements of the high speed RAM IC's require that the write-enable pulse width be at least 13 ns long. The 50-MHz oscillator produces a square wave with a 50% duty cycle (10 ns low, 10 ns high). The circuit is therefore used to adjust the duty cycle to 35% (13 ns low, 7 ns high).

ORDERING INFORMATION

Note: The following items are available from Convention Systems, 1214-315 Southampton Dr. SW, Calgary AB, Canada T2W 2T6, (403) 253-4427. Send check or money order. Shipping is by ground delivery. Contact Convention Systems for additional charges if overnight delivery is desired. All items are postpaid, except as noted.

- **Etched, drilled and plated main and keyboard PC boards—$99.00.**
- **Preprogrammed EPROM, GAL16V8-15LP, and GAL16V8-10LP (IC44–IC46)—$99.00**
- **Milled-out case with plastic overlay—$79.00.**
- **Probe assembly—$99.00**
- **AC adapter—$15.00**
- **LCD panel—$150.00**
- **IC30 V25 microprocessor—$29.00**
- **Manual—$32.00**
- **Complete kit, including probe assembly and AC adapter—$695.00 plus $20.00 S & H.**
- **A complete assembled unit, including probe assembly and AC adapter—$695.00 plus $20.00 shipping and handling.**

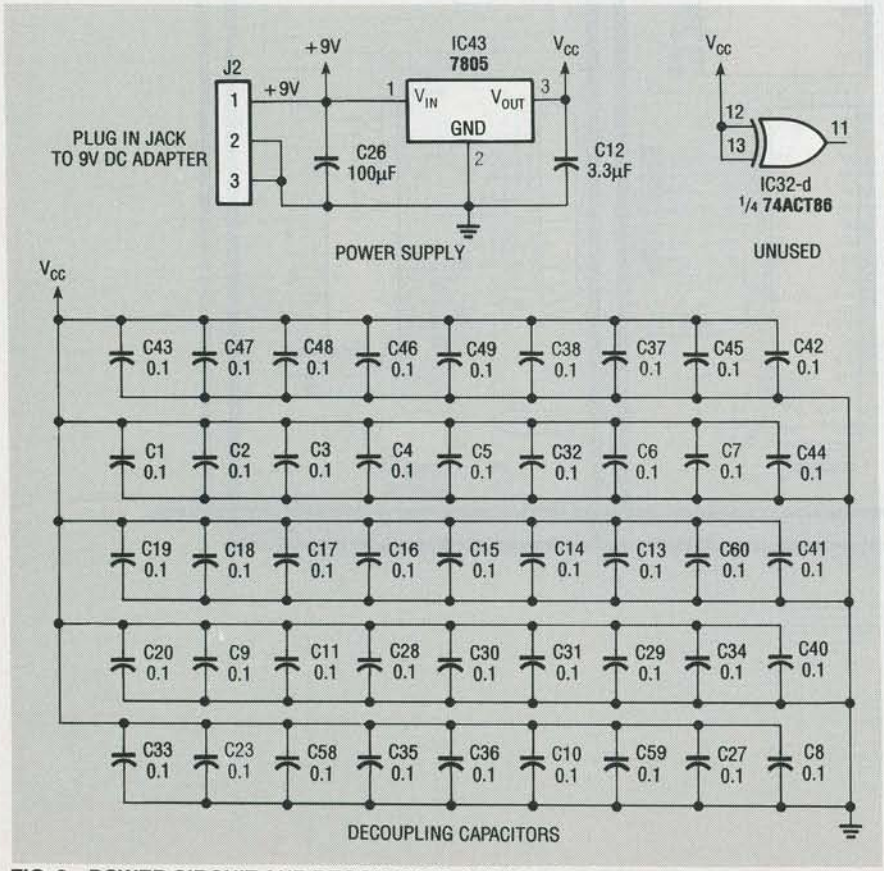


FIG. 6—POWER CIRCUIT AND DECOUPLING CAPACITORS. Each IC is decoupled by a 0.1 µF capacitor.

A divider chain, which produces the 22 clock frequencies, is formed by IC33, IC34, IC35, IC36, and IC37. Multiplexer IC34 selects the 50-MHz or 20-MHz oscillators, the 25-MHz or 5-MHz signals from IC33, or the external K line. A bi-quinary divider chain is formed by IC33, IC35, IC36, and IC37. IC33, a 74ACT160, is similar in function to IC35-IC37, which are 74LS390 dual-decade counters. It is used at the beginning of the chain because the 74LS390 can handle a maximum frequency of only 20 MHz.

The various clock sources are multiplexed into IC38, an 8-to-1 multiplexer. The STCLK (state clock) signal is produced by IC38. That signal is used to drive the acquisition state machine and to sample the input data lines. Eight-bit latch, IC39, is used to select the source and/or frequency of the STCLK signal.

The external clock enters pin 4 of IC32-b, an XOR gate. By setting pin 5 to a high level, the clock signal can be inverted before being presented to the multiplexers. To sample on the rising edge of the external clock, pin 5 is set to 0. To sample on the falling edge, pin 5 is set to 1.

The microprocessor, keyboard interface, LCD panel interface, serial interface, RAM and ROM is shown in Fig. 5. The microprocessor used is the V25 (IC30) from NEC electronics, which is 100% code compatible with the Intel 8088 microprocessor (used in the IBM XT class of computers). The V25 includes two serial channels, a DMA controller, and parallel I/O ports. Using this part allowed us to implement the entire microprocessor section using only seven IC's!

There is one ROM site, IC46, and one RAM site, IC40. The ROM site is a 32-pin JEDEC socket which will accept 1-, 2-, or 4-Mbit EPROMS. The logic analyzer software currently fits in a 1 Mbit part (128K × 8). The RAM site accepts either 32K or 128K static RAM IC's. In order to permanently store the configuration of the logic analyzer, the RAM site uses a Dallas semiconductor component called a SmartSocket. That device consists of a standard socket, along with a 3-volt lithium battery, and

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a controller chip. Coupled with a standard low-power SRAM, the SmartSocket provides all of the benefits of standard non-volatile memory. The logic analyzer currently uses a 32K × 8-RAM.

The TTL levels of the V25 are converted to RS-232 levels by IC41, a Maxim MAX232 RS-232 transceiver. The part requires only a +5-volt supply and has integral charge-pumps to create the necessary −10-volt and +10 volt RS-232 levels.

The negative contrast-voltage for the LCD panel is generated by IC42, also a MAX232 chip. The V25 address and control lines are decoded by IC44 and IC20 to produce device selects for the memory, LCD, and control registers. A programmable logic device (PLD) from Lattice Semiconductor, IC44, (a GAL16V8) produces the control signals required by the LCD panel. It also generates the RAM and ROM chip selects. The chip selects for the registers which control the logic analyzer section are produced by IC20.

The LCD is a 240 × 64 pixel graphics display with built in RAM, controller, and microprocessor interface. That display allows the logic analyzer to run a true windowed graphics interface under the control of the V25.

The TL7705 is a reset and power-supply monitor circuit. It produces a glitch-free reset signal on power up. It will also reset if the drops below 4.75 volts.

Each IC on the circuit board is de-coupled using a 0.1 μF capacitor. That is shown in the large capacitor array in Fig. 6. The power supply uses a standard three-terminal voltage regulator, IC43. Because the logic analyzer draws approximately 600 mA, a TO-3 type case and heat sink are used.

The analyzer is powered from a plug-in wall transformer which supplies an unregulated 9 volts DC. Note that the logic analyzer can also run off batteries. Six D-cell alkaline batteries will run the analyzer for over eight hours.

Next month when we continue, we'll show you how to build the logic analyzer, and how to use it to troubleshoot circuits. **R-E**