For stable, low distortion audio signals

Function Generator with digital readout

This attractively housed Function Generator produces sine, triangle and square waves over a frequency range from below 20Hz to above 160kHz with low distortion and good envelope stability. It has an inbuilt 4-digit frequency counter for ease and accuracy of frequency setting.

by JOHN CLARKE

Apart from a good multimeter and a power supply such as the one described last month, the next most useful piece of test equipment in the laboratory or home workshop is an audio generator. In the past 15 years or so, this would normally be a solid-state Wien bridge oscillator but more recently the function generator has come into its own, particularly where the potentially very low distortion of the former circuit is not required.

The particular advantage of a function generator is that it has good envelope stability. This means that the output level stays constant regardless of small or large changes in the frequency setting. This is not the case with typical solid state Wien bridge oscillators which are stabilised with a thermistor. These Wien bridge oscillators can fluctuate violently in output level when the frequency is changed and take several seconds to settle. This can be very frustrating when trying to measure the frequency response of a circuit or component such as a loudspeaker.

Using that attractive, low profile case for the Function Generator meant that a different approach was required to the conventional dial scale. If this was used it would have to be of small diameter and, in any case, it would be subject to the normal drawbacks of calibration accuracy, and considerable cramping at the high end of the scale.

This problem has been solved at one stroke by incorporating a 4-digit counter. This eliminates the need for any dial scale or any calibration procedure. The frequency counter uses the 50Hz mains as a timebase to give an accuracy of about ±2%.

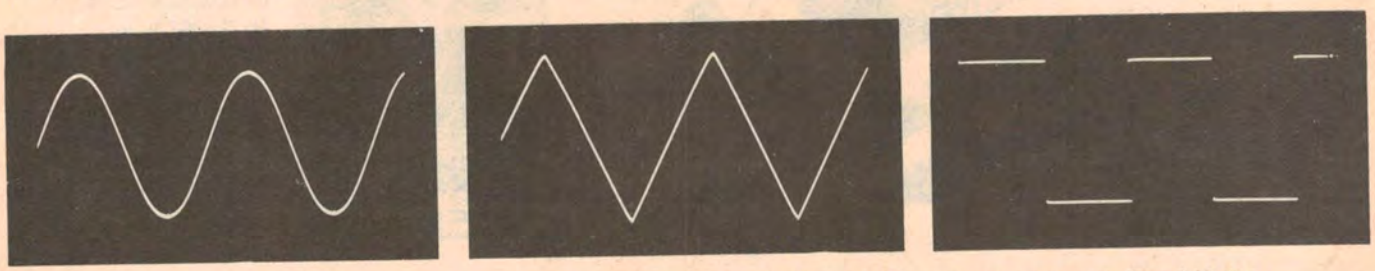
We used an XR-2206 IC from EXAR to generate the waveforms for our Function Generator. The operation of the IC can be described in four blocks: a voltage controlled oscillator (VCO), an analog multiplier and sine wave shaper, a unity gain buffer and a set of current switches.

Block Diagrams

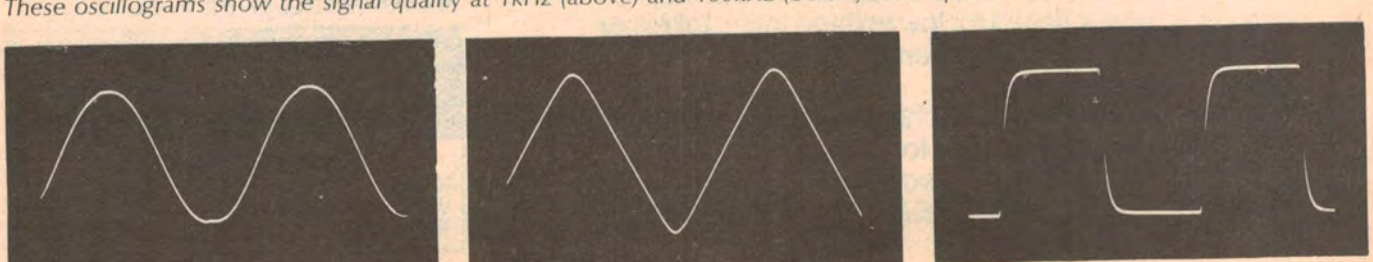
As can be seen in Fig. 1, the IC is capable of many operations including amplitude modulation (AM), frequency shift keying (FSK), and frequency modulation, via the current switches. The VCO is the major function block of the circuit, which generates the triangle and square waveforms at a frequency controlled by the current switches. Resistors tied from pins 7 and 8 are used to program the current switches and determine the VCO frequency.

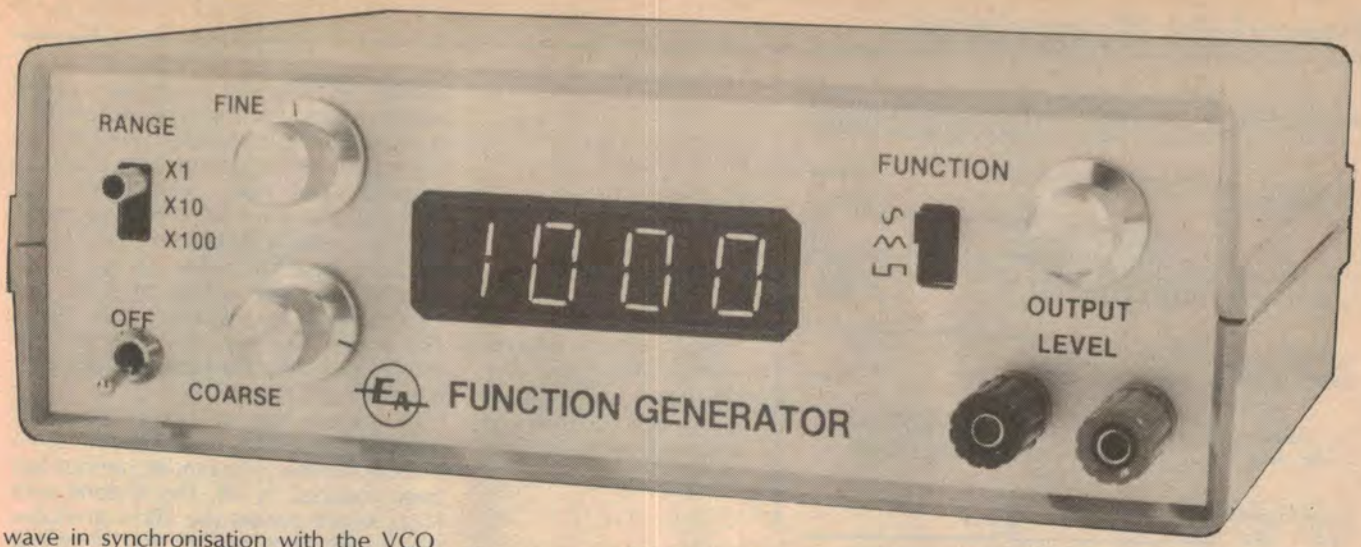
The multiplier and sine wave shaper performs several tasks. It accepts the triangular waveform from the VCO and reshapes this to a sine wave. In addition, the output level of these two waveforms is controlled by a resistor at pin 3 to ground and with the voltage at pin 1. Either sine or triangle is selected with a resistor across the waveform adjust pins (13, 14), or open circuit, respectively, while the unity gain amplifier buffers the sine or triangle waveform.

The sync output at pin 11 is an open collector output that provides a square



These oscillograms show the signal quality at 1kHz (above) and 100kHz (below). The square wave rise time is 0.4us.





wave in synchronisation with the VCO frequency.

Fig. 2 shows a simplified block diagram of the frequency meter. This can be divided into three parts: counter and display, latch and reset and timebase. The timebase gives three counter update times: 20ms, 200ms and 2s. Let us look at the counter operation in the 2s update situation.

The 50Hz mains signal is squared by a Schmitt trigger and then fed to two decade dividers for an overall division of 100, giving a waveform with a period of two seconds. This waveform is fed to the latch and reset circuitry so that the input signal to be counted (from the function generator) is gated into the counter in one-second bursts, every two seconds. At the end of each one-second count period, the value of the count is latched (stored in 16 flipflops, four for each digit) and displayed. The counter is then reset, ready for the next count.

When the update time is two seconds, as discussed above, the display indicates the frequency directly in Hertz. For the 0.2 second update time, the reading must be multiplied by 10 and for the .02 second (20ms) update time, multiplied by 100.

Having discussed the circuit in block form, let us now look at the complete circuit diagram in detail.

IC1, the XR-2206 monolithic function generator, is connected to provide both the sine and triangle wave signals. R2 and R3 are trimpot resistors which are used to preset the level of the sine and triangle waves. When switch S1 is in position 2, a triangle wave is produced at pin 2 and the output level of this wave is determined by R2 since R3 is short circuited with S1c. When S1b is in position 1, a sine wave is produced and the output level of this is determined by R2 and R3. R3 is adjusted so that the sine wave level is the same as the triangle wave level.

In the sine wave mode, the sine wave shaper is brought into play to "round off" the peaks of the triangle wave. Critical adjustment of R4, between pins 13 and 14 of IC1, gives minimum distortion of the sine wave. R1, the symmetry adjustment between pins 15 and 16, is adjusted for equal positive and negative swings of the sine and triangle waveforms. Adjustment of these trimpots will be discussed later in this article.

S2a is used to select the three frequency ranges by switching separate timing capacitors across pins 5 and 6. Frequency adjustment is with the fine and coarse variable resistors and the 4.7kΩ resistor sets the maximum frequency for each range. The frequency of the generated signal is a function of the capacitor value between pins 5 and 6 and the frequency

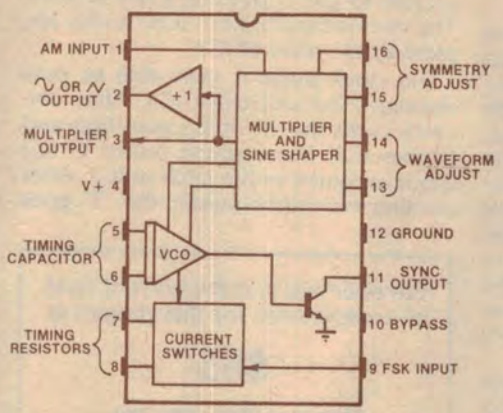


FIG. 1

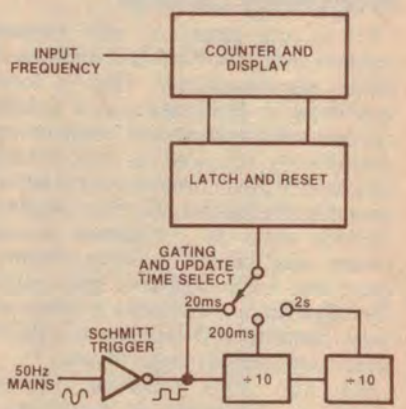


FIG. 2

adjust resistors. The actual formula is $F = 1/RC$. Since C is a constant for each range, the frequency is proportional to 1/R.

With this 1/R relationship, the actual change in frequency with respect to the change with resistance is hardly linear especially when the resistance is small. This tends to give an unusable control at the low resistance end if only the coarse control were available. With the addition of a low value fine control, frequency changes are easily accomplished at the low end of the resistance range. The fine control has little effect at the high resistance end of the coarse control since, at this end, large changes in resistance are required for a small change in frequency.

The open-collector square wave output of IC11, pin 11, is provided with an external 2.2kΩ pullup resistor to drive the input of IC7a, a Schmitt trigger which provides buffering and further squaring of the waveform. IC7c acts as a further buffer to drive an attenuator and then the transistor output stage. The attenuator (voltage divider) consists of 1.8kΩ and 2.2kΩ resistors, to adjust the level of the square wave to the same peak-to-peak level.

S1a selects the sine, triangle or square wave and the signal is attenuated with the 22kΩ level potentiometer. The resulting signal from the wiper of the pot is fed to the input of the emitter follower output stage.

The emitter follower stage consisting of the NPN BD139 and PNP BD140 transistors is a complementary symmetry arrangement. The NPN transistor drives the output for positive input signals and the PNP transistor drives for the negative input signal. To prevent crossover distortion at the transition when one transistor takes over the signal from the other, the transistors are biased on so that a quiescent current flows through both transistors. 2.2kΩ and 1kΩ base bias resistors set this current at around 40mA.

Heavy supply decoupling, consisting of the 100Ω resistors and 47μF capacitors across each supply rail, ensures good rip-

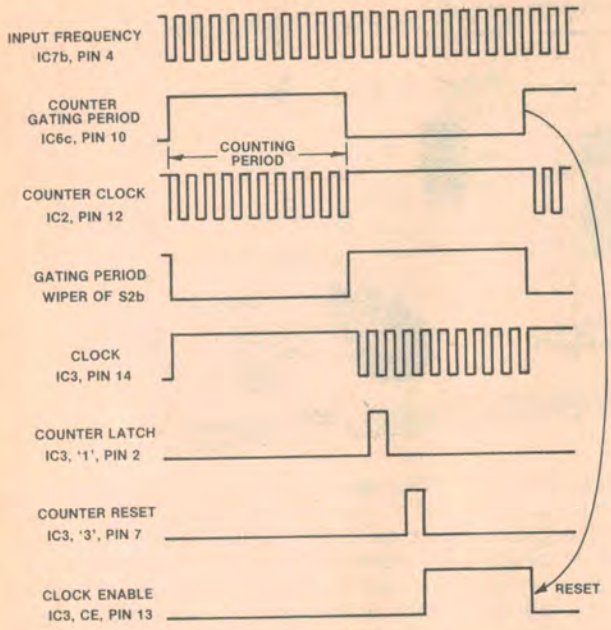


FIG. 3

These timing waveforms illustrate the operation of the inbuilt frequency counter in the Function Generator.

ple rejection. This allows the output signals to be attenuated, to millivolt levels without hum and noise swamping the signal.

Output impedance of the stage is a nominal 600Ω for all output levels.

Frequency Counter

IC2 is the heart of the frequency counter and is a 74C926, made by National Semiconductor. This is loosely described by the makers as a 4-decade counter with multiplexed 7-segment output drivers. As well as the 4-decade counters, it also contains a 4-bit latch for each decade (the four flipflops alluded to earlier), BCD to 7-segment decoder drivers and the multiplexing circuitry to drive the seven segment lines and the four digit driver transistors. It drives common cathode LED displays via BC337's which are used as digit drivers.

For the 50Hz timebase reference signal, a connection is made to the transformer secondary via a 10kΩ resistor. This is clipped by diodes connected to the positive and negative 5V supplies and then fed to the input of IC7d, another Schmitt trigger, to be squared up. This signal is then fed to two 4017 decade dividers in cascade (IC4 and IC5) to produce a 0.5Hz signal (2-second pulses) which gates the 4-digit counter, as described previously.

The timing operation of the circuit is best explained with the waveform diagrams of Fig. 3. Firstly we will assume S2b to be in position 1 for the purposes of explanation. When the waveform at the wiper of S2b is low, the output of IC6c, connected as an inverter, is high and the input frequency from IC7b is allowed to pass to the output of IC6a and to the clock input of IC2. IC2 then counts the number of clock pulses. When the wiper of S2b goes high, the output of IC6c goes low and the clock signal to IC2 is prevented from passing to IC6a and further clocking IC2. IC2 then stops counting the clock signal.

When switch S2b is in position 1, the 50Hz is divided by 100 and this signal is applied to pin 12 of IC6d, a NAND gate. The inverted signal from IC6c is also applied to the reset of IC3.

The clock signal is now able to pass through IC6d and clock IC3. After one clock cycle, the "1" of IC3 goes high and latches IC2. The counted pulses of IC2 are now stored in the latch of IC2. After another two clock pulses, the "3" goes high and IC2 is reset, ready to count the next set of clock pulses. When the "4" output goes high at the next clock cycle, the CE or clock enable is disabled (high) and remains high until reset with pin 10 of IC6c going high.

We estimate that the current cost of components for this project is

$85

This includes sale tax.

So the complete cycle of events in counting the clock pulses occurs in this sequence. The cleared counter of IC2 begins to count the clock pulses and is stopped counting when half the timebase period has completed. One clock cycle after this, the counter is latched and the latched count is displayed on the display. The counter is then reset with IC3 and IC3 waits for the end of the timebase cycle when it is reset.

With S2b in position 1, the displayed count is in Hz since the counter counts over the period of 1 second. When S2b is in position 2, the display is in Hz x 10 since the counter counts only over 0.1 seconds. The third position of S2b provides a .01s or 10ms counting time and the display is in Hz x 100. If the signal for this timebase were to be taken directly from the output of IC7d, the display would be updated every 20ms. This would lead to a very fast changing display and make the last digit appear as a flickering 8.

To alleviate the fast update time, the counting period has been kept the same but the number of counting periods has been reduced by 10. This is done with IC6b, which passes the 20ms timebase signal only when pin 10, the "4" output of IC4 goes high or once in every ten 20ms cycles.

Note that S2 selects both the gating time of the frequency meter section and the capacitor of the function generator, IC1.

Power for the circuit is derived from a full-wave centre tapped supply, providing positive and negative supply rails. Filtering is provided with 1000μF capacitors connected from each supply rail to ground.

There are three 5V regulators, one positive and two negative. One −5V regulator supplies IC1 and IC7 while the other supplies IC2 and the associated logic ICs. The reason for this unusual arrangement is to isolate the severe multiplexing noise generated by IC2, from the function generator, IC1. This results in an output waveform free from the noise generated on the other negative supply line.

The 1μF and 10μF capacitors connected at the input and output of each regulator prevent instability in the regulators and provide transient and ripple rejection at the regulated output.

It should be noted that while IC2 is powered from the negative 5V rail, its CK, LE and R inputs are driven from IC6 and IC3 which are powered from ±5V rails. This means that these signals will swing above the Vcc line for IC2 by +5V. However, although IC2 can only be operated from a maximum supply voltage of 6V it can safely handle signal voltages up to 15V without damage.

Construction

We constructed our Function Generator in a Pac-tec case measuring 207 x 64 x 159mm and mounted the components on two PC boards. The main PC board is coded 82ao3a and measures 169 x 126mm, and the display PC board is coded 82ao3b and measures 83 x 46mm. A Scotchcal front panel artwork has been produced for the front panel of the Pac-tec case and measures 199 x 61mm.

The larger of the two PC boards is

designed to be screwed to the base of the case and the smaller PC board soldered at right angles to the main PC board. Check that the copper runs right to the edge of the 82ao3a PC board. If not, file the PC board until the copper is flush to the edge.

Next the components can be soldered to the PC board. Use the overlay diagram to help you position the components. It is easier to place the low profile components on the PC board first, such as the links, resistors and diodes followed by the ICs. When soldering the CMOS ICs, solder the supply rails first with the barrel of the soldering iron earthed and then solder each pin quickly. Pay particular attention to orienting the ICs correctly.

When all the components have been positioned, check your work and make sure that all the polarised components such as the diodes, capacitors, transistors and ICs are correctly oriented. Now work can begin on the display PC board. Place the links in first and then the displays. The displays are oriented so that the ribs at the top edge of the display are at the top. When soldering the displays keep them all in line and butted close together.

Placing the PC boards aside for the moment, work can begin on the front panel. We used countersunk screws to support the slider switches so that the Scotchcal panel can be placed over the screws and provide a front panel finish unmarred with screws. In doing this, construction is more difficult, since the rectangular holes for the switches have to be shaped before the Scotchcal label is applied to the front panel, however, the final result is well worth the effort.

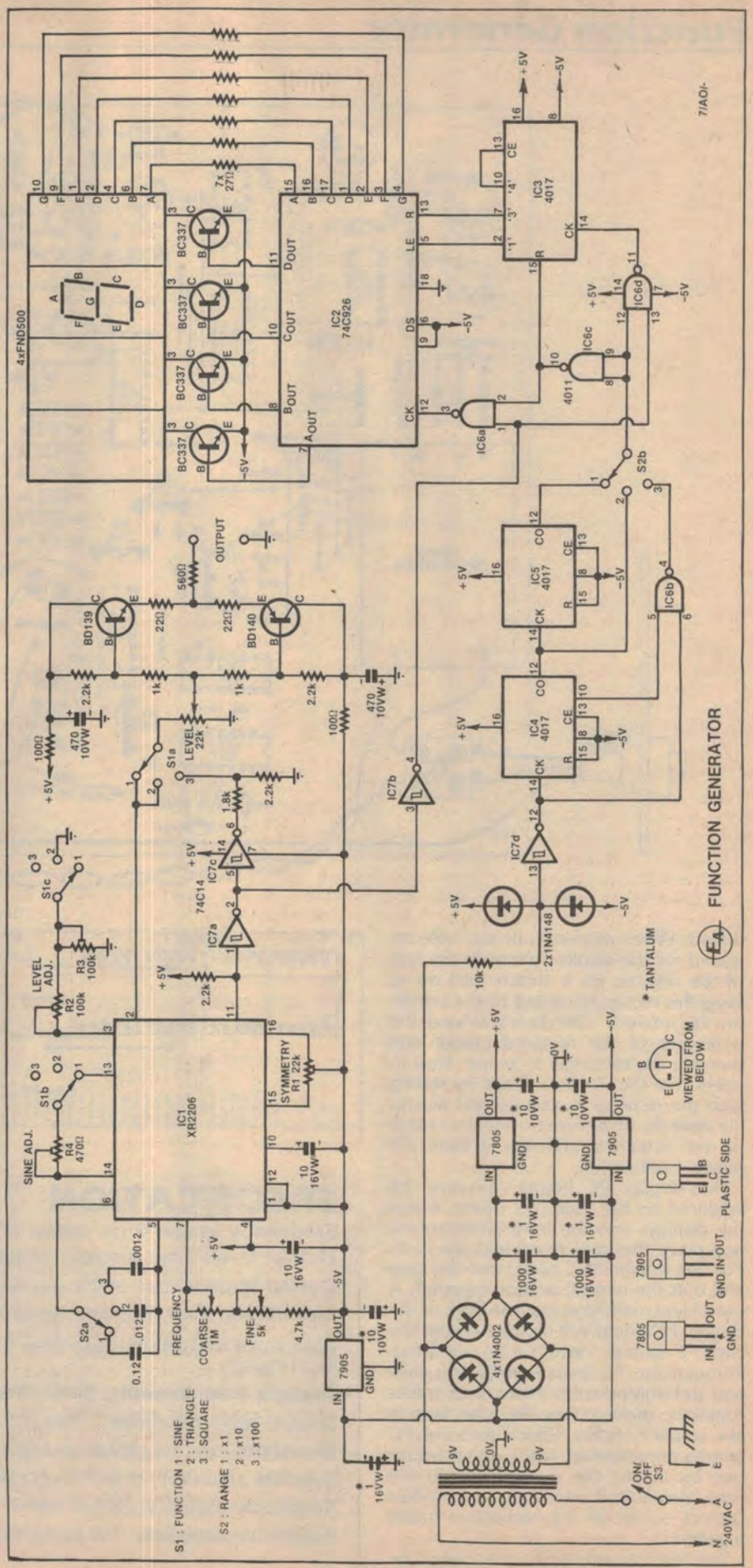
Our prototype used a 2-pole slider switch and a 3-pole slider switch, which agrees with the circuit and wiring diagram. However, these have different actuators, round for the 2-pole and square for the 3-pole. So for a better visual effect, it would be better to install two 3-pole sliders,with one pole unused on the Range switch.

We have found that the Scotchcal will stick better to the smooth surface of the plastic panel rather than the stippled side. So use the smooth side of the plastic as the front face of the panel.

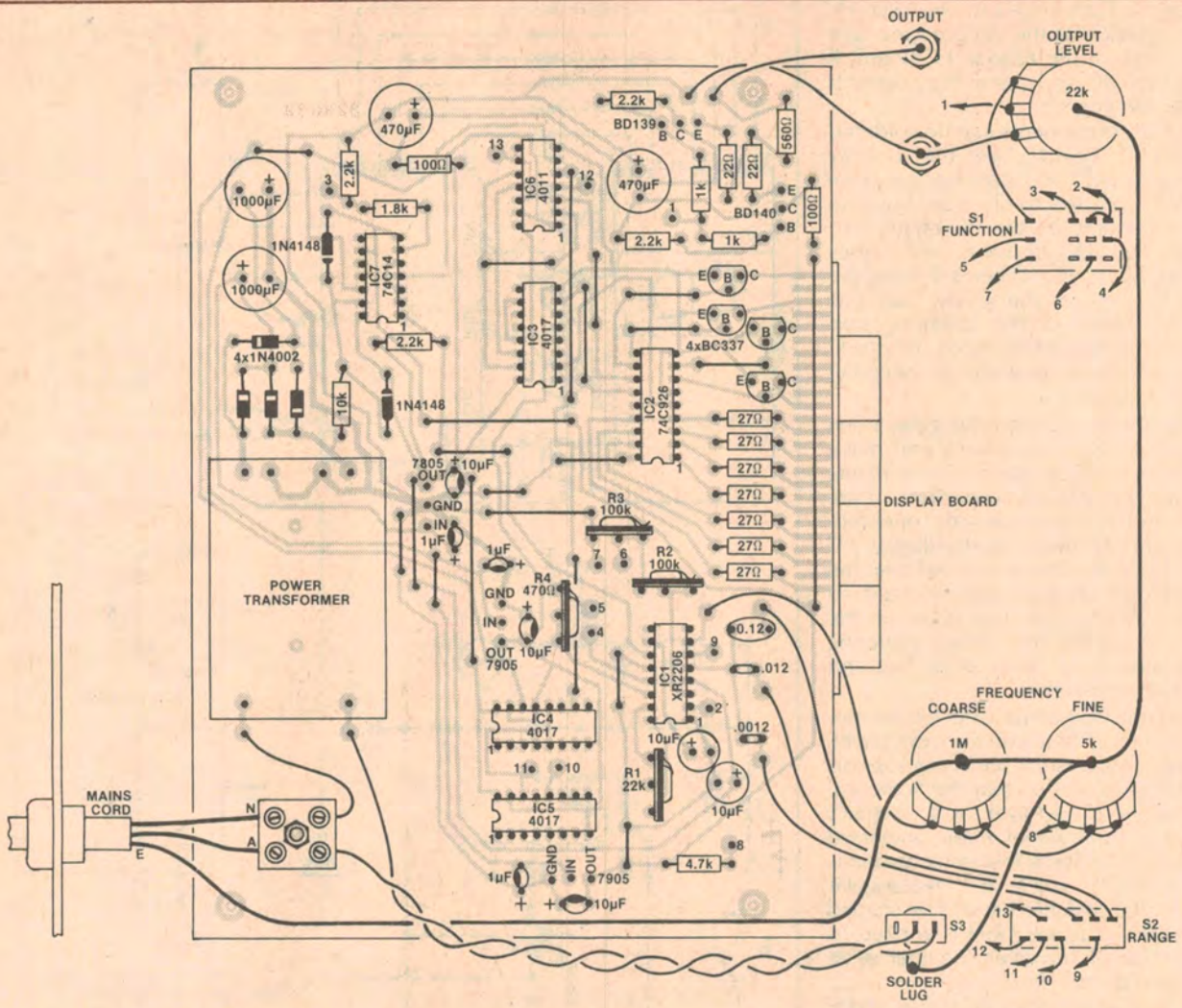
Using the Scotchcal art work as a guide, mark up the positions required for the slider switches. Drill and file the rectangular holes and drill the mounting holes and countersink them. Mount the slider switches and check that the rectangular hole is large enough not to affect the operation of the switch slider. The Scotchcal panel can now be positioned on the front panel.

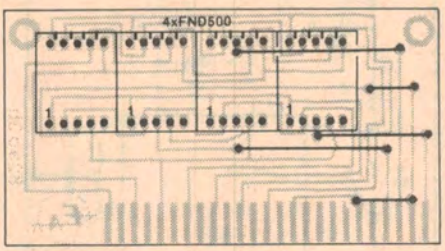
Now cut the holes in the Scotchcal panel for the switches and use the slider switch actuators to guide the Scotchcal when placing it on the plastic front panel baseplate.

The holes for the on/off switch, terminals and potentiometers can now be



WIRING DIAGRAM





These wiring diagrams show the PC boards from the component side. The display board (left) butts against the main board at right angles and is soldered to it via the edge connector strips. Use 250VAC-rated cable for all mains wiring.

drilled. When marking out the hole required for the display, measure the size of the display, 61 x 16mm, and try to keep this rectangle central to the border on the artwork. Drill holes around the perimeter of the required cutout and then file the rectangle to shape. Stop to check that the size is to shape by testing with the displays as you go and always file inwards, otherwise the file may catch on the Scotchcal and tear it from the plastic front panel.

The display PC board can now be soldered to the main PC board. Insert the displays into the front panel cutout and place the front panel into the case. Position the main PC board into the case and butt the two PC boards together. A pencil line marked across the back of the display PC board will indicate where the two PC boards have to be soldered. Remove the PC boards from the case and tack solder two of the copper tracks together, making sure that the boards are at right angles. Check that the PC boards are soldered in the correct position by testing the construction in the case. Readjust if necessary, and, when correct, solder all the respective tracks together.

The internal wiring can now begin. Fit

SPECIFICATION

Frequency range: From below 20Hz to 170kHz in three ranges.

Output level: Continuously variable from 3mV to 2.5V peak-peak.

Output impedance: 600Ω (nominal).

Waveforms: Sine, Triangle, Square.

Sine wave distortion: Less than 0.7% at 1kHz; 1% at 10kHz and 2% at 100kHz.

Triangle wave linearity: Better than 1% at 1kHz.

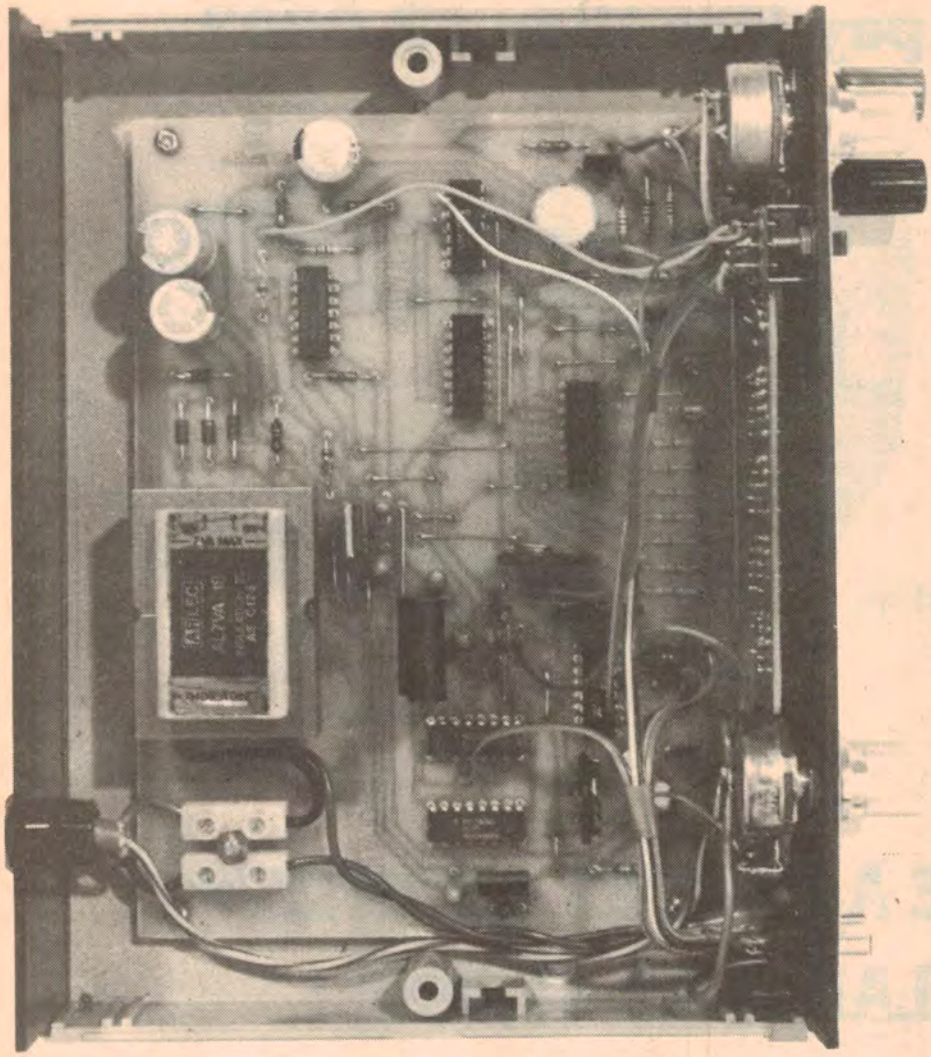
Square wave rise-time: 0.4us (6V/us at maximum output level).

Overshoot, etc: Negligible overshoot, droop or ringing.

Readout accuracy: ±2% + one digit.

Amplitude stability: Better than 0.1dB on all ranges.

Power consumption: 7W at 240VAC.



A view inside the prototype, showing the completed PC board assembly. Note the clip on heatsink for one of the negative regulators.

the potentiometers, mains switch and terminals to the front panel and wire them to the PC board with the aid of the wiring diagram. Several layers of insulation tape should be wrapped around the mains switch after the mains wires have been soldered to it. We also placed some layers of tape over the mains entry to the transformer under the PC board as a safety precaution. The terminal block mounts directly onto the PC board as shown. The earth is soldered to the rear of the potentiometers and to the on/off switch washer.

The mains cable is clamped to the rear of the case with a cord grip grommet. A small clip on heatsink is required for the negative regulator which supplies IC2.

When the wiring is complete, check your work against the wiring diagram and, if all is correct, the generator is ready to be switched on. Check that all the regulators supply the correct voltage and that the digital display is functioning. Different frequencies should be obtained when the coarse frequency control is adjusted. Try the control on all ranges.

Setting up

Setting up the Function Generator can be achieved in one of two ways: by using an oscilloscope (if available), or by using a loudspeaker or headphones. For either method, the symmetry trimpot, R1, and the sine adjust trimpot, R4, should initially be adjusted for a midway setting. The level adjust trimpot should be set to the minimum resistance setting (toward the rear of the case) and setting up begun with these settings.

When using an oscilloscope, the maximum level of the sine wave can be determined before clipping by adjusting either R2 or R3. Then switch to the triangle waveform and adjust R2 to give a triangle wave level the same as the previous sine wave setting. Return to the sine wave and adjust the level with R3 only to a level just before clipping. The triangle wave and sine wave levels should now be the same.

PARTS LIST

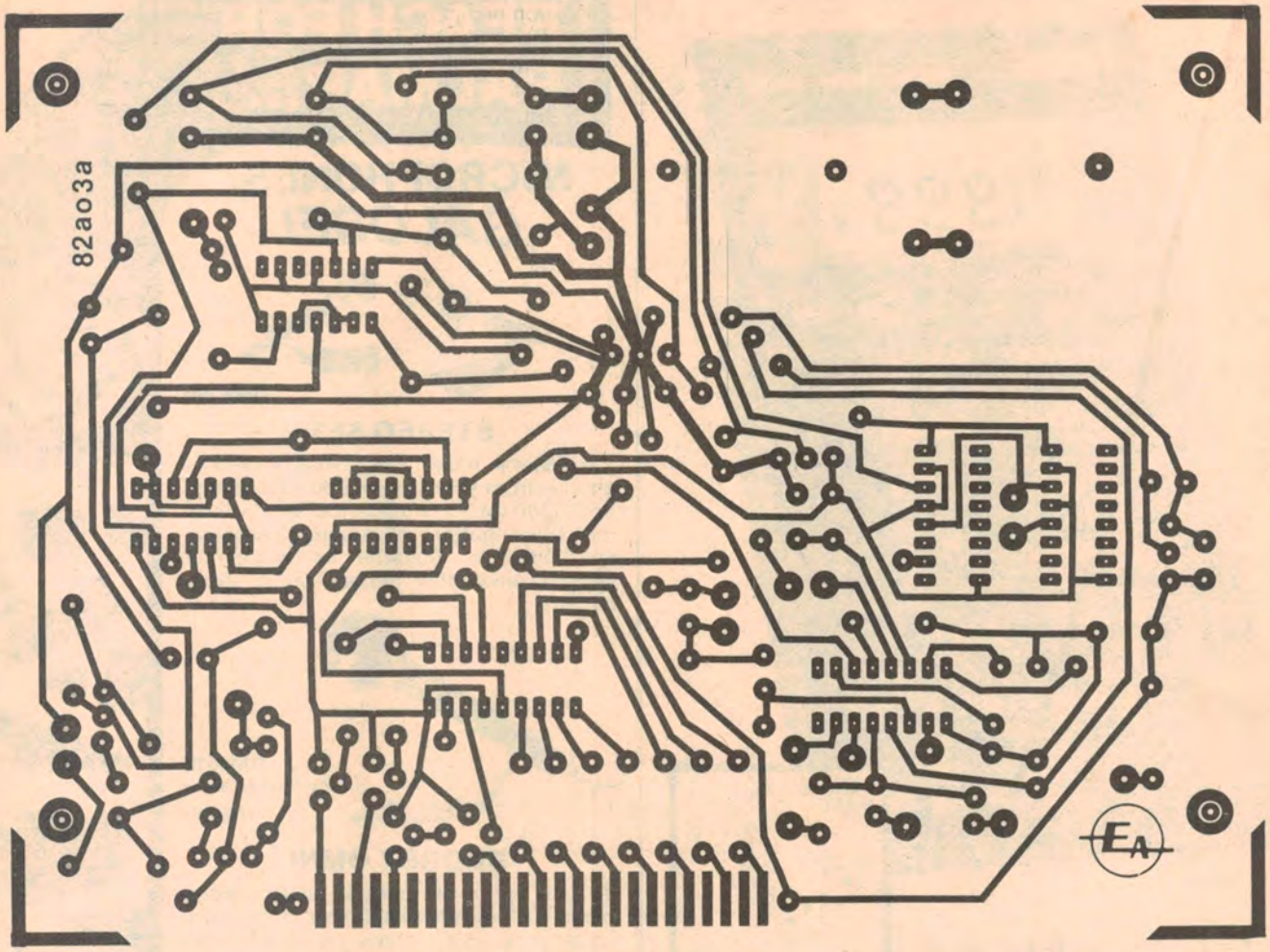
1 printed circuit board, code 82ao3a, 169 x 126mm
1 printed circuit board, code 82ao3b, 83 x 46mm
1 Arlec AL7VA/18 or Ferguson PL18/5VA PC mounting transformer
1 Scotchcal front panel, 199 x 61mm
1 Pac-tec case, 207 x 64 x 159mm
1 clip-on T0-220 heatsink
1 SPDT switch
2 3-pole, 3-position slide switches (see text)
1 mains cord and plug
1 2-way insulated terminal block
1 cordgrip grommet
2 binding post terminals, one red, one black
3 knobs

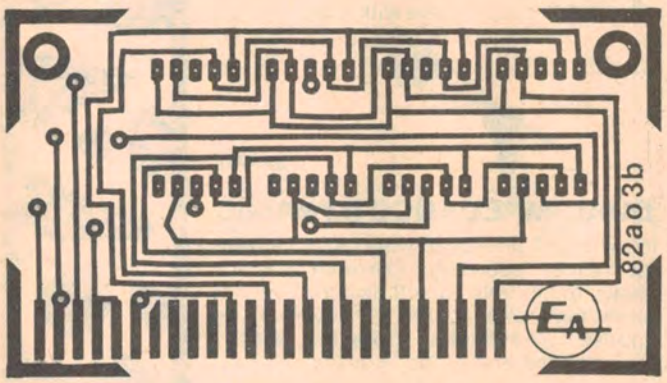
SEMICONDUCTORS
1 XR-2206 monolithic function generator
1 74C926 4-digit counter
3 4017 decade counter/dividers
1 74C14 hex Schmitt trigger
1 4011 quad NAND gate
2 7905 three terminal 5V negative regulators
1 7805 three terminal 5V positive regulator
4 1N4002 rectifier diodes
2 1N914, 1N4148 small signal diodes
1 BD139 NPN transistor
1 BD140 PNP transistor
4 BC337 NPN transistors
4 FND500 common cathode LED displays

CAPACITORS
2 1000µF/16VW PC electrolytic
2 470µF/10VW PC electrolytic
2 10µF/16VW PC electrolytic
3 10µF/10VW tantalum
3 1µF/16VW tantalum
1 0.12µF metallised polyester
1 .012µF metallised polyester
1 .0012µF metallised polyester

RESISTORS (¼W 5%)
1 x 10kΩ, 1 x 4.7kΩ, 4 x 2.2kΩ, 1 x 1.8kΩ, 2 x 1kΩ, 1 x 560Ω, 2 x 100Ω, 7 x 27Ω, 2 x 22Ω.
2 x 100kΩ large vertical trimpot
1 x 22kΩ large vertical trimpot
1 x 470Ω large vertical trimpot
1 x 1MΩ (lin) potentiometer
1 x 5kΩ (lin) potentiometer
1 x 22kΩ (lin) potentiometer

NOTE: Components specified are those used in the prototype. Components with higher ratings may generally be used providing they are physically compatible.





Full size artwork for both of the PC boards.

R4 can be adjusted for best visual sine wave output and the symmetry trimpot, R1, adjusted for a symmetrical waveform. The distortion trimming should be done at 1kHz.

If no oscilloscope is available, then satisfactory results can be achieved with either a loudspeaker or with headphones. Connect to the output terminals and increase R2 and R3 together when listening to the sine wave. Adjust the output level potentiometer to a suitable listening volume. The point at which the sine wave clips will be immediately obvious from the marked increase in distortion. Back the two trimpots off slightly from this point. If both the trimpots are set to the same resistance value, the sine and triangle wave should be of a similar output level.

Now disconnect the loudspeaker or headphones, switch to sine wave and connect a multimeter across the output. With multimeter set to read 200mV DC or less, adjust R1 for a zero reading. If no meter is available with reasonable sensitivity, set R1 to the centre of its range.

In adjusting the sine wave for symmetry, you are equalising the positive and negative swings of the waveform.

Now reconnect the loudspeaker and adjust R4 for minimum distortion on sine wave at 1kHz. This is done by listening closely for the purest tone. At one extreme (minimum resistance) odd harmonics will predominate while at the other extreme, even harmonics will predominate, so there is a definite setting in between where the tone is purest. With careful setting, it is possible to adjust the distortion by this method to less than 0.7%.

With both setting up methods, the clipping point of the sine wave should be readjusted after trimming the distortion. The maximum expected output level of the sine wave is around 6V peak to peak.

If you have access to a distortion analyser, it is possible to obtain a minimum harmonic distortion of around 0.5% by critical adjustment of R1, R3 and R4. This will result in distortion of less than 1% at 10kHz and around 2% at 100kHz. These figures will naturally be slightly higher if you have used the methods described above. Even so, for most audio work, this is entirely satisfactory.