Maximum voltage detector needs no a-d conversion

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A detector that determines which of a set of analog voltages has the greatest positive value is useful for pattern-recognition systems and other classifying schemes. Only the relative magnitude of the input voltages is important in these applications, so that costly analog-to-digital converters are not needed.

As shown in the figure, a sample set of voltages is introduced at the noninverting port of a bank of 711 dual differential voltage comparators, which initially switch each amplifier high. All inverting inputs are driven by any monotonically increasing waveform, such as a ramp voltage.

Each comparator switches into the low state as the ramp voltage exceeds the particular sample voltage connected to its input, until only one comparator remains in the high state. The signal at this op amp input has the greatest amplitude in the sample set.

The combinational logic at the 7430 NAND gate array then generates a pulse to the 74174 device, clocking the lone logic 1 signal from the op amp input into the D input of its associated flip-flop and presenting it to the processing device. By this time, the ramp voltage has returned to its minimum value, and the next sample set may be again introduced.

As shown, the range over which the sample-set voltages may be detected lies between zero and 5 volts. This range may be changed by suitable adjustment of the ramp and supply voltages to the comparators. The use of complementary-metal-oxide-semiconductor logic circuits is advised when the operating voltage to the comparators exceeds 5 volts. ☐

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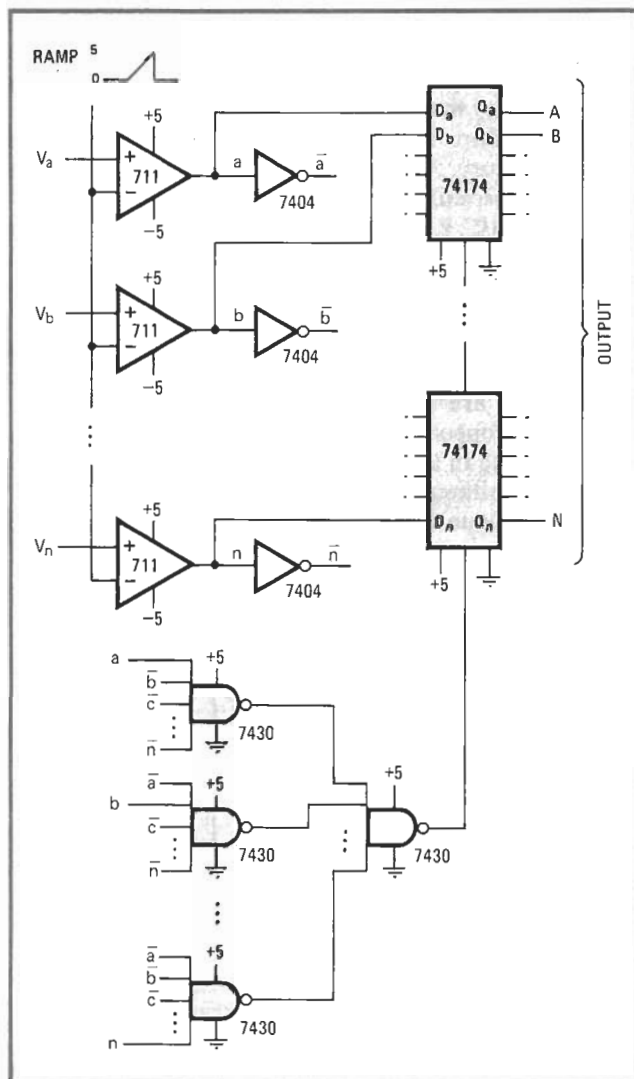
Maximum-voltage detector. Relative maximum of sample set $V_1 - V_n$ is determined by ramp generator and logic circuit. Sample voltages drive all comparators high if values lie above the minimum ramp voltage. Logic detects lone op amp remaining high during the ramp sweep and clocks that state to its D flip-flop.