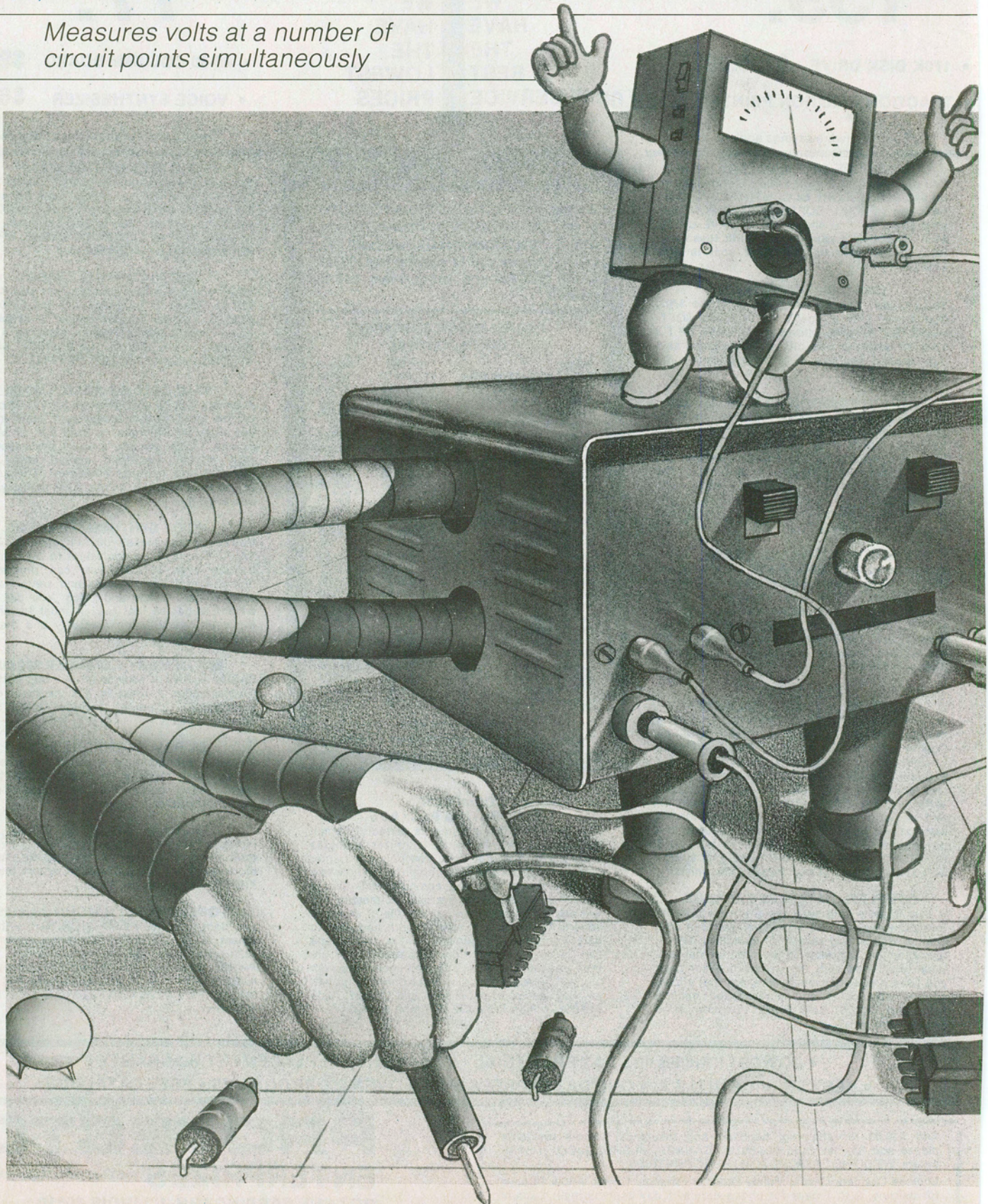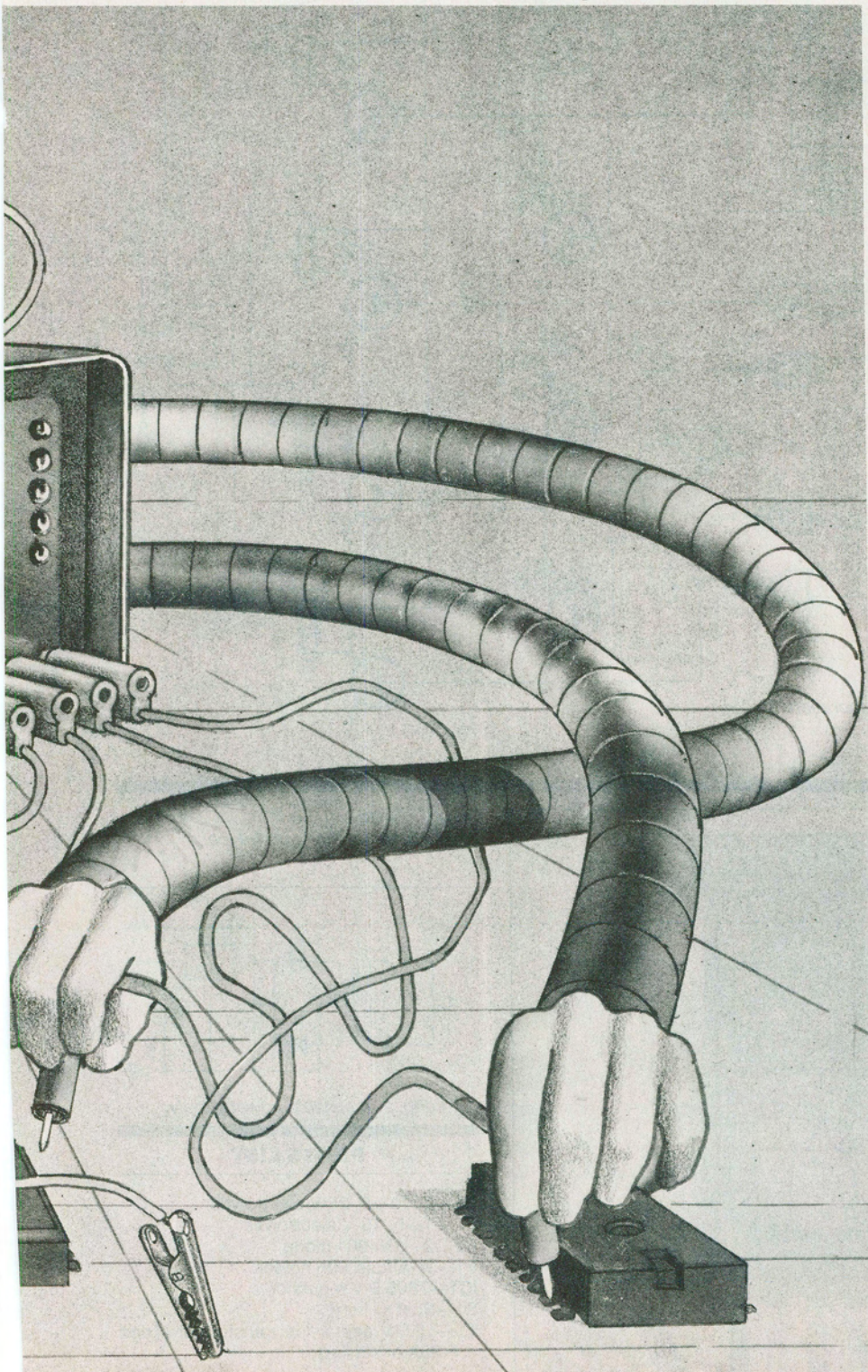# A MULTIPLE TEST-POINT

Measures volts at a number of circuit points simultaneously

MONITOR

By George Gooder

HAVE you ever had a situation arise in troubleshooting or aligning an electronic circuit when adjustments of a potentiometer, capacitor, or coil caused two or more test point signals to vary simultaneously? When this happens, you must either move your test equipment inputs from one point to another or use several pieces of the same equipment to monitor each test point at the same time.

The Multiple Test-Point Monitor described in this article overcomes this problem. It can measure up to four test points at intervals of 1 to 10 seconds. All four test points can have the same polarity, or two can have positive polarity and the other two negative. The monitor can also be set to operate on two test points only or "look" at one preselected test point indefinitely.

Circuit Operation. As shown in Fig. 1, the circuit is based on *IC2*, a 4-bit shift register. The inputs to this register are loaded with a binary "1000" when pins 4, 5, and 6 are low, and pins 9 and 10 are high.

When pin 10 is forced low and the right shift is activated by a signal on pin 2, clock pulses from *IC1* shift the 1 bit to the right thus changing the binary word at pins 12 through 15. After a 2- or 4-bit shift (whichever is selected by *S2*), the 1 bit returns to the A output (pin 15).

Switch *S2* performs two functions. It initializes the *IC2* ABCD inputs to binary 1000 and sets the system to shift 2- or 4-bit positions. When *S2* is momentarily activated, it places a low at pin 1 of *IC3A* (a set-reset flip-flop) which forces its pin 3 high. This high is coupled to pin 10 of *IC2*. With pin 9 of *IC2* tied to high, the next clock pulse will initialize *IC2*. The low-to-high transition at *IC3A* pin 3 is also fed to the clock input of *IC6A* to toggle this flip-flop. When *IC6A* is set, *IC2* shifts 4 bit positions, and when *IC6A* is reset, *IC2* shifts 2 bit positions. The shift is actuated by a closure of momentary switch *S2* for one clock pulse.

Transistors *Q1* and *Q2* are driven by the A and B outputs of *IC2*, while *IC4A* and *IC4B* gate bits C and D from *IC2* to transistors *Q3* and *Q4*, with *IC6A* inhibiting or enabling the two gates. When *IC6A* is set, the gates are enabled, and when *IC6A* is reset, they are inhibited. Gate *IC4B*'s output at pin 6 is also fed to *IC5A* to reenter the 1 back into the shift register A position after 4 shifts, while *IC4C* shifts the 1 back to the shift register when the system is in a 2-bit monitor position. Gate *IC4C* is enabled or inhibited by *IC6A* depending on whether the latter IC is set or reset. Gate *IC5B* puts bits A and B from *IC2* through to one section of *S3* to activate *Q5*. Transistor *Q5* and relay *K5* form a polarity-switching network that allows negative signals to be monitored at *J1* and *J2* without changing the voltmeter leads.

The clock signal generated by *IC1* can be adjusted from one pulse per second to one pulse every 10 seconds by potentiometer *R3*. The clock output is fed to one input of AND gate *IC4D*, whose other input comes from the set-reset
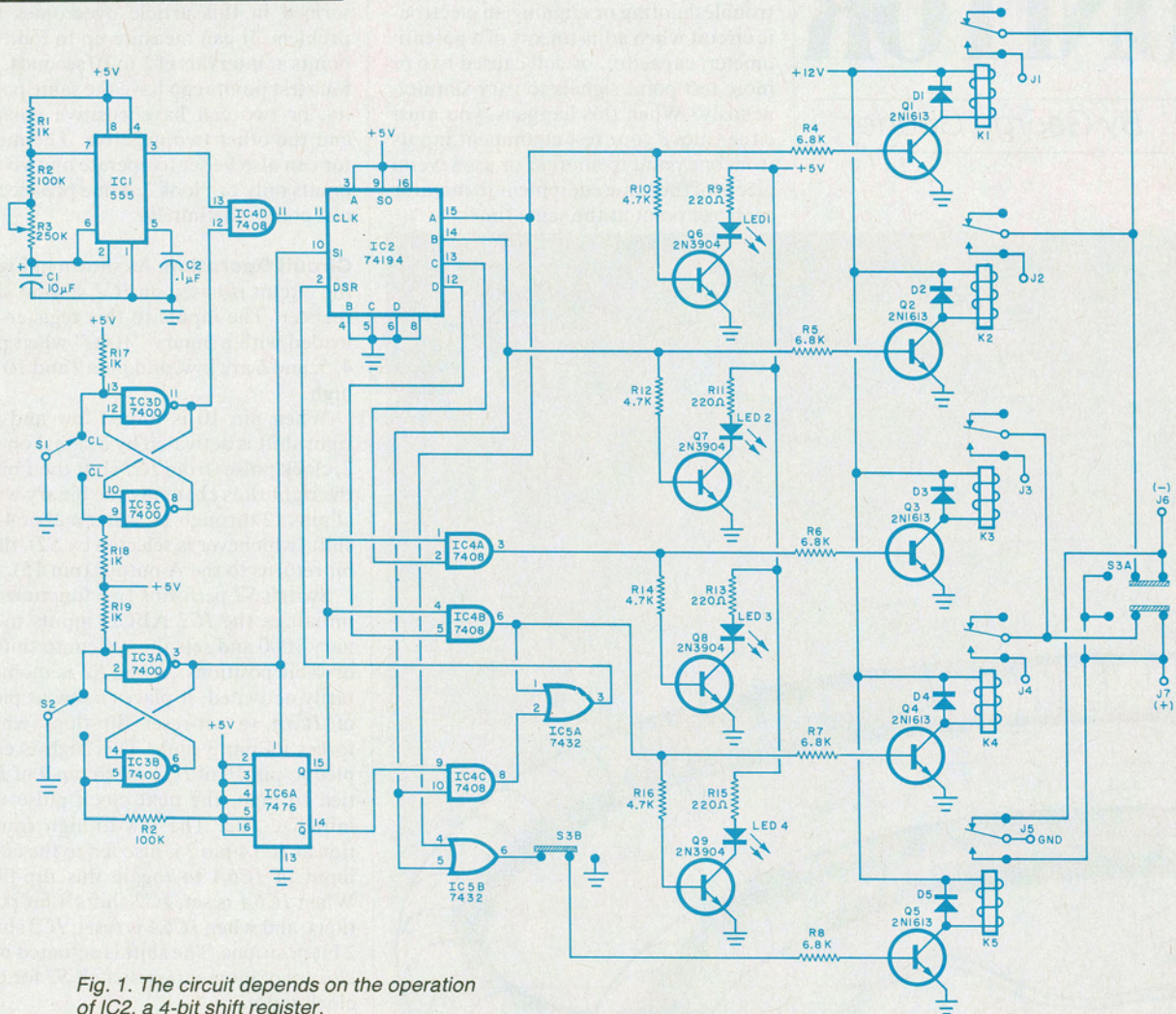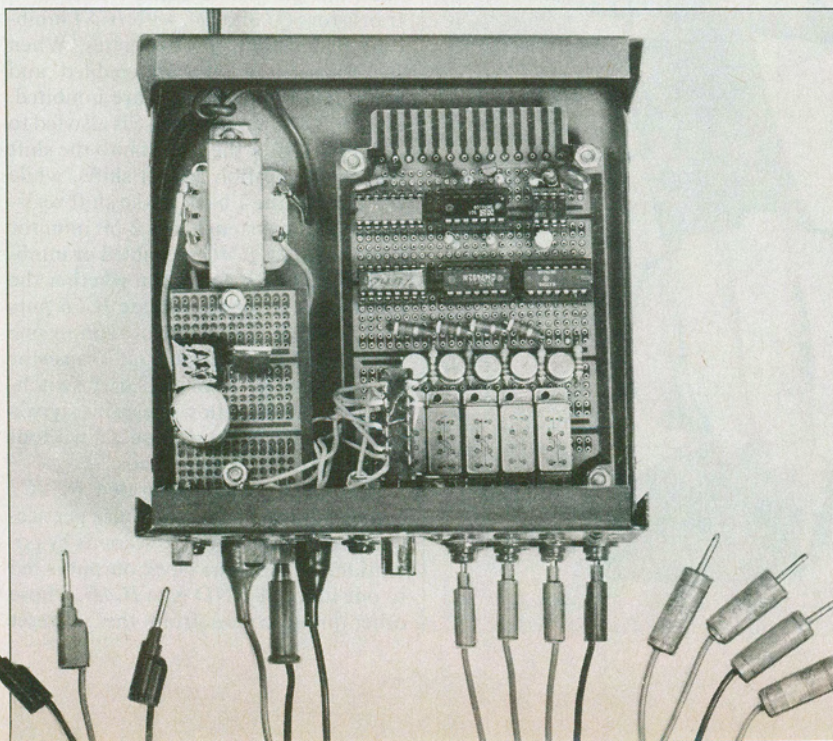
Fig. 1. The circuit depends on the operation of IC2, a 4-bit shift register.

At left is a view of the inside of the author's prototype.

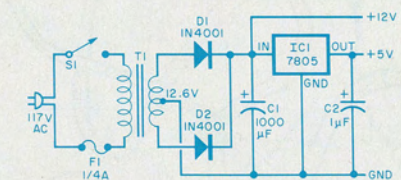Fig. 2. A suitable power supply.

PARTS LIST

C1—1000-µF, 25-V electrolytic
C2—1-µF, 10-V electrolytic
D1,D2—1N4001 diode
F1—¼-A fuse with holder
IC1—7805 5-V regulator
S1—Spst switch
T1—12.6-V center-tap transformer (Triad F-25X or similar)

flip-flop formed by *IC3C* and *IC3D*.

The *IC3* flip-flop is switched by the operation of *S1* to either enable or inhibit the clock signal from reaching *IC2*. Stopping the clock signal allows indefinite monitoring of one selected test point.

The four lines driving relay drives *Q1* through *Q4* are monitored by transistors *Q6* through *Q9*, each of which has a LED and associated current-limiting resistor as a collector load. When the line goes high, it activates both sets of transistors thus selecting one line and indicating it by the glowing LED.

Construction. Since parts placement is not critical, any type of construction can be used. Once a board has been constructed, it can be mounted with the associated relays and a power supply (see Fig. 2 for a circuit) in a convenient enclosure. The front panel should mount the four input banana connectors *J1* through *J4*, the system ground connector *J5*, clock speed control *R3*, and the three switches (*S1* through *S3*).

Input connectors *J1* through *J4* are connected to the signals of interest, while *J5* is connected to the tested system's ground. Connectors *J6* and *J7* connect to the monitoring device being used (voltmeter, scope, etc.) in accordance with the polarity specified by *J6* and *J7*. ◇

BEEP! BEEP! BE....

Add a power-failure sensor to any ac digital clock

By James Antonakos

MOST digital clocks do not have the backup circuits (reserve power supply and oscillator) necessary to keep them running during a power outage. Thus, it is possible that someone glancing casually at a clock can be misled as to the time. One way to combat this problem is to install the "Power Out Sensor" in your digital clock. After a power failure, the circuit will "beep" until you reset the clock.

Circuit Operation. When power is first supplied to the circuit, a positive spike, produced by *C1*, is applied to the SET input of flip-flop *IC1*. This causes the Q output to go high and enables one half of the dual timer, *IC2*. The latter oscillates at about 5 Hz, alternately enabling the other half, a 1-kHz oscillator. The circuit will continue to oscillate until the flip-flop is reset by momentarily closing *S1*. This forces Q low and disables the timer. The circuit will remain in this state because the inputs to the 4027 are grounded through *R3*. Therefore, the circuit is actuated only when power is shut off and then re-applied.

The output from *IC2* is applied to emitter follower *Q1*, which drives the speaker through *R10*. The value of the latter resistor is selected for the desired audio level. If the clock is a radio alarm, its speaker can be used, or any small type of speaker can be added. If desired, the audio oscillator output from pin 9 of *IC2* can be used to drive any external audio system.

Construction. Assembly is not critical. The prototype was built on a standard perf board cut to fit into the clock to be used. A printed-circuit board could be used but is not required and is time-consuming to prepare.

Because CMOS integrated circuits are used, the supply voltage can be any value between 5 and 18 V, a range suitable for most applications. The current drain for the alarm is only 30 mA and can be safely drawn from most clock power supplies. ◇
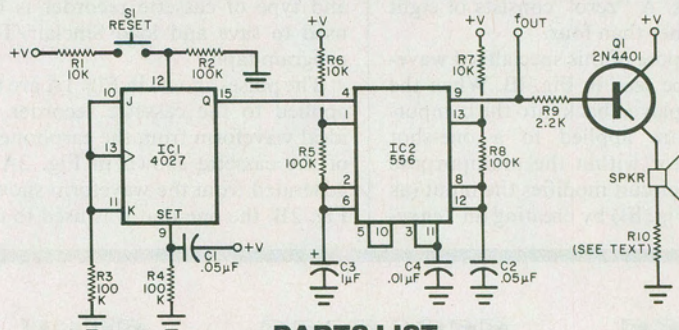
PARTS LIST

C1, C2, C4—0.05-μF capacitor
C3—1-μF, 35-V electrolytic
IC1—4027 CMOS dual JK flip-flop
IC2—556 dual timer
Q1—2N4401 transistor
R1, R6, R7—10-kilohm, ¼-W resistor
R2 through R5, R8—100-kilohm, ¼-W resistor
R9—2.2-kilohm, ¼-W resistor
R10—See text
S1—Normally open pushbutton switch
SPKR—8-ohm speaker
Misc.—Mounting hardware, perf board, IC sockets, etc.