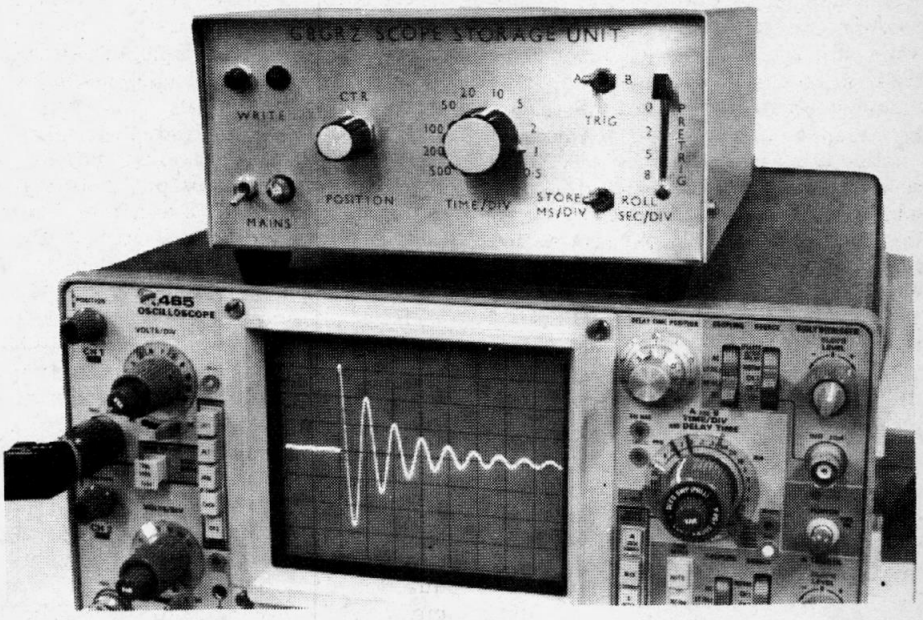
# Add-on oscilloscope waveform store — 1

## Digital unit for audio waveform storage and display using a dual-channel oscilloscope

**by R. D. Fastner**

The instrument described here employs digital storage techniques to allow an ordinary dual-channel oscilloscope to function as a storage type. The input signal to the oscilloscope is extracted, converted to digital form, stored, converted back to the analogue form and displayed on the oscilloscope screen. A useful feature is that the waveform before the trigger pulse can be displayed. Circuitry is included to remove the "steps" in the waveform which would ordinarily be the result of a sampling process. Interfacing with the oscilloscope is not dealt with in detail, since requirements vary with facilities existing already.



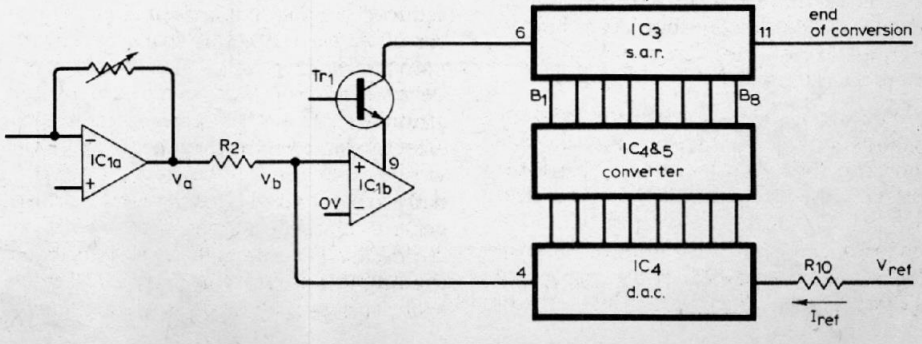

*The storage unit in use, displaying a test waveform.*

THIS IS a mains-powered instrument designed to give a storage facility to a non-storage oscilloscope. The instrument consists of an analogue-to-digital converter, 8000 bits (1000 × 8) of memory, a digital-to-analogue converter and a step eliminator, which converts the normal step output of the d.a.c. to straight lines. This greatly improves the presentation of stored waveforms with few samples. There is also some control circuitry to control the read/write, sync. and blank functions. A crystal oscillator is used for simplicity and stability, and its frequency is divided down in a 1, 2, 5 sequence to give 10 time/division ranges. There is also a roll mode of operation which gives an extra nine time/division ranges below that of the normal storage mode. A useful pretrigger function enables the unit to store the waveform leading up to and away from the trigger point – a mode which is not possible with normal c.r.t. storage. An advantage of this system of storage is that the waveform may be expanded and analysed after being stored.

Since the unit may be used to store digital waveforms with fast transitions a tracking a-d converter was rejected because of its slow full-scale slew rate. The successive-approximation type used will reach any level in a maximum time of 2% of a division, assuming the input changes state during the first of the two samples. On the other hand, the slew time of the tracking type of converter depends on the input levels, and has a maximum time of $2^n$ clock pulses. Reduction of this time can be accomplished by increasing the clock frequency when the difference between input and digital output is greater than a specified amount. The frequency can then be reduced when the difference between the levels has been reduced. There is the disadvantage, in this mode of operation, that more complex circuitry is needed to detect the levels at which the higher speed clock is gated in and out.

Random-access memory i.cs were rejected as storage elements in favour of shift registers, because the register's sequential operation suited the circuit operation. One disadvantage of r.a.ms is the need for address lines, which results in more components and greater complication in p.c.b. layout. Another is the increased complexity of the circuitry, especially regarding roll and pretrigger functions.

*Fig. 1. Block diagram of the input circuit and d-a converter.*




### Analogue-to-digital converter

Analogue input waveforms are converted to 8-bit binary form to provide 256 discrete levels on conversion back to analogue form for display. The converter, shown in Fig. 2, is in action continuously, whether the instrument is reading or writing. It uses three integrated circuits to perform its major functions: a MC14559 c.m.o.s. successive-approximation register (not the locmos version, which has a higher propagation delay); a MC1408-L8 bipolar, 8-bit digital-to-analogue converter; and MC1407 bipolar a-d control circuit, which is a wideband amplifier and comparator. Transistor $Tr_1$ shifts vol-

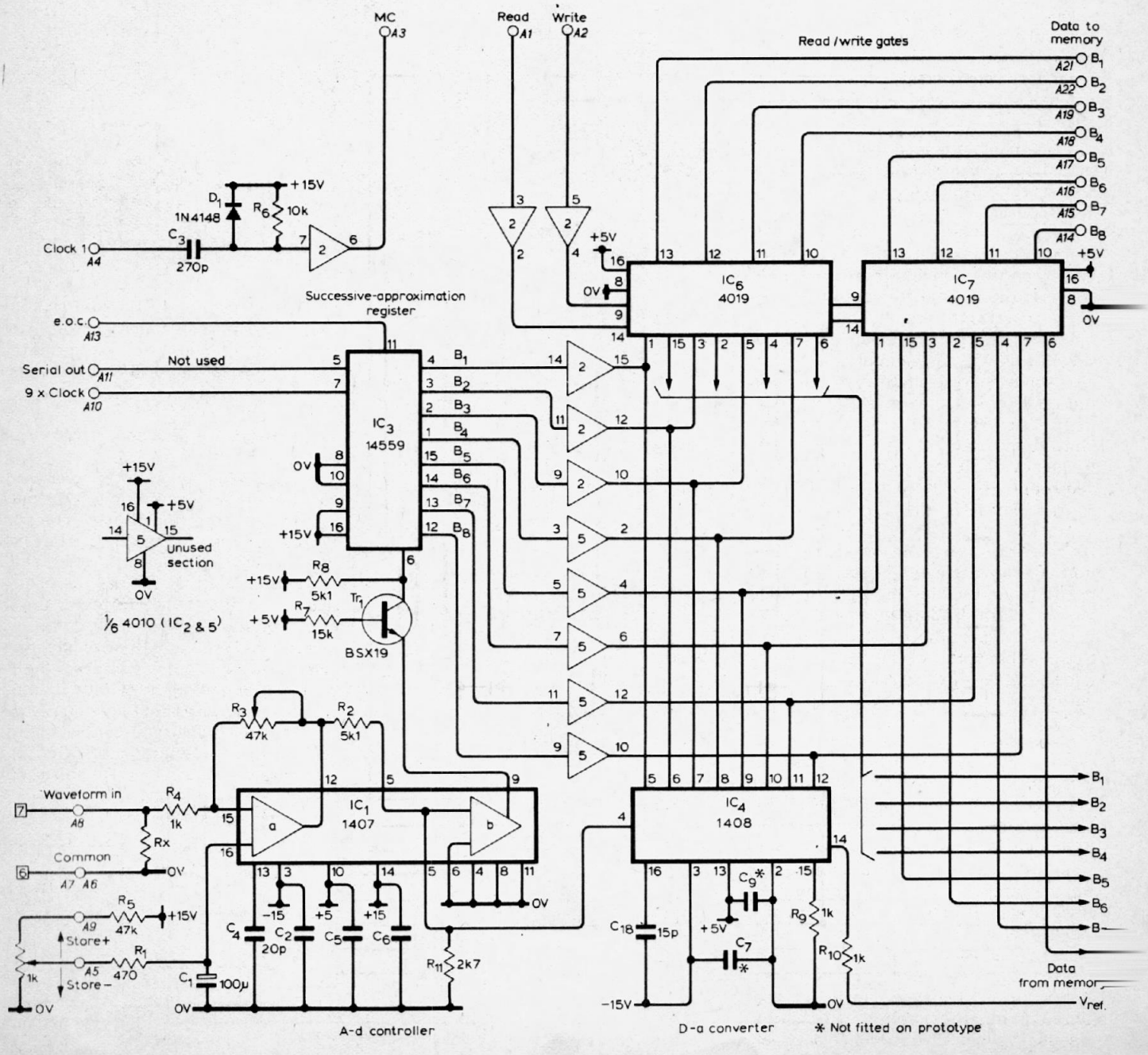
tage levels from the bipolar 5V of the MC1407 ($IC_1$) to c.m.o.s. 15V for $IC_3$ and, similarly, the eight buffers in $IC_{2,5}$ shift levels back to 5V for the bipolar MC1408-L8 – $IC_4$.

**Operation.** In essence, the converter is an analogue-digital-analogue feedback loop. The block diagram of Fig. 1 shows the input amplifier, $IC_{1a}$, whose output is taken to a voltage comparator, $IC_{1b}$. Via the level shifter, $Tr_1$, the comparator controls the successive-approximation register, $IC_3$, which is clocked. The digital outputs of the s.a.r. are buffered and applied to the digital-to-analogue converter, $IC_4$, whose output is then taken back to the comparator. The loop circulates until the two comparator inputs are zero.

Assume that, in Fig. 2, the s.a.r. is reset, with B1 to B8 low: $IC_4$, the d-a converter in the a-d loop, is drawing no current via its output pin 4. Also assume some positive output, $V_a$, from $IC_1$, pin 12. The comparator sees a positive voltage, $V_b$, on its non-inverting input, $IC_1$, pin 5; its output, pin 9, is high. Transistor $Tr_1$, the 5V-15V level shifter, is off and its collector is high. This high voltage is fed into the s.a.r. D input, $IC_3$, pin 6 which, on receipt of the first clock input, enables B1, the most significant bit, which appears on $IC_3$, pin 4, to be set. When the m.s.b. goes high, it is converted down to the 5V level and is fed into $IC_4$, pin 5. $IC_4$ now draws $I_{ref}/2$, and $V_b$, the voltage at the comparator input is now $V_a - I_{ref}/2 \times R_2$. If this voltage is positive, the comparator output will be high; if negative, the output will be low.

If it is high, the next clock pulse sets $IC_3$, pin 3, which is bit 2, high. This causes $IC_4$ to draw $I_{ref}/2 + I_{ref}/4$, hence the current corresponding to each bit is half that for the previous one. Now, $V = V_a - (I_{ref}/2 + I_{ref}/4 \times R_2)$ and is aga compared as before. This time, if $V_b$ i negative, the comparator output is low and the next clock pulse simultaneously resets B2 and sets B3. The output of $IC_3$ draws $I_{ref}/2 + I_{ref}/8 \times R_2$ and again the $IR$ product is subtracted from $V_a$ and the result compared. This sequence is continued for all eight bits, each being generated, added to the previous bit, compared and reset or remaining set to keep $V_b = 0$. At the end of the sequence, $IC_3$, pin 11, which is "end of conversion" (e.o.c.), goes high and is used to

*Fig. 2. Circuit of the a-d converter. The gates in $IC_{6,7}$ are controlled by the read/write circuitry and connect the digitised input to the memory or the output of the memory to its input for re-circulation.*



generate a pulse, which sets a flip-flop and strobes the data into memory by means of a write pulse and $IC_{6,7}$. The complete sequence is nine clock cycles long, the e.o.c. being half a cycle wide.

## Memory

Sixteen NE2528, dual 250-bit, c.m.o.s. shift registers are used for the memory, operated from +5V and −8V (no 0V). The data is clocked through by a modified end of conversion (e.o.c.) pulse generated by the a-d converter.

Since the memory is, in effect, eight large shift registers, as seen in Fig. 3, all that is required for operation is a clock and some read/write gating. Two 4019 and-or gates, seen in Fig. 2, are used for this gating, controlled by the read and write inputs. The latter enables the gates from the a.d.c. to the memory input, whilst the latter inhibits the gates from the memory output to input. When the unit is in a 'write' condition, the first bistable in the memory acts as a latch, eliminating the need for separate latches.

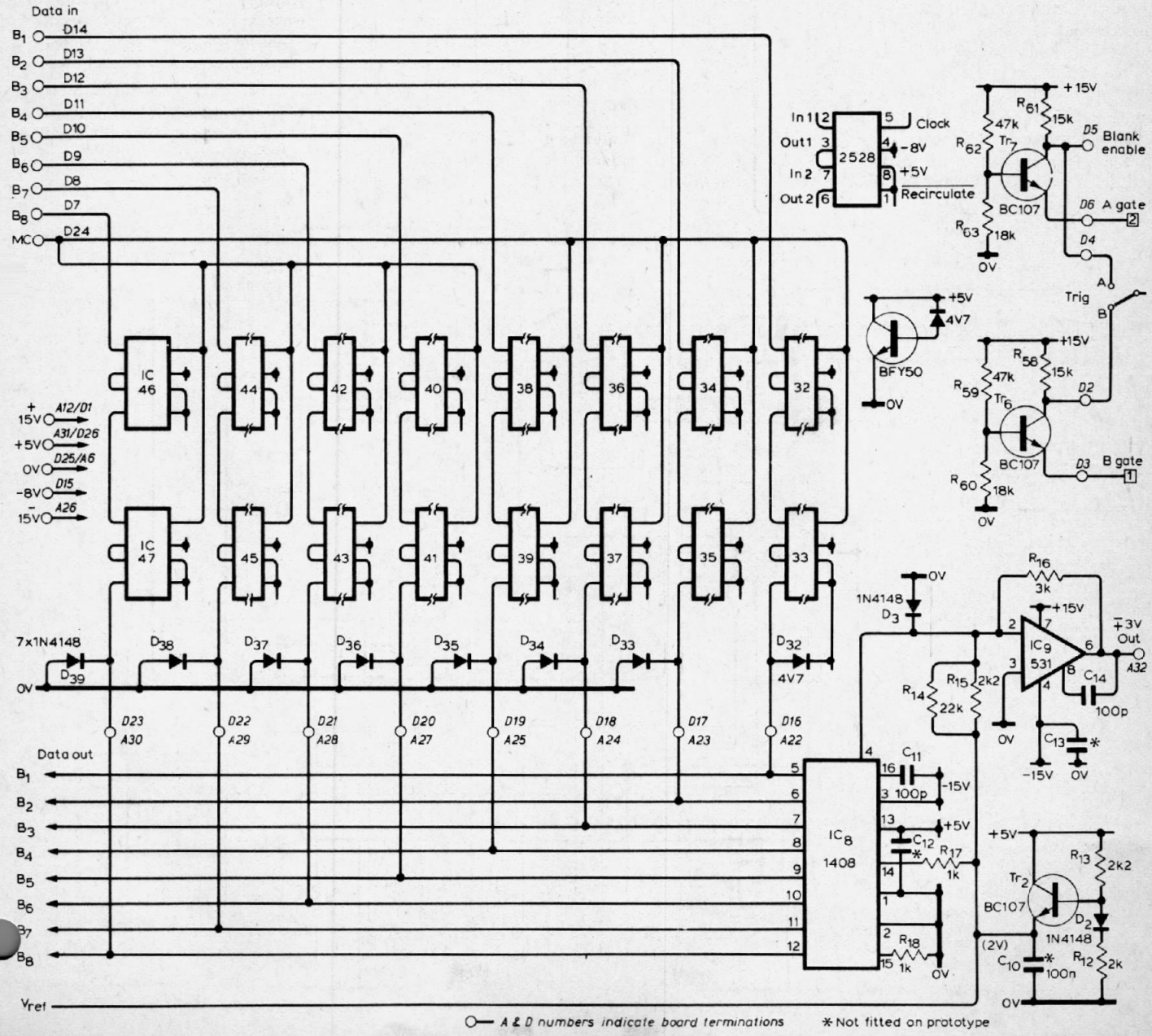
The NE2528 shift registers require a high clock pulse width of not less than 200ns and a low pulse width of not greater than 100μs; if the clock pulse is low for longer than 100μs data is lost, but it may stay high indefinitely. For this reason, $R_6$ and $C_3$ in Fig. 2 are required to form a pulse generating circuit, whose function is to limit with width of the clock pulse to approximately 3μs when on low clock rates. Omission of these components results in the stored waveform deteriorating as the memory i.cs warm up.

*Fig. 3. Circuit of the memory and d-a converter. $IC_9$ provides the output for the step eliminator of Fig. 5.*

Outputs $B_{2\text{-}8}$ are clamped by 1N4148 diodes to prevent them forcibly switching on the d.a.c. inputs. Output $B_1$ is clamped by a 7.4V zener diode from +5V because it was found that if this input went 0.7V negative, the output appeared to have "crossover distortion." Several d.a.c. chips were tested and all showed this distortion. No mention of this phenomenon was found in the specifications of the d.a.c. chip.

## D-a converter

A second MC1408-L8 i.c., $IC_8$, is used for the d-a conversion as shown in Fig. 3. Since the device has a constant current-output it is followed by a current-to-voltage converter, $IC_9$. The inputs to the d.a.c. are taken from the outputs of the memory. A positive current corresponding to $B_1$ is fed into the output of the d.a.c. via $R_{14}$ and $R_{15}$, causing the output of $IC_9$ to become



bipolar. If $B_1$ were presented to $IC_{8/9}$, pin 4 would draw $I_{ref}/2 = V_{ref}/R_{17} \times ½ = 2V/1k \times ½ = 1mA$. $R_{14}$ and $R_{15}$ in parallel equal approximately 2kΩ. $R_{14}$, the "select-on-test" resistor, is chosen so that with $B_1$ only the final output from the unit is 0V; i.e., it is an offset adjustment. $R_{14}$ and $R_{15}$ are connected to $V_{ref}$ and, assuming their combined value is 2kΩ, supply the 1mA to $IC_8$, pin 4. As $IC_9$ input is a virtual earth, $IR_{16} = 0$ and therefore the output will be 0V. The voltage output from the circuit ranges from:

$-IR_{14}R_{15}R_{16} = -V_{ref}R_{16}/R_{14}R_{15} = -3V$

to

$-I_{d.a.c.(max)} + IR_{14}R_{15}R_{16} = 2.97$

or about ±3V.

The characteristics of the d.a.c. are such that the m.s.b. current switch is the fastest to operate and the least signficant bit is the slowest, with the intermediate bit-switching times increasing with decreasing significance. the transition $B_1$ off – $B_{2\text{-}8}$ on, to $B_{2\text{-}8}$ off – $B_1$ on, results in some period of time when $B_1$ has switched on but $B_{2\text{-}8}$ (or any combination) have not switched off. During this short period of time all eight bits appear to be on and the output of the d.a.c. tries to draw maximum current, resulting in a negative-going spike. Diode $D_3$, a 1N4148 or similar, is included in the circuit to "fill in" this spike. If this diode is omitted $IC_9$ output would try to follow the spike and a positive glitch would appear at the output.

The reference voltage generator is basically a potential divider buffered by an emitter follower $Tr_2$. The 1N4148 diode is included for thermal stabilisation.

## Clock

A 1.8 MHz crystal oscillator, seen in Fig. 4, is used to generate the maximum clock frequency required, which is nine times the maximum sample rate. This is divided down under control of the time/division switch, $S_{5a}$, to give a nine times clock output for each of the normal store mode ranges. As the output is fed only to the s.a.r. the whole circuit is operated from a +15V supply. MC14510 decade counters are used for the first two stages, $IC_{20\text{-}21}$, and a CD 4029 binary/decade counter, $IC_{22}$, for the third.

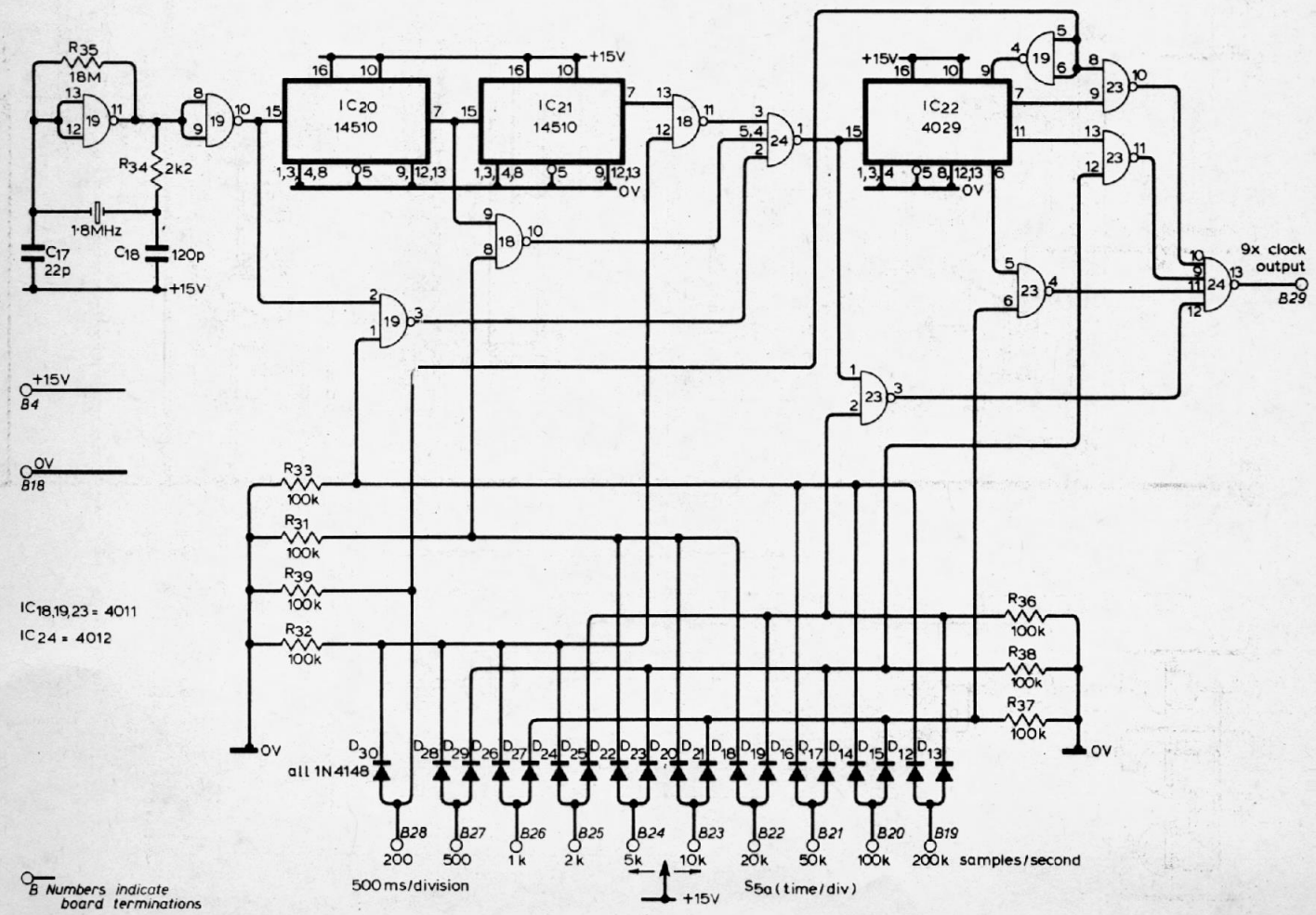
The output from the crystal oscillator is divided down by gating it into, or around, counters as required. Gates are operated in pairs and are enabled from the time/div. switch by diode logic. Ranges above 0.5s/div. use decade counters in the first two stages and a binary counter in the last. Binary outputs 1 and 2 are used to give divisions of 2 and 4 respectively. The 0.5s/div. range is derived in a similar manner, except that the third counter is operated in the decade mode and the output is taken from the terminal count. If starting of the oscillator is unreliable the 18 megohm resistor in the circuit may be reduced to 10 megohms. This resistor sets the bias level at the input of the nand gate.

*Fig. 4. Crystal oscillator and dividers, with gating for selection of final clock frequency.*

## Step eliminator

The function of this circuit, shown in Fig.5, is to convert the normal step output of the d-a converter to something more presentable. It consists of a differential amplifier, followed by a sample-and-hold circuit and an integrator. The output is taken from the integrator, $IC_{29}$, via an inverting buffer, $IC_{28}$. The integrator time constants are selected by the time/div. switch.

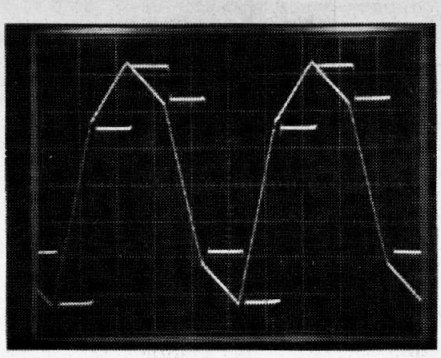
Assuming the input and output of the circuit are at 0V, the differential amplifier $IC_{25}$ will also be at 0V and, when the 4016 analogue gate $IC_{26}$ is strobed, the storage capacitor $C_{28}$ will also be at 0V. When the strobe pulse is removed, the 4016 gate is disabled and has an impedance of several megohms. The voltage stored by $C_{28}$ is buffered by $IC_{27}$, a LM301 voltage follower, and fed to the input of the integrator, which will remain at 0V by virtue of the virtual earth configuration.



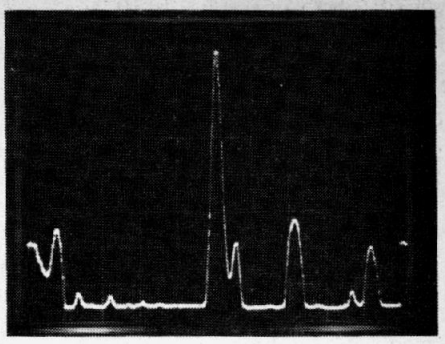
If an input step of 2V is now received, the output from $IC_{25}$ will go to −2V, since it has unity gain. After approximately 2.5μs, which is the time allowed for settling, $IC_{26}$ is strobed by a 0.5μs pulse, the storage capacitor being charged to −2V, and is fed via $IC_{27}$ to the integrator, which is made to perform a positive-going ramp at a rate determined by the −2V and the timing components $R_{50\text{-}52}$ and $C_{31\text{-}40}$. Since the storage capacitor imposes a heavy load whilst charging, a reservoir capacitor, $C_{24}$, is connected from the output of $IC_{25}$ to 0V to supply the current during the strobe time.

The integrator output voltage is shown simply in Fig. 6. Input current $I_{in}$ = fed-back current $-I_F = V_{in}/R$. $V_c = Q_c/C$ and $Q_c = I_F t$, therefore $V_c = -I_F t/C$. But $I_F = V_{in}/R$, so $V_c = -V_c = -V_{in} t/CR$. $CR$ is chosen to equal the same period $t$, so that $V_0 = -V_{in}$ by the end of the sample period, and therefore the integrator output = +2V.

If the second sample is also +2V, the output of $IC_{25}$ will be (+2) − (+2) = 0V, i.e. there will be no difference between the two inputs. After the next strobe, 0V will be presented to the integrator input and, since $I_{in} = 0$, $I_F$ must also be zero, and the output will remain at +2V. A third sample of −1V will make $IC_{25}$ output (=2) − (−1) = +3V. This, when fed to the integrator, will cause it to fall linearly by 3V from +2V, resulting in a



*The action of the step eliminator, using a waveform with a fewer number of steps than normally seen to illustrate the effect. The result of inaccuracy in the choice of integrator capacitors can be seen. Frequency in was 40kHz at 200 kHz sampling rate. Oscilloscope sweep 20μs/div., storage unit speed 2ms/div.*



*Pre-trigger of 5 divisions (graticule very faint). Large pulse is trigger.*

*Typical trace at 100 samples per cycle of the input.*

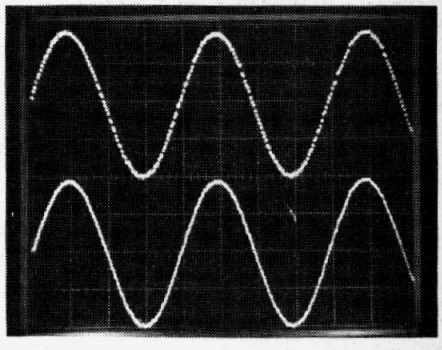
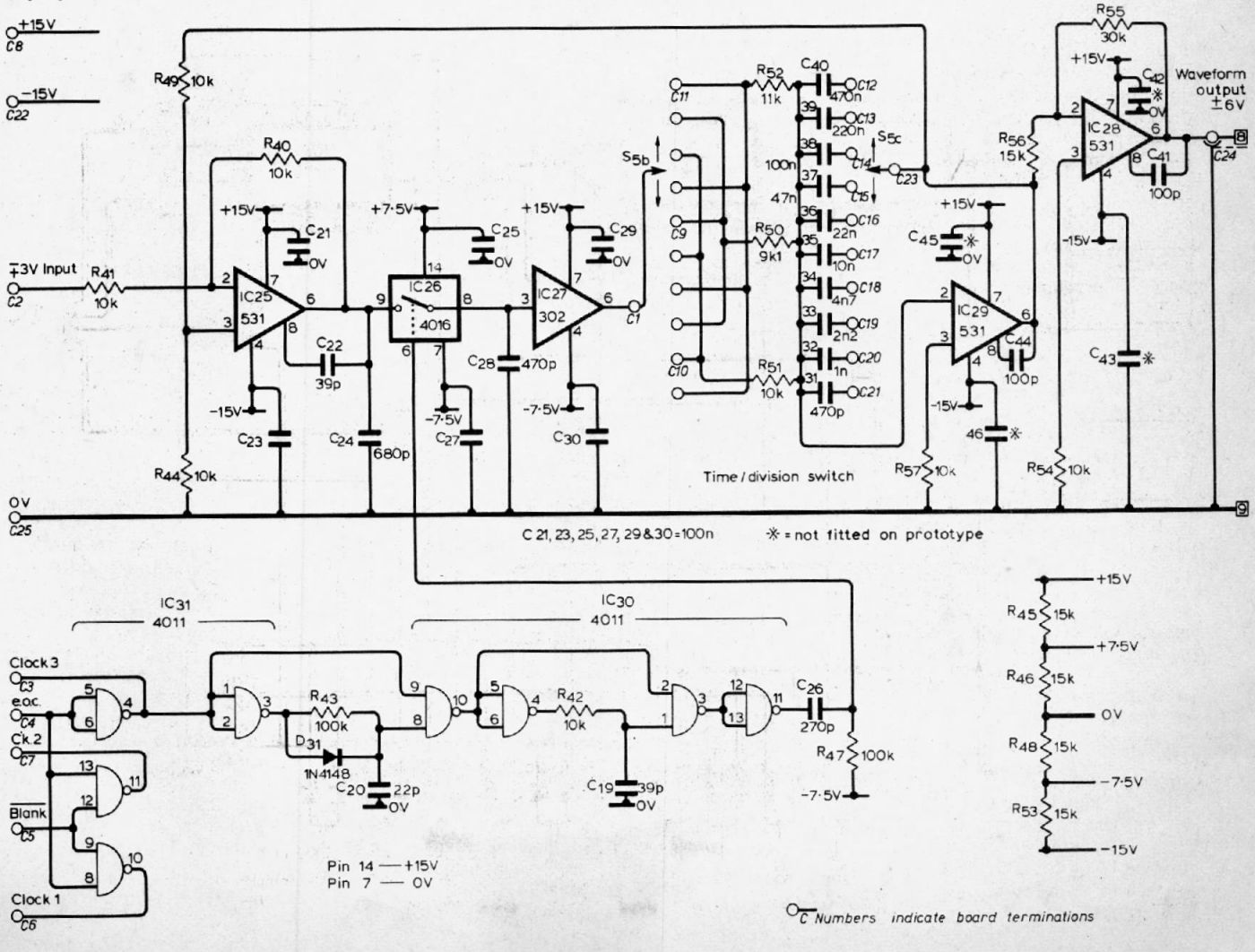


*Fig. 5. Step eliminator and output amplifier. The faster ranges of the integrator should have close-tolerance capacitors to achieve the correct slopes.*



voltage of −1V by the next strobe pulse. Photograph 1 shows the resulting effect, the slight errors in levels being due to the timing components not being selected for the correct time constants.

The input to the analogue gate is limited to slightly less than the supply voltage to the device. For the bipolar inputs required by the integrator, $IC_{26}$ is operated from a ±7.5V supply. Thus, for safety, the input is limited to ±6V. This, in turn, limits the d.a.c. and integrator outputs to ±3V since, if both were at opposite extremes, the resulting output from $IC_{25}$ would be ±6V.

**Strobe pulse generation.** The circuit, $IC_{30\text{-}31}$, consists of a positive transition detector, following an inverter, which gives a positive transition approximately 2.5μs after the negative-going edge of the e.o.c. pulse. This delay

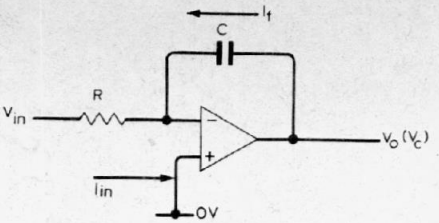



*Fig. 6. Derivation of the integrator output voltage.*

is required to allow for the data to emerge from the memory, the d.a.c. to settle and to allow the output of $IC_{25}$ to charge $C_{24}$ after the step input. The first positive transition detector is followed by a second one which gives a low going 0.5μs pulse after the positive going edge of the previous stage. Level shifting of the 0 to +15V pulse to −7.5V to +7.5V to be compatible with the gate $IC_{26}$ is by capacitive coupling in $C_{26}$ with a pull down to −7.5V by means of $R_{47}$. For use with oscilloscopes with 8 divisions horizontally the 1.8MHz crystal, which gives 1,000 samples in 10 divisions at 0.5ms/div., may be replaced with one of 2.25MHz or 1.125MHz. The former gives 1,000 samples in 8 div. at 0.5ms/div. and the latter 1,000 samples in 8 div. at 1ms/div. The higher of the two may be too high for the a-d converter to operate reliably, and the lower reduces the unit time/div. ranges to 9. The time constants of the step eliminator will need to be reduced from 5 to 4μs, 10 to 8μs and 20 to 16μs and their decades (330 + 69, 680 + 120pF, 1500 + 100pF used with 10kΩ).

**Printed circuit boards**

A set of four double sided p.c.bs is available, at £14.00, including postage and packing, from M. R. Sagin at 23 Keyes Road, London N.W.2.

# Add-on oscilloscope waveform store

## 2 — Control circuitry, setting-up and operation

by R. D. Fastner (G8GRZ)

Digital storage techniques allow an ordinary dual-channel oscilloscope to function as a storage type. The input signal to the oscilloscope is extracted, converted to digital form, stored, converted back to the analogue form and displayed on the oscilloscope screen. A useful feature is that the waveform before the trigger pulse can be displayed. Circuitry is included to remove the "steps" in the waveform which would ordinarily be the result of a sampling process.

**Control circuitry** These circuits seen in Fig. 7 are operated from a 15V supply and consist of the sync counter, blank-length counter, store read/write bistable, roll read/write bistable and store-full bistable. "A" and "B" gate-level shifters, sync + and blank buffers are also part of these circuits but are not described in detail.

**Sync. counter.** This consists of three MC14510 decade counters, the input being derived from the e.o.c. pulse via $IC_{31}$ in Fig. 5. The last stage (100's) is preset to the number of divisions required for pretriggering, i.e., 2(200) for two divisions pretrig. The terminal count from pin 7 of $IC_{12}$ is used to flip over bistable flip-flops when the memory is "full". It is also used, after being delayed for one count, as a sync pulse.

**Blank-length counter.** One half of a 4013 dual "D" type flip flop, $IC_{13}$ and a 4024 seven stage binary counter, $IC_{14}$, are used in this part of the circuit. Its function is to count the number of "divisions" after the tenth division displayed in order to reset the blank bistable. The count length is determined by the number of divisions the scope continues to sweep after the tenth division before flyback. The counter length is set by diodes and may range from 2% to 2.55 divisions. A length of 1.5 divisions is selected in the circuit diagram.

**Store read/write bistable.** When in the store mode, the outputs from this bistable, half a 4013, $IC_{16}$, opens or shuts the gates at the input of the memory. These outputs, when selected by $IC_{15}$, are labelled Read and Write for the Q and $\overline{Q}$ outputs respectively. When Read is high and Write is low, the gates, $IC_{6\text{-}7}$ in Fig. 2, are enabled to allow the data from the memory output to flow to the memory input, hence allowing it to recirculate. Simultaneously, Write is low and this closes the gates from the a-d convertor to the memory input. When the Write button is depressed, the outputs reverse allowing the memory to be "written". This condition is once again reversed when the sync counter terminal count goes high.

**Roll read/write bistable.** The function of this circuit, $IC_{16}$, in the roll mode, is similar to that described previously, except that it is controlled by the sync counter. The effect is to change the read/write lines once per sweep for one sample, i.e., the waveform is sampled once in a thousand. This bistable is also used to delay the sync pulse by one "sample" to allow for the analogue delay in the step eliminator. When in the roll mode the Q output inhibits the counter for one count, causing it to count 1001.

**Store-full bistable.** This is made up from two sections of a 4011, $IC_{17}$, to form a bistable. When in the store mode, its function is to inhibit the sync counter between the time that the write button is depressed and the scope's sweep being detected (A or B gate going high). It is also used to preset the sync counter at the beginning of the write cycle.

### Interfacing

This unit has been designed and built around the Tektronix 465 oscilloscope. For it to operate with other instruments the inputs and outputs of the unit may need to be interfaced with those of the oscilloscope.

Feeding the output waveform into the second channel of the oscilloscope should present no problems, as the output voltage has been selected so that the waveform may be expanded and compressed and at 2V/div most instruments should be able to do this. However, if desired, the gain of $IC_{28}$, the output buffer, may be altered as required by altering the feedback resistor.

The sync + output also should present no problems. If the 0 to +15V edge is too high for the oscilloscope to trigger on reliably, a simple potentiometer divider may be placed across the output and the sync signal taken from the junction of the two resistors. The pull up on $Tr_4$ emitter should not be increased, as the increased capacitive effect between base and emitter will reflect back into the high impedance c.m.o.s. logic. This may cause trouble when in the roll mode.

The blank signal, fed into the Z mod. or axis input of the oscilloscope, has an output of 0 to +15V, the output being at +15V during the blank period. If inversion is required to give 0V during the

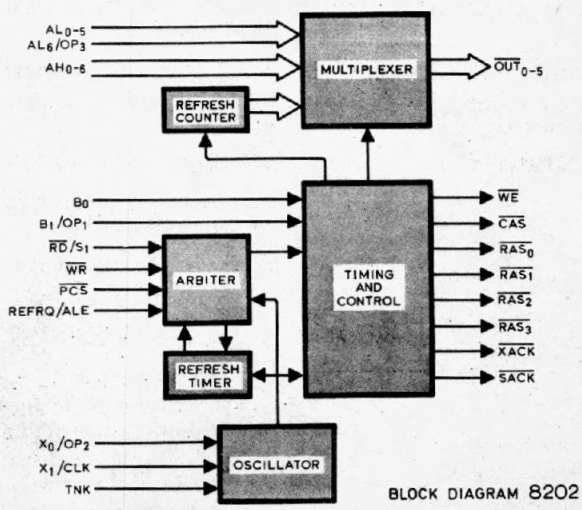



*Fig. 7. Control circuit*

blank period, $Tr_3$ base could be taken to the Q output of the blank bistable. Again, if the levels present a problem, a simple potentiometer divider could be used, as for sync +.

Due to the very large number of oscilloscope models, it is impractical to go into detail when describing the pick-off points for "A" trig, "B" trig and waveform in. All instruments of worth have trigger and blanking circuits, the former being derived from the input amplifier, via a buffer, and the latter from the sweep controlling logic.

Minimum interference is caused to the operation of the oscilloscope by taking the "waveform in" signal via an interface buffer from the "trigger buffer". This buffer can be some form of operational amplifier in the non-inverting mode (high impedance) or a simple emitter follower. The sweep waveform is usually obtained from an integrator, whose input is a step derived from the trigger circuit. Also from this circuit an unblanked signal is derived which enables the "trace" during sweep. Either of these two signals may be buffered and used for the A and B trig. Care should be taken to ensure that they are clean, and the signal does not have "chopped blanking" waveforms superimposed on it, or that the A sweep signal does not have B sweep signals (or vice versa) mixed with it. For correct blanking circuit operation within the storage unit, the "A" trig should stay high for at least 10 divisions (10 × storage unit store time/div setting) and is independent of "B" timebase which may be a positive pulse.

Some scopes have A and B gate outputs using higher output levels. In these cases $R_{67}$, $R_{68}$ are changed so that $Tr_{67}$ base voltages are a little less than the "high" input voltage.

**Practical considerations**

Care should be taken when mixing analogue and digital circuits and it is recommended that the impedances around the input amplifier should be kept low to reduce adjacent track crosstalk. It was found that the wire from the position pot to the non-inverting input of the input amplifier had several microvolts of hum induced in it by the mains transformer. To stop this being superimposed on the output of this amplifier, a capacitor C, has been added from the non-inverting input to 0V. The storage capacitor, $C_{28}$, in the sample-and-hold section of the step eliminator is floating when the analogue switch is off, and therefore board leakage should be reduced as far as possible to prevent discharge (or charge) of this capacitor. Also the tracking to and from this capacitor should be kept as short as possible to reduce hum pick up. It has been found that slight amounts of "tilt" and hum on the integrator input have negligible effect on its output even on low displayed time/div settings.

**Setting up**

Only two adjustments need to be made, the first being to null the offset voltages of the d-a and output stages. This is achieved by selecting $R_{14}$ so that with B1 only present the "waveform out" is 0V. The second adjustment is to set the gain of the input amplifier so that when a voltage proportional to ±3 divisions is fed into the unit, an output of ±6V or ±3 divisions is obtained.

To null the offset voltages first disconnect the +15V supply to the store/roll switch. This disables the read/write lines which in turn disables the read/write gates. Bits 1-8 at the memory input will now be low. Disconnect B1 to the memory input and connect it to +5V, The d-a convertor will now only see B1, and $R_{14}$ may now be selected so that the output of the unit is as near as possible to 0V. The offset voltages of the d.a.c., step eliminator, and output buffer have now been nulled. Reconnect up the supply to the switch and B1 to the memory output.

Setting up the gain is accomplished in the following way. Connect up the inputs and outputs between t oscilloscope and unit. If a single t base instrument is used connect the "B trig input to 0V. Set both oscilloscope and unit to 1ms/div, the oscilloscope to "A" timebase only, and Auto trig on Ch1. Set the unit to Store mode and "B" trig, and press the Write button. The write indicator should come on and stay on. Feed into the Ch1 input of the oscilloscope a sine wave of approximately 500Hz and ±3div in amplitude (symmetrically about 0V). Ch2 should be displaying the processed waveform and the gain control $RV_2$, in conjunction with theposition control $RV_1$ may be adjusted to give a unit output of ±6V (about 0V). If the input is increased above ±3 div the output should saturate at ±6V. In the above, it is assumed that the channel whose output is used as the input to the unit is Ch1.

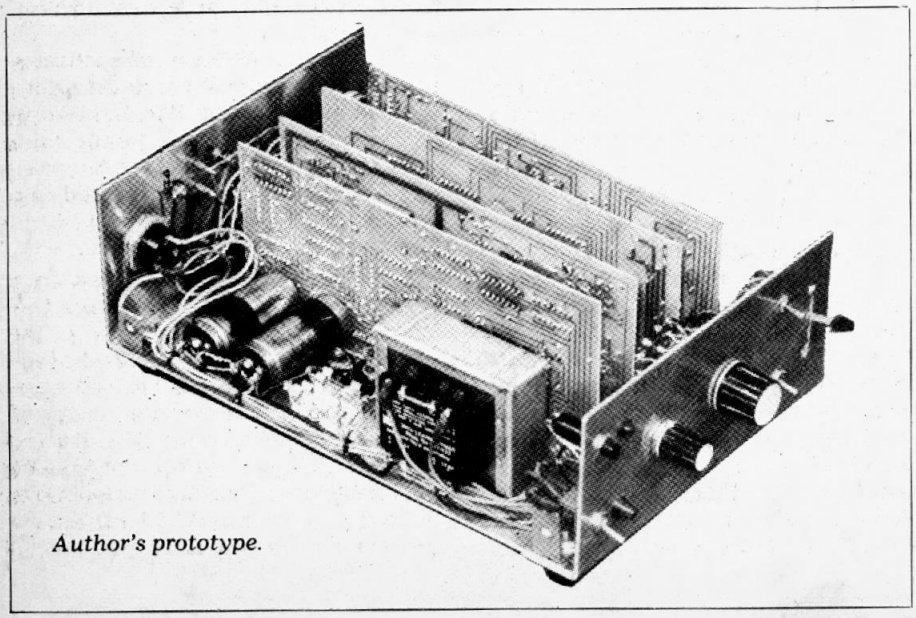
The maximum position voltage required is a little more than the maximum input voltage. If the input voltage is 50mV/div for 6 div, this gives an input voltage $V_A$ of 300mV, and the position voltage $V_B$ will also be around 300mV. A value for $R_5$ of 47kΩ satisfies this requirement.

**Operation**

**Store mode.** The oscilloscope is operated normally in either the single-sweep or normal trigger mode. So that the displayed waveform is stored as originally displayed, the time/div switches of the oscilloscope and unit should be set to the same positions. When storage is complete the oscilloscope should be triggered from the unit sync output.

The Write button is depressed before the oscilloscope triggers; this resets the store read/write bistable and causes the Write indicator to light and the data from the a-d converter to be gated into the memory. The Store Full bistable will be reset by $IC_{16}$, pin 12 and its $\overline{Q}$ output on pin 3 is gated with $IC_{16}$, pin 12 in $IC_{17}$, pin 4. The output of the gate is inverted by $IC_{18}$ and the resulting high output is fed to the chip enable input of $IC_{10}$, inhibiting it. The circuit remains in this state, i.e. Write high, sync counter disabled and the unit waiting for the oscilloscope to be triggered.

When the oscilloscope triggers, the A gate will go high, indicating that the sweep has commenced. This high is level-shifted to +15V and $IC_{17}$, pin 10 goes low, setting $BS_2$, $BS_2$ Q output is fed into a pulse-forming circuit which produces a positive-going pulse of approximately 3μs duration. This pulse presets the sync counter to 200 if 2 divisions of pretrigger has been selected. The $\overline{Q}$ output of $BS_2$, causes $IC_{17}$ pin 11, to go high. This, via $IC_{18}$, pin 3, enables the sync counter, which proceeds to count up a further 800 samples to 1000. At the count of 1000 $IC_{12}$ terminal count goes high clocking $BS_1$ and setting it. "Read" will now be high and the gating is enabled to allow the data in



*Author's prototype.*

memory to recirculate the a-d converter was operating prior to the oscilloscope triggering, the data in the memory will consist of 200 samples, which have not been displaced by new data, and the 800 samples fed into the memory after the oscilloscope triggered. Hence, 2 divisions pretrigger and 8 posttrigger. The counter is preset in a similar manner for each of the other pretrigger positions.

Also, at the instant the terminal count goes high, $BS_3$, the roll read/write bistable, is reset. The $\overline{Q}$ output clocks $BS_4$, the blank bistable, so setting it. This has two effects: the first is to cause Blank to go high, blanking the oscilloscope's trace. The second is to inhibit Clock 1 to the memory, Clock 2 to the sync counter and Enable to the blank-length counter. These two actions result in the unit locking up, with the oscilloscope in a blanked condition, for the duration taken for the blank-length counter to time out. When the desired count (selected by diodes) is reached $BS_4$ is reset, re-enabling the sync counter and memory. During the blank period the memory presents the first sample to be displayed at its output. This is done so that the step eliminator can ramp the "false sample" between the end and the beginning of the stored waveform, (i.e. sample 1000 and sample 1) whilst the trace is blanked. The first clock pulse after the blank phase clocks $BS_3$, setting it. Sync goes high which, if the oscilloscope were set to ext. trig. would trigger the oscilloscope at the start of the stored waveform. Thus the complete store cycle is: Write button depressed-unit locks up waiting for the oscilloscope to trigger; oscilloscope triggered; counter preset; counter counts up the number of "divisions" required; terminal count reached; unit "switched" into Read; oscilloscope blanked and unit "locked up" with the first sample at the output of the memory; oscilloscope ends sweep and flyback; blank circuit times out allowing the stored waveform to be displayed. The oscilloscope trigger source is set to external so that it triggers from the unit. Triggering the unit from the "B" timebase allows delayed storage to take place.

The unit can be used to store a peak level, whilst observing the incoming waveform, by setting the oscilloscope to "A Intens by B" and setting the "B" trigger level to the peak level to be detected/stored. For example, if the normal input waveform level to the scope is ±15 divisions, the "B" timebase may be set to trigger at +1.6 div. Thus, if the input goes above +1.6 div the unit will store the waveform around this point (store peak detected).

**Role mode.** This extends the oscilloscope's lowest range from 0.5 s/div to 500 sec/div. The waveform appears to move from right to left, in similar manner to a paper strip recorder, with the latest level appearing on the right. When 0.5 sec/div is selected, the waveform is displayed at 0.5ms/div whilst "moving" from right to left. This provides a display that is easy to view since the whole waveform can be seen instead of a moving dot. Switching the unit to 'store' holds the waveform. The Roll mode is achieved by inhibiting the sync counter for one count, causing it to count to 1001, which means that the oscilloscope triggers on successive samples. Hence, the waveform then appears to roll round. Whilst the counter is inhibited, the read/write lines change over so that the sample before the oscilloscope triggers is "up-dated" and appears at the end of the sweep.

At the count of 999, $IC_{12}$, pin 7 (terminal count) is low and the unit is in the Read mode. $BS_3$ $\overline{Q}$ is low, the sync counter is enabled and Sync+is high. On the next clock pulse (1000)$IC_{12}$, pin 7 goes high and the previous low terminal count is clocked through $BS_3$. This inhibits the sync counter via $BS_3$ $\overline{Q}$ and causes the unit to go into the Write mode. The next clock pulse (1001) again clocks the previous high terminal count state through $BS_3$. Sync + goes high, triggering the oscilloscope, and the sync counter is again enabled. The unit goes into Read mode for the next 999 clock pulses. In this roll mode the unit does not lock up during the blank phase, and the oscilloscope triggers on alternate sync pulses, i.e. the sync pulse follows immediately after the end of 10 divisions.

It is regretted that it is impracticable to publish the printed board design for the storage unit, but *Wireless World* can supply photocopies (made on a rather better machine than in the past) to readers who send a stamped, addressed envelope to their offices.


## Acknowledgements

The author would like to acknowledge his indebtedness to Gould Advance Ltd, whose OS4 oscilloscope gave rise to the ideas of roll, pre-trigger and step-elimination, although it should perhaps be pointed out that the design of the present instrument was started three years ago – before the OS4000 was made public. Thanks are also due to Tektronix, who lent a C-5A camera for the screen photographs. □


**Circuit elements**

| Qty | I.cs |
|---|---|
| 2 | CD 4010 hex. non-inverting buffer/convertor |
| 6 | CD4011 quad 2-input Nand gates |
| 1 | CD4012 dual 4-input Nand gate |
| 2 | CD 4013 dual "D" type flip-flop |
| 1 | CD 4016 quad analogue gate/switch |
| 3 | CD 4019 quad And-Or-Select gates |
| 1 | CD 4024 7-stage binary counter |
| 1 | CD 4029 presettable binary/decade up/down counter |
| 5 | MC 14510 presettable decade up/down counter |
| 1 | MC 14559 successive-approximation register |
| 2 | MC 1408-L8 8-bit digital-to-analogue convertor |
| 1 | MC 1407 a-d control circuit |
| 4 | NE 531 high-speed differential op-amp |
| 16 | NE 2528 dual 250-bit shift register |
| 1 | LM 302 voltage follower |

**Transistors**

| | |
|---|---|
| 1 | BSX19 n-p-n |
| 3 | 2N2906 p-n-p |
| 3 | BC107 n-p-n |

**Diodes**

| | |
|---|---|
| 35 | 1N4148 general-purpose |
| 1 | BZY 88 C4V7 Zener |
| 1 | 1.8 MHz crystal (for oscilloscopes scopes with 10 horizontal divisions) |

**Resistors**

| | | |
|---|---|---|
| 1 | 470R | ½w 2% |
| 2 | 560R | |
| 1 | 820R | |
| 5 | 1k | |
| 1 | 2k | |
| 3 | 2k2 | |
| 1 | 3k | |
| 2 | 5k1 | |
| 1 | 9k1 | |
| 10 | 10k | |
| 1 | 11k | |
| 8 | 15k | |
| 2 | 18k | |
| 1 | 30k | |
| 2 | 33k | |
| 3 | 47k | |
| 15 | 100k | |
| 1 | 18M | ½w 5% |
| 1 | 1k pot. | |
| 1 | 47k trimpot | |

**Capacitors**

| | | |
|---|---|---|
| 1 | 15p | tubular ceramic |
| 1 | 20p | |
| 2 | 22p | |
| 2 | 39p | |
| 4 | 100p | |
| 1 | 120p | |
| 3 | 270p | |
| 1 | 470p | |
| 1 | 680p | |
| 16 | 100n | disc ceramic |
| 1 | 470p | 1% mica |
| 1 | 1n | |
| 1 | 2n2 | |
| 1 | 4n | |
| 1 | 10n | |
| 1 | 22n | paper, polyester, etc |
| 1 | 47n | |
| 1 | 100n | |
| 1 | 220n | |
| 1 | 470n | |
| 1 | 100µ | electrolytic 10V |

**Switches**

| | | |
|---|---|---|
| 1 | 3-pole | 10pos. rotary |
| 1 | 1-pole | 2-throw toggle |
| 2 | 1-pole | 2-throw toggle |
| 1 | 1-pole | push button |
| 1 | 1-pole | 4-pos. lever |

**Specification**

The unit gives a storage area of 6 divisions vertical and 10 divisions horizontal.

**Input from oscilloscope:**
+300 mV for all positive storage
−300 mV for all negative storage
± 150 mV for bipolar storage
The input levels are easily adjusted to suit the oscilloscope and the 0V position is adjusted by a control on the front panel.

**Time/div. ranges:**
Store mode: 500, 200, 100, 50, 20, 10, 5, 2, 1, 0.5 ms/div.
Roll mode 500, 200, 100, 50, 20, 10, 5, 2, 1, 0.5 s/div.
Thus the range is from 0.5ms/div to 500 s/div in 19 ranges.

**Waveform output to oscilloscope:**
± 6V (2V/div)-irrespective of input polarity; i.e. 0V appears as −6V for all positive storage,
+6V for all negative storage,
and 0V for bipolar storage.
The output levels are easily adjustable.

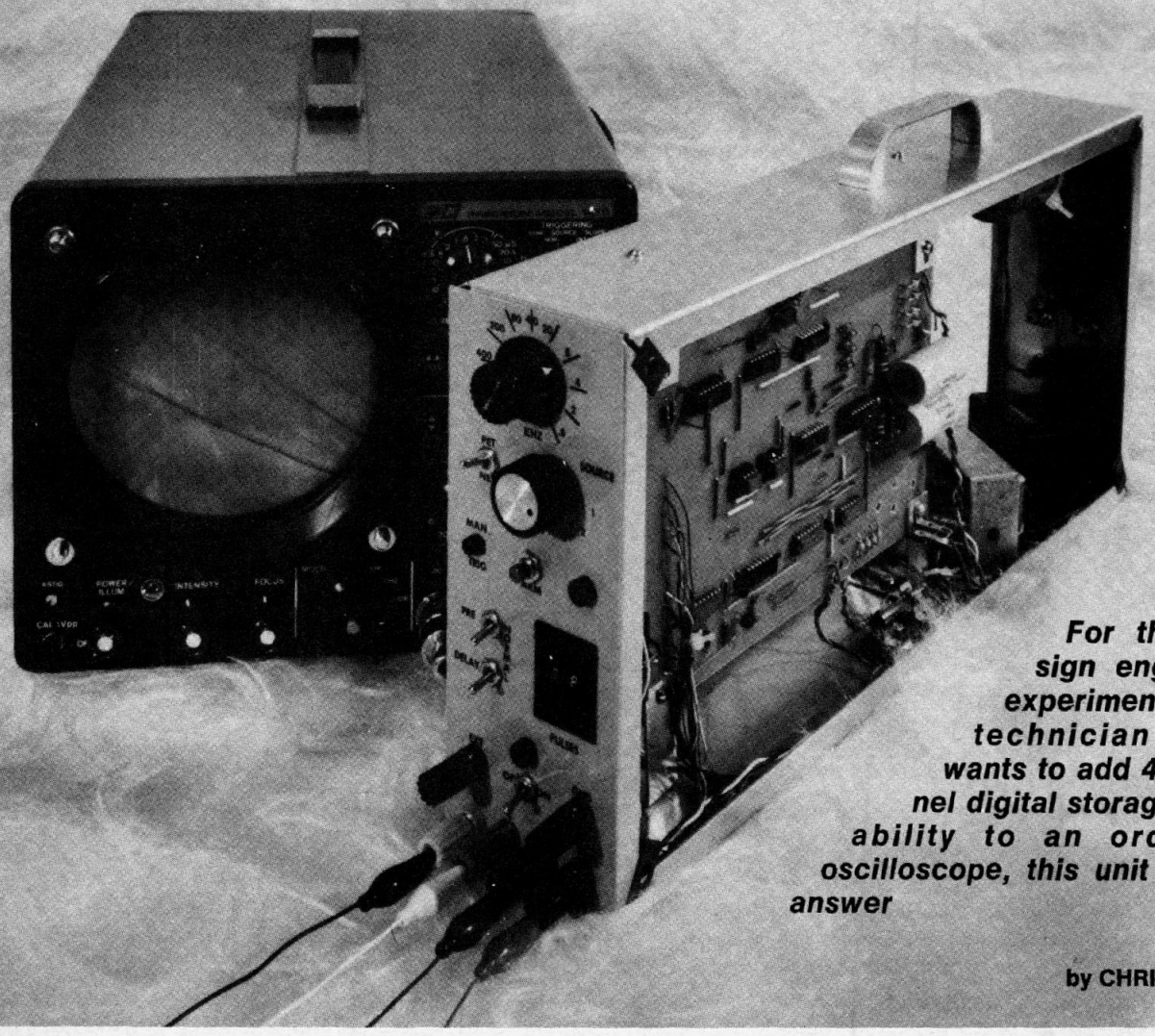
**Sync to oscilloscope**
0 to +15V edge at the start of the stored waveform. This is fed into the Ext Trig input of the oscilloscope.

**Blanking to oscilloscope:**
+15V level after the tenth division the length of which is selected to suit the oscilloscope.

**A-Gate from oscilloscope:**
+5V logic level, going high at the start of "A" timebase sweep. Level must be maintained for at least 10 divisions during display stored waveform period.

**B-Gate from oscilloscope:**
+5V logic level or pulse going high at the start of "B" timebase (approx 10µs min).

# BUILD THIS Digital Scope Memory



***For the design engineer, experimenter or technician who wants to add 4-channel digital storage capability to an ordinary oscilloscope, this unit is the answer***

**by CHRIS TITUS**

THE DIGITAL STORAGE SCOPE CONTROLLER (DSSC) is an extremely versatile and powerful accessory that can be used with any oscilloscope with X-Y capabilities. This accessory permits the professional digital designer, technician or amateur to monitor the time relationships between four TTL signals originating from a breadboard, printed circuit board or single integrated circuit! Unlike a conventional storage scope that has a long-persistence phosphor on the CRT face, the DSSC "stores" the four TTL pulse trains in an MOS memory. Once the memory has been filled, the data is continuously fed to the oscilloscope fast enough to produce four distinct, static, flicker-free traces on the screen.

The DSSC consists of a memory, an X and Y axis controller, a time base and a main control section. The time base (see Fig. 1) is a crystal clock and a series of divide-by-ten counters. At the highest frequency of 2 MHz, 4 bits of TTL data are stored in the memory every 500 ns. At the lowest frequency of 800 Hz, the sample interval would be 1.25 ms. Within this range of frequencies, we can diagnose problems in such projects as the Mark 8 Minicomputer or the TV Typewriter. We can also test flip-flops, shift registers, counter-decoder circuits or even another DSSC!

The DSSC has four digital storage channels, each one 256 bits long. The data is stored in two N2527V IC's, IC13 and IC14 (see Fig. 2). Each contain two, 256-bit shift registers and recirculate logic (see **Radio-Electronics** December, 1974). At a data acquisition frequency (sample interval) of 2 MHz, we can acquire one bit of information every 500 ns until we have accumulated our maximum capacity of 256 bits. This would give us a total monitoring time of 128 ms. At 800 Hz (clock frequency), maximum acquisition time is 320 ms.

The X-axis controller is a sawtooth wave generator that provides separate but simultaneous positive and negative ramps. The sawtooth wave provides the X-axis scope deflection for the digital data as it is fed to the Y-axis, providing the complete display. The 2 different ramps are available because some scopes require a positive ramp and others a negative ramp to sweep the electron beam from left to right. Determination of the type of ramp your scope will require is described in the Construction section.

The Y-axis controller is designed around a two-bit Digital-to-Analog converter (DAC). The four data outputs of the shift registers go into a 4:1 multiplexer and the A and B select pins of the multiplexer are driven by a 2 bit counter. The same two-bit counter drives the DAC inputs. The counter is pulsed once

each time the shift registers have been clocked 256 times. The output of the multiplexer would then consist of data from one of the other four shift registers *and* the DAC would produce a new offset voltage. The different analog voltage output steps of the DAC are then summed with the digital output of the 4:1 multiplexer to provide the 4 separate traces. Therefore, during the display of the stored data, we have 4 separate traces on the CRT face, each composed of 256 bits of TTL data.

The control section (Fig. 3) permits the user to operate the DSSC in the PRE-TRIGGER, NORMAL and DELAY record modes. In the PRE-TRIGGER mode, the DSSC is continuously acquiring data, once the DSSC is armed. The data is shifted from one memory location to another until it is shifted out of the last location and lost. When a valid trigger pulse occurs, the memory contains the last 256 "samples" that entered the memory before the trigger pulse occurred. We continue to acquire data until the number of data "samples" is equal to a number established by internal user-selectable jumpers. Assume that we had decided to use 100 of the 256 memory locations to store pre-trigger data. This would mean that after a trigger pulse occurred, we would acquire 156 additional points (we would add binary jumpers until they added up to 156—128 + 16 + 8 + 4) before the shift registers began to recirculate the data and the display began. The displayed data would be about 2/5 (100/256) pre-trigger data and about 3/5 (156/256) post-trigger data. The data would be displayed from left to right with the earliest pre-trigger data on the left of the screen.

We can also delay data acquisition by setting two thumbwheel switches (TWS) to any number between 0 and 99. When the ARM pushbutton is activated, the number set on the TWS is entered into a series of programmable down counters. Only after these counters have counted down to 0, one count per trigger pulse, will the next pulse be permitted to trigger the DSSC. Thus, if we set 46 on the TWS, we will need 47 pulses to trigger the DSSC.

Where do valid trigger pulses come from? Ideally, we should be able to monitor any one of the 4 data inputs for either a positive-to-negative (1 to 0–NET) or a negative-to-positive (0 to 1–PET) transition and use this to trigger the DSSC. The CHANNEL SELECT switch permits us to choose any one of 6 trigger sources. Four of these are the 4 data input lines, the other two being a MANUAL TRIGGER pushbutton and a separate EXTERNAL TRIGGER binding post. The EXTERNAL TRIGGER position permits us to monitor a signal for triggering purposes only. In this manner, one of the four traces will not be wasted storing the trigger pulse. With the PET/NET switch, we can also determine which edge (positive or negative—PET or NET) will be used to trigger the DSSC.

The DELAY mode of operation is very useful for diagnosing faults in logic that only become apparent after a particular number of pulses have occurred. If your logic becomes unsynchronized or halts after it has been pulsed 32 times, we could enter 27 on the TWS and store only the data present at the four inputs after the 28th (or 1 more than the number set on the TWS) pulse. This way the display will be composed of data present before, during and after the 32nd pulse had occurred!

## Construction

Use care in soldering all components to the PC boards, using a low wattage (25-35W) soldering iron. If you are soldering the IC's directly to the PC boards, make sure that they are *completely functional* (test them yourself to be sure). When you make the jumpers use insulated wire. This not only makes the project more attractive, but prevents the possibility of a short-circuit during the construction and testing. Once you've soldered the components to the PC boards, you can remove the flux with denatured alcohol or rubbing alcohol. Make sure that the polarity of all diodes and the orientation of all IC's is correct before soldering. *Note* that in this section, a capitalized word or abbreviation represents a pad on one of the two PC boards that a wire will be soldered to.

## Time base board

Build the power supplies on the mem-

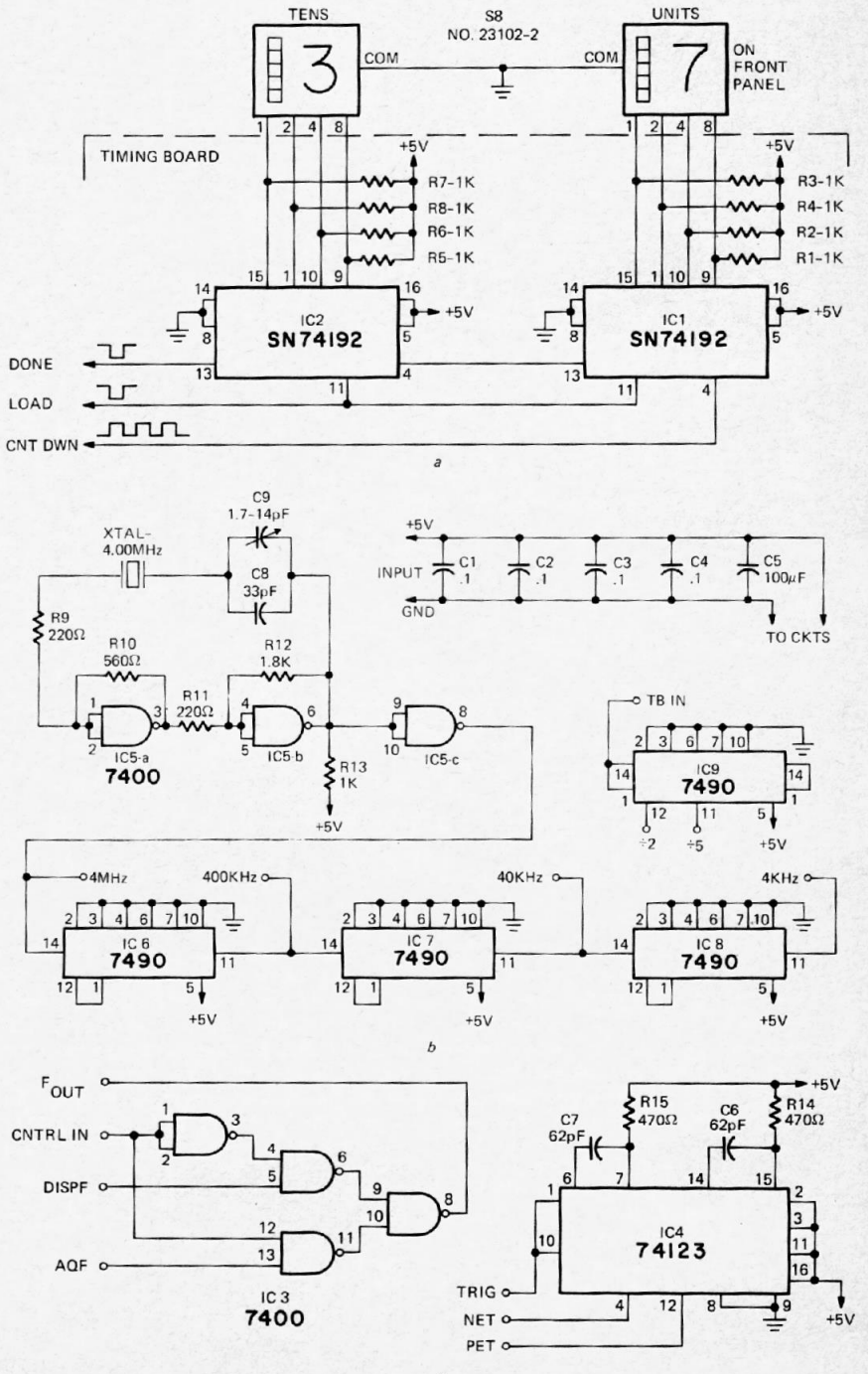



**FIG. 1—THE TIME-BASE BOARD CONTAINS THREE SETS OF CIRCUITRY. As you can see they do not interconnect with each other. They do connect to either the memory board or the controls on the instrument.**

oard (Fig. 4). Note the orientation of the diodes and capacitors. The 10,000-μF capacitor and Q3 should be connected to the board with 10-inch jumpers. These components will eventually be mounted on the chassis. Check the output voltages of the supplies, making sure you have +5, +12 and −12.

Wire all the components and jumpers to the time-base board. Don't forget to add a +5V and ground jumper between the memory and time base boards. Adjust trimmer capacitor C9 so that ½ of the adjustable portion is meshed with ½ of the fixed portion. Observe the 4-KHz signal from the 4-KHz pad on the time base board or from pin 11, IC8. If there is no signal, move back up the chain of 7490 decade counters, IC8, IC7 and IC6 until the problem is located. Wire a jumper from any one of the time base outputs to TB IN, near IC9. Verify the functionality of the divide-by-2 and divide-by-5 circuits. IC9, a decade counter, has been wired to perform both the divide-by-2 and divide-by-5 functions.

Wire the thumbwheel switches using 10-inch jumpers. Be sure to connect the commons of both sections (terminals marked COM) to the ground located between IC2 and IC3. Set the thumbwheel switches to any number between 10 and 20 and momentarily ground LOAD. Verify that pulsing CNT DWN with a positive going pulse one more time than the number set on the switches produces a negative going pulse on DONE. The pulsing *MUST* be done with a debounced switch or a TTL oscillator.

Jumper any two frequencies from crystal clock section of the Time base board to the AQF and DISPF inputs (1 to each input) near IC3. Put CNTRL IN to +5V and then ground making sure that both frequencies are available at FOUT depending on the voltage level at CNTRL IN.

## Memory board

Add all the remaining components to the memory board except the MOS shift registers, IC13 and IC14. Wire a jumper between the 40-KHz output of the time base and the SWEEP input between IC19 and IC20. Connect YOUT to your scope and observe the four-step staircase, going down from left to right. If you only have two steps, check the Q outputs of IC16, pins 11 and 15. They should be changing, one twice as fast as the other.

Connect XOUT to the scope and observe the sawtooth, doing the same for −XOUT. One output should be a positive ramp and the other a negative ramp. If there is no sawtooth, make sure pin 3 of IC11 is being clocked and that the resulting output, pin 6 of IC11 is a short positive-going pulse. Also check the orientation of the

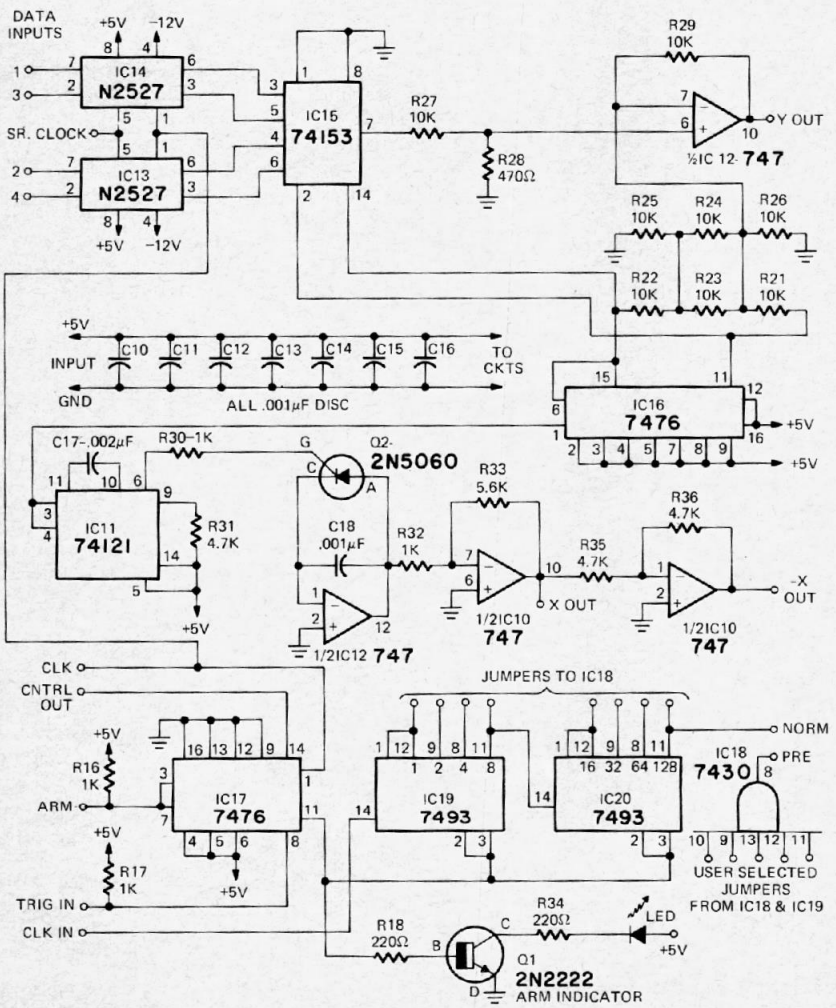



**FIG. 2—MEMORY BOARD CIRCUIT. The memory is all in IC14 and IC15. Each one is an N2527.**

### PARTS LIST

**All resistors are ¼ W, 10% unless otherwise noted**

R1-R8, R13, R16, R17, R30, R32—1000 ohms
R9, R11, R18, R34—220 ohms
R10—560 ohms
R12—1800 ohms
R14, R15, R28—470 ohms
R19—47 ohms, 1W
R20—220 ohms, ½W
R21-R26, R27, R29—10,000 ohms
R31, R35, R36—4700 ohms
R33—5600 ohms
C1-C4, C10-C16—.1-μF ceramic disc
C5—100-μF 6V electrolytic
C6, C7—62-pF ceramic disc
C8—33-pF ceramic disc
C9—1.7—14-pF trimmer; Johnson 189-505-5 or equal
C18—.001-μF polystyrene
C17—.002-μF ceramic disc
C19, C20—500-μF 25V electrolytic
C21—10,000-μF 10V electrolytic
Q1—2N2222 general purpose NPN
Q2—2N5060 SCR
D1-D8—IN4001 or equal
D9, D10—12V, 1W Zener, 1N4742 or equal
IC1, IC2—74192 synchronous decade up/down counter—TTL
IC3, IC5—7400 quad nand gate—TTL
IC4—74123 monostable multivibrator—TTL
IC6, IC7, IC8, IC9—7490 decade counter—TTL
IC11—74121 monostable multivibrator—TTL
IC10, IC12—747 dual operational amplifier
IC13, IC14—N2527V dual 256 bit static shift register (Signetics)—MOS
IC15—74153 dual four-to-one multiplexer—TTL
IC16, IC17—7476 dual J-K flip-flop—TTL
IC18—7430 8-Input positive nand gate—TTL
IC19, IC20—7493 4-bit binary counter—TTL
Q3—LM309K or equal
T1—24VCT ½A power transformer
T2—6.3V 1A power transformer
LED—MV 5020 or equal
XTAL—4.0000 MHz crystal available from International Crystal, 10 North Lee, Oklahoma City, OK 73102
Order as: 4,000 KHz EX series crystal $3.95
S1—2 pole, 11 position, 2 deck rotary switch, NON-SHORTING (1 pole/deck)
S2—1 pole, 6 position rotary switch, NON-SHORTING
S3, S4, S5, S9—SPDT miniature toggle switch
S6, S7—SPST normally open, momentary pushbuttons
S8—Digitran 23102-2; 2 module thumbwheel switch, BCD complement with one common

**Misc.**

Mounting hardware, fuseholder, line cord, fuse, power (110 VAC) switch, 6-5 way binding posts. 2 BNC connectors for the X and Y signals, pilot light, rubber feet, Bud chassis AC 412 and bottom plate BPA 1520.

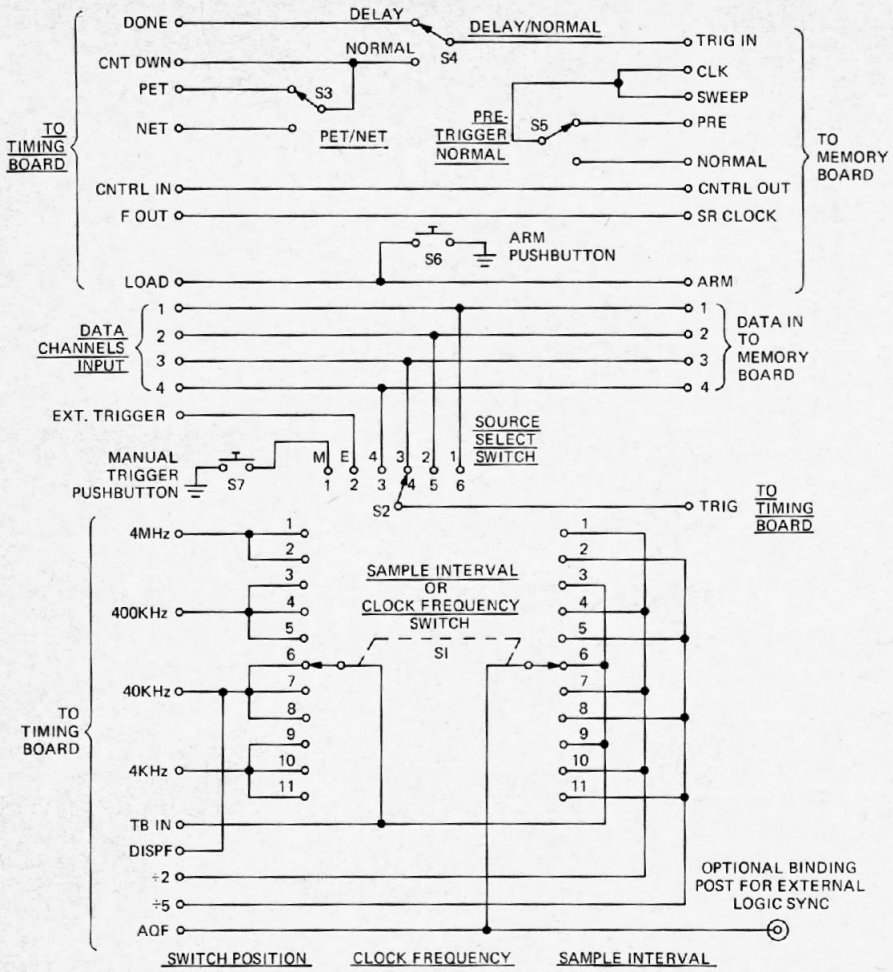
The Johnson 189-505-5 is available from:

Circuit Specialists Co., Box 3047
Scottsdale, AZ 85257

— or —

Bursten Applebee, 3199 Mercier St.
Kansas City, MO 64111

**Both the memory and time base Glass Epoxy printed circuit boards, drilled, cut to size and ready for component insertion is available for $12.95 postpaid from Techniques Inc., 235 Jackson Street, Englewood, NJ 07631. New Jersey resident should add 5% sales tax.**




| SWITCH POSITION | CLOCK FREQUENCY | SAMPLE INTERVAL |
|---|---|---|
| 1 | 2 MHz | 500 ns |
| 2 | 800 kHz | 1.25 μs |
| 3 | 400 kHz | 2.50 μs |
| 4 | 200 kHz | 5 μs |
| 5 | 80 kHz | 12.5 μs |
| 6 | 40 kHz | 25 μs |
| 7 | 20 kHz | 50 μs |
| 8 | 8 kHz | 125 μs |
| 9 | 4 kHz | 250 μs |
| 10 | 2 kHz | 500 μs |
| 11 | 800 Hz | 1.25 ms |

**FIG. 3—FRONT PANEL CONTROLS ARE SHOWN IN THIS DIAGRAM. They connect to both the memory and time-base circuit boards. Foil patterns for these boards will be published with the second part of this article.**

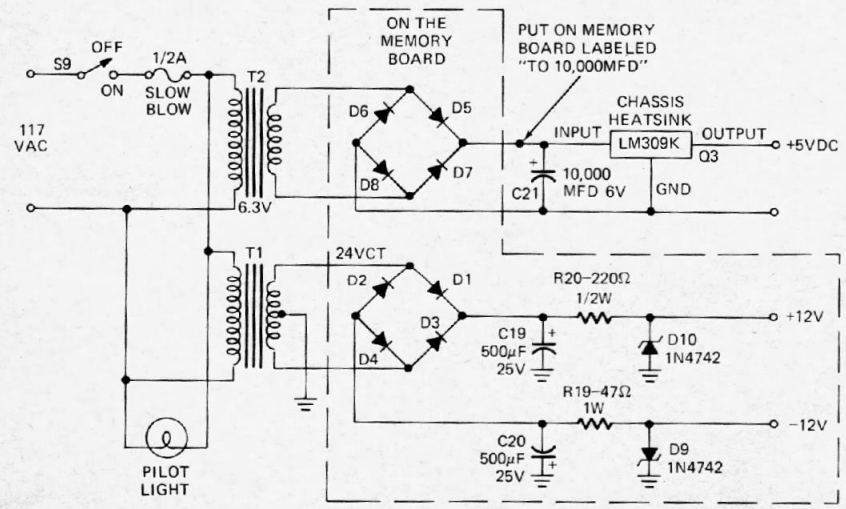



**FIG. 4—POWER SUPPLY FOR THE SCOPE MEMORY. Note that the circuitry inside the dashed lines is on the memory board. Don't build it twice.**

SCR and Q2 making sure that the gate of the SCR is being pulsed.

Move the 40-KHz jumper to SR CLOCK near IC13, and note the 156-Hz output on NORM, near IC20. If there is no pulsing output, go back up the chain of the divide-by-2 circuitry until the problem is located, IC19 and/or IC20.

Add your light-emitting-diode (LED) ARM indicator. Wire one end to the LED terminal between IC17 and IC18 and the other end to +5V. Momentarily ground ARM and the LED should turn on. If not, check pin 11 of IC17 for a logic 1 (+5V). Make sure that the polarity of the LED is correct. Also check pin 14 of IC17 for a logic 1. Momentarily ground TRIG IN, the LED should go out, but pin 14 of IC17 should still be a logic 1. By grounding CLK pin 14, IC17 should go to a logic 0 (ground).

Since the shift registers are reasonably expensive, use sockets or Molex strips for these two IC's. Add the shift registers, IC13 and IC14. Momentarily ground ARM and then individually ground or connect to +5V the four DATA INPUT pads. Grounding or connecting to +5V, one input pad at a time should only effect one input, pins 3, 4, 5 and 6, of IC15. Check these pins with a VTVM, VOM, scope or logic probe, while connecting the DATA INPUT pads to ground and +5V. If you don't observe any changes, the shift registers are bad. Don't forget, at 40 KHz, the data will take 6.4 ms to "percolate" through the shift registers before appearing at the input pins of IC15.

Wire up all the SPDT and rotary switches with 12" jumpers and connect them to the appropriate pads on the PC boards. Add the jumpers between IC18 and IC19 and IC18 and IC20. There should be no jumpers between IC19 and IC20. If you want 50 pre-trigger data points, add jumpers until they add up to 206 (128 + 64 + 8 + 4 + 2). Remember, the jumpers represent the number of data points to be stored *after* a trigger pulse occurs, when the DSSC is in the PRE-TRIGGER mode.

We will complete this article next month and present foil patterns and parts layout overlays for the scope memory.

*(to be continued)*


*"Yes, I am an authority on* Test Patterns, *but I'm afraid your History Exam is your own problem."*