Large-screen TV storage CRO adapter

Synchronised display ● Graticule ● One-shot triggering

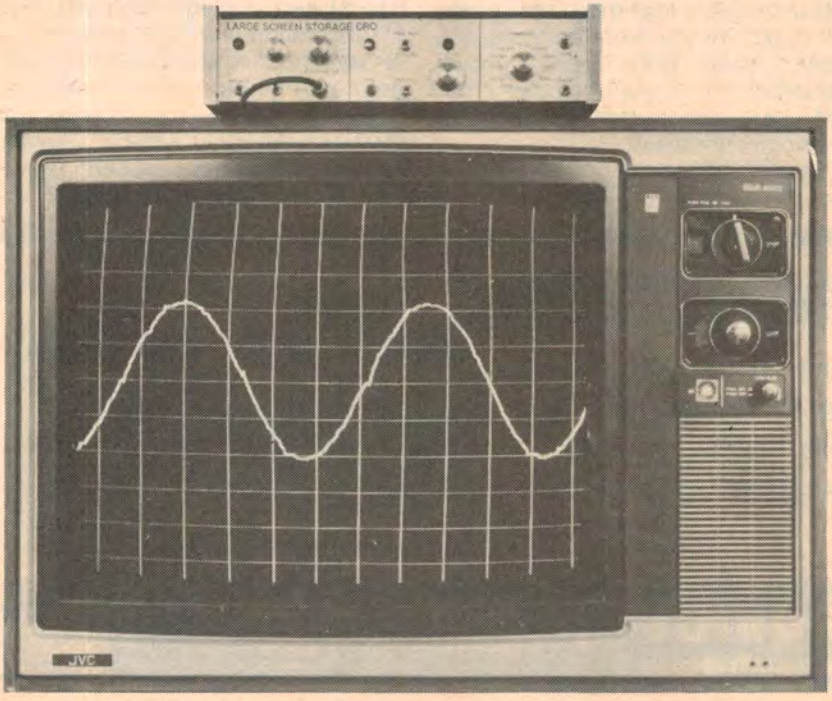
While oscilloscopes are now available at quite reasonable cost, storage CROs still remain beyond the means of most hobbyists. For around $100, however, our new Large Screen Storage CRO converts a normal TV into a storage CRO with features such as a fully synchronised display, electronic graticule, one-shot triggering and optional storage of up to four screen displays.

by RON DE JONG

Back in May 1980 we published a design to adapt any TV set for use as a large screen oscilloscope. Using only seven low cost ICs, this simple design allowed waveforms up to 300kHz to be displayed. While this adapter was very popular and is still being sold, it does have drawbacks which can be expected from a simple design. For a start, high frequency waveforms were displayed as a series of dots.

Due to the digital techniques used in generating the display, our new TV CRO also has a storage facility plus the ability to display very slow waveforms since there are no problems with persistence of the screen trace. These features can be used to display such "slow" waveforms as ECG or other biomedical signals, seismic waveforms and various transducer data like temperature. The storage facility is useful for capturing transient waveforms like human speech and it clearly displays the "voicing" of musical instruments, eg, electronic organs.

Perhaps the most obvious feature of this CRO is that it uses a TV as a display. This can be an advantage in classrooms, lectures or demonstrations where the large screen size of a TV makes it easily visible.



One feature our Storage CRO has over conventional CROs is that the timebase is crystal locked and fixed with respect to an electronic graticule consisting of 10 vertical by 12 horizontal grid lines. There are 12 timebase settings as follows: 32μs, 64μs, 128μs, 1.02ms, 2.05ms, 4.1ms, 8.2ms, 16.4ms, 32.8ms, 65.5ms, 131ms and 262ms per division. Accuracy of the crystal timebase is 50 parts per million.

Looking at the front panel of the unit we can see that the unit has the usual controls found on CROs: input attenuator, shift, AC/DC input coupling, BNC input socket, trigger level, one-shot/continuous switch, free-run/synced switch. The one-shot/continuous switch selects either continuous updating of the displayed waveform or a one-shot display in which case the trigger is armed via the ARM button, turning the SET LED on. When the CRO is triggered the SET LED turns off and the screen is updated with one sweep. Each time the ARM button is pressed, a new waveform will be displayed when the unit is triggered.

Additional front panel features include a LED above the trigger level control which indicates whether the unit is being triggered, thus allowing rapid adjustment of the trigger level. A HOLD/RUN switch freezes the currently displayed waveform and a PAGE located beneath the HOLD/RUN switch, switches from one stored screen display to another so that two waveforms can be captured and then compared by switching between the two "pages".

The unit interfaces to a normal TV set either via the antenna inputs or via a direct video connection. Input to the unit is via a standard BNC connector and the maximum input sensitivity is about 25mV per division.

The operation of the unit is in a sense similar to our previous TV CRO adapter

LEFT: This photograph shows the Large-Screen Storage CRO displaying a 6kHz sinewave. Note the electronic graticule.

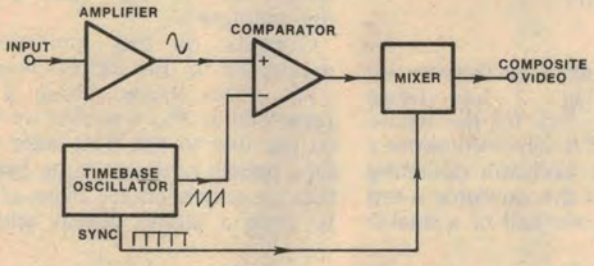
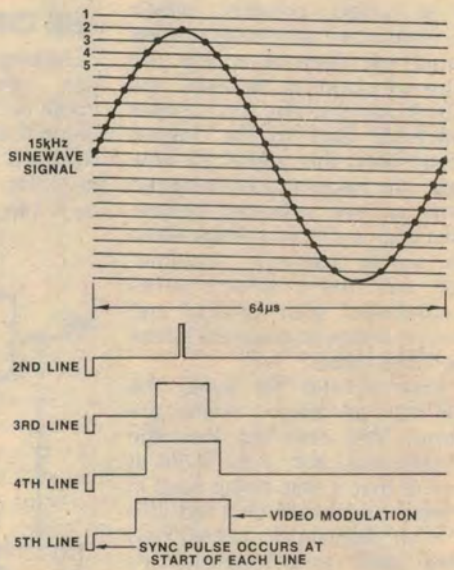


FIG. 1

ABOVE: Basic scheme for a TV CRO adapter. The input signal is compared with a timebase signal and mixed with the timebase sync pulses to produce a composite vide output.

RIGHT: The diagram shows how a basic adapter would display a 15,625kHz sinewave signal. Note the sync pulses at the start of each line, and that one complete cycle occurs during each horizontal scan of the screen.



in that the unit relies on the normal deflection system of the TV. By generating a video signal that turns the electron gun in the TV on at the appropriate times a picture of the waveform is built up.

In a normal television the entire screen is scanned 50 times a second. Each scan or "field" consists of 312.5 horizontal lines which are written from left to right across the screen. Clearly the field frequency is 50Hz and the line frequency is 312.5 x 50 or 15,625Hz.

Let's assume that we wish to display a sinewave signal and that by some stroke of luck its frequency happens to be exactly the same as the line frequency of the TV. Referring to Fig. 1 we can see that one complete cycle occurs during each horizontal scan of the screen. This input signal is compared to a ramp signal which falls linearly from some initial value at the start of each field with the output of the comparator connected to the video input of a TV.

In effect the ramp signal represents the vertical position of the current line being scanned. So as the TV scans across one line and the sinewave goes through one complete cycle the comparator will generate a high signal when the sinewave is above the ramp signal and a low signal when it is below the ramp. If this signal is combined with suitable horizontal and vertical sync signals the resultant composite video would generate a sinewave "picture" in which the area above the sinewave would be white and the area below would be black.

This is not exactly what we want but it is a start! Now if instead of comparing the input signal to just one ramp we compare it to two ramps, one just slightly below the other in voltage, then the two comparator outputs will be similar except that one sinewave picture is slightly lower than the other. If we invert one comparator output and OR it with another comparator output we obtain a thin sinewave where the two pictures overlap.

SYNCHRONISING THE DISPLAY

The resultant sinewave picture will appear stationary but only because it is locked to the line frequency of the television. Most signals however are not, and the only practical way of achieving a locked or synced picture for all input waveforms is shown in Fig. 2.

Basically the input signal is converted into a sequence of eight-bit binary numbers using an A-D converter and these numbers or bytes are stored in consecutive locations in RAM (Random

SPECIFICATIONS

TIMEBASE: 32µs, 64µs, 128µs, 1.04ms, 2.05ms, 4.1ms, 8.2ms, 16.4ms, 32.8ms, 65.5ms, 131ms, 262ms
INPUT SENSITIVITY: 25mV/div
INPUT IMPEDANCE: 1MΩ
FREQUENCY RESPONSE: DC to 100kHz
TRIGGERING: Adjustable trigger level and single shot facility.
DISPLAY: Approximately 200 sampled points on screen, each point is stored as an 8-bit binary number — ie, there are 256 discrete voltage levels.
GRATICULE: 10 vertical x 12 horizontal lines on screen
STORAGE: 2 pages (optional 4)
VIDEO OUTPUT: 1.5Vp-p from 100Ω output impedance

Access Memory). The rate at which the input signal is sampled and converted is set by the timebase clocking the "sampling counter" which generates the consecutive memory addresses. The counter is reset by a trigger circuit so that another input waveform is stored in RAM. Since the trigger is activated at one particular point in the input waveform, the input waveform stored in RAM always starts at the same point and effectively represents a locked image of the input signal.

At the same time as the input is being stored in RAM it is also being read out of RAM by a video counter which generates consecutive addresses starting from zero at the start of a line and reaching the full count at the end. The data read from the RAM by this counter is D-A converted back to the original signal except that this signal is now locked to the line frequency of the video circuits. Now, as we indicated before, this locked signal is simply compared to two ramp signals using a "window" comparator and the resultant video signal is combined with vertical and horizontal sync pulses to generate a final composite video signal.

So we have synced (or sunk) the unsyncable but as always there are complications. We assumed that the data was being read out of the RAM at the same time that it was being read in with two sets of address being fed into the RAM. Such memory is called "two port" RAM and unfortunately it's expensive and almost impossible to obtain.

Our solution is more complex but yields excellent results. What we have done is to rely on the vertical and horizontal blanking periods, ie, those times when the TV picture is blanked out at the end of each field and line scan. Using an address multiplexer, we let the video counter access the RAM while the picture is being generated and we let the sampling counter access RAM during the blanking periods.

Due to the speed limitations of the A-D converter that we have used, we can only sample at a maximum rate of 2μs. If we divide the period of one line trace, 64μs, by the number of sampled points, say 256, we find the required access time to be 250ns for the RAM or 200ns due to other restrictions. Of course it would be nice to have more points on screen and thus a higher resolution but it is difficult to get RAMs faster than 200ns.

With this information we can conclude that it would take 256 x 2μs or 512μs to take one complete picture of the input waveform at the highest timebase frequency. At this particular timebase setting and at the next two of 4μs and 8μs, we can sample during the vertical blanking period which lasts 1.6ms in our design. Hence at the beginning of each field, one entire waveform is sampled and for the remainder of the field the waveform is read out of memory and displayed.

Now for timebase settings greater than 8μs it is not possible to store an entire waveform during the vertical blanking period and we have to use another scheme in which we sample only during horizontal blanking periods. Since these occur at 64μs intervals we can successfully sample at 64μs intervals or multiples thereof such as 128μs, etc. Note that there is a gap in the timebase settings in that 16μs and 32μs sampling rates are not available.

THE CIRCUIT

Looking now at the circuit diagram we can see how Fig. 2 has been implemented. The clock for the whole unit is IC22a and IC22b which comprise a standard TTL crystal oscillator operating at 8MHz. Output of the oscillator is fed to IC14b which is one half of a dual-D flipflop. The $\overline{Q}$ output of the flipflop is fed back to the data input so that the flipflop changes state after each clock pulse, dividing the input frequency by two and generating a 4MHz clock.

The 4MHz clock goes to IC1 and IC2, both 74LS163 synchronous binary counters. We have arranged these counters in a parallel clocking configuration with the carry out of IC1 connected to the "T" input of IC2, resulting in completely synchronous operation of the two counters, ie, all the counter outputs change state at the same time. Briefly the carry output of IC1 is low until the counter is in its highest binary count, ie all outputs 1. Now the "T" input of IC2 inhibits its counting when low and permits counting when high, so IC2 will only be clocked each time IC1 changes from its high count of 1111 to 0000.

Referring to Fig. 2 again, IC1 and IC2 together comprise the video counter with their 8 binary outputs counting from 0 to 255 and hence addressing the entire stored waveform. Since these counters are clocked at 4MHz the addressing sequence takes 256 x 0.25μs or 64μs, which is the period of one line scan.

IC3 and IC4 are also 74LS163 synchronous counters and they are connected in the same configuration as IC1 and IC2. Together these two counters are the sampling counter shown in Fig. 2. The multiplexer which switches the address lines of the RAM between the sampling and video counters comprises IC5 and IC6, both of which are 74LS158 quad 2-to-1 line demultiplexers.

Outputs of the multiplexer are connected to the address lines of two 2114 200ns RAMs. These RAMs are organised as 1K x 4 so that we have had to use two to get 8-bit wide memory. One benefit of these RAMs, however, is that we only need 256 bytes of memory to store a screen display and yet we have 1K bytes available. In other words we can store up to four screen displays without any additional circuitry. To simplify switching we elected to just have two "pages" by simply switching one of the spare address lines high or low using switch S5 and leaving the other spare address line fixed.

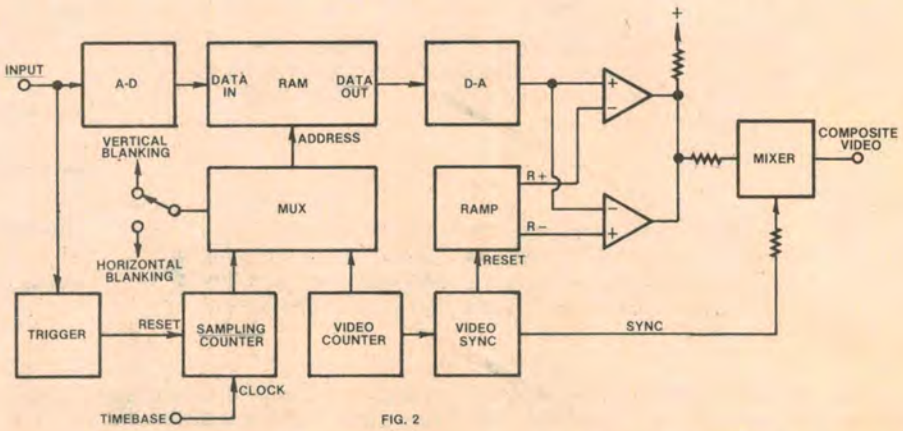
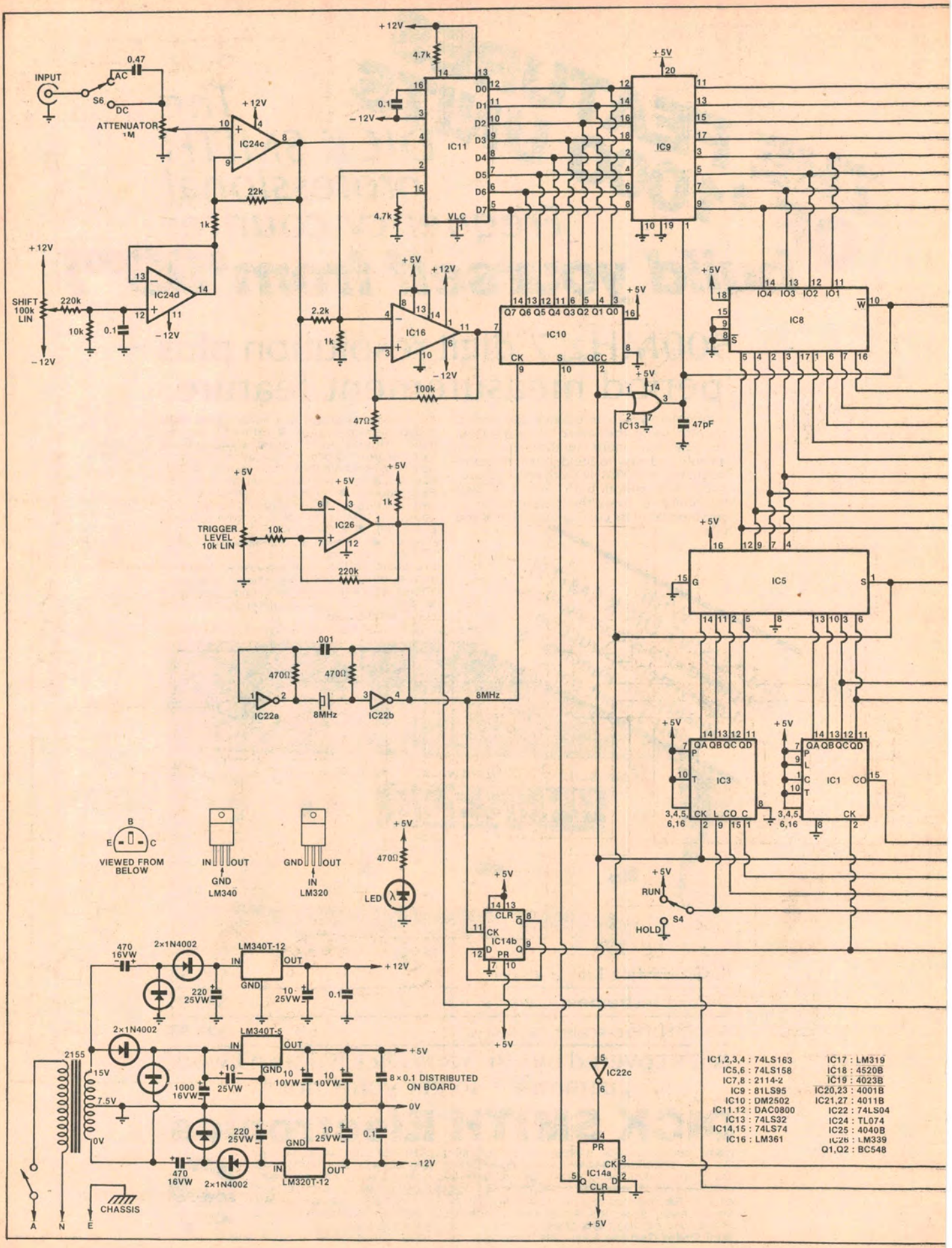
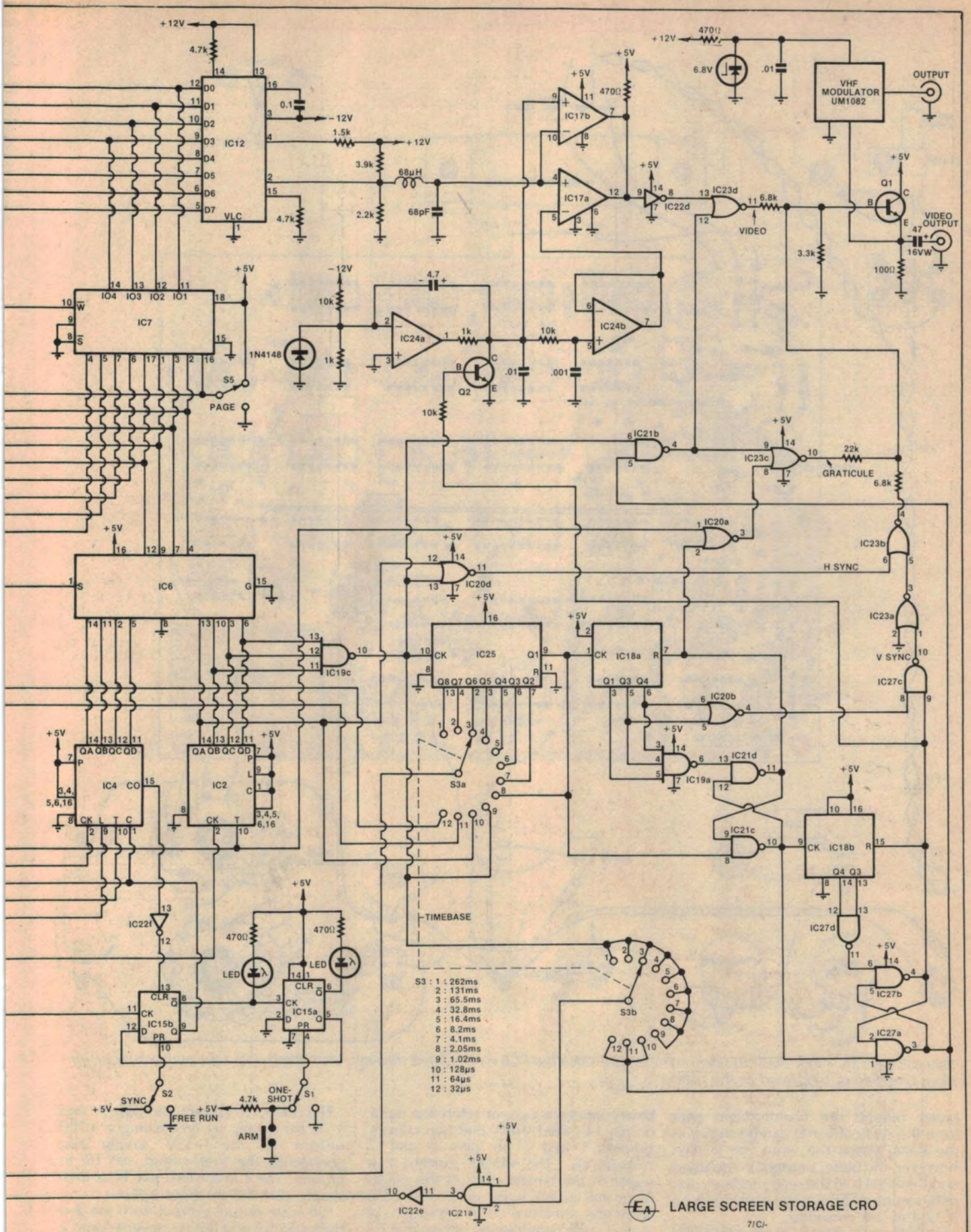


Fig. 2: Basic scheme for a storage CRO adapter with fully synchronised display. The incoming signal is sampled by an A-D converter and stored in RAM.

The RAMs have four combined input-output data lines labelled 101, 102, 103, 104 plus a device-select pin labelled $\overline{S}$ and a write select pin $\overline{W}$. The $\overline{S}$ pin is connected to ground so the RAMs are permanently enabled while the eight IO lines of the two RAMs are connected to IC12, a DAC0800 D-to-A converter, and also to the outputs of IC9 which is an octal Tri-state latch. The inputs to the latch come from IC10 and IC11 which comprise an A-D converter.

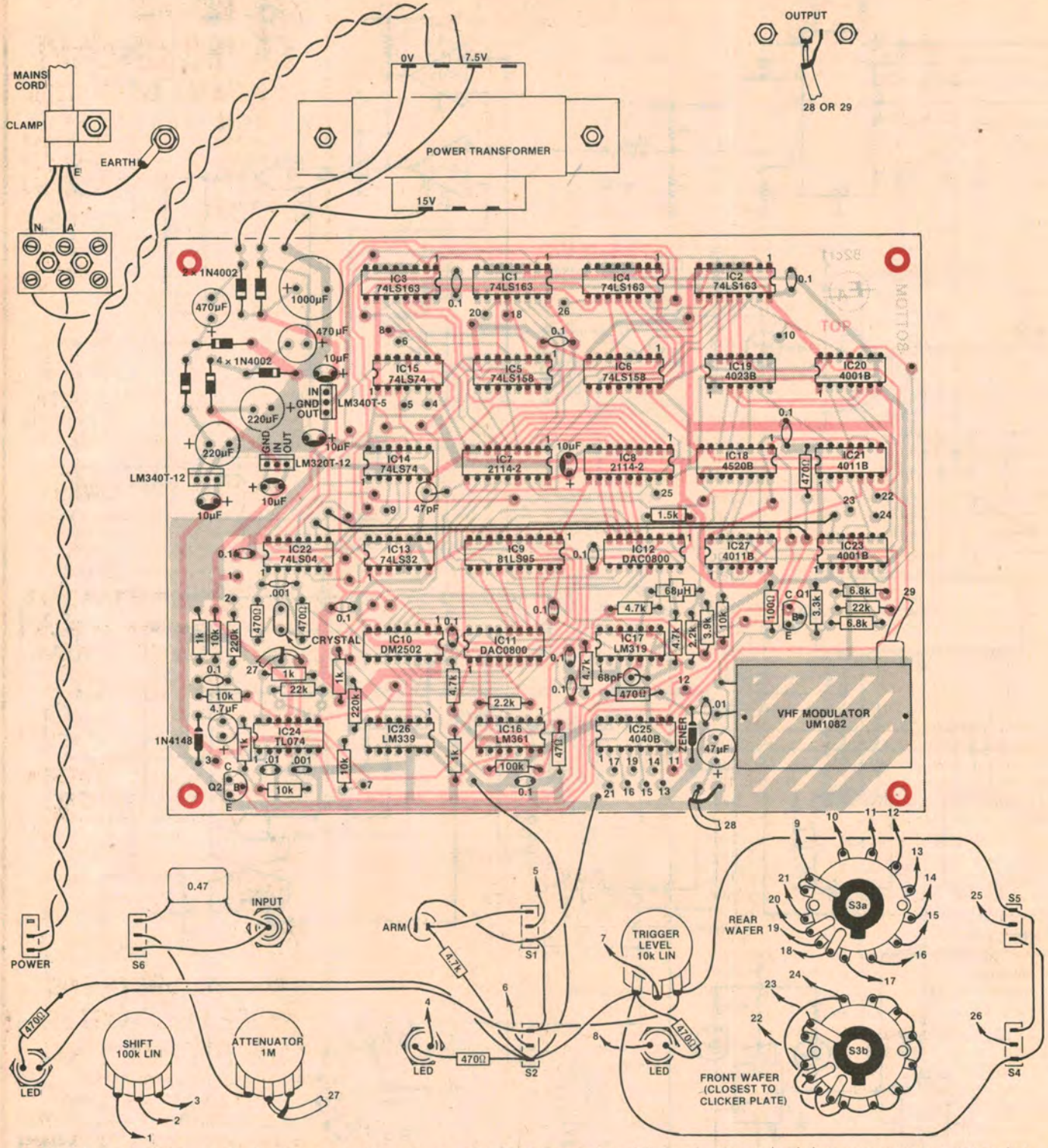
Now the write-enable line of the RAMs is also connected to the output-enable pin of the Tri-state buffer IC9 so that when the write line of the RAMs is low, ie, the RAMs are in the write mode, the


INPUT
0.47
AC
S6
DC
ATTENUATOR 1M
+12V
IC24c
22k
1k
IC24d
SHIFT 100k LIN
220k
10k
0.1
-12V
4.7k
IC11
D0 D1 D2 D3 D4 D5 D6 D7
VLC
IC9
+5V
2.2k
IC16
100k
47Ω
IC10
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
CK S QCC
IC13
47pF
IC8
IO4 IO3 IO2 IO1
W S
TRIGGER LEVEL 10k LIN
IC26
220k
IC5
G S
.001
470Ω
IC22a
8MHz
IC22b
IC3
IC1
QA QB QC QD
CK L CO C
CK
CO
VIEWED FROM BELOW
B E C
IN OUT GND
LM340
GND OUT IN
LM320
LED
IC14b
CLR CK D PR Q
RUN
HOLD
S4
470 16VW
2×1N4002
LM340T-12
220 25VW
10 25VW
0.1
LM340T-5
1000 16VW
10 10VW
8×0.1 DISTRIBUTED ON BOARD
2155
15V
7.5V
0V
LM320T-12
CHASSIS
A N E
IC22c
IC14a
IC1,2,3,4 : 74LS163
IC5,6 : 74LS158
IC7,8 : 2114-2
IC9 : 81LS95
IC10 : DM2502
IC11,12 : DAC0800
IC13 : 74LS32
IC14,15 : 74LS74
IC16 : LM361
IC17 : LM319
IC18 : 4520B
IC19 : 4023B
IC20,23 : 4001B
IC21,27 : 4011B
IC22 : 74LS04
IC24 : TL074
IC25 : 4040B
IC26 : LM339
Q1,Q2 : BC548



LARGE SCREEN STORAGE CRO

7/C/-



You will have to solder on both sides of the board, since the PCB is not plated through. Unmarked dots represent a connection from one side of the board to the other.

butter outputs are enabled and data from the A-D converter can be stored in the RAM. When the write line is high however, the buffer outputs are disabled and the RAM is in the read mode so that data can be read out and converted by IC12, the D-A converter.

Looking more closely at the DAC0800 D-A converters, these devices have eight binary inputs, a current reference input on pin 14 called Vref+ and two current outputs I and $\bar{I}$ on pins 4 and 2 respectively. The output current I is equal to the binary value of the digital input and its full scale value is 255/256 times the reference current into pin 14 while $\bar{I}$ is the complement of I, so that $I + \bar{I}$ always equals the full scale current.

The reference current into pin 14, Vref +, is set simply by connecting a 4.7kΩ resistor to the +12V supply and connecting the Vref– input, pin 15, to ground. The current into pin 14 is then simply 12/4.7kΩ or about 2.55mA.

Full scale output current from pin 2 is then 2.55mA and this is converted into a voltage in the desired range by the 3.9kΩ

and 2.2kΩ resistors connected to pin 2. The output voltage is, as we mentioned earlier, the input waveform continually repeated with each line scan. Due to the way we have sampled this waveform, however, the output will merely be a stepped representation of the input consisting of 256 points and 256 discrete voltage levels. To get a reasonably smooth image we then have to filter the waveform and this is accomplished by the 68μH choke and 68pF capacitor which, taken together with the impedance of the DAC output resistors, forms a second order Butterworth filter with a cutoff of about 2.5MHz.

Since the data points are clocked out at a rate of 4MHz, the highest frequency of the signal is 2MHz so the 2.5MHz cutoff point is high enough not to attenuate this signal appreciably but low enough to remove the harmonics. This smoothed output signal is then compared with the two ramp signals by IC17, an LM319 dual comparator. The outputs of the comparator are open collector so that the two outputs can be just connected together to achieve wi-OR-ed function. This output is buffered by IC22d, an LS TTL inverter and combined with the sync signals to generate our composite video signal.

Getting back to the A-D converter, this comprises another DAC0800 D-A converter, IC11, a successive approximation register DM2502, IC10, and IC16, an LM361 fast comparator.

The method used to achieve A-D conversion is called successive approximation and basically involves dividing the maximum input voltage range in two then testing whether the input signal is above or below the halfway mark. Having established this, we then divide the upper or lower half (whichever the input voltage is in) into half again and check in which half of this range the voltage is. At this stage we would have found in which quarter of the permissable voltage range the signal is in and thus have a 2-bit binary value for the input. By successively dividing these intervals we can establish an 8-bit (or more) binary value for the input.

In practice the 2502 achieves this scheme by setting its most significant bit (MSB) bit 7 high and all the others low, generating a binary digit which is half the maximum binary value. This is converted into a voltage by the DAC and then compared to the input voltage by the comparator, IC16. The result of this comparison is then stored in the successive approximation register as bit 7, which will be 1 if the input is greater than half and 0 if it is less than half. Bit 6 is now set high and the process repeated to determine whether it should be 0 or a 1 and so on for bits 5 to 0.

The DAC is connected in the same fashion as IC12 except that its output, pin 2, goes straight to the inverting input of the comparator IC16. The analog input signal is also fed to the inverting input but via a 2.2kΩ resistor and in effect the current through this resistor and that from the DAC are summed at this point and compared to ground at the noninverting input. The 100kΩ resistor and 47Ω resistor provide a small amount of positive feedback to improve stability.

Clock rate of the 2502 is 8MHz so that each bit is converted in 125ns. Naturally the delay in the DAC output and comparator should be less than this figure and in fact the typical settling time of the DAC output (current within ±½ LSB) is 100ns and propagation delay of the LM361 is 20ns maximum.

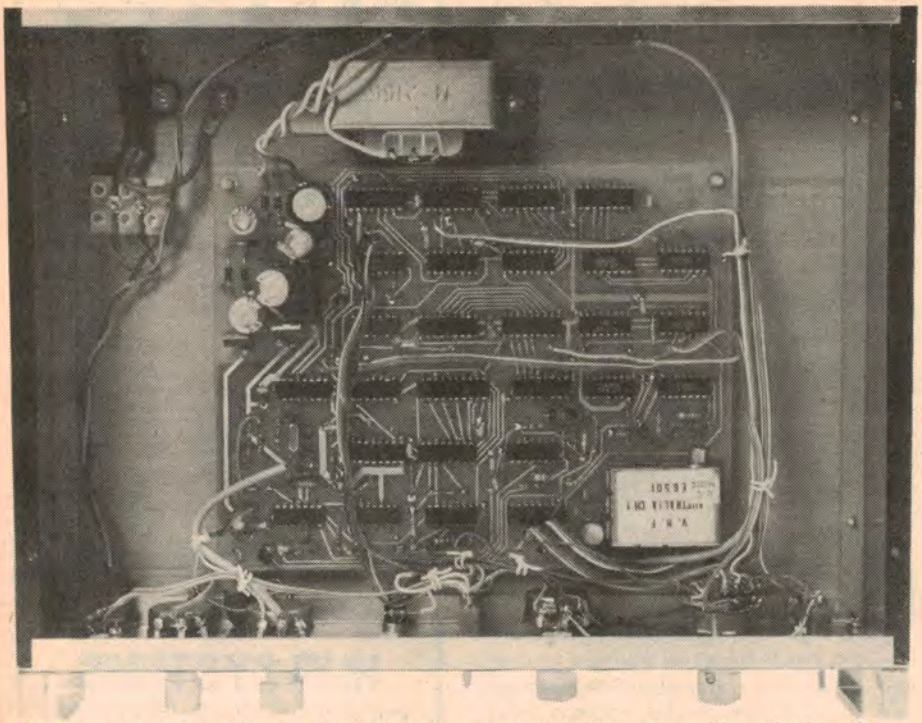
Two other pins on the 2502 register are the S or start input, pin 10, which must be low temporarily to start conversion, and the Qcc or conversion complete signal, pin 2, which is high during a conversion and low after conversion. Qcc is connected to the sampling counters IC3 and IC4 clock inputs so that just prior to conversion the counters are clocked and will present the correct address when the converted byte is ready to be loaded into RAM.

The timebase frequency which is selected via switch S3a goes to the clock input of IC14a, a D flipflop. The rising edge of this clock causes the zero at the data input, pin 2, to appear at the Q output, pin 5. This output is connected to the start input of the 2502 and initiates a conversion cycle causing Qcc to go high. Qcc is inverted by IC22c and applied to the preset input of the flipflop, pin 4, causing the Q output to return to 1. This satisfies the timing requirements for the S input and also resets the 2502 for the next timebase pulse.

Vertical blanking or horizontal blanking signals are buffered by IC21a and IC22e and used to select either the sampling counter or video counter via the select pin, pin 1, of the multiplexers IC5 and IC6. It is also ORed with the Qcc signal by IC13a to generate a write signal for the RAMs.

Like most static RAMs the 2114 don't like their address lines changing during a write operation (poor little beggars), ie, when the $\overline{W}$ signal is low. Due to the necessarily simple timing arrangement we have had to use, we found it necessary to delay the write signal marginally, using a 47pF capacitor.

As indicated in Fig. 2 the sampling counter is reset by the input trigger circuits. This is accomplished by IC15b which has its clock connected to the output of the trigger circuit and its Q output connected to the clear input of the sampling counter IC3 and IC4. The clear input of the flipflop is connected to the carry-out of the counters so that when the counters reach their last count, the carry output goes high, is inverted by



Despite circuit complexity, the unit is easy to build. Note that although this photo shows the modulator, we elected to use the direct video output from pin 28.

IC22f and clears the flipflop. The Q output then goes low and clears the counters, thus removing the carry out signal and therefore the clear input to the flipflop.

The flipflop and sampling counters remain in this state until the positive-going edge of the trigger pulse clocks in a high from the data input, pin 12, which sets the Q output high and enables the sampling counter to start counting through the whole sequence and store a complete input waveform.

Data input to the flipflop is not always high and is in fact connected to the Q output of another flipflop, IC15b. With switch S1 set in the CONTINUOUS position the preset input of the flipflop is grounded, forcing the Q output pins high and thus enabling continuous sampling of the input waveform as already described.

In the ONE SHOT position of S1, the preset input of IC15a is connected to the ARM pushbutton and a 4.7kΩ resistor. If the ARM button is pressed, it sets IC15a's Q output high and enables a sample of the input waveform to be made. At the end of the sampling sequence, IC15b's Q output goes low to clear the counters and the $\bar{Q}$ output goes high. This is connected to the clock of IC15a and clocks in a zero from the data input, pin 2, setting its output low hence stopping any further updating of the input waveform. A new sample of the input waveform can then only be made by pressing the ARM button again.

The SET LED connected to the $\bar{Q}$ output of IC15a indicates whether the trigger is armed. Another LED connected to the $\bar{Q}$ output of IC15b will turn on whenever sampling is in progress, ie, the clear to the counters is high. At low timebase frequencies it will blink on during each screen scan, while at higher frequencies it will appear to be on continuously.

Additional controls are switch S2 which is connected to the preset input of IC15b. In the SYNCED position the preset input is high and the CRO performs normally but in the FREE RUN position the flipflop output is forced high, regardless of triggering, and the sampling counters will continuously count without regard to any starting point on the input waveform. The input waveform will therefore appear to drift across the screen just as in a normal CRO which has lost triggering. Switch S4 is connected to the load input of the sampling counters and in the RUN position does not affect normal operation but in the HOLD position it forces the outputs of the counter high, disabling sampling.

THE SYNC CIRCUITS

Having covered the main features of the CRO circuit we can look at the sync circuits. Firstly IC19c, a three input NAND gate, decodes the last two counts of the video counter IC2. Output of the gate is the horizontal blanking pulse which occurs at the end of each line and is 8μs wide. This signal is further combined with the QA output of IC2 by the NOR gate IC20d to generate a horizontal sync pulse. The horizontal blanking pulse is also used to clock IC25, a 4040 CMOS ripple counter which supplies most of the timebase frequencies as well as a divide-by-two output for IC18.

The clock input to IC18a is a square-wave with a period of two lines (ie, 128μs). This is divided by IC18a which is one half of a dual 4-bit binary counter which divides by 13 in conjunction with IC19a and IC21c, d. What happens is that when the counter reaches the desired count of 13, this state is decoded by IC19a, a three input NAND gate which generates a low pulse setting the RS flipflop made up of two NAND gates IC21c, d. This in turn resets the counter, the RS flipflop remaining latched until the clock input goes low, resetting the flipflop via pin 8 of IC21c.

Accordingly, the reset signal to the counter is high for one line period every 26 lines and we have used this to generate the horizontal lines in the graticule. The carry out signal of IC1 is a .25μs pulse every 4μs and forms the vertical lines in the graticule. This is combined with the reset signal by IC20a to form the graticule signal.

The output of the divider, from pin 10 of IC21c, is now divided by 12 to obtain the vertical sync and blanking pulses. This is accomplished by IC18b which operates in the same manner as IC18a except that it divides by 12. The count is detected by IC27d and the flipflop is composed of IC27a and IC27b. The output of this divider is low for 25 lines and high for the remaining 287 lines in the 312 line field. This pulse is used as the vertical blanking interval.

The vertical blanking pulse is NANDed with the output of NOR gate IC20b by IC27c. The NOR gate decodes four states of the counter, ie it is high for only 8 lines of every 26 lines and so the output of IC27c will be low for 8 lines at the start of each vertical blanking pulse, forming our vertical sync pulse.

Vertical sync pulses from IC27c are NORed with horizontal sync pulses from IC20d by IC2b, generating a combined sync pulse. Both the graticule video signal and the "waveform" video signal are blanked by the combined blanking pulse from IC21b. The blanked outputs from IC23c and IC23d are resistively mixed via 6.8kΩ and 22kΩ resistors. The higher value 22kΩ resistor is used for the graticule signal so that it provides a light background display.

Sync pulses are also combined via a 6.8kΩ resistor from IC23b and a 3.3kΩ

We estimate the current cost of parts for this project is about

$110

including sales tax.

resistor to ground. This composite video signal is next buffered by Q1 which is a BC548 in emitter-follower configuration. The low output impedance of this stage is suitable for directly driving the video input stage of a TV set via the 47μF coupling capacitor or it can drive an optional VHF modulator for which provision has been made on the board. The suggested modulator is type UM1082 from Dick Smith Electronics.

The only circuits which remain to be discussed now are the input amplifier, trigger circuit, ramp generator and power supply.

Input to the CRO is via switch S6 which passes the signal direct for DC coupling or via a 0.47μF capacitor for AC coupling. This is followed by a 1MΩ potentiometer which provides input attenuation. The wiper of the pot goes to the input of IC24c which is one quarter of a TL074 quad BI-FET op amp arranged as a non-inverting amplifier. Gain of the stage is set by the voltage divider ratio of the 22kΩ and 1kΩ resistors to 23.

One feature of this amplifier is that instead of the 1kΩ resistor being returned to earth it goes to the output of IC24d, another op amp. This stage provides the shift function by adding a DC offset to the amplifier. The shift control itself is simply a potentiometer swept between +12 and −12V, attenuated via 220kΩ and 10kΩ resistors, filtered by a 0.1μF capacitor and then buffered by IC24d.

The trigger circuit uses one comparator from an LM339 quad comparator package, IC26. The amplified input signal from IC24c goes to the inverting input of the comparator while the non-inverting input goes to a 10kΩ potentiometer swept between earth and 5V. This "trigger level" pot sets the voltage at which the comparator with toggle. The 1kΩ resistor on the output is a pull up required because of the open-collector output of the comparator. The 10kΩ and 220kΩ resistors connected to the non-inverting input provide a small amount of positive feedback to improve stability.

Power for the unit is obtained from a 15V centre-tapped transformer which feeds a full-wave rectifier circuit, 1000μF capacitor and an LM340T-5 three-terminal regulator. The regulator provides a 5V supply to the TTL and CMOS circuits. 10μF and 0.1μF capacitors on the output are distributed around the board to provide high frequency decoupling.

The transformer also drives two identical voltage-doubler circuits which both provide +17V into an LM340T-12 positive 12V regulator and −17V into an LM320T-12 negative 12V regulator. We have used doubler circuits because the ±12V supplies require very little current.

Ramp waveforms are obtained from IC24a and IC24b, both BI-FET op amps. IC24a is a standard ramp circuit with the non-inverting input grounded and the inverting input connected effectively to a −1.1V source via the 10kΩ and 1kΩ voltage divider. Since the op amp will adjust its output so as to keep the inverting input at the same voltage as the non-inverting input (virtual earth) the output will rise linearly, keeping a constant charging current into the 4.7μF capacitor.

The ramp must be synchronised to the vertical sync of the video circuits, so we have a simple resetting circuit using transistor Q2. This transistor is switched on by the vertical blanking pulse via a 10kΩ current limiting transistor and, when switched on, pulls the positive side of the 4.7μF capacitor to ground while a 1N4148 diode on the other side of the capacitor clamps it to ground (or −0.6V), causing the capacitor to discharge ready for a new ramp. The 1kΩ resistor on the output of the op amp isolates it from the transistor.

Output from this stage is the R+ signal and this is delayed via a 10kΩ and .001μF capacitor and buffered by IC24b to generate an R− ramp. Due to variations in offset voltages of the op amps and comparators, the .001μF capacitor may have to be altered to achieve a reasonable trace width. (Increasing this capacitor increases the line width.)

CONSTRUCTION

Well that finally covers the circuit description (phew!). The construction is certainly a lot easier and involves mounting most of the components on one doubled-sided PC board labelled 82cr1 and measuring 190 × 146mm.

While the PC board is double sided it does not have plated-through holes, considerably reducing cost. The plate throughs are replaced by pin throughs, ie, IC pins or component leads are used to achieve a connection from one side of

PARTS LIST

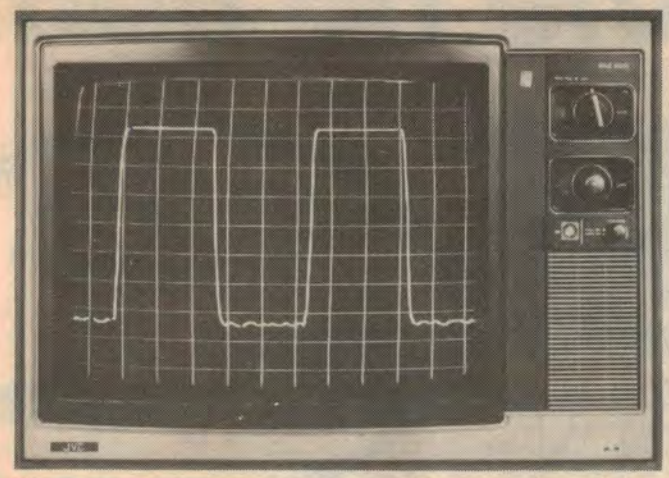
1 PC board, 82cr1, 190 × 146mm
1 Horwood instrument case, 305 x 232 x 78mm
1 2155 mains transformer
1 UM 1082 TV modulator
1 1-pole 12-position rotary switch
6 SPDT miniature toggle switches
1 momentary contact pushbutton
1 10kΩ linear potentiometer
1 100kΩ linear potentiometer
1 1MΩ linear potentiometer
1 8MHz crystal
1 panel mounting RCA socket
1 BNC socket
4 plastic board supports
1 3-way mains terminal strip
1 mains cable and plug
1 cable clamp and earth lug
4 rubber feet
½ metre of 10-way rainbow cable
½ metre of shielded audio cable
1 68uH RF choke

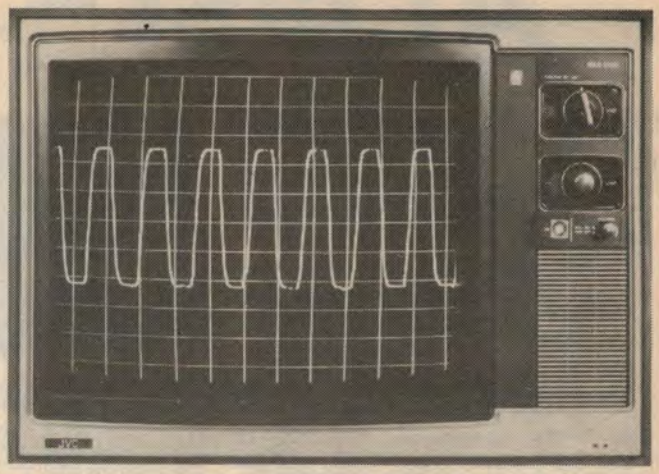
SEMICONDUCTORS
4 74LS163 synchronous binary counters
2 74LS158 quad 2-to-1 demultiplexers
2 2114 RAM (200ns access time or better)
1 81LS95 octal Tri-state buffer
1 DM2502 successive approximation register
2 DAC0800 D-A converters
1 74LS32 quad OR gate
2 74LS74 dual D flipflops
1 LM361 fast comparator
1 LM319 dual fast comparator
1 LM339 quad comparator
1 4520B dual binary counter
1 4023B triple three-input NAND gate
2 4001B quad NOR gates
2 4011B quad NAND gates
1 4040B ripple counter
1 TL074 quad BI-FET op amp
1 74LS04 hex inverter
1 LM340T-12 regulator
1 LM340T-5 regulator
1 LM320T-12 regulator
2 BC548 NPN transistors
1 6.8V 400mW zener diode
6 1N4002 diodes
1 1N4148 diode
2 green LED bezels
1 red LED bezel

CAPACITORS
1 1000μF 16VW PC electrolytic
2 470μF 16VW PC electrolytic
2 220μF 25VW PC electrolytic
1 47μF 16VW PC electrolytic
3 10μF 16VW PC electrolytic
2 10μF 10VW PC electrolytic
1 4.7μF 25VW PC electrolytic
1 0.47μF 400VW greencap
13 0.1μF ceramic or greencap
2 .01 μF greencap
2 .001μF greencap
1 68pF ceramic or polystyrene
1 47pF ceramic or polystyrene

RESISTORS (all ¼W 5%):
2 x 220kΩ, 1 x 100kΩ, 2 x 22kΩ, 5 x 10kΩ, 2 x 6.8kΩ, 5 x 4.7kΩ, 1 x 3.9kΩ, 1 x 3.3kΩ, 2 x 2.2kΩ, 1 x 1.5kΩ, 5 x 1kΩ, 7 x 470Ω, 1 x 100Ω, 1 x 47Ω

NOTE: THE "B" suffix on a CMOS part number indicates a buffered device. Where specified these devices must be used.





These two photographs show a 6kHz square wave signal (left) and a 17kHz square wave signal (right).

the board to the other. Hence, if there is a pad on the top of the board it must be soldered to, as well as the pad on the bottom. In the case where there is no component lead or IC pin, a short length of wire must be soldered in and then cropped close to the board.

The first step in construction is to mount the ICs, resistors and capacitors using the component overlay diagram shown elsewhere in this article as a guide. Make sure that the ICs, diodes and electrolytics are correctly oriented and take the usual precautions against damage to the CMOS ICs due to static electricity, ie, use an earthed soldering iron and solder the supply pins first, pins 7, 14 or pins 8, 16. Solder the leads to the pads on the underside of the board as well as those on the top of the board. If you wish to use IC sockets, then we would recommend using Molex IC pins.

We housed our unit in a Horwood Instrument case with black Marviplate sides and aluminium front and back panels and measuring 305 x 232 x 78mm. Drill mounting holes for the PC board, transformer, terminal strip, etc, using internal photographs of our unit as a rough guide. Mounting holes for the front panel controls can be obtained by using a photocopy of the actual size artwork for our front panel. If you wish to use a Scotchcal front panel then this can be affixed directly and the panel drilled.

Some tips for those unfamiliar with Scotchcal panels: the panels can be cut to size by just scoring along the border with a sharp utility knife and bending the panel back and forth along the line to obtain a clean break. Care should be taken when affixing the panel as once it is stuck, it is impossible to remove in any worthwhile condition. Always drill or file from the Scotchcal side of the panel, being careful not to lift it.

Install the front panel controls, LEDs and sockets and mount the PC board in the unit using Richco plastic board supports or tapped brass spacers. The board can now be wired to the controls using rainbow cable. For neat connections and ease of servicing we would recommend that PC stakes be used on the board.

LED bezels on the front panel are wired as shown on the wiring diagram but note that 470Ω resistors must be wired in series with either the anode or cathode lead of the LEDs.

The mains cable should enter the unit via a grommeted hole and be securely clamped near the entry point. The earth wire should be secured to the case directly using a lug and the active and neutral wires terminated in an insulated terminal strip. Wires to the transformer primary and the power on/off switch should be mains-rated cable and any exposed lugs or terminals on the switch or transformer covered with spaghetti or insulation tape.

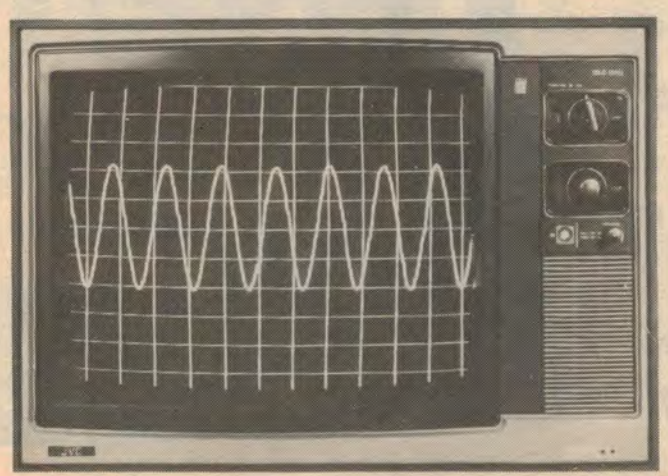
If direct video connection to the TV is desired, then an RCA socket should be installed on the back panel and connected to the video output on the board.

If you are using the VHF modulator instead of direct video then use a 75Ω coaxial TV cable such as RG-58 with an RCA plug on one end, which connects to the socket on the modulator, and a Belling Lee line plug on the other for connection to the 75Ω aerial input on the TV. Some older sets do not have a 75Ω aerial input and in this case it is necessary to use a 75Ω to 300Ω balun.

At this point it is worthwhile going over the PC board again and carefully rechecking the orientation of the ICs, diodes and electrolytics and check that all the pads on the top of the board have in fact been soldered. Also check for solder bridges or cold solder joints; these are the most common faults.

After making the appropriate connections to the TV and switching on, connect an audio oscillator to the input and switch HOLD/RUN to RUN, ONE-SHOT/CONTINUOUS to CONTINUOUS and adjust the shift, attenuator and trigger level to obtain a trace. Note the green LED above the trigger level indicates that the unit is triggering.

FOOTNOTE: Full sized PCB and front panel artworks for this project have not been published in order to save space. Finished PCBs and front panels are available from the usual retailers (see back page), or you can buy transparencies through our Information Service.



LEFT: An 18kHz sine-wave signal. Non-linearities in all the waveforms shown are due to quantising errors. These could only be cured by much faster sampling in the A-D and D-A process.