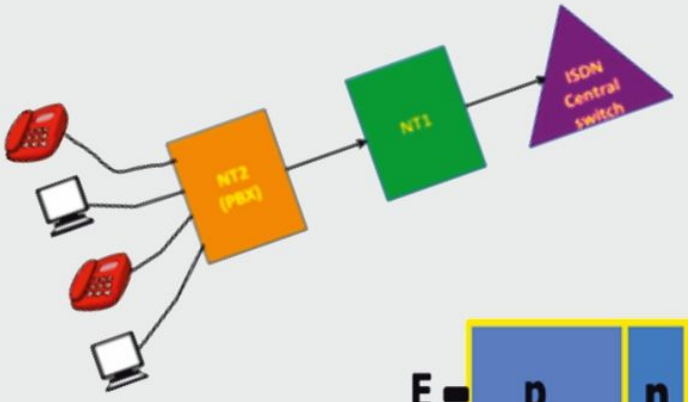
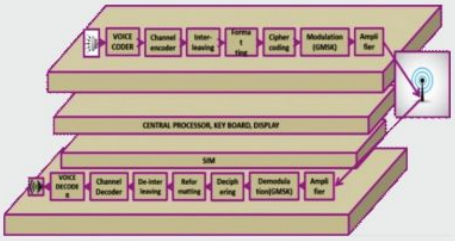
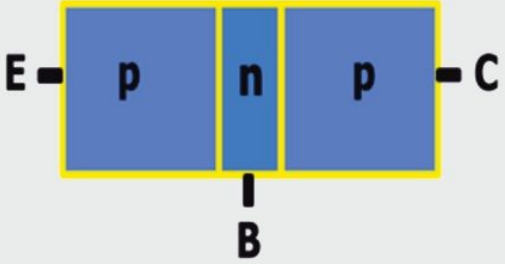
Ramani Kumar
P. Meena Priya Dharshini

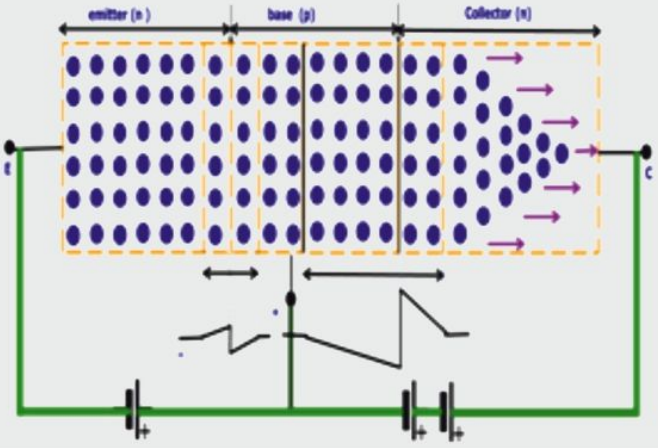
Basic Electronics

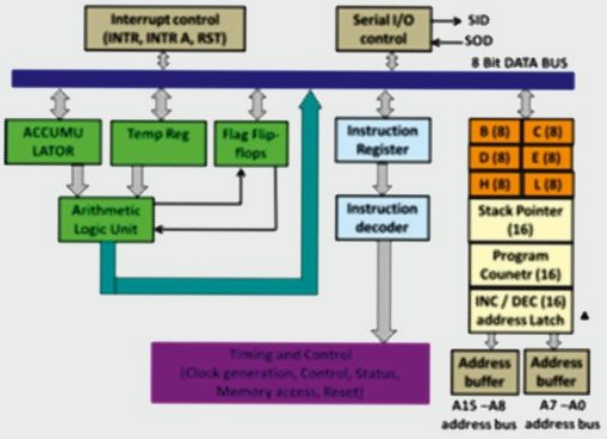
FIRST AND SECOND SEM
Visvesvaraya Technological University syllabus
(Effective from the Academic Year 2015-2016)











BASIC ELECTRONICS
Ramani Kumar | P. Meena Priya Dharshini

BASIC ELECTRONICS

As per VTU Syllabus - Effective from the academic year 2015 -2016
[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I and II Subject Code 15ELN15 / 15ELN25

V RAMANI KUMAR
(Retired Emeritus Professor)
AND
P. MEENA PRIYA DHARSHINI
(Associate Professor, CMR Institute of Technology Bangalore)

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About the book and the author……..

Why we wrote (write?) this book?
There are so many books on Basic electronics. Why one more?

I thought quite a lot about it.
I am from the Industry. I had worked in Telecom R&D for nearly 35 years (electronics, embedded and wireless).
I have been part of huge R&D teams of some of the best Telecom institutions of India

- DRDO Bangalore, Gujarat communications Baroda, Escorts Telecom Delhi, Solidaire Chennai, Telecom Technology Ltd Chennai (and Hong Kong), Tata Telecom Chennai, Bharti Telecom, Delhi and Premier Evolvics, Coimbatore

So what?

I had the fortune of working with hundreds of engineers everywhere …..fresh engineers straight out of the college. I had trained them in circuit designs, embedded designs and telcom/wireless system designs. I know the gap between the industry expectations and the academic objectives, better than many professionals or academicians.

I thought I am qualified enough to address this gap. I taught in Engineering colleges too and tried to bring an Industry perspective into every lecture of mine. The students as well as the faculty seemed to like this approach.
This encouraged(s) me to write a book on basic electronics
The approach is simple, bringing out the design issues at every opportunity, with an objective to make the student master the concepts. At the same time I have not lost sight of the precious objective – Marks in the examination……
Simple structured presentation of the syllabus, with plenty of illustrations, should help demystification of electronics.

I acknowledge the great support from Mrs P. Meena Priya Dharshini who brought in an academic perspective to this book. Her contribution has been immense and very vital.

I dedicate this book to

My wife **Karpagam** for her unstinted support in this journey.
Shri **N Sitaram** [(Director DRDO (Retired)]…… from whom, I learnt designs, designs and designs……

This text book follows ***the latest VTU syllabus verbatim effective from the academic year 2015 -2016 (As per Choice Based Credit System (CBCS) scheme)*** and is brought out in just 180 pages. I am sure, the student world will welcome this.

Browse my website eazyece.com frequently, for updates on this book and other topics…….

Good luck,

Ramani Kumar

Why I wrote this book?

I am Mrs P. Meena Priya Dharshini, an Associate professor, working in CMR Institute of Technology, Bangalore. I obtained my BE degree in EIE from Tamilnadu college of Engineering, Coimbatore and my ME degree in Applied Electronics from Bannari Amman Institute of Technology, Sathyamangalam. I have 10 years of teaching experience. My area of interest is Wireless Communication and Embedded System Design. I have published several papers in various national and international journals.

Basic Electronics is one of the important core subjects, in the field of Electronics, Telecommunication, Electrical, Computer Science, Information Science and Mechanical Engineering. There has been an increase in the demand for a suitable textbook on this subject. The content of the book are presented in a simple, precise and systematic manner. Numerous solved examples, self-explanatory sketches and a large number of problems with answers have been presented in each chapter to aid conceptual understanding of the subject. The language used in explaining the various concepts is extremely simple. All the topics have been profusely illustrated with diagrams for easy understanding.

Having been myself a teacher in the field of Electronics and Communication Engineering, I am sure that this book will enrich the students' knowledge in the subject and would be welcomed by the teachers and students of all engineering institutions.

I am highly indebted to Mr.Ramani Kumar, who encouraged me from time to time with his valuable suggestions and guidance in the preparation of the manuscript.

Meena Priya Dharshini

Syllabus:

BASIC ELECTRONICS

[As per Choice Based Credit System (CBCS) scheme] (Effective from the academic year 2015 -2016)

SEMESTER - I/II **Subject Code 15ELN15 / 15ELN25**

Course objectives:
The course objective is to make students of all the branches of Engineering to understand the efficacy of Electronic principles which are pervasive in engineering applications

Module -1

Semiconductor Diodes and Applications (Text-1): p-n junction diode, Characteristics and Parameters, Diode approximations, DC load line analysis, Half-wave rectifier, Two-diode Full-wave rectifier, Bridge rectifier, Capacitor filter circuit (only qualitative approch), Zener diode voltage regulators: Regulator circuit with no load,
Loaded Regulator. Numerical examples as applicable. (6 hours)

Bipolar Junction Transistors: BJT operation, BJT Voltages and Currents, BJT amplification, Common Base, Common Emitter and Common Collector Characteristics, Numerical examples as applicable. (4 hours)

Module -2

BJT Biasing (Text-1): DC Load line and Bias Point, Base Bias, Voltage divider Bias, Numerical examples as applicable. (04 Hours)

Introduction to Operational Amplifiers (Text-2): Ideal OPAMP, Inverting and Non Inverting OPAMP circuits, OPAMP applications: voltage follower, addition, subtraction, integration, differentiation; Numerical examples as applicable.
(06 Hours)

Module – 3

Digital Electronics (Text-2): Introduction, Switching and Logic Levels, Digital Waveform (Sections 9.1to 9.3). Number Systems: Decimal Number System, Binary Number System, Converting Decimal to Binary, Hexadecimal

Number System: Converting Binary to Hexadecimal, Hexadecimal to Binary, Converting Hexadecimal to Decimal, Converting Decimal to Hexadecimal, Octal Numbers: Binary to Octal Conversion. Complement of Binary Numbers.

Boolean Algebra Theorems, De Morgan's theorem.

Digital Circuits: Logic gates, NOT Gate, AND Gate, OR Gate, XOR Gate, NAND Gate, NOR Gate, X-NOR Gate. Algebraic Simplification, NAND and NOR Implementation (Sections 11.7 and 11.8): NAND Implementation, NOR Implementation. Half adder, Full adder.
(10 Hours)

Module-4

Flip-Flops (Text-2): Introduction to Flip-Flops (Section 12.1), NAND Gate Latch/ NOR Gate Latch, RS Flip-Flop, Gated Flip-Flops: Clocked RS Flip-Flop (Sections 12.3 to 12.5).
(05 Hours)

Microcontrollers (Ref.1): Introduction to Microcontrollers, 8051 Microcontroller Architecture and an example of Microcontroller based stepper motor control system (only Block Diagram approach).
(05 Hours)

Module-5

Communication Systems (Text-2): Introduction, Elements of Communication Systems, Modulation: Amplitude Modulation, Spectrum Power, AM Detection (Demodulation), Frequency and Phase Modulation. Amplitude and Frequency Modulation: A comparison.
(06 Hours)

Transducers (Text-2): Introduction, Passive Electrical Transducers, Resistive Transducers, Resistance Thermometers, Thermistor. Linear Variable Differential Transformer (LVDT). Active Electrical Transducers, Piezoelectric Transducer, Photoelectric Transducer.
(04 Hours)

Course outcomes:
After studying this course, students will be able to: ·
Appreciate the significance of electronics in different applications,

- Understand the applications of diode in rectifiers, filter circuits and wave shaping,
- Apply the concept of diode in rectifiers, filters circuits ·
- Design simple circuits like amplifiers (inverting and non inverting), comparators, adders, integrator and differentiator using OPAMPS, ·
- Compile the different building blocks in digital electronics using logic gates and implement simple logic function using basic universal gates, and
- Understand the functioning of a communication system, and different modulation technologies, and
- Understand the basic principles of different types of Transuducers.

Question paper pattern:

- The question paper will have ten questions.
- Each full Question consisting of 16 marks
- There will be 2 full questions(with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. David A. Bell, **"Electronic Devices and Circuits**", Oxford University Press, 5th Edition, 2008.
2. D.P. Kothari, I. J. Nagrath, **"Basic Electronics"**, McGraw Hill Education (India) Private Limited, 2014.

Reference Books: MuhammadAli Mazidi, **"The 8051 Microcontroller and Embedded. Systems. Using Assembly and C."** Second Edition, 2011, Pearson India.

Chapter 1: Semiconductor Theory

1.1 ATOM –Structure

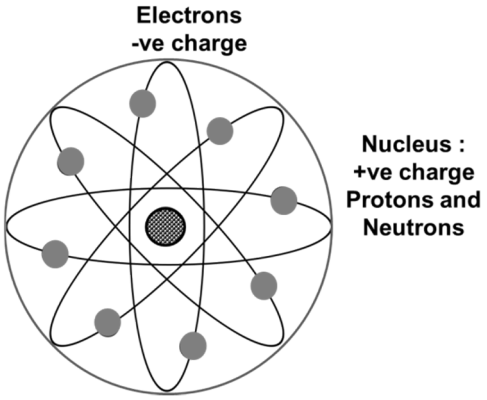


Fig 1.1 Atom - Structure

- Atom consists of a nucleus. Electrons in several orbits move around the **nucleus**..
- Contains three basic Particles –**Protons, Neutrons & electrons.**
- Nucleus contains two types of particles
  - **Protons :** Positively charged particles.
  - **Neutrons :** Particles with neutral charge.
- **Electrons:** Negatively charged particles (Charge = 1.602X 10^{-9} Coulombs).

Usually protons and electrons will be equal in number .Therefore, atoms are normally neutral, electrically.

- If an atom loses an electron, it means that it has lost some -ve charge & hence has a net + ve charge …….. and vice versa.

1.1.1 Holes & Electrons (Silicon & Germanium)

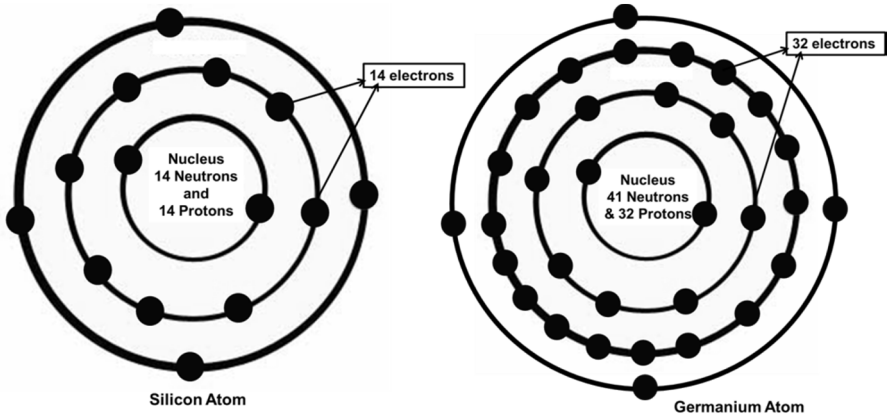


Fig 1.2

Pls recall,

1. Electrons can occupy only some fixed orbits, called **shells**.
2. Each shell can be occupied by only some **specific number of electrons**.
3. The outer most shell called **valence shell**, may be only partially filled by electrons.
4. Figure 1.2 gives a 2 D simplified orbital arrangement of silicon & germanium atom.
5. Absence of an electron in a shell, is defined as a **hole**.
6. Silicon & Germanium atoms are **electrically neutral (outer shell has 4 holes and 4 electrons each**)

1.2 Electron &Hole Dynamics

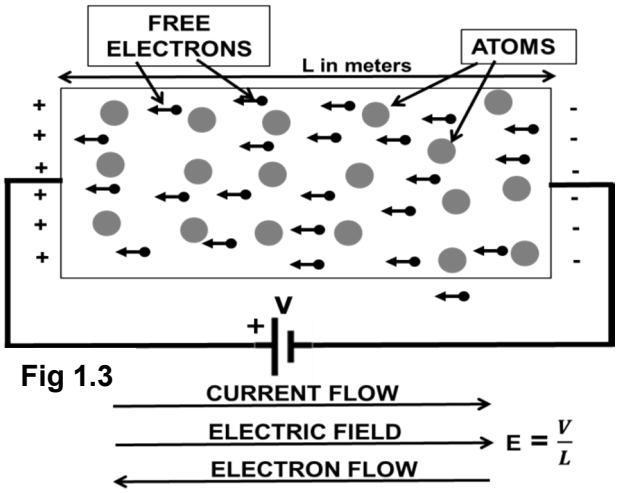


Fig 1.3

Refer fig 1.3.

- **Electrons** are –vely charged particles. Electrons are **repelled by –ve voltage**. Therefore, they will move towards a terminal **where + ve voltage is applied**.
- **Holes** are **+vely charged** particles. Holes are repelled by + ve voltage. They will move towards a terminal **where -ve Voltage is applied**.
- Please note the direction of the current flow is **always opposite** to the direction of electron flow.

1.3 N type & P type Semiconductors

1.3.1 Intrinsic semiconductor: It is very pure chemically. It has **equal numbers of** electrons (-ve) and holes (+ve). It has **poor conductivity.**

1.3.2 Extrinsic semiconductor:

- When a **small amount, of impurity is added** to a pure semiconductor, the conductivity of the semiconductor is increased manifold.
- Such materials are known as extrinsic semiconductors.
- The deliberate addition of a **desirable impurity**, is called **doping.**
- Doping yields two types of semiconductors viz p type and n type.
- The impurity atoms are called **dopants.**
- Such a material is also called a **doped semiconductor.**
- **Silicon & Germanium** are the standard semiconductor atoms, used by the industry.

Some of the popular dopants used, in doping the tetravalent Si or Ge are,

Trivalent atoms such as Boron or Aluminium, for producing p type semiconductors.

Pentavalent atoms such as Arsenic or Phosphorous, for producing n type semiconductors.

n type: Refer fig 1.4. **Pentavalent (5)** impurities like Arsenic (As), Antimony (Sb), Phosphorous (P), when added to either silicon or germanium, will produce N type semiconductors. **Electrons are the majority carriers**.

p type: Refer fig 1.5. **Trivalent (3)** impurities like Indium (In), Boron (B), Aluminium (Al) when added to either Silicon or Germanium, will produce P type semiconductors. **Holes are the majority carriers**.

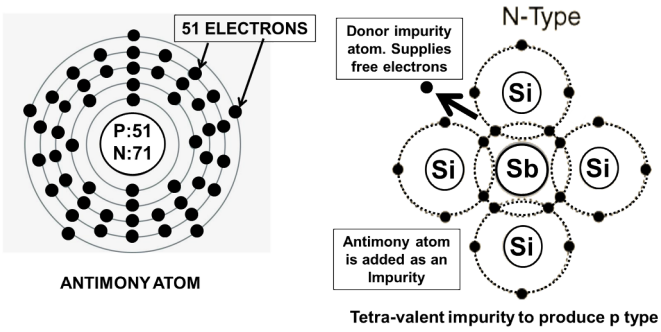


Fig 1.4 n-type pentavalent atom

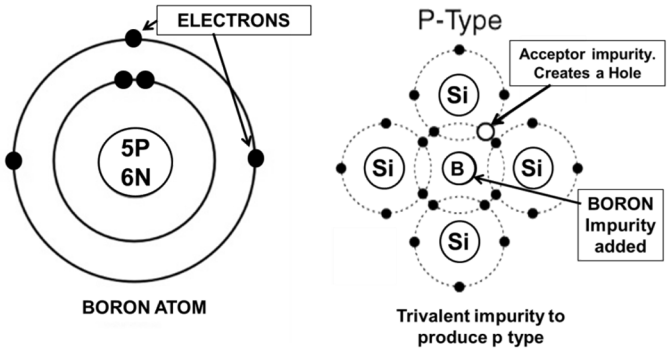


Fig 1.5 p-type trivalent atom

Majority and minority carriers

Majority carriers:

- The more abundant charge carriers
- Primarily responsible for current transport in a semiconductor.
- n-type semiconductors: Electrons
- p-type semiconductors: Holes.

Minority Carriers:

- The less abundant charge carriers
- n-type semiconductors: Holes
- p-type semiconductors: Electrons.

1.4 pn junction

Figure 1.6 shows independent p type independent n type semi-conductor.

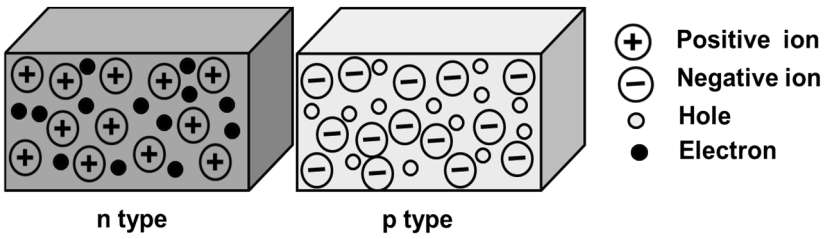


Fig 1.6 Semiconductor material n-type and p-type

Fig 1.7 shows a p type and n type conductor joined together (fabricated) to form a p-n junction

- There is no external voltage (bias) applied.
- Initially, pn junction is electrically neutral.

- **Majority carriers of n type are electrons.**
- **Majority carriers of p type are holes.**

1.4.1 Diffusion

Refer fig 1.7. Due to thermal agitation, electrons and holes start moving randomly, even if there is no bias. Look at the diffusion process below.

Few electrons close to the junction, start crossing the junction, to reach p side	Few holes close to the junction, start crossing the junction, to reach the n side

These electrons combine with some holes in the p side, to create some –ve ions.	These holes combine with electrons in the n side to create some +ve ions.
Due to these ions, a -ve voltage build up (barrier) is created, on the p side.	Due to these ions, a +ve voltage build up (barrier) is created on the n side.

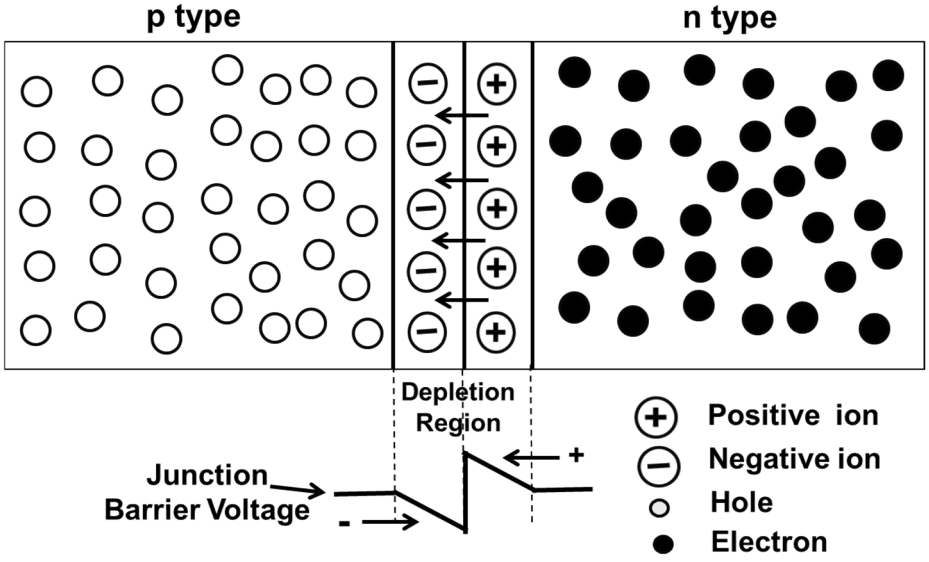
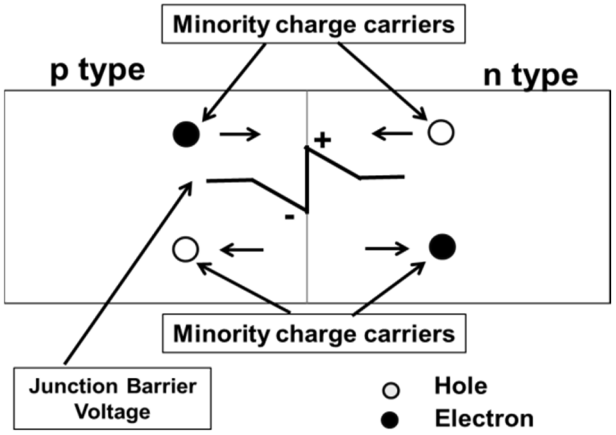


Fig 1.7 p-n junction diode – No bias voltage

This barrier voltage build up is shown in the figure 1.8.



- Barrier voltage is typically **0.7 V, for Silicon**.
- Barrier voltage is typically **0.3 V, for Germanium.**
- At around the barrier voltage, **electrons (from n side) are repelled by the – ve barrier voltage in the p side.**
- At around the barrier voltage**, holes (from p side) are repelled by the +ve barrier voltage in the n side.**
- Therefore further diffusion stops.

Fig 1.8 Barrier Voltage at p-n junction

1.4.2 Depletion region

- In the diffusion process mentioned above, **when the barrier potential is reached, further diffusion stops.**
- No charge carriers (electrons or holes) will be present, closer to the junction.
- Only ionized atoms (+ve and –ve), will be present on either side of the junction.
- This region is known as **depletion region**.

1.5 pn junction biasing

1.5.1 Reverse biased p-n junction

What is reverse bias?

Refer figure 1.9.

An external dc voltage (bias) is applied to a diode such that, p side is connected to the –ve terminal and n side is connected to the +ve terminal of a battery.

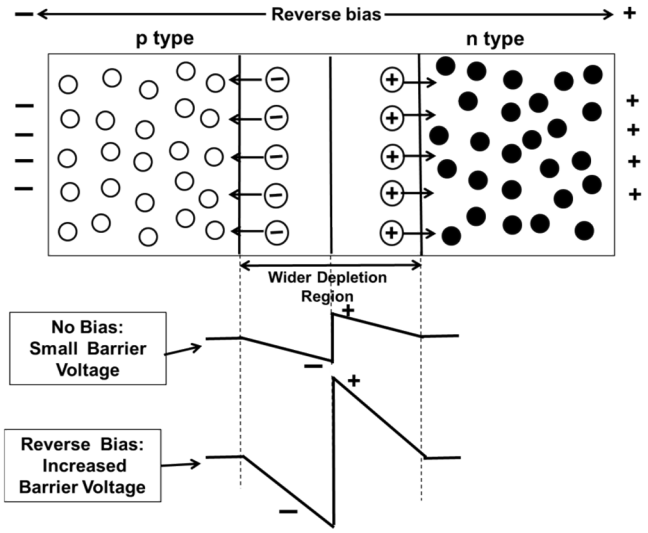


Fig 1.9 Reverse biased p-n junction

- This biasing arrangement increases the barrier voltage, as shown in the figure.
- Barrier voltage at n, becomes more +ve and the barrier voltage at p becomes more –ve.
- Electrons (majority carriers) in the n side, are repelled away from the junction and are attracted towards the +ve terminal.
- Holes (majority carriers) in the p side, are repelled away from the junction, and are attracted towards the –ve terminal.
- Consequently, depletion region further widens and barrier voltage increases as shown.

Result: Majority carriers cannot flow across junction and therefore, under reverse bias conditions, no current flow is possible. In other words, forward current does not flow.

1.5.2 Forward biased p-n junction

Refer figure 1.10.

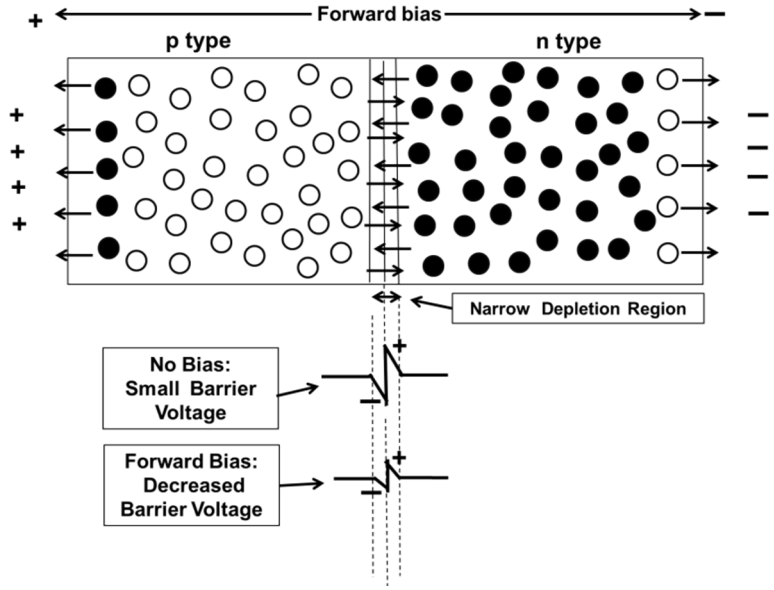
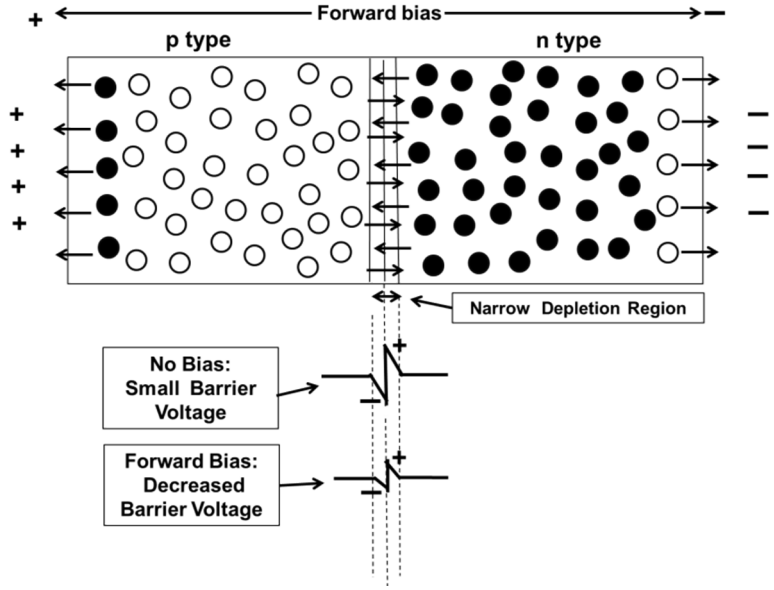


Fig 1.10 Forward biased p-n junction

What is forward bias?

An external dc voltage (bias) is applied to a diode such that **n side is connected to the – ve terminal and p side is connected to the +ve terminal of a battery.**

- This biasing arrangement decreases the barrier voltage, as shown in the figure 1.10.
- Barrier voltage at n, becomes less +ve and the barrier voltage at p becomes less –ve.
- Electrons (majority carriers) in the n side, are attracted across the junction, **towards the p side and are attracted towards the +ve terminal.**
- Holes (majority carriers) in the p side, are attracted across the junction, **towards the n side and are attracted towards the –ve terminal.**



- Consequently, depletion region decreases and the barrier voltage also reduces, as shown.

Result: Majority carriers will flow across junction and therefore, under positive bias conditions, current flow is possible. In other words, forward current flows.

Fig 1.10 Forward biased p-n junction

Chapter 2: Semiconductor Diodes and Applications

Syllabus: Semiconductor Diodes and Applications (Text-1) : p-n junction diode, Characteristics and Parameters, Diode approximations, DC load line analysis, Half-wave rectifier, Two-diode Full-wave rectifier, Bridge rectifier, Capacitor filter circuit, Zener diode voltage regulators: Regulator circuit with no load, Loaded Regulator, Numerical examples as applicable.

2.1 p-n junction diode

What is a diode?

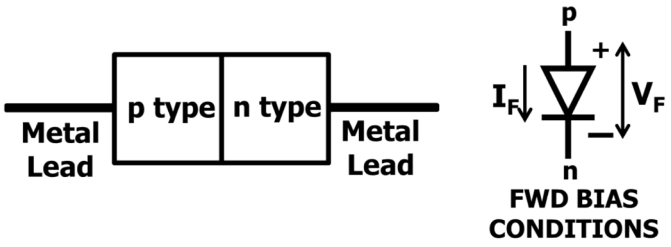


Fig 2.1 Semiconductor diode with leads

Draw the circuit symbol and indicate current flow.

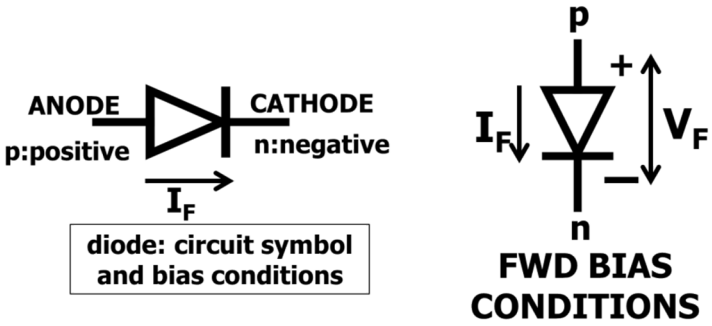


Fig 2.2

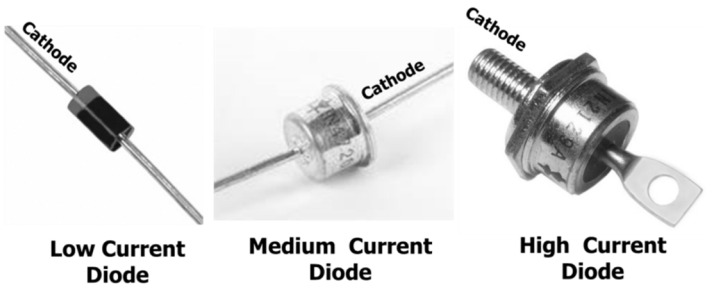


Fig 2.3

Refer fig 2.1 and 2.2

- It is a semiconductor device with a p-n Junction.
- It is a one way device.
- Allows current to flow when forward biased (p: + ve and n: - ve).
- Almost totally blocks current flow when reverse biased (p: - ve and n: +ve).
- Therefore, a diode is a 2 terminal component.
- It has two electrodes called anode and cathode.
- Anode is attached to p side and cathode to n side.

Diodes Power classification: Refer fig 2.3.

- **Low power diodes:** Usually small diodes can handle low currents up to 100mA. Power dissipation will be less than 800 milli-watts.
- **High power diodes:** Large diodes can handle high currents (1 to 10 Amperes). Power dissipation will be between 1 watt and 10 watts.
- Look at the table below

Diode size	Cathode Identification	Forward current (mA)	Reverse voltage (V)
Small-	Color band or dot	100	75
Medium	Diode Symbol	400	200
Large	Threaded portion	Few amperes	Few hundreds

2.2 Characteristics and parameters:

2.2.1 Diode characteristics: Refer fig 2.4 and 2.5

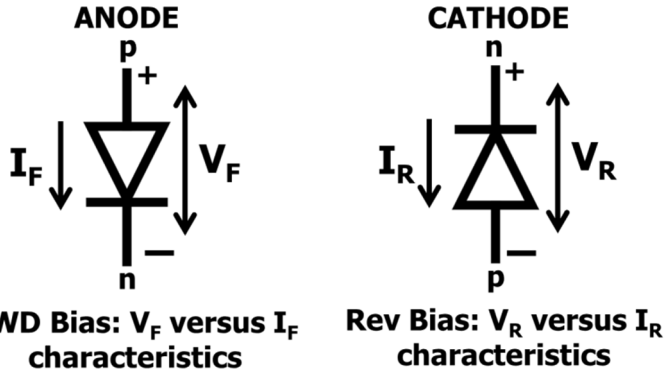


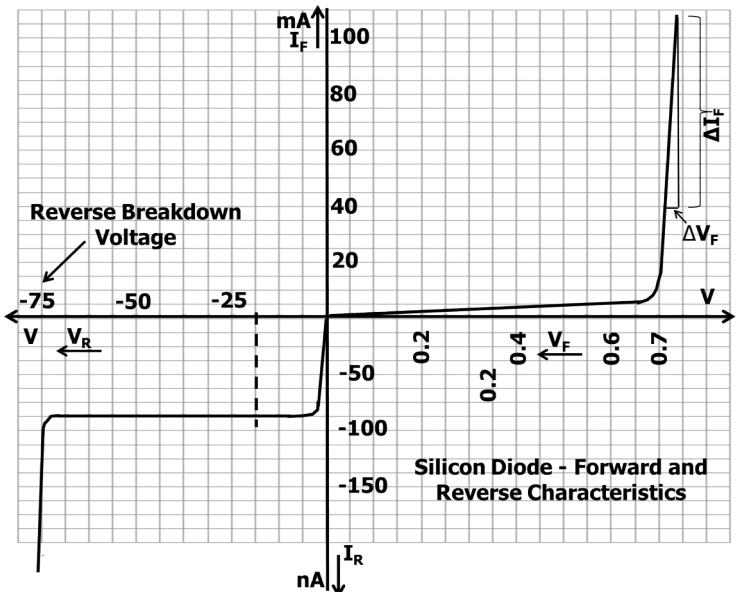
Fig 2.4

- It is the study of, 'voltage-across-the-diode' versus 'current- through-the-diode'.
- As we know, diode is a p-n junction semi-conductor device.
- When it is **forward biased**, diode characteristics is a **study of forward voltage V_F & forward current I_F.**
- When it is **reverse biased**, the diode characteristics is a study of reverse voltage **V_R & reverse current I_R.**

2.2.2 Forward characteristics (Silicon): Refer fig 2.5

Up to 0.7 V

- As the forward bias is increased from **0.1 to 0.7 V**, the diode hardly conducts the **forward current is very low** (less than 100 mA).



Beyond 0.7 V

- As the forward bias is increased **beyond 0.7 V**, the **forward current increases** very sharply.
- Increasing the **forward bias beyond say 1.0 V, will destroy a diode** due to excessive forward current.
- A **current limiting resistor is needed** in the circuit to protect the diode.

Fig 2.5 Silicon diode – Fwd and Rev characteristics

2.2.3 Reverse characteristics (Silicon)

0 to -50 V

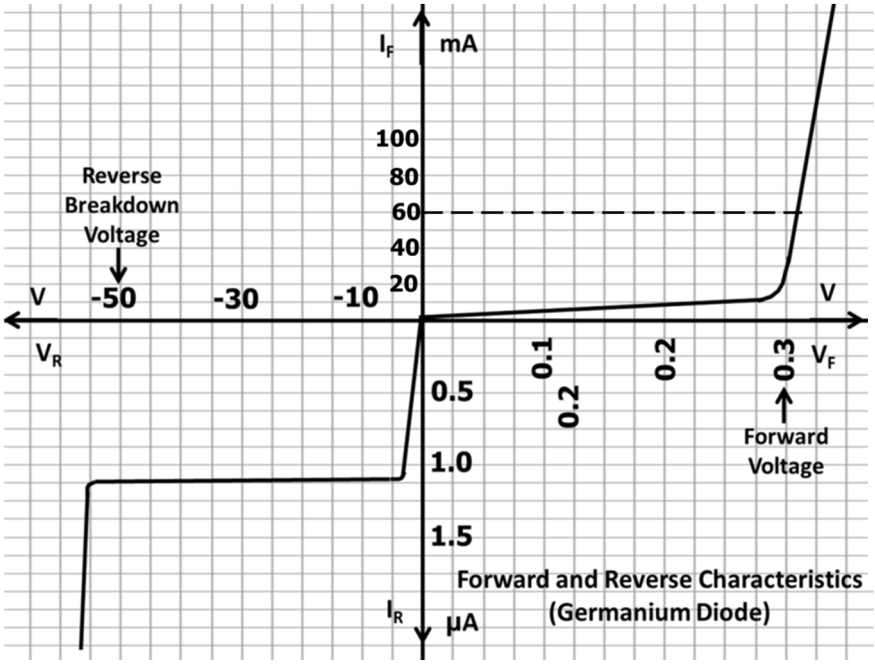
- Please **note the change of scale, in the y axis between forward & reverse characteristics**.
- **Reverse current I_R, is often very low** (not more than 1 μA) for reverse voltages up to -75 V for silicon
- **I_R is negligible compared to I_F.**

- For all practical purposes the diode behaves like an open circuit.

Beyond -75 V:

- **Reverse break down** happens (we shall study this later).
- The current **increases abruptly**.
- This **can destroy the diode**, unless protected by a **current limiting resistor**

2.2.4 Diode characteristics (germanium)

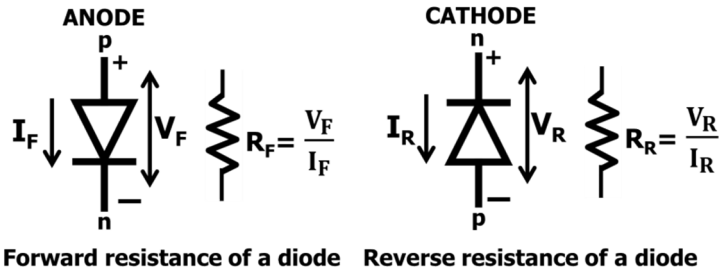


Refer fig 2.6.

- The characteristics are similar to that of silicon diode.
- Forward voltage is 0.3 V instead of 0.7 V.
- Reverse break down voltage is -50 V instead of -75 V.
- Reverse current is -1.0 μA instead of -100 nA.

Fig 2.6 Germanium diode – Fwd and Rev characteristics

2.2.5 Forward & Reverse resistance : Refer fig 2.7



Forward resistance of a diode Reverse resistance of a diode

Fig 2.7

Problem 2.1: In fig 2.6, calculate the forward resistance of the germanium diode, at I_F= 60mA

At I_F = 60 mA, V_F = 0.33 V (approx)

Therefore, forward resistance

$$(R_F) = \frac{V_F}{I_F} = \frac{0.33\ V}{60\ mA} = 5.5 \text{ ohms.}$$

Problem 2.2: In fig 2.5, calculate the reverse resistance of the silicon diode at V_R =20V.

At V_R = 20 V, I_R = 90 nA (approx)

Therefore, reverse resistance (R_R) $= \frac{V_R}{I_R} = \frac{20\ V}{90\ nA}$ = 222 Mega ohms (approx)

2.2.6 Some of the important diode parameters.

V_F - Forward voltage drop (0.3 V for Ge and 0.7 V for silicon).

I_F - Forward current .

V_R - Reverse voltage.

r_d - Dynamic resistance = $\frac{\Delta V_F}{\Delta I_F}$

V_{BR} - Break down voltage {50 V for Ge and 75 V for Si).

P_D - Power dissipation.

2.2.7 Dynamic resistance r_d

Recall the forward resistance that was calculated in problem 2.1. $\mathbf{R_F = \frac{V_F}{I_F}}$**.** This is the **DC resistance** of the diode, at one particular value of forward current. When the input varies by ΔV_F, there will be large variation, in forward current (ΔI_F). This is shown in fig 2.5

Dynamic resistance $\mathbf{r_d = \frac{\Delta V_F}{\Delta I_F}}$. r_d is also known as ac resistance or incremental resistance

There is another way of calculating dynamic resistance. It is not discussed here since it is beyond the scope of this book.The formula is $\mathbf{r_d = \frac{26\ mV}{I_F}}$

Problem 2.3: What is the dynamic resistance of a diode with a forward current of 5 mA

$\mathbf{r_d = \frac{26\ mV}{5\ mA}}$ = 5.2 Ω.

Problem 2.4: For the dynamic characteristic shown in fig 2.8, determine the dynamic resistance at 40 mA.

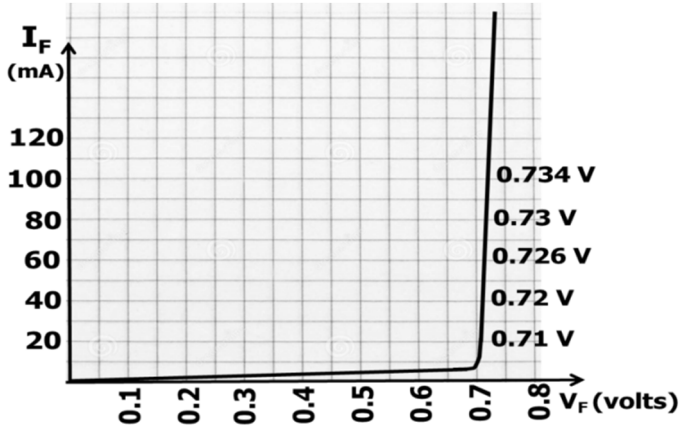


Fig 2.8

I_F = 40 mA.

Therefore, take a small interval around 40 mA as ΔI_F, say from 20 mA to 60 mA.

ΔV_F for this range = 0.726 V - 0.71 V = 0.016 V

ΔI_F for this range = 60 mA - 20 mA = 40 mA

$\therefore r_d = \frac{\Delta V_F}{\Delta I_F}, = \frac{0.016V}{16\ mV}$ = 0.4 Ω

2.3 Diode approximations:

2.3.1 Ideal Diode:

Refer fig 2.9 a

In the forward bias condition

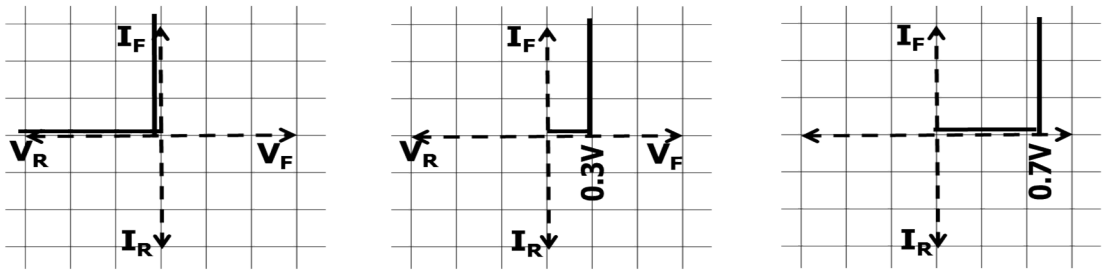
It will have no forward resistance and will not drop any voltage across it. **R_F = 0 Ω and V_F = 0 V.**

In the reverse bias condition, an ideal diode will never have any reverse current, no matter what the reverse voltage is. **$V_R = \infty$, $I_R = 0$**

Therefore, what is an ideal diode?

1. Fwd Resistance = 0 Ohm
2. Fwd Voltage drop = 0 V
3. Rev resistance = Infinity
4. Rev current = 0 amp

Refer fig 2.9 b and 2.9 c
However, in practice, it is different as seen already in figures 2.5 and 2.6.



Ideal Diode Characteristics
VF = 0 V, IR = 0 mA

Germanium Diode Characteristics
VF = 0.3 V

Silicon Diode Characteristics
VF = 0.7 V

(a) **(b)** **(c)**

Fig 2.9 Diode Characteristics

What are the assumptions of a near ideal diode (Si)?
Fwd Voltage drop = constant
Rev current = negligible (can be ignored)

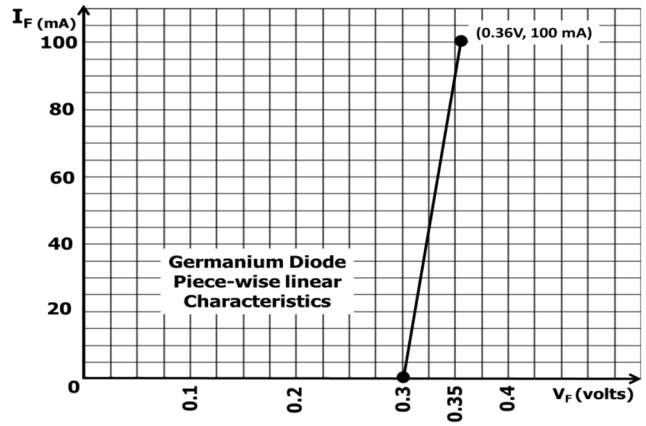
2.3.2 Practical diode

What is a practical diode (Si)?
Fwd Resistance = 0 to 20 Ohms
Fwd Voltage drop = 0.6 to 1.0 Volt
Rev current = few micro amps

2.3.3 Piece-wise approximation of a diode

The smooth diode curve of fig 2.5 or 2.6 can be approximated by taking samples at very close intervals and interconnecting adjacent samples through short straight lines.

Problem 2.5: Construct a piece wise linear characteristics of a germanium diode, given that its dynamic resistance is 0.6 Ω and forward current is 100 mA .
Look at fig 2.10



It is a Ge diode. V_F = 0.3 V
Mark Point A = (0.3 V, 0 mA)
How to find B?

ΔI_F = 100 mA – 0 mA = 100 mA
ΔV_F = ΔI_F X r_d
= 100 mA X 0.6 Ω = 60 mV.
= 0.06 V
Point B = {(0.3 V + 0.06 V), 100 mA)}
= **{(0.36 V, 100 mA)}**

Fig 2.10

Join A B. The piece wise linear characteristic is the thick line segment shown.

2.3.4 DC equivalent circuits of a diode

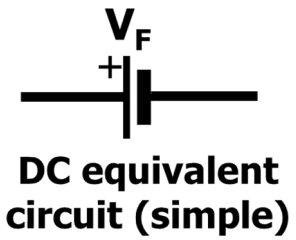


Fig 2.11

What is an equivalent circuit?
The electrical behaviour of the given circuit is accurately modelled using a combination of, simple electrical components such as Resistor (R), Inductor (L) and Capacitor (C).

Why equivalent circuit?
Equivalent circuit simplifies analysis of a complex circuit.

Some equivalent circuits of diodes are shown in fig 2.11 and 2.12. Eqvt circuit of an ideal diode is shown in Fig 2.12 (a) . In fig 2.12 (b) a practical diode with specific voltage drop V_F =0.7 V (Si) or 0.3 V (Ge) is shown. Has a constant V_F and negligible DC resistance (Zero)

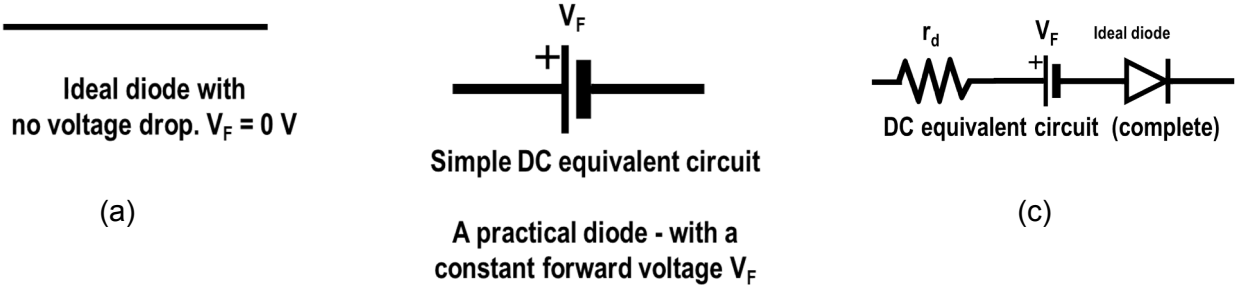


Fig 2.12 Diode Equivalent circuits

In fig 2.11(c), a more complete equivalent circuit, with a specific V_F and a specific r_d is shown. r_d represents the ΔV_F part.

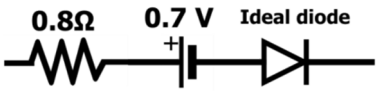


Fig 2.13

Problem 2.6: For the fig 2.13, what will be the drop across the silicon diode, if I_F = I0 mA and dynamic resistance is 0.8 Ω.

Ideal diode. $\therefore V_F$ = 0.7 V (Silicon, by default), I_F = 10 mA (given)

Drop across r_d = I_F X r_d = 10 mA X 0.8 Ω = 8 mV.

$\therefore$ Total drop across the diode = 0.7 V + 8 mV. = 0.708 V.

Problem 2.6: In the circuit shown in fig 2.14, calculate I_F . **(Unless otherwise mentioned, the diode is silicon by default.**

E = I_F.R + V_F

10 V = (I_F X 2.2K) + 0.7 V

$\therefore$ I_F = $\frac{10\text{ V} - 0.7\text{ V}}{2.2\text{ K}}$ = 4.22 mA.

Problem 2.7: For the same circuit in fig 2.14, what is the new I_F if the diode has a dynamic resistance of 0.3 Ω and R = 5 Ω .
The circuit is redrawn in fig 2.15.

$\mathbf{E = I_F.R + I_F.r_d + V_F}$

10 V = (I_F X 5 Ω) + (I_F X 0.3 Ω) + 0.7 V

$\mathbf{I_F = \frac{E - V_F}{R + r_d}} = \frac{10\text{ V} - 0.7\text{ V}}{5\ \Omega\ + 0.3\ \Omega}$ = 9.3 V / 5.3 Ω = 1.76 A

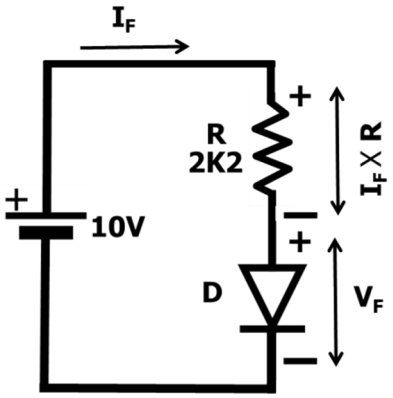


Fig 2.14

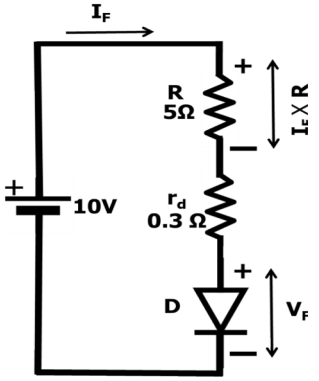


Fig 2.15

2.4 D C load line analysis (Diodes)

This topic mainly revolves around three subtopics
a) DC Load line
b) Diode V-I Characteristics
c) Q point.

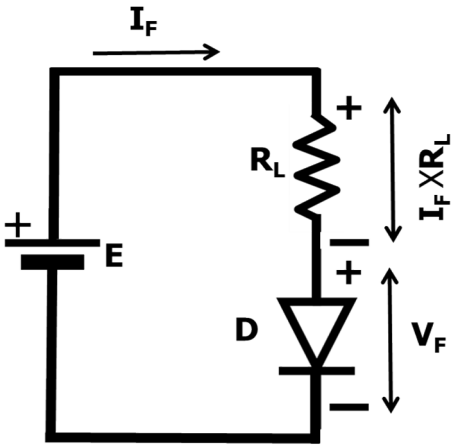


Fig 2.16

2.4.1 How to draw a DC Load line? Refer fig 2.16

As per Kirchoff's Law,

$\mathbf{E - (I_F\ X\ R_L) - V_F} = 0$

$E - V_F = I_F\ X\ R_L$

$\mathbf{\frac{E}{R_L} - \frac{V_F}{R_L} = I_F}$

$\therefore I_F = V_F \left(\frac{-1}{R_L}\right) + \frac{E}{R_L}$

$\frac{E}{R_L}$ for a given circuit, is a constant.(say C)

$\therefore I_F = V_F \left(\frac{-1}{R_L}\right) + C$

This is of the form y = mx + c (Straight line equation).where slope $\mathbf{m = -\frac{1}{R_L}}$

The variables are the **DC conditions, I_F and V_F. Hence the name, DC load line.**

Problem 2.8: Let us draw a DC load line for the ckt in fig 2.16 where E = 6 V and R_L = 150 Ω

$\mathbf{E = (I_F\ X\ R_L) + V_F}$

6 V = 150 I_F + V_F

(A) If I_F = 0, Then V_F = 6 V. For a diode,

V_F = 6 V is of course absurd but a DC

load line does not take the device characteristics into account

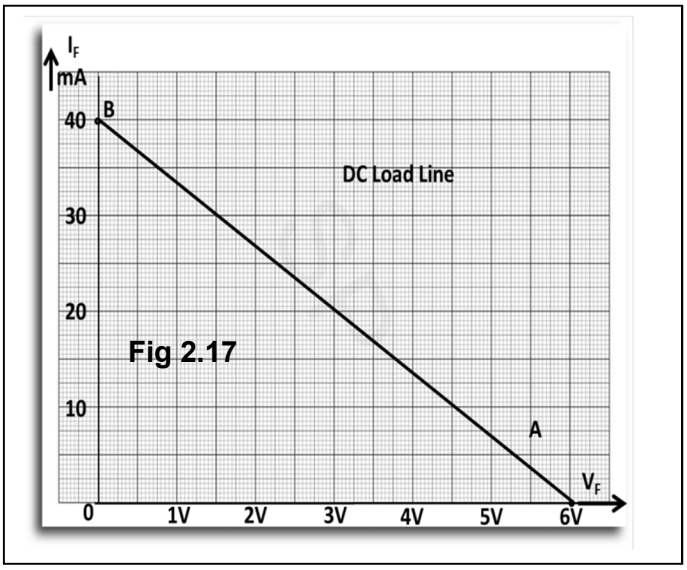
∴ **Point A = (6 V, 0 mA)**

(B) If V_F = 0, Then $I_F = \frac{6V}{150\ \Omega}$ = 40 mA.

∴**Point B =(0 V, 40 mA)**

Draw a graph using the above values.

- A has coordinates V_F = 6 V , I_F = 0 mA.
- B has coordinates V_F = 0 V , I_F = 40 mA.
- Join AB as a Straight line.
- This is the load line.
- Note, slope of this load line = **m =** $-\frac{1}{R_L}$



2.4.2 Diode VI characteristics

This is the same curve in fig 2.5 and 2.6. Diode VI characteristic is the forward bias region (first quadrant). This curve is super- imposed on the D C load line drawn above.

2.4.3 Q point (Quiescent point, DC bias point) – Refer fig 2.18

This is the point of intersection of DC load line and the diode V-I characteristics.

Problem 2.9: The Q point is (0.7 V , 35.3 mA). How?

For a silicon diode, V_F = 0.7 V.

Recall from fig 2.16,

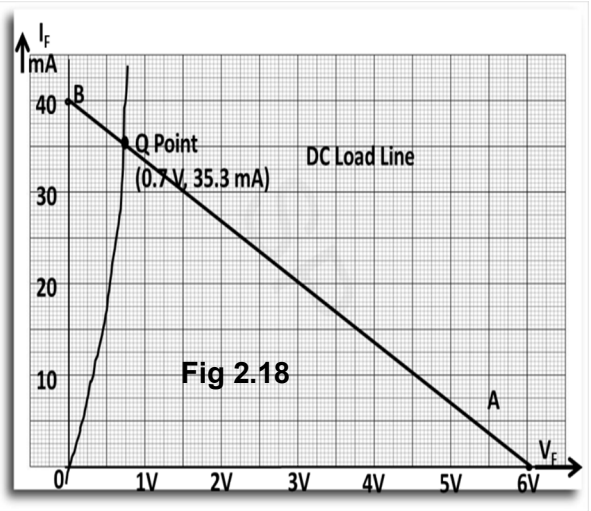
6 V = 150 I_F + V_F

6 V = 150 I_F + 0.7 V

5.3 V = 150 I_F

I_F = 35.3 mA

∴ **Q point is (0.7 V , 35.3 mA).**



For the given circuit this Q point is fixed

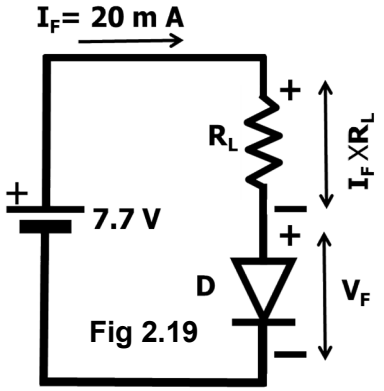
Conclusion:

(1) For a given V_F and I_F, the Q point is unique.

(2) V_F for diodes is generally constant (0.7 V for Si and 0.3V for Ge)

(3) Therefore, for altering the Q point I_F should be changed

(4) I_F can be changed by either changing Input voltage E or R_L



Problem 2.10: Find the load resistance for this circuit in fig 2.19, for I_F = 20 mA

1) Draw Load line
$V_F = E - I_F R_L$
a) For $I_F = 0$, $V_F = E = 7.7$ V.
∴ **Plot A at (7.7 V , 0 mA)**

b) Next, plot Q (Inter-section of diode characteristics and I_F = 20 mA line)

c) Join AQ and extend it to B. You will find B intersecting Y axis at I_F = 22 mA

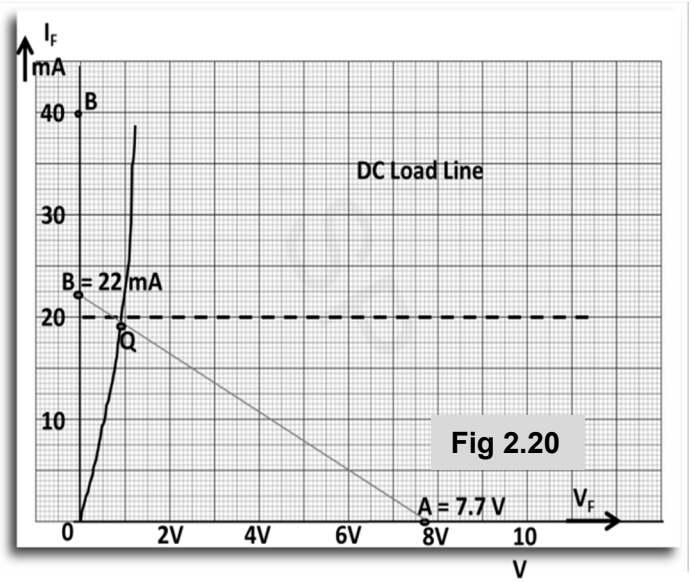


Fig 2.20

Why? Let us find I_F through circuit analysis

Problem 2.11: What is R_L from the load line?
We know that $V_F = E - I_F R_L$
ΔV_F = 7.7 V - 0.7 V = 7.0 V.
ΔI_F = 20 mA – 0 mA = 20 mA.
$R_L = \frac{\Delta V_F}{\Delta I_F} = \frac{7V}{20\ mA}$ = 350 ohms

Using the equation $\mathbf{V_F = E - I_F R_L}$
When $V_F = 0$, $E = I_F R_L$
$7.7\ V = I_F \times 350\ \Omega$
$\therefore I_F = 7.7\ V / 350\ \Omega = 22$ mA.

2.4.4 Diode Parameters

1. I_F (max) - Maximum forward DC current permissible
2. V_F - Forward voltage drop (0.7 V for Si and 0.3 V for Ge)
3. V_{BR} - Maximum reverse voltage that can be applied, beyond which break down occurs
4. r_d - Dynamic resistance
5. I_R - Reverse saturation current (current flow when diode is reverse biased)
6. Knee voltage - that forward voltage beyond which, forward current increases exponentially
7. P - continuous maximum power dissipation permissible at 25 deg C

2.5 Rectifiers

Define ''Rectifier''

Rectifier is a device such as diode, **that converts alternating current to direct current (ac to dc)**.

How is diode rectification done?

The rectification is done, by converting ac current to dc current, by suppression or inversion of alternate half cycles of the input.

2.5.1 Half wave rectifier (HWR):

Look at figure 2.21. A simple half wave rectifier is shown.

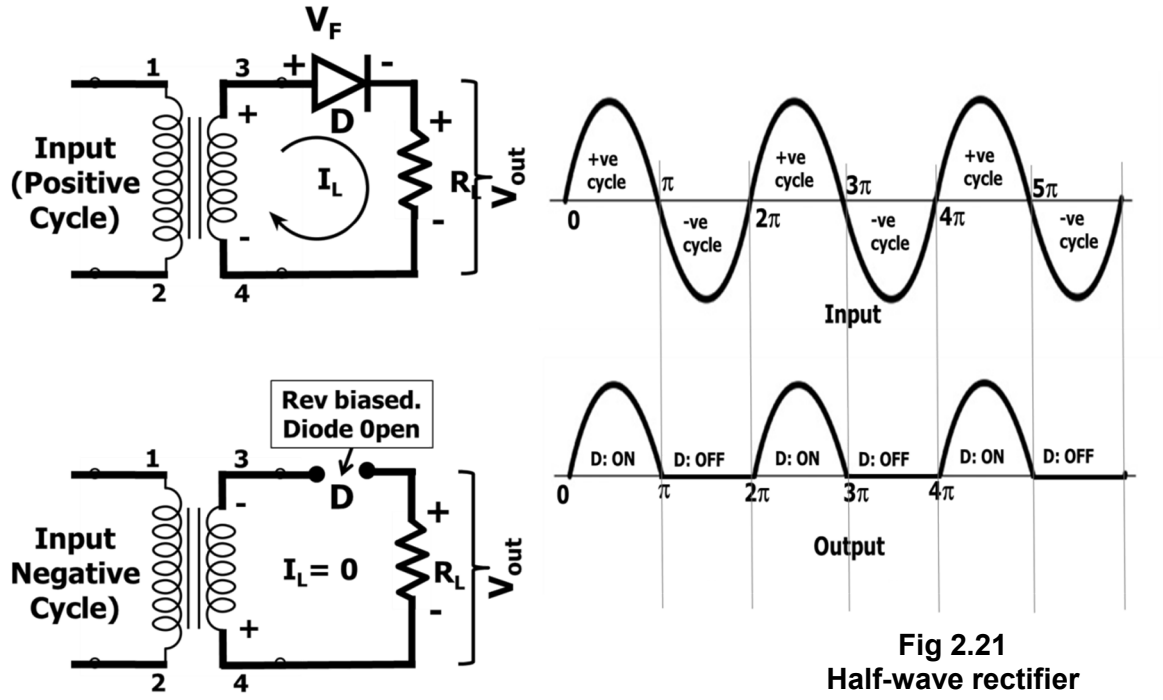


Fig 2.21
Half-wave rectifier

HWR Operation

Refer fig 2.21

- The input is fed through a transformer primary (terminals 1 and 2.).
- During +ve cycle of input, terminal 3 is +ve and terminal 4 is –ve.
- Diode gets forward biased and the current flow is clock wise, as shown in fig.
- Output voltage is I_L R_L.
- During – ve cycle of input # 4 is +ve and # 3 is –ve. Diode is reverse biased and diode behaves like an open circuit, as shown. No current flows in the circuit.
- The output voltage is zero. The peak inverse voltage across diode is, the input voltage (peak value).
- The Wave forms are shown in fig 2.21

Problem 2.12: For the circuit shown, determine the peak output voltage, peak load current and diode peak inverse voltage. The ac input is 10V, the load resistance is 1 kΩ and the diode is germanium.

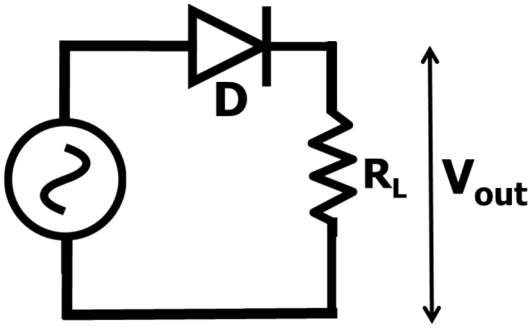


Fig 2.22

Important : Unless otherwise mentioned, the input is always specified as rms.

The relation between peak value & rms value is $V_{rms} = V_{peak} / \sqrt{2}$ and $I_{rms} = I_{peak} / \sqrt{2}$ and so on.

Input voltage is 10 V rms.

Input peak voltage: $V_{p\,in} = \sqrt{2}$ X 10 V = 14.14 V

Output peak voltage: $V_{p\,out} = V_{p\,in} - V_F$

$= 14.14 - 0.3$ V = 13.84 V.

Peak load current = 13.84 V / 1 KΩ = 13.84 mA.

Peak inverse voltage = PIV = $V_{p\,in}$ =14.14 V.

2.5.2 Full wave rectifier (FWR):

-
- As the name implies **rectification happens, for both +ve and –ve cycles of the input** wave. Full wave rectifier, therefore, **uses 2 diodes.**
- A transformer input full wave rectifier (FWR) is shown in fig 2.23. The transformer becomes complex, with a centre-tap operation.

FWR Center tap transformer:

Look at fig 2.23.

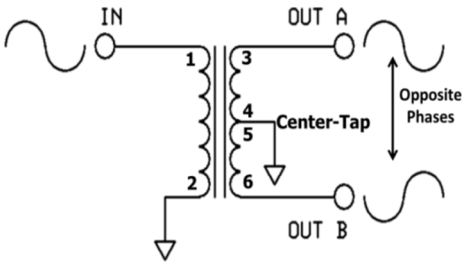


Fig 2.23 Center-tap transformer

It consists of a primary winding (1,2) and two secondary windings (3,4 and 5,6)

One end of, each of these secondary windings, is joined together. **In the figure 4 and 5 are joined.**

The windings normally have the same number of turns and therefore the 4, 5 junction becomes truly **a center tap.**

The sense of these two secondary windings is in such a way, that the **two secondary outputs always oppose each other, in phase.**

FWR Operation:

A full wave rectifier using two diodes is shown in fig 2.24.

NOTE center tap is at ground (0V) potential.

Note, diode cathodes are returned to ground through the load resistor R_L

Input: + ve half cycle (Refer fig 2.25)

- Terminal 3 is +ve, with respect to ground (center tap) and D1 is forward biased.
- Terminal 6 is –ve, with respect to ground (center tap) and D2 is reverse biased.
- Current flows in the Dl loop as shown. (I_{L1})
- Resultant output ($V_{out\ 1}$) is a +ve half cycle (Same phase as input).

Input: - ve half cycle (Refer fig 2.26)

- Terminal 6 is +ve, with respect to ground (center tap) and D2 is forward biased.
- Terminal 3 is –ve, with respect to ground (center tap) and D1 is reverse biased.
- Current flows in the D2 loop as shown. (I_{L2})
- Resultant output ($V_{out\ 2}$) is a +ve half cycle (Inverted with respect to input).
- The load current flows through R_L in the same direction (right to left) whether the input is a +ve half cycle or –ve half cycle. The load current is, the sum of the individual diode currents.
- Waveforms are shown in fig 2.27.

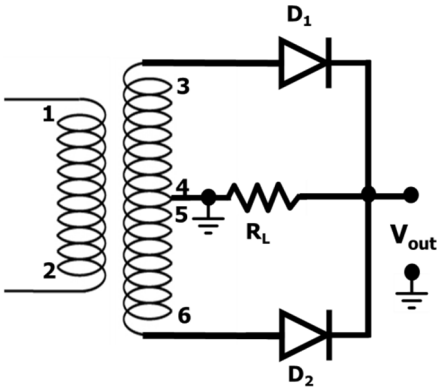


Fig 2.24 Full-wave rectifier Circuit (Two diodes)

2.5.2.3 Transformer related parameters

Let input voltage be $V_p = V_{pm}$ sin wt.

Let wt = α

$\therefore V_p = V_{pm}$ sin α (primary)

$V_s = V_{sm}$ sin α.

If the transformer has a turns ratio

$\mathbf{N_p : N_s}$, then $\frac{N_S}{N_P} = \frac{V_{sm}}{V_{pm}}$

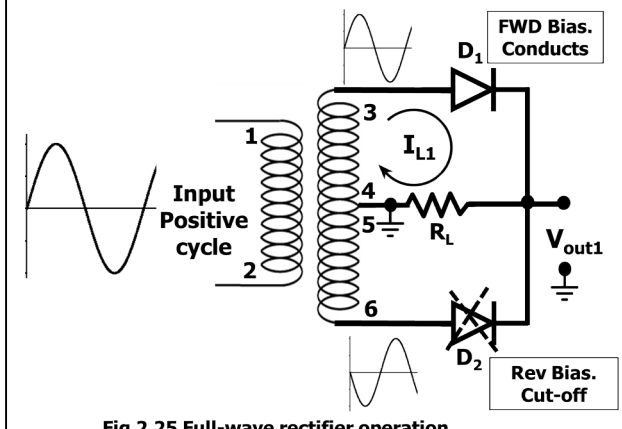


Fig 2.25 Full-wave rectifier operation

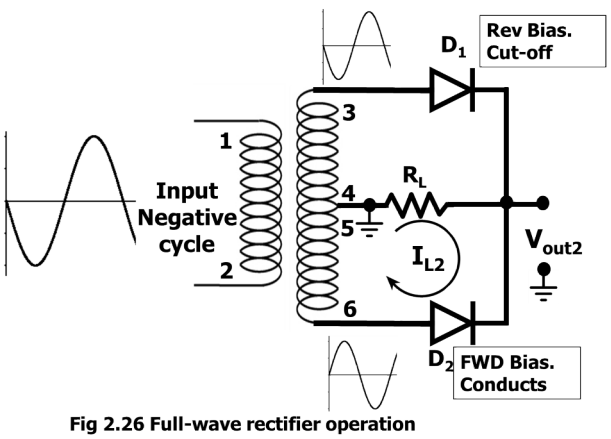


Fig 2.26 Full-wave rectifier operation

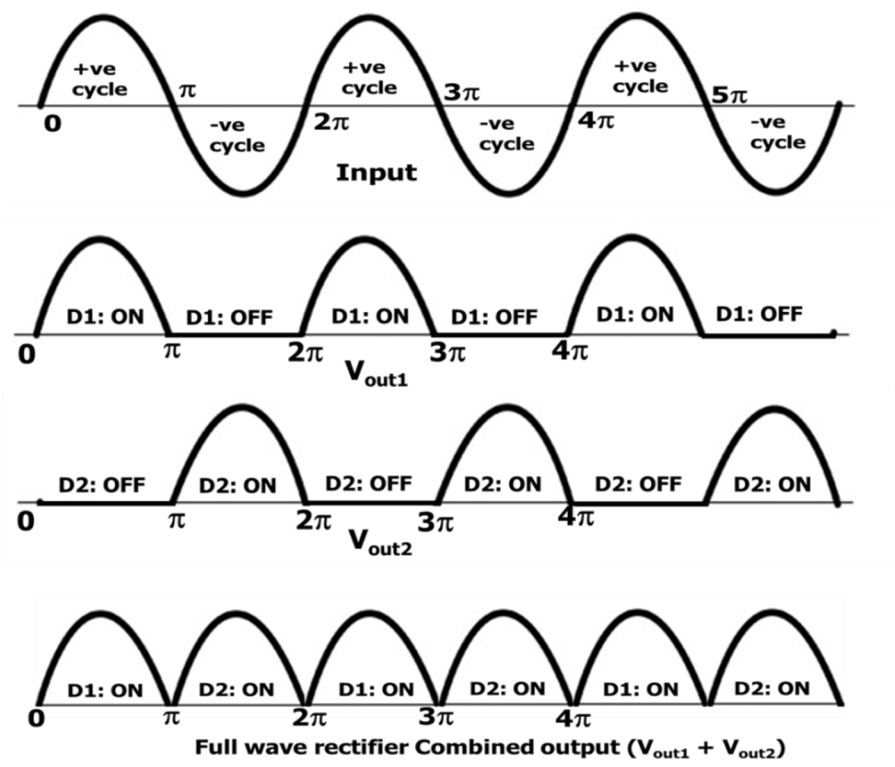


Fig 2.27 Full-wave rectifier waveforms

Transformer secondary resistance: The winding resistance R_s of transformer secondary, often comes into play, during current power calculations. .

Problem 2.13: If the transformer in the previous example is used, what is the peak secondary current in this circuit in fig 2.28? Assume secondary has a resistance of 5 ohms.

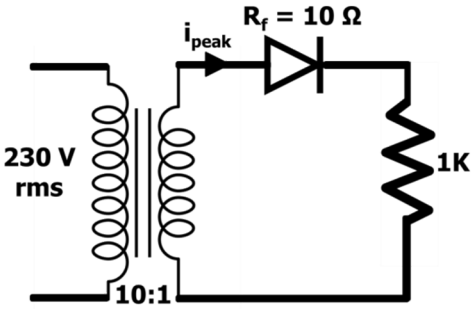


Fig 2.28

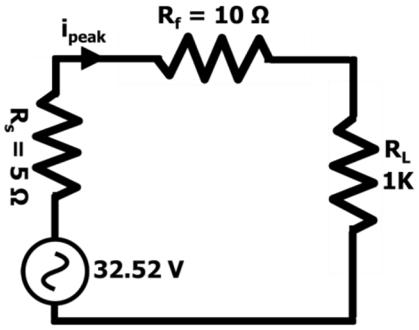


Fig 2.29

Secondary peak voltage = 32.52 V. (previous example) . Refer equivalent circuit in fig 2.29.

Look at secondary equivalent circuit $\mathbf{i_m} = \frac{V_S}{R_S + R_f + R_L}$

i_{peak} (secondary) $= \frac{32.52\ V}{5\Omega + 10\Omega + 1000\Omega}$

= 32 .52 V / 1015 ohms = 32.04mA

-

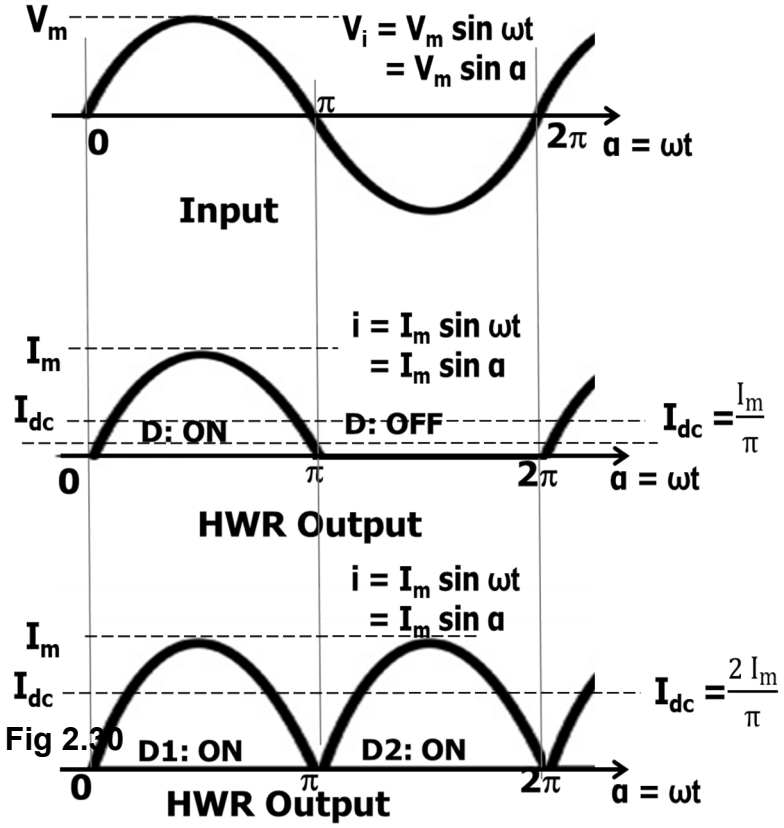


Fig 2.30

Fig 2.30 Rectifier equations

2.5.3 RECTIFIERS EQUATIONS (Refer fig 2.30)

Half wave	Full wave
DC Current I_{dc} $I_{dc} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin\alpha\, d\alpha$ $= \frac{I_m}{2\pi}[-\cos\alpha]_0^{\pi}$ $= \frac{-I_m}{2\pi}[-1-1]$ $I_{dc} = \frac{I_m}{\pi}$ $I_{dc} = \frac{V_m}{\pi\,(R_f + R_L + R_S)}$	DC Current I_{dc} $I_{dc} = \frac{1}{\pi}\int_0^{\pi} I_m \sin\alpha\, d\alpha$ $= \frac{I_m}{\pi}[-\cos\alpha]_0^{\pi}$ $= \frac{-I_m}{\pi}[-1-1]$ $I_{dc} = \frac{2I_m}{\pi}$ $I_{dc} = \frac{2V_m}{\pi\,(R_f + R_L + R_S)}$
DC output Voltage V_{dc} $V_{dc} = I_{dc}R_L = \frac{I_M}{\pi}R_L$ $= \frac{V_M}{\pi\left(1 + \frac{R_f}{R_L}\right)}(\text{Assume } R_S = 0)$	DC output Voltage V_{dc} $V_{dc} = I_{dc}R_L = \frac{2I_M}{\pi}R_L$ $= \frac{2V_M}{\pi\left(1 + \frac{R_f}{R_L}\right)}(\text{Assume } R_S = 0)$
RMS current I	RMS current I

$I = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2 d\alpha}$ $I = \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_m{}^2 \sin^2\alpha\, d\alpha} \quad I = \frac{I_m}{2}$	$I = \sqrt{\frac{1}{\pi}\int_0^{\pi} i^2 d\alpha}$ $I = \sqrt{\frac{1}{\pi}\int_0^{\pi} I_m{}^2 \sin^2\alpha\, d\alpha} \quad I = \frac{I_M}{\sqrt{2}}$
RMS output voltage across load $V_{rms} = I \times R_L = \frac{I_m}{2} \times R_L$ $V_{out} = \frac{V_M}{2\left(1 + \frac{R_f}{R_L}\right)}$	RMS output voltage across load $V_{rms} = I \times R_L = \frac{I_M}{\sqrt{2}} \times R_L$ $V_{out} = \frac{V_M}{\sqrt{2}\left(1 + \frac{R_f}{R_L}\right)}$
DC Output Power $P_{dc} = I_{dc}{}^2 R_L = \frac{I_m{}^2 R_L}{\pi^2}$ $= \frac{V_m{}^2 R_L}{\pi^2 (R_L + R_f)^2}$	DC Output Power $P_{dc} = I_{dc}{}^2 R_L = \frac{4 I_m{}^2 R_L}{\pi^2}$ $= \frac{4 V_m{}^2 R_L}{\pi^2 (R_L + R_f)^2}$
Total AC Input Power $P_{Diode} = I^2 R_f = \frac{I_m{}^2}{4} R_f$ $P_{RL} = I^2 R_L = \frac{I_m{}^2}{4} R_L$ $P_{in} = P_{Diode} + P_{R_L}$ $= \frac{I_m{}^2}{4}(R_f + R_L)$	Total AC Input Power $P_{Diode} = I^2 R_f = \frac{I_m{}^2}{2} R_f$ $P_{RL} = I^2 R_L = \frac{I_m{}^2}{2} R_L$ $P_{in} = P_{Diode} + P_{R_L}$ $= \frac{I_m{}^2}{2}(R_f + R_L)$
Rectifier efficiency $N = \frac{P_{dc}}{P_{in}} = \frac{\left(\frac{I_m{}^2}{\pi^2} \times R_L\right)}{\left[\frac{I_m{}^2}{4}(R_f + R_L)\right]}$ $= \frac{4}{\pi^2} \frac{R_L}{R_f + R_L}$ $= \frac{0.406}{1 + \left(R_f / R_L\right)}$ $= \frac{40.6}{1 + \left(R_f / R_L\right)}$	Rectifier efficiency $N = \frac{P_{dc}}{P_{in}} = \frac{\left(\frac{4 I_m{}^2 R_L}{\pi^2}\right)}{\left[\frac{I_m{}^2}{2}(R_f + R_L)\right]}$ $= \frac{8}{\pi^2} \frac{R_L}{R_f + R_L}$ $= \frac{0.812}{1 + \left(R_f / R_L\right)}$ $= \frac{81.2}{1 + \left(R_f / R_L\right)}$
Ripple Factor $r = \frac{I_{ac}}{I_{dc}}$ Please Note $I^2 = I_{dc}{}^2 + I_{ac}{}^2$ $\therefore \; r = \frac{\sqrt{I^2 - I_{ac}{}^2}}{I_{dc}} = \sqrt{\left(\frac{I}{I_{dc}}\right)^2 - 1}$	Ripple Factor $r = \frac{I_{ac}}{I_{dc}}$ $= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$

Form Factor is defined as	Form Factor is defined as
$F = \frac{I}{I_{dc}}$	$F = \frac{I}{I_{dc}}$
$F = \frac{\left(I_M/2\right)}{\left(I_M/\pi\right)} = \frac{\pi}{2} = 1.57$	$F = \frac{I}{I_{dc}} = \frac{\left(I_M/\sqrt{2}\right)}{\left(2I_M/\pi\right)} = 1.11$
Hence Ripple Factor $r = \sqrt{F^2 - 1}$	Hence Ripple Factor $r = \sqrt{F^2 - 1}$
$r = \sqrt{1.57^2 - 1}$	$r = \sqrt{1.11^2 - 1}$
$r = 1.21$	$r = 0.48$

Transformer utilization factor (TUF)

What is transformer utilization factor?

$$TUF = \frac{\text{DC Power delivered to load}}{\text{AC Power rating of transformer}}$$

Half wave Rectifier

$P_{DC} = {I_{DC}}^2 \times R_L = \left(\frac{I_m}{\pi}\right)^2 \times R_L$

$P_{ac}(rms) = V_{rms} \times I_{rms}$

$P_{ac}(rms) = \frac{V_M}{\sqrt{2}} \times \frac{I_M}{2}$

$I_m = \frac{V_M}{R_S + R_f + R_L}$

But $V_m = I_m R_L$

$\therefore$ TUF = $\left(\frac{{I_m}^2 R_L}{\pi^2}\right) \Big/ \left(\frac{{I_m}^2 R_L}{2\sqrt{2}}\right)$

= $2\sqrt{2}/\pi^2$ = 0.287

Full wave Rectifier

$P_{DC} = {I_{DC}}^2 \times R_L = \left(\frac{2I_m}{\pi}\right)^2 \times R_L$

$P_{ac}(rms) = V_{rms} \times I_{rms}$

$P_{ac}(rms) = \frac{V_M}{\sqrt{2}} \times \frac{I_M}{\sqrt{2}}$

But $V_m = I_m \times R_L$

$\therefore$ TUF = $\frac{\left(\frac{4}{\pi^2} \times {I_m}^2 R_L\right)}{\left(\frac{{I_m}^2 R_L}{2}\right)}$

= $\frac{8}{\pi^2}$ = 0.812

Problem 2.14 : The input signal is 50v in amplitude with a frequency of 50 H_Z. Calculate

(a) Rectifier efficiency

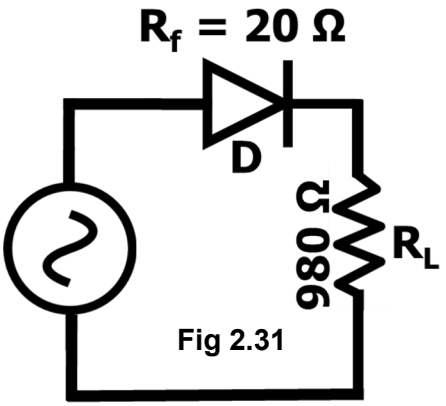


Fig 2.31

(b) Ripple Factor

Refer fig 2.31, Before we find m, we need to find

(a) Peak, Average (DC) and rms values of load current
(b) DC power output
(c) AC Power input
(d) Note, there is no transformer, ∴ Rs = 0

(a) Peak load current = $I_m = \frac{V_m}{R_f+R_L+R_S} = \frac{50}{20+980\Omega}$ = 50mA

$I_{dc} = {}^{I_m}/_{\pi} = \frac{50}{3.14} = 15.92\text{mA} = 15.92 \times 10^{-3}\text{A}$

$I_{rms} = \frac{I_m}{2} = \frac{50}{2} = 25\text{mA} = 25 \times 10^{-3}\text{A}$

(b) $V_{DC} = I_{DC} \times R_L = 15.92 \times 10^{-3} \times 980\Omega = 15.6\text{ V}$

$P_{DC} = {I_{DC}}^2 \times R_L = 15.92^2 \times 980 = 248.4\text{ mW}$

(c) AC Power input = $(I_{rms})^2 \times (R_L + R_f)$
= $(25 \times 10^{-3})^2 \times (980 + 20)$
= 625 mw

(d) Rectifier efficiency = $\frac{P_{dc}}{P_{ac\,in}}$ = $\frac{248.4\,mW}{625\,mW}$ = 39.74%

(e) Ripple factor = $\sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$ = $\sqrt{\left(\frac{25\text{ mA}}{15.92\text{ mA}}\right)^2 - 1}$ = 1.21

(f) % regulation = $\frac{V_{no\,load} - V_{full\,load}}{V_{load}}\ X\ 100\%$

(g) $V_{no\,load}$ = V_{DC} = $\frac{V_m}{\pi} = \frac{50}{\pi}$ = 15.91 V

(h) V_{load} = V_{DC} = 15.6 V

(j) Therefore % regulation = $\frac{15.91-15.6}{15.6}$ = 1.98%

Problem 2.15: For the example 2.14, already solved, find

(a) Peak, average & rms load currents
(b) DC Power output & ac power input
(c) Efficiency
(d) Form factor
(e) Ripple Factor

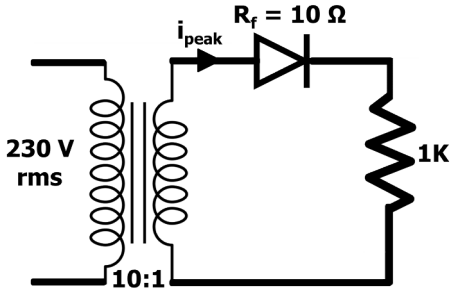


Fig 2.32

Refer fig 2.32. From 2.14, the peak secondary voltage V_m = 32.52 V

(a) Peak, average & rms load

$I_m = \frac{V_m}{R_S+R_f+R_L} = \frac{32.52}{5+10+1000} = \frac{32.52}{1015}$ = = 32.04mA

$I_{DC} = \frac{I_m}{\pi} = \frac{32.04\text{ mA}}{\pi} = 10.2\text{mA}$

$$I_{rms} = \frac{I_m}{2} \qquad = \frac{32.04\ mA}{2} \quad = 16.02mA$$

(b) DC Power output & ac power input

$V_{DC} = I_{DC} \times R_L \quad = 10.2\ mA \times 1000\ \Omega \quad = 10.2\ V$

$P_{DC} = (I_{DC})^2 \times R_L = (10.2mA)^2 \times 1000\Omega = 104\ mW$

$P_{ac\ in} = (I_{rms})^2 \times (R_S + R_f + R_L) \qquad = (16.02)^2 \times (5 + 10 + 1000) = 260.5mW$

(c) Efficiency $= \frac{P_{DC}}{P_{ac\ in}}\% = \frac{104mW}{260.5mW}\ \%$ = 39.92%

(d) Form factor $= \frac{I_{rms}}{I_{dc}} \quad = \frac{16.02mA}{10.02mA}$ = 1.57

(e) Ripple Factor γ $\qquad = \sqrt{F^2 - 1} \qquad = \sqrt{1.57^2 - 1} = 1.21$

Problem 2.16: The input to a full wave rectifier is 25 sin 100πt. The load resistor is 200Ω. Silicon diodes (0.6 V) with 50 Ω diode resistance is used. What is the peak output voltage, peak current and peak inverse voltage?

The diodes are silicon (0.6 V).

What is the frequency of the signal?

Input = 25 sin 100πt, Compare this with V = V_m Sin ωt.

$\therefore V_m$ = 25V (peak) ω = 2πft = 100πt $\therefore$ f = 50Hz

Input voltage (peak) = 25 V

Output voltage (peak) = 25 V ─ V_F = 25 V ─ 0.6 V = 24.4 V

Output Current = 24.4V/(200Ω + 50Ω) = 97.6 mA

PIV = Peak inverse voltage is the voltage across the diode, during reverse bias conditions

PIV of FWR = $2V_M$= 2 X 25 V= 50 V

Problem 2,17: In a full wave rectifier the secondary of the transformer used is 30 – 0 – 30 V. The secondary resistance is 20Ω. The diodes have forward resistance of 20 Ω and load resistor of 170 Ω

(a) Calculate Peak, average and rms currents,

(b) Calculate DC output power, ac input power and efficiency

(c) Calculate form factor, ripple factor and % regulation.

The secondary of a FWR is from a center tapped transformer. Look at the figure 2.33

30V is the rms value (not peak value)

The diode is fed through one half of the secondary (0 – 30 V)

$\therefore$ RMS input for each diode $V_{rms} = 30\ V$

$V_m = 30 \times \sqrt{2} = 42.42\ V$

$$I_m = \frac{V_m}{R_S + R_f + R_L}$$

Secondary resistance given = 20 Ω (for full secondary)

R_s= 10 Ω for each half of the secondary.

$I_M = \frac{42.42\ V}{10\Omega + 20\Omega + 170\Omega} = \frac{42.42V}{200\Omega} = 212mA$

$I_{DC} = \frac{2I_M}{\pi} \quad = \frac{2 \times 212mA}{\pi} = 134.9mA$

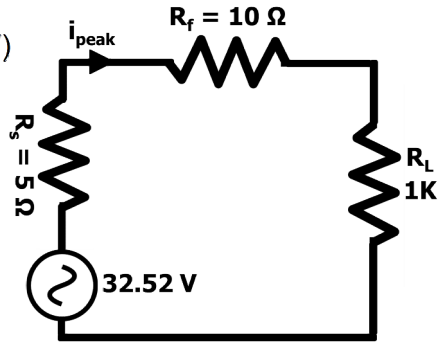


Fig 2.33 Equivalent Circuit

$I_{rms} = \frac{I_M}{\sqrt{2}} = \frac{212mA}{\sqrt{2}} = 149.9mA$

$P_{DC} = {I_{DC}}^2 \times R_L = (134.9)^2 \times 170 = 3.1\ W$

$P_{ac\ in} = {I_{rms}}^2 \times (R_S + R_f + R_L) = (149.9)^2 \times (10 + 20 + 70) = 4.49\ W$

$\eta = \frac{P_{DC}}{P_{ac}}\% = \frac{3.1\ W}{4.49\ W} \times 100 = 69\%$

Form Factor $= \frac{I_{rms}}{I_{DC}} = \frac{149.9}{134.9} = 1.11$

Ripple Factor $= \sqrt{(F)^2 - 1} = \sqrt{(1.11)^2 - 1} = 0.48$

% Regulation $= \frac{V_{NL} - V_{FL}}{V_{FL}}$

$V_{DC}(\text{No Load}) = \frac{2V_M}{\pi} = \frac{2 \times 42.42}{\pi}$ = 27 V

$V_{FL} = I_{DC} \times R_L = 134.9 \times 170 = 22.9\ V$

% Regulation $= \frac{27V - 22.9V}{27V} \times 100 = 15.2\ \%$

2.5.4 Bride rectifier (BR)

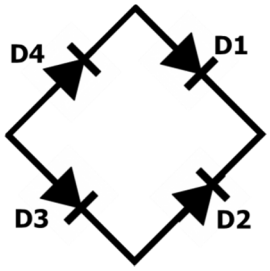


Fig 2.34. Bridge.

What is a bridge in a bridge rectifier?

A Basic bridge rectifier is shown in fig 2.34

It is an arrangement of **4 diodes** in such a way that

- full wave rectification happens
- **2 diodes conduct during the +ve** input cycle and the **other two diodes conduct during the -ve** input cycle.

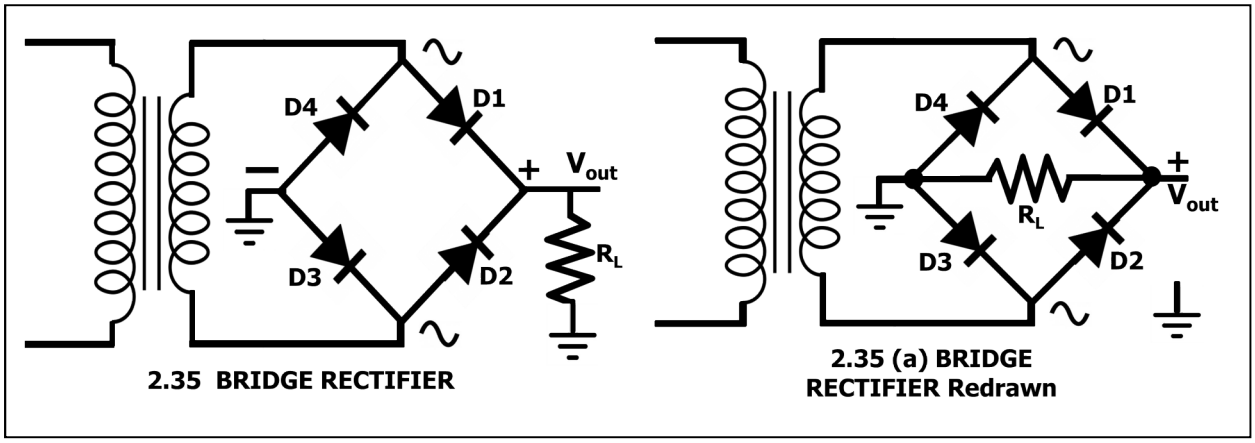
It is a full wave rectifier .

It consists of 4diodes

- It does not require a center tap secondary.
- Input is applied in the primary winding.

BR Operation:

A bridge rectifier is shown in fig 2.35



The same bridge rectifier is redrawn to provide more clarity in fig 2.35(a).

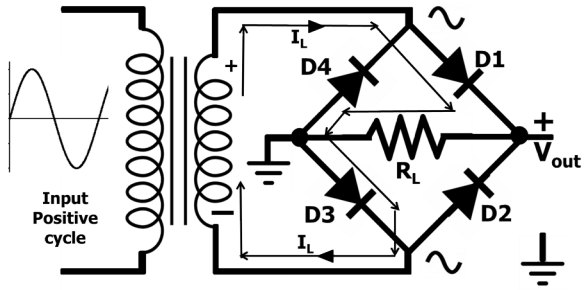


Fig 2.36 BRIDGE RECTIFIER (Redrawn)
Positive cycle (Only D1 and D3 conduct)

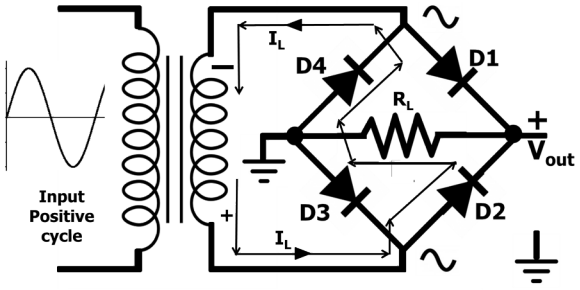


Fig 2.36 (a)BRIDGE RECTIFIER
Negative cycle (Only D2 and D4 conduct)

+ve cycle:

When the input is a +ve cycle, top of the secondary is +ve and the bottom is –ve.

Diodes D1 and D3 will conduct as shown in fig 2.36.

– ve Cycle:

When the input is a -ve cycle, bottom of secondary is +ve and the top is –ve.

Diodes D2 and D4 will conduct as shown in fig 2.36(a).

Note, the current through R_L, **is in the same direction (right to left)**, in both cycles

Equations of bridge rectifier:

They are same as that of FWR, except I_m

$$I_m = \frac{V_m}{R_s + R_f + R_f + R_L}$$ [since, 2 diodes are involved, per cycle]

$$I_{DC} = 2\,\frac{I_m}{\pi}, \qquad V_{DC} = 2\,\frac{V_m}{\pi}, \qquad I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$P_{DC} = (I_{DC})^2 \, X \, R_L = \frac{4}{\pi^2} I_m^2 \, R_L$$

$$P_{ac} = I^2_{RMS} (R_S + 2\,R_f + R_L) = \frac{I_m^2}{2} [R_S + 2R_f + R_L]$$

$$\text{Efficiency } (\eta) = \frac{8}{\pi^2} [\, R_L / (R_S + 2R_f + R_L)\,] \,\% = 81.2\,\%$$

F = 1.11, Ỹ = 0.48, TUF = 0.812

2.5.5 Comparison of rectifiers

Compare advantages & disadvantages of all the three rectifiers.

H W	F W	Bridge
Only one diode. Easy design.	2 diodes. Complex design.	4 diodes. Complex design.
No centre-tap transformer	Centre-tap transformer	No centre-tap transformer

Ripple factor high. (1.21)	Ripple factor Low. (0.48)	Ripple factor low. (0.48)
TUF low. Inefficient.	TUF High. Efficient.	TUF high. Efficient.
Low efficiency 40.6%.	High efficiency 81.2%.	High efficiency 81.2%.
Output load voltage & current low	Output load voltage & current high.	Output load voltage & current high.
Uni-directional current through transformer. Therefore transformer can saturate.	No net dc current through transformer. Therefore transformer will not saturate.	Current is continuous always hence transformer can be small & Inexpensive.
PIV of diode low (V_m)	PIV of diode high (2 V_m)	PIV of diode low (v_m)

Problem 2.18: In a bridge rectifier, the transformer primary voltage is 200 sin wt. The transformer step down ratio is 4 : 1. The secondary resistance is 10 ohms. Forward resistance of the diode is 20 ohms and the load resistance is 450 ohms.

Calculate I_m, I_{DC}, I_{rms}, V_{DC}, Ripple factor, Efficiency (η) and PIV of the diode.

V_p = 200 sin wt N1: N2 = 4 : 1 $\therefore V_s = \frac{200 \text{ Sin wt}}{4}$ = 50 sin wt V_m = 50 V.

$\mathbf{I_m} = \frac{\mathbf{V_m}}{\mathbf{R_s + 2R_f + RL}} = \frac{50 \text{ V}}{10 + (2 \text{ X } 20) + 450}$ = 100 mA

$\mathbf{I_{DC}} = \frac{\mathbf{2I_m}}{\boldsymbol{\pi}} = \frac{200}{\pi}$ = 63.6 mA

$\mathbf{I_{rms}} = \frac{\mathbf{I_m}}{\sqrt{2}} = \frac{100}{1.414}$ = 70.7 mA

$\mathbf{V_{DC}} = \mathbf{I_{DC} \text{ X } R_L}$ = 63.6 X 450 = 28.6 V

$\mathbf{P_{DC}} = \mathbf{(I_{DC})^2 \text{ X } R_L}$ = $(63.6)^2$ X 450 = 1.82 W

$\mathbf{P_{ac}} = \mathbf{I_{rms}^2 \text{ X } (R_s + 2 R_f + R_L)}$ = $(70.7)^2$ X (10 + 40 + 450) = 2.49 W

Efficiency = $\frac{\mathbf{P_{DC}}}{\mathbf{P_{ac}}}$ % = $\frac{1.82 \text{ W}}{2.49 \text{ W}}$ % =73.09 %

Ripple factor = $\sqrt{\left(\frac{\mathbf{I_{rms}}}{\mathbf{I_{dc}}}\right)^2 - \mathbf{1}}$ = $\sqrt{\left(\frac{70.7}{63.6}\right)^2 - 1}$ = 0.4854

PIV for a bridge rectifier = V_m = 50 V

2.5.6 Rectifiers: Quick reference guide

Parameters	**HW**	**FW**	**BR**
Load current I_m	$\frac{V_m}{R_s + R_f + RL}$	$\frac{V_m}{R_s + R_f + RL}$	$\frac{V_m}{R_s + 2R_f + RL}$
I_{DC} – Average DC current	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$
V_{DC} - Average DC voltage	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$

I_{rms}	$\frac{I_m}{2}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
V_{rms}	$\frac{V_m}{2}$	$\frac{V_m}{\sqrt{2}}$	$\frac{V_m}{\sqrt{2}}$
P_{DC} - DC Power output	$\left(\frac{I_m}{\pi}\right)^2$	$\left(\frac{2I_m}{\pi}\right)^2$	$\left(\frac{2I_m}{\pi}\right)^2$
P_{ac} - AC Power output	$\left(\frac{I_m}{2}\right)^2 (R_s + R_f + R_L)$	$\left(\frac{I_m}{\sqrt{2}}\right)^2 (R_s + R_f + R_L)$	$\left(\frac{I_m}{\sqrt{2}}\right)^2 (R_s + 2R_f + R_L)$
Efficiency	40.6%	81.2%	81.2%
Form factor	1.57	1.11	1.11
Ripple factor	1.21	0.482	0.482
TUF	0.287	0.812	0.693
Ripple freq	f	2f	2f
PIV	V_m	2 V_m	V_m

2.6 Capacitor Filter Circuit

2.6.1 Half-wave rectifier with Capacitor filter

Fig 2.37 shows a HW rectifier, with a capacitor filter. Let us assume an ideal diode . V_F =0

Operation

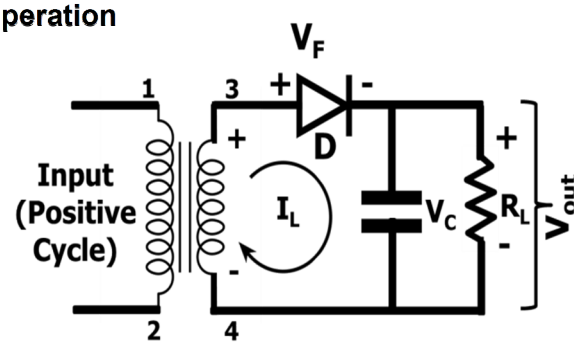


Fig 2.37 Capacitor Input filter

What happens in cycle 1? 0 to 90 deg (Refer fig 2.38)

- Input is switched on. During the first quarter positive cycle (0 to 90 deg) of the input, the diode conducts and the capacitor charges to the peak value of the input .

90 deg to 360 deg [Refer fig 2.38(a)]

- From 90 deg to 360 deg of the first cycle the *diode does not conduct .*

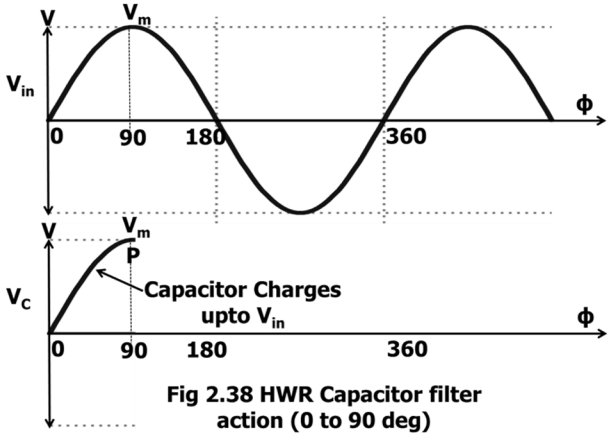


Fig 2.38 HWR Capacitor filter action (0 to 90 deg)

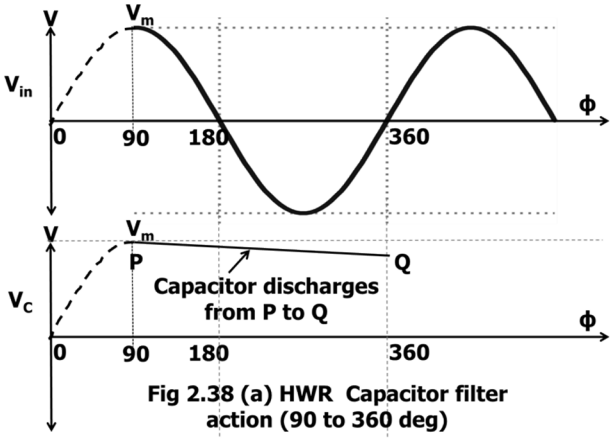


Fig 2.38 (a) HWR Capacitor filter action (90 to 360 deg)

Why ? (Refer fig 2.40 and 2.41)

- Let us say the sine wave has a peak voltage V_m =5 V. Up to P, the capacitor charges, simply following the input voltage. Therefore, the capacitor voltage will be 5V at P.

- The input voltage starts reducing beyond P (< 5 V). But the capacitor is already at 5V. Therefore, the diode finds itself getting reverse biased beyond P. (Cathode = 5 V and anode is , 5 V)

- Refer fig 2.39. The capacitor slowly discharges from its 5 V, through the resistor R_L The rate of discharge is determined by the time constant R_LC. Greater the time constant, slower will be the discharge.

What happens in Cycle 2? (Refer Diagram 2.39.)

- The capacitor is fully charged up to 5 V at P. The capacitor discharges in the rest of the cycle 1 and up to Q in cycle 2.
- Let us say, at Q the capacitor has discharged up to 4 V.
- The input also is at 4V at Q and rising. Look at interval QR. In this interval, the input (anode) will be more +ve than the capacitor (cathode). The diode gets forward biased in QR. Consequently the capacitor charges again by following the input. At R, the input is 5 V & the capacitor also is at 5 V.
- Beyond R, the input voltage will be less than that of capacitor. Diode is reverse biased. Capacitor starts its slow discharge. This cycle keeps repeating.

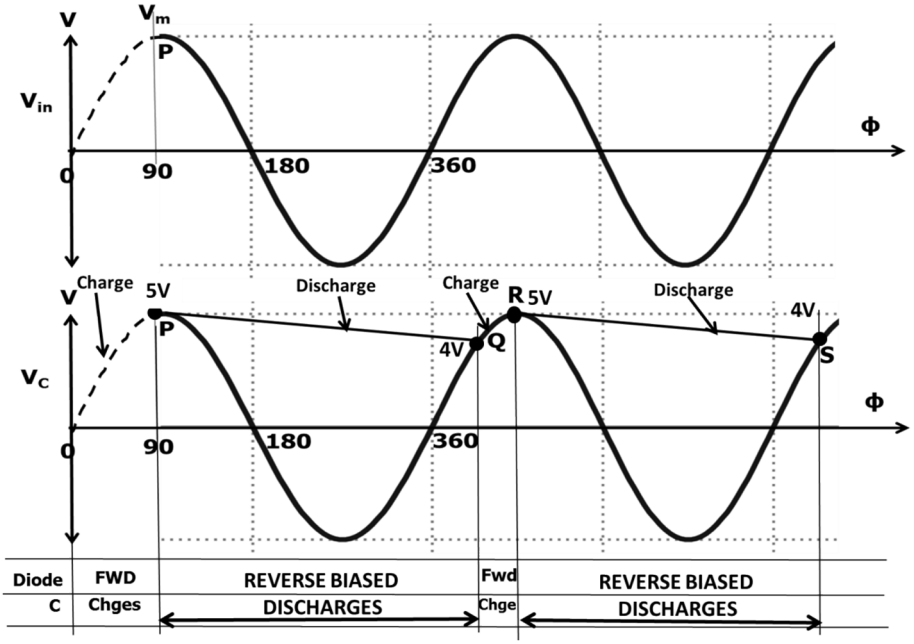


Fig 2.39 HWR Capacitor filter action (2 cycles)

Time constant

- The capacitor in HW rectifier, has two time constants, one for charging and one for discharging.
- Charging is through the diode whose resistance R_f is very low.
- Time constant is small and the capacitor charges very quickly. (Imagine filling up a bucket with a very large inlet tap).
- Discharging is through the resistor R_L whose value is relatively high.

- Time constant is large and the capacitor discharges very slowly. (Imagine emptying the bucket through a very small outlet tap).

2.6.2 Full wave rectifier with capacitor filter

The theory is exactly similar to HW rectifier discussed earlier. The circuit diagram of FWR and the wave forms are shown in fig 2.40.

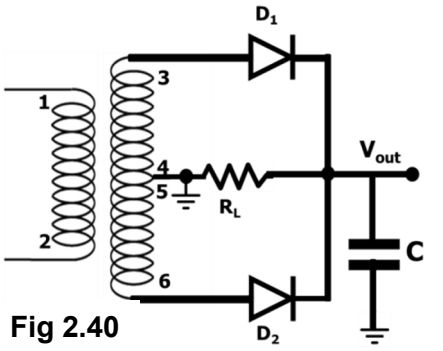


Fig 2.40

Full wave rectifier with Capacitor filter

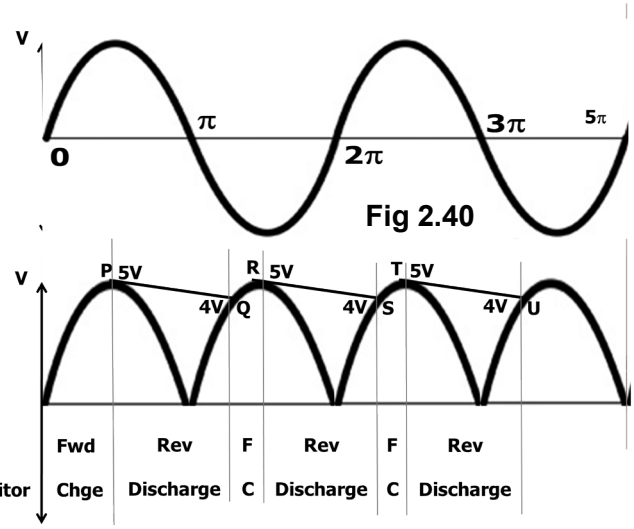


Fig 2.40

Wave forms are shown in fig 2.40(a)

Why capacitor filter? **Fig 2.40(a) FWR - Capacitor filter action (2 cycles).**

Output ripple will be less as seen above. The ripple factor ϒ, frequency, capacitor value and the load resistor are inter-related by the equation,

$$\gamma = \frac{1}{4\sqrt{3}\,CfR_L}$$

Problem 2.19: If a full wave rectifier is fed a sine wave of 10 V, 400 Hz, what is the capacitor value required, if the load current required is 20 mA and ripple factor is 2 %

Full wave rectifier →.Ripple = 2f = 800 Hz.

What is R_L?

$V_{DC} = \frac{2V_m}{\pi}$

$I_{DC} \times R_L = \frac{2V_m}{\pi}$ $\qquad R_L = \frac{2V_m}{\pi} \times \frac{1}{I_{DC}}$

Sine wave i/p = 10 V (rms) [unless otherwise mentioned V is rms]

V_m = 10 V X $\sqrt{2}$ = 14.14 V

I_{DC} = 20 mA

$\therefore R_L = \frac{2 \times 14.14}{20 \times 20 \times 10^{-3}}$ = 450 Ω

Ripple factor $\gamma = \frac{1}{4\sqrt{3}\,CfR_L}$

$\frac{2}{100} = \frac{1}{4X1.732X800X450}$ = 2 X 10^{-5} = 20 micro farad (μF)

2.7 Zener diode voltage regulator

Refer fig 2.41

- Zener diode is a special type of diode.
- It is widely used as a **voltage reference** in DC regulated power supplies
- Zener is always used in the **reverse bias** conditions.
- When the reverse bias exceeds a specified value, reverse current (I_R) flows, almost **unlimited.**
- This voltage is called **break down voltage or Zener voltage or Knee voltage.**
- The Zener diode circuit Symbol is shown here.

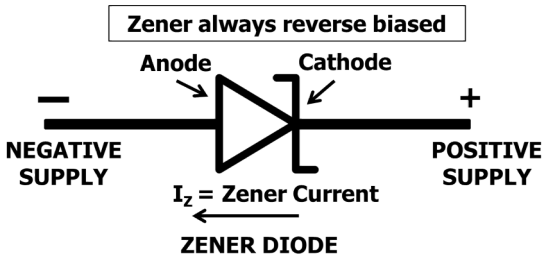


Fig 2.41 Zener Diode - Symbol , biasing and current flow

2,7,1 Zener characteristics

Fwd characteristics: The forward characteristics is same as that of a normal diode.

Rev characteristics (refer fig 2.42 and 2.43)

- The diode is operated in **reverse bias mode (Anode: – ve, Cathode: +ve).**
- Up to some reverse voltage, reverse current is low.
- Beyond a specific reverse voltage, the **pn junction breaks down**.
- This is known as **Zener break down.**
- Large **unlimited reverse current** flows.
- The zener diode **maintains a steady voltage over a large current range** as seen in the figure.
- It is necessary to **limit the current** by using a series resister R1.
- The break down action is **reversible**. Zener diode can be used again and again.

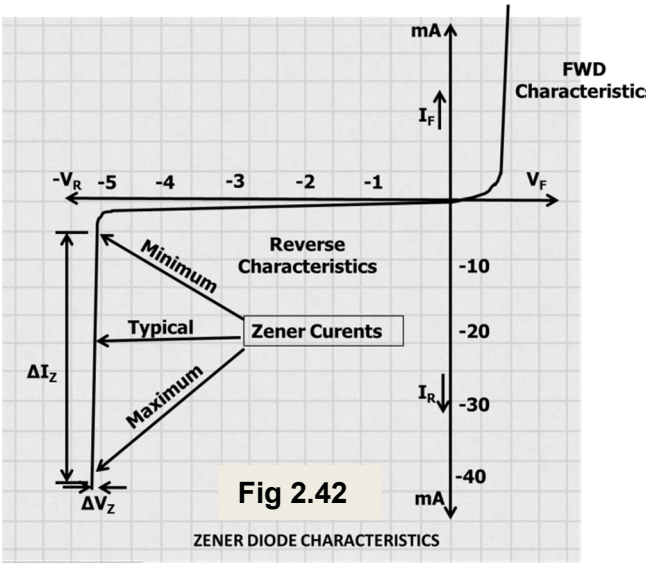


Fig 2.42 Zener Diode Characteristics

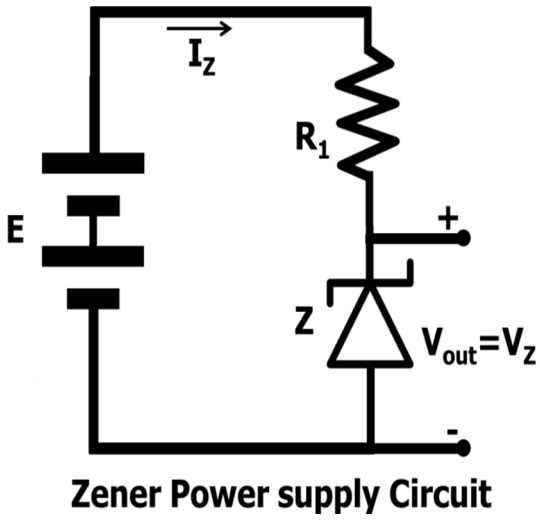


Fig 2.43

What is the zener current in this circuit without a load resistor? (fig 2.43)?

$$I_z = \frac{E - V_Z}{R_1}$$

What is the zener current in the circuit in fig 2.44, with a load resistor R_L? What is the load current in this circuit?

$$I_z + I_L = \frac{E - V_{out}}{R_1} = \frac{E - V_Z}{R_1}$$

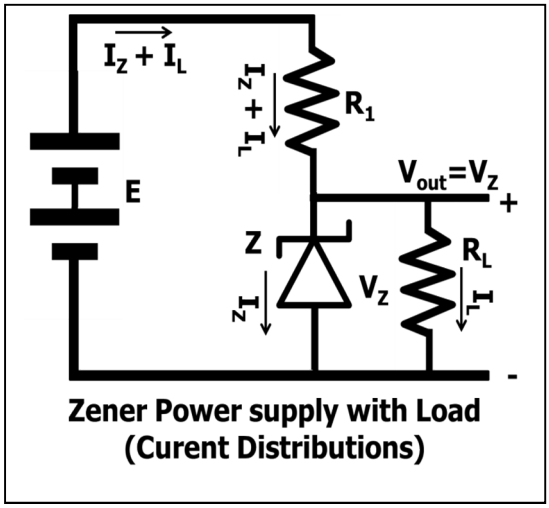
$$I_L = \frac{V_Z}{R_L}$$

2.7.2 Zener break down mechanism

Case 1

Very narrow depletion region

- **Reverse voltage produces very high field strength**.
- What is field strength? Voltage per distance **(Volts / Distance.)**
- **Electrons break away from their atoms due to this field strength**.
- ∴ Due to this electron flow, depletion region is converted into a conductor (from insulator)
- This is called **ionization by electric field**
- This is one of the Zener break down mechanisms
- Usually occurs when **reverse bias is < 5V**



Zener Power supply with Load (Curent Distributions)

Fig 2.44

Case 2

Depletion region very wide

- In the reverse bias mode reverse saturation current flows.
- There are electrons moving in reverse saturation current.
  - **When these electrons travel in the wide depletion region, these electrons gain a lot of energy**
  - These energetic electrons **collide with atoms** and cause their **electrons to break-free**.
  - Due to these new electrons, **more collisions** occur and more electrons get released
- This is known as **Avalanche break-down**.

2.7.3 Power dissipation of a Zener

What is maximum power dissipation P_D of a Zener?

The **Zener operates in a break down mode. (Reverse bias**).

Once break down happens, **current through the Zener is unlimited**.

This **current should be limited** through a resistor.

Otherwise Zener will dissipate too much power, get heated and **burn itself out**.

Power dissipated in the **Zener $P_D = V_Z \times I_Z$** (refer figure 2.44)

Every Zener has a specification for **Maximum power dissipation P_D max** and the designer should ensure that the Zener is **operated with in P_D max (by choosing E & R carefully)**

Problem 2.20: What should be value of R, in fig 2.45, if the Zener break down voltage is 8 V and P_D max = 400 mW

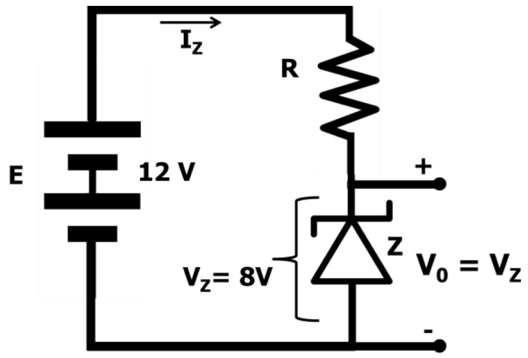


Fig 2.45

P_D = V_Z X I_Z
400 mW = 8 V X I_Z
$\therefore$ I_Z = 50 mA
The resistor must ensure I_Z is < 50 mA
Input voltage = 12 V
Zener voltage = 8 V
Voltage across resistor R = 4 V
Current through resistor R = 50 mA

$\therefore$ Value of R $= \frac{4\ V}{50\ mA}$ = 80 Ω

R = 80 Ω

Problem 2.21: V_Z =10V, R =500. For this circuit in fig 2.46, what is the current through the Zener?
What is P_D of Zener?

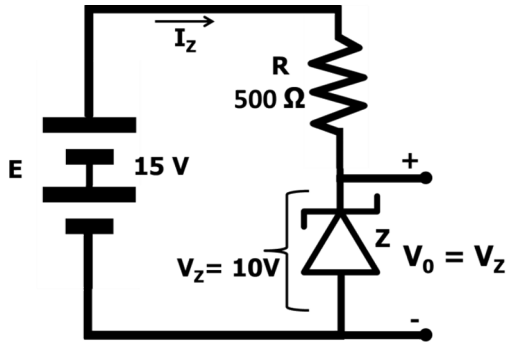


Fig 2.46

V_Z = 10 V. R = 500 Ω

$\therefore$ Voltage across resistor = 15 V – 10 V = 5 V

Current through R $= \frac{5\ V}{500\ \Omega}$ = 10 mA

Current thro Zener also = 10 mA

P_D of zener = V_Z X I_Z = 10 V X 10 mA
= 100 mW.

2.7.4 Equivalent circuit of Zener

DC Equivalent circuit

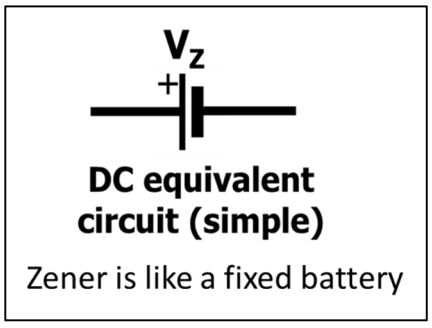
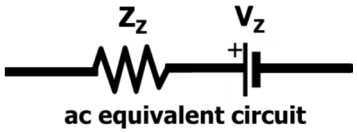


Fig 2.47

ac Equivalent circuit



Recall, diode has a dynamic resistance (r_d). Similarly, zener also has a dynamic impedance (Z_z)

Fig 2.48

Problem 2.22: A Zener has a break down voltage of 5 V and a dynamic Impedance (Z_z) =30 ohms. Zener current is 25 mA. How much will the Zener voltage change when the Zener current changes by ±10 mA? (Refer fig 2.48)

V_z = 5 V, I_z = 25 mA, ΔI_Z = ±10 mA, Z_z =30 ohms.

$\Delta V_Z = \Delta I_Z \times Z_z$ = ± 10 mA X 30 ohms = ±300 mV

V_Z (Maximum) **= $V_Z + \Delta V_Z$** = 5 V + 300 mV = 5.3 V

V_Z (Minimum) **= $V_Z - \Delta V_Z$** = 5 V - 300 mV = 4.7 V

2.7.5 Zener diode voltage regulator

What is a voltage regulator?

A voltage regulator ensures that the **output voltage is constant** for the following conditions.

a) **When the input voltage is varied** between a specified minimum & maximum range.

b**) When the load current is varied** from no load (0 A) to its rated full load current.

In practice, the **output voltage cannot be rock steady. It will have minor variations up and down**.

Problem 2.23: How a 5V, 200 mA regulator behaves typically, <u>when input voltage varies</u>
Voltage regulation (example)

Input voltage	12 V	10 V	8 V
Output Voltage	5.1 V	5.0 V	4.9V

Example: How a 5V, 200 mA regulator behaves typically, <u>when load current varies</u>
Current regulation

Load Current	200 mA	100 mA	0 mA (no load)
Output voltage	5.0 V	5.1 V	5.2 V

How zener diode acts as a regulator?

Refer Fig 2.49 (only reverse characteristics)

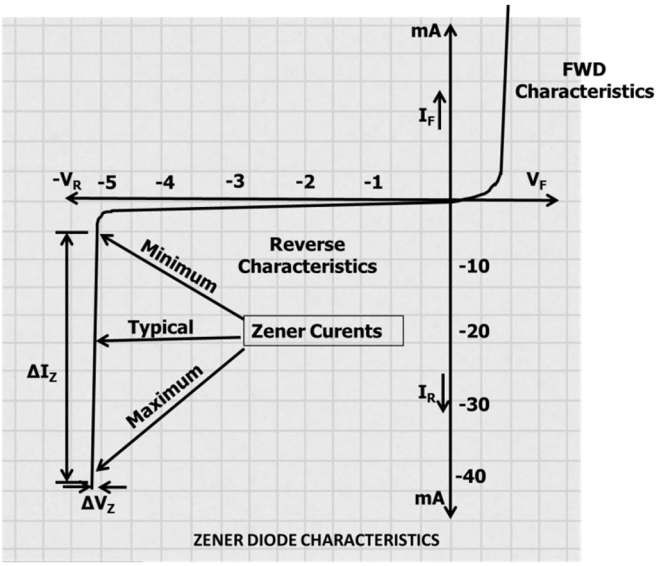


Fig 2.49

Recall, zener diode operates in the reverse bias conditions.

- **When reverse bias reaches V_Z (5 V in this example), zener break down happens and the reverse current shoots up.**
- **The zener voltage is steady around 5.0 V, even though the current varies from 2 mA to 40 mA and beyond.**
- This shows that zener can, always maintain a constant voltage across it, for a wide range of current variations through it.
- This is the property of a **good voltage regulator**

- The **zener requires a certain minimum current,** to break-down and act as a regulator. In this example, the minimum current required, is shown as 5 mA.
- Similarly, the **zener cannot support, beyond a certain maximum current**. Else, it will **exceed its maximum permissible power dissipation.** In this example, maximum current is 40 mA.

- Usually, it is prudent to **operate the zener, halfway between these two extremes.**

2.7.6 Zener diode as a shunt regulator.

Problem 2.24: Find out I, I_z and I_L for this circuit in fig 2.50

We are **sure of two nodes here**.

Node A = 12 V Node B = V_Z = 6 V

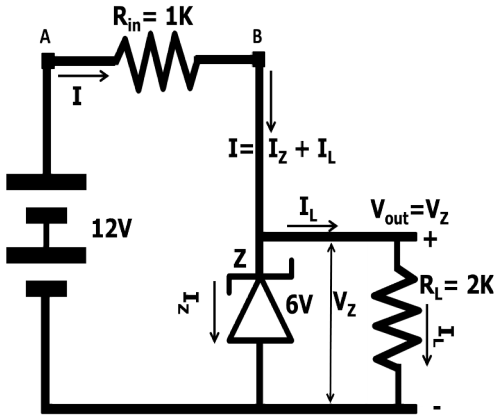


Fig 2.50

a) Find I_L

Voltage across R_L = Voltage of Zener

V_O = V_Z = 6 V

I_L = $\frac{V_Z}{R_L}$ = 6 V / 2K = 3 mA

b) Find I (current through R_{in})

One end of R_{in} is Node A and the other end is Node B. R_{in} =1 K

∴Voltage across R_{in} = V_A –V_B = 12 V – 6 V = 6 V.

Current through R_{in} = 6 V / 1K = 6 mA

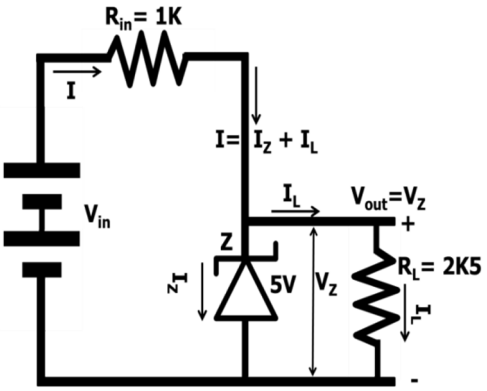


Fig 2. 51

c) Current thro Zener

I = I_Z + I_L

6 mA = I_z + 3 m A

∴ I_Z = 3 m A.

Problem 2.25: Calculate the input voltage range for which output will be constant, for the circuit in fig 2.51. The zener must operate between 5mA and 20mA.

R_L = 2.5 K, V_z = 5

∴ I_L = 5 V / 2.5 K = 2 mA. Note I_L is always 2 mA in this circuit.

1) Calculate V_{in} min	2) Calculate V_{in} max
V_{in} min happens when I_Z is min = 5 mA	**V_{in} max happens when I_Z is max** = 20 mA.
I = I_L + I_Z min = 2 mA + 5 mA = 7 mA	I = I_L + I_Z max = 2 mA+20 mA = 22 mA
∴The current thro R_{in} = I = 7 mA	∴The current thro R_{in} = I = 22 mA
Voltage drop across R_{in} = I X R_{in} = 7 mA X 1K = 7 V	Voltage drop across R_{in} = I X R_{in} = 22 mA X1 K = 22 V
∴ V_{in} (min) required = Voltage across R_{in} + V_Z = 7 V + 5 V = 12 V	…V_{in} (max) = Voltage across R_{in} +V_Z = 22 V + 5 V = 27 V.

Problem 2.26: The zener in fig 2.52, is required to deliver a load current of 20 mA at a constant output voltage of 6 V. The minimum current of the zener is 5 mA. P_D max of zener is 240 mW. The input varies between 10 V to 12 V. What should be the value of the series limiting resistor?

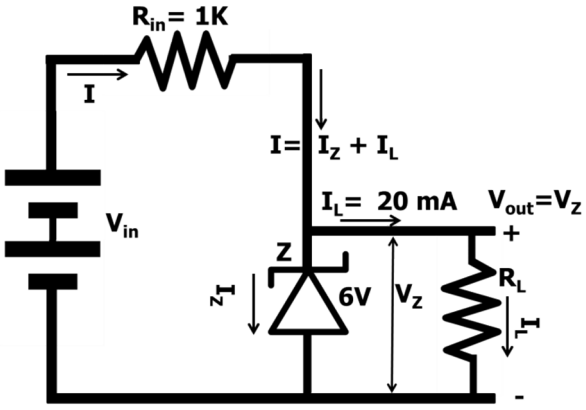


Fig 2.52

V_{oul} = 6 V = V_z, P_D max = 240 mW,
I_Z min = 5 mA, Input : 10 V to 12 V, I_L =20 mA

1) <u>To find I_z max</u>
I_z min = 5 mA (given) but what is Iz max?
P_D max = 240 mW (given).
P_D = I_z max X V_Z
240 mW = I_z max X 6 V
I_z max = 40 mA

2) <u>To find I_{max} and I_{min}</u>
I_{max} = I_z max + I_L = 40 +20 = 60 mA
I_{max} = I_z min + I_L = 5 + 20 = 25 mA

3) <u>To find R_{min}</u>
R_{min} happens when when V_{in} is max and I is Imax
V_{in} (max) = V_z + I_{max} R_{min}
12 V = 6 V + 60 mA X Rmin
$\therefore$ **R_{min}** = $\frac{6\ V}{60\ mA}$ = **100 Ω**

4) To find R_{max} ?
R_{max} happens when V_{in} is minimum and I is I_{min}
V_{in}(min) = V_z + Imin R_{max}
10 V = 6 V + 25 mA X R_{max}
R_{max} = $\frac{4\ V}{25\ mA}$ = **160 Ω**
$\therefore$ The value of R should be between 100 Ω and 160 Ω.

<u>Relationships to remember.</u>

1. **How to find I_z max?** Use the relation: P_D = I_z max X V_Z
2. **How to find I_{max} and I_{min}?** Use the relation I_{max} = I_z max+I_L & I_{max} = I_z min+ I_L.
3. **How to find R_{min}?** R_{min} happens when when V_{in} is max and I is Imax
4. **How to find R_{min}?** R_{max} happens when V_{in} is min and I is I_{min}
5. **How to find V_{in} max and V_{in} min?** Use the relations V_{in} (max) = V_z + I_{max} R_{min} and V_{in}(min) = V_z + I_{min} R_{max}

2.7.7 Numerical Problems

Problem 2.27: Design a Zener for an o/p of 5 V. Load current =10 mA, Zener Power = 400 mw, I/P voltage = 10 ± 2V.

Soln

$$R_L = \frac{V_Z}{I_L} = \frac{5}{10 \times 10^3} = 500 \text{ ohms}$$
$$P_Z = 400 \text{ mw}$$
$$I_Z = \frac{P_Z}{V_Z} = \frac{400 \times 10^{-3}}{5} = 8 \text{ mA}$$
$$I_S = I_Z + I_L = 80 + 10 = 90 \text{ mA}$$

Case 1 When input = 12 V (10 + 2)

R Series = $\frac{12-5}{90 \text{ mA}} = 77.77 \text{ ohms}$

Case 2 When input = 8 V (10 - 2)

R Series = $\frac{8-5}{90 \text{ mA}} = 33.33 \text{ ohms}$

Problem 2.28 : A full wave rectifier supplies power to 1 k Ω load. The ac applied to the diodes is 300 V – 0 – 300 V. If the diode resistance is 25 Ω, find

(a) Average load current
(b) Average load voltage
(c) rms value of ripple voltage
(d) efficiency

Neglect transformer resistance.

Soln

300 V – 0 – 300 V is rms., R_f = 25 Ω, R_L = 1000 Ω

$$V_m = 300\sqrt{2} = 424 \text{ V}$$
$$I_m = \frac{V_m}{R_f + R_L} = \frac{424}{1000 + 25} = 0.414 \text{ A}$$
$$I_{dc} = {}^{2\, I_m}\!/_{\pi} = 0.263 \text{ A}$$
$$I_{rms} = {}^{I_m}\!/_{\sqrt{2}}$$

$$V_{dc} = I_{dc} \times R_L = 263 \text{ V}$$

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$
$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{{I_{dc}}^2 R_L}{{I_{rms}}^2 (R_L + R_f)}$$

$$= \frac{\left(4\,I_m^{\,2}\,R_L/\pi^2\right)}{\left(I_m^{\,2}/2\right)(R_L + R_f)}$$

$$= \frac{8}{\pi^2}\left(\frac{R_L}{R_f + R_L}\right) = 79.01\% \text{ (approx)}$$

Problem 2.29 : An ac voltage of 25 V is connected in series with a silicon diode. The load resistance is 100 Ω. I_f = 10 Ω (Fwd resistance of diode) find, peak current through the diode and peak voltage thro R_L and V_{dc}

Soln

V_{rms} = 25 V, R_L = 1 K, R_f = 10 Ω

$I_m = V_{rms} \times 2 = 50V \qquad \left(\text{in HWR}: \frac{V_m}{2} = V_{rms}\right)$

$V_m = \frac{V_m}{R_f + R_L} = 49.5\ \text{mA}$

$V_{dc} = \frac{V_m}{\pi} \cdot \frac{R_L}{R_f + R_L} = 15.71\ \text{mA}$

Max output across load = $I_m R_L$ = 49.5 V

Problem 2.30 : Ideal diodes are used in a bridge rectifier. The source voltage is 230 V, 50 Hz. Load resistance is 200 ohms. Transformer turns ratio is 4 : 1. Find dc o/p voltage and frequency of output.

Freq of O/P in Bridge (Full-wave) rectifier = 2f = 100 Hz

V_{rms} = 230 V, R_L = 200 Ω, Turns ratio = 4 : 1

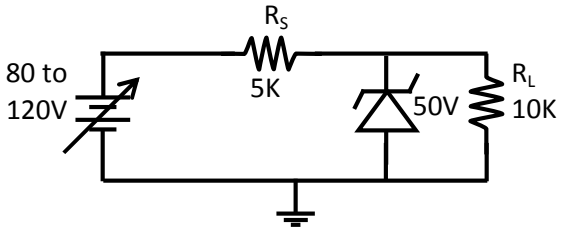
∴ I/P to Bridge diodes = 230 / 4 = 57.5 V (rms)

$V_m = V_{rms} \times \sqrt{2} = 81.3\text{V}.$

$V_{dc} = \frac{2\,V_m}{\pi} = 52\ \text{V}.$

$P_{dc} = I_{dc}^{\,2} \cdot R_L = \frac{(V_{dc})^2}{R_L} = \frac{52 \times 52}{200} = 13.2\ \text{W}.$

Problem 2.31 : For the circuit shown, fine max and min vale of Zener current.



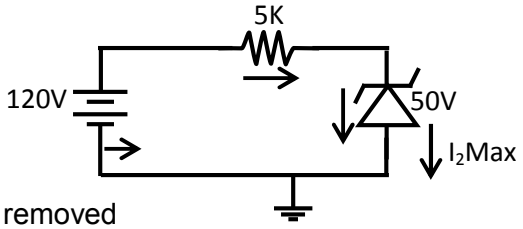
Case 1

I_2 (Max) occurs when

(a) R_L is removed and

(b) V_{in} is maximum

$I_Z\text{Max} = \frac{120-50}{5K} = 14\ \text{mA}.$



The entire current flows thro Zener since R_L is removed

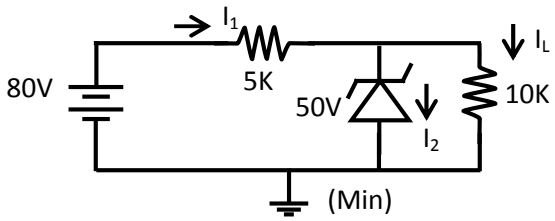
Case 2

I_2 (Min) occurs when

(a) 10K is connected (R_L)

(b) V_{in} = Min = 80 V

since Zener voltage = 50 V, voltage across R_L also is 50 V



$$I_L = \frac{50V}{10K} = 5 \text{ mA.}$$

$$I_1 = \frac{80-50}{5K} = 6 \text{ mA.}$$

$\therefore$ I_Z min = $I_1 - I_L$ = 6 — 5 = 1mA

Problem 2.32 : A 24 V, 600 mw Zener diode is used to provide 24 V stabilized supply to a variable load. Input is 32 V. R_L = 1200 Ω.

Calculate

(1) The series resistance required.

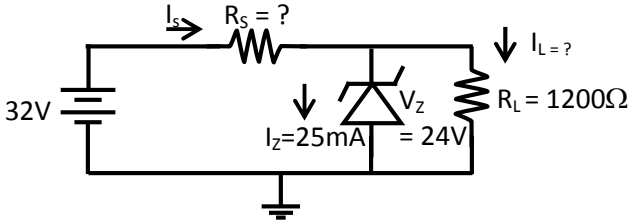
(2) Zener current when load = 1200 Ω

Soln :

P_Z = 600 mw, V_Z = 24 V. I_Z = ?

(a) $P_Z = V_Z \times I_Z$ $\quad \therefore I_Z = \frac{600\ mw}{24V} = 25\ mA$

(b) I_L =? $\quad \frac{24\ V}{1200\ \Omega} = 20\ mA$ [since Zener voltage = 24 V, voltage across R_L also is 24 V]



(c) I_S = ? $\quad I_S = I_Z + I_L$ = 25 + 20 = 45 mA

(d) Rs = ? $\quad R_s = \frac{Volage\ across\ R_S}{Current\ thro\ R_S} = \frac{32\ V - 24\ V}{45\ mA} = \frac{8\ V}{45\ mA} = 177.78\ \Omega$

Problem 2.33 : In a 2 diode full wave rectifier, the voltage across half the secondary is 100 V. Load Resistance is 950 Ω and R_f = 50 Ω . Find load current of RMS current.

V_{rms} = 100 V $\quad I_{dc}$ = ? $\quad I_{rms}$ =?

$$I_{rms} = \frac{V_{rms}}{R_L + R_f} = \frac{100}{950 + 50} = 100\ mA$$

$$V_m = V_{rms} \times \sqrt{2} = 100 \times 1.414 = 141.4\ V$$

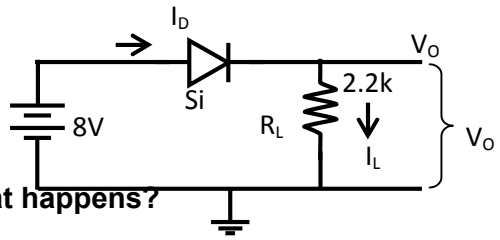
$$I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi\left(R_L + R_f\right)} = \frac{2 \times 141.4}{\pi \times 1000} = 0.08998\ A = 89.98\ mA$$

Problem 2.34 : What is V_O? What is the diode current?

The diode used is silicon, therefore V_f = 0.7 V

The voltage across RL = 8 – 0.7 V = 7.3 V

Current thro RL = Current ho diode = $\frac{7.3\ V}{2.2\ K} = 3.32\ mA$



Problem 2.35 : If the diode is reversed in example 8, what happens?

The diode is reverse biased,

There is no current flow anywhere

Output across R_L = 0 V.

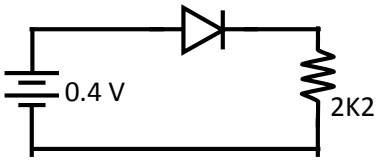
Current I_L = 0

Current I_D = 0

Problem 2.36 : If the supply voltage is 0.4 V in example 8, what happens?

The diode is not sufficiently forward biased (silicon diode needs 0.7 V to conduct). Diode does not conduct

$\therefore$ I_L = 0, I_D = 0, V_R = 0



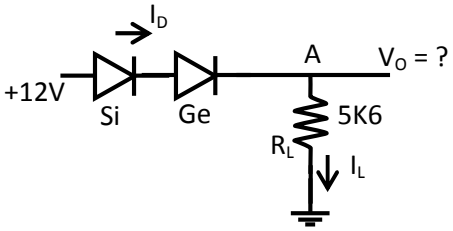
Problem 2.37 : V_O = ? I_D = ?

Voltage at A = 12 V – Silicon Diode drop – Germanium diode drop

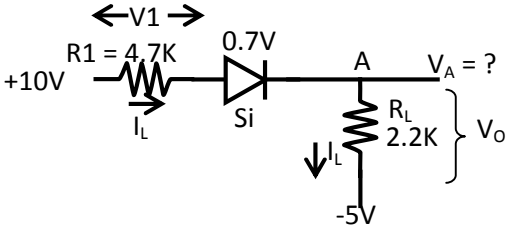
= 12 V – 0.7 V – 0.3 V = 11 V.

$I_L = \frac{11\ V}{5600\Omega} = 1.96\ mA$

I_D = I_L = 1.96 mA



1) V_A = ? V_O = ? I_L = ?



Method 1

KVL : Kirchoffs Voltage law

As per KVL : $-10V + (I_L \times 4.7K) + 0.7V + (I_L \times 2.2K) + 5V = 0$

I_L = 2.07 mA

$V_1 = I_L \times R_1$ = 2.07 mA x 4.7 K = 9.73 V (approx)

The DC Voltage at A = 10 – V1 – 0.7

= 10 – 9.73 – 0.7 = -0.43V.

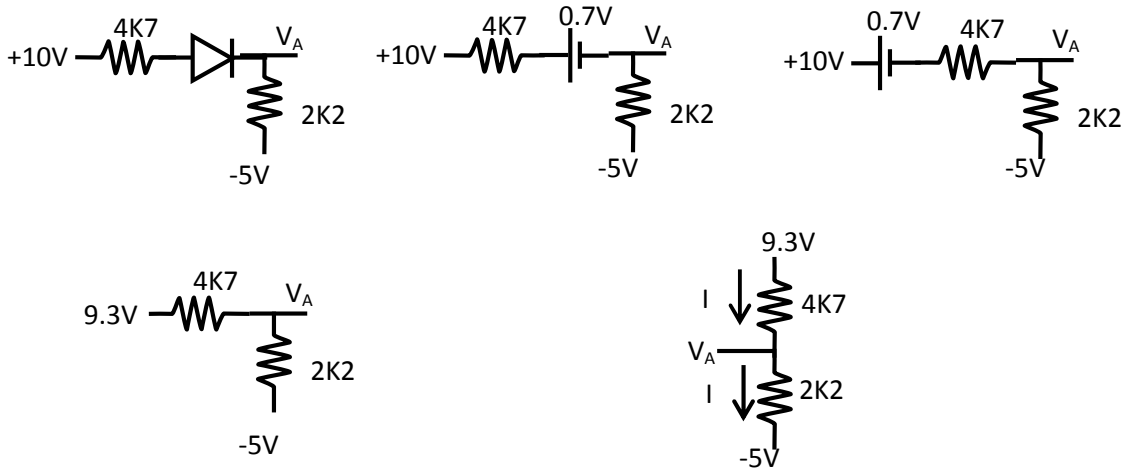
V_O = $I_L \times R_L$ = 2.07 mA x 2.2 K = 4.55 V (approx)

Method 2

If you are not yet familiar with kirchoff's laws,

Draw equivalent circuit

i)



Total Current I = ?

Total Voltage = 9.3 V + 5 V = 14.3 V

Total Resistance = 4K7 + 2K2 = 6.9 K

$\therefore I = \frac{14.3\ V}{6.9\ K}$

Find I

Drop across 4K7 = I x 4.7 K

Drop across 2K2 = I x 2K2 & so on ……

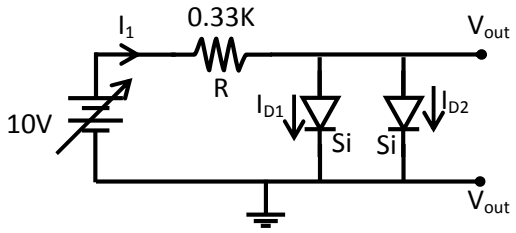
Problem 2.38 : Analyze this circuit.

(a) I_1 = ? $\frac{10\ V - V_{out}}{0.33\ K}$

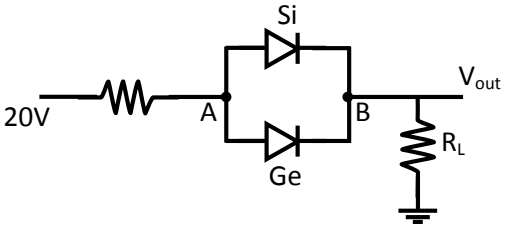
(b) V_{out} = ? V_{out} = 0.7 V (since both are silicon didoes with 0.7 V drop)

(a) $I_L = \frac{10 - 0.7\ V}{0.33\ K}$ = 28.18 mA

(b) What is ID1 & What is ID2?
I_1 is shared equally by diode 1 and diode 2
$\therefore I_{D1} = I_{D2} = I_1/2$ = 14.09 mA

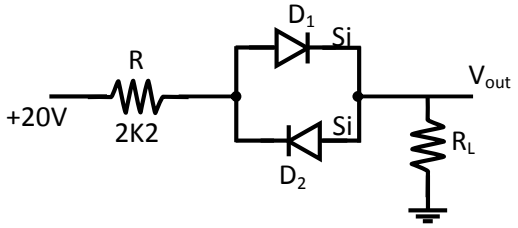


Problem 2.39 : What is V_{out}?



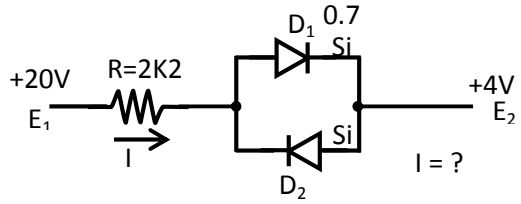
Across AB there are 2 diodes Si and Ge.
When Germanium conducts V_{AB} will be frozen at 0.3V.
On the other hand Si diode requires 0.7 V to conduct, which it will never get. Therefore Si diode will never ever be able to conduct.
$\therefore$ Vout = 20 V – V_{ge} = 20 V – 0.3 V = 19.7 V

Problem 2.40 : What is V_{out}?



If input is +20 V, D1 is FWD biased & will conduct.
Diode D2 will always be reverse biased and will not conduct.
$\therefore V_{out} = 20 - 0.7\ V = 19.3\ V$

Problem 2.41 : What is I ?

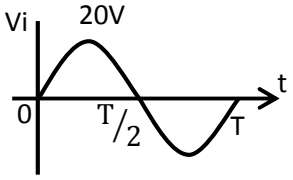


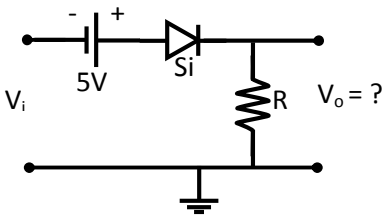
D1 - FWD biased & will conduct
D2 - REV biased & will NOT conduct

$$I = \frac{E_1 - E_2 - V_f}{R}$$

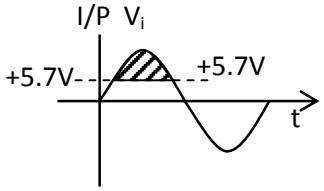
$$I = \frac{20\ V - 4\ V - 0.7\ V}{2.2\ K} = \frac{15.3\ V}{2.2\ K} = 6.95\ mA$$

Problem 2.42 : For the circuit shown, what is the o/p waveform?



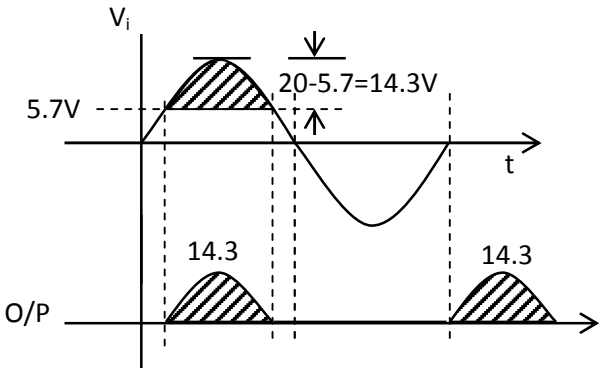


When Will the diode become forward biased ?



(a) Cathode is at 0 V
(b) Anode is at +5V (due to series Battery)
(c) ∴Diode will conduct if and only if the input sine wave goes above +5.7V.
(d) ∴The o/p wave form will be that portion of Input Sine wave with amplitude > +5.7V as shown in fig (Hatched)

(e) The output will be zero when I/P is below +5.7V.



Chapter 3 Bipolar Junction Transistors

Syllabus: Bipolar Junction Transistors: BJT operation, BJT Voltages and Currents, BJT amplification, Common Base, Common Emitter and Common Collector Characteristics, Numerical examples as applicable.

3.1 Transistor Introduction

What is a transistor?

- A transistor is a semiconductor device . It is a **3 layer device**. Two types of arrangements are possible -- **npn or pnp.**
- It has three layers – **emitter, base and collector**
- Transistor is a **current controlled** device and NOT a **voltage controlled** device.
- A very **small amount of current in the base region can control a large amount of current between emitter and collector**. This means transistor can be used in **current amplification** and therefore power amplification..
- Transistor can be used as a **basic switch (on–off switch) in digital logic circuits**

3.1.1 Transistor construction and circuit symbols:

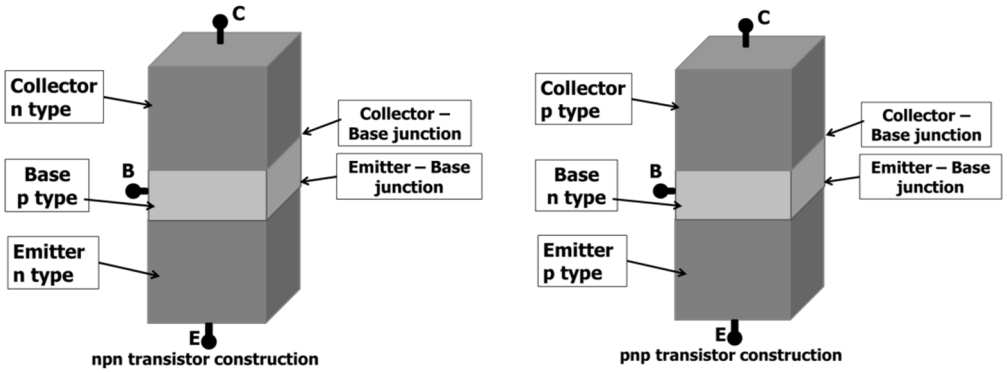


Fig 3.1

Figure 3.1 shows two types of transistor packages in semiconductor form – NPN and PNP.

PNP Transistor:

In PNP, **a n type semiconductor is sandwiched** between two p type semiconductors. The transistor has three terminals – **E**mitter (p type), **B**ase (n type) and **C**ollector (p type)

NPN Transistor:

In NPN, a **p type semiconductor is sandwiched** between two n type semiconductors. The transistor has three terminals – **E**mitter (n type), **B**ase (p type) and **C**ollector (n type)

Transistors have **two pn junctions, a collector base junction and an emitter base junction**.

3.1.2 Circuit Symbols:

The circuit symbols for an NPN transistor and a PNP transistor are shown in fig 3.2. The **emitter is always identified thro an arrow**. The direction of the arrow indicates the direction of the current flow.

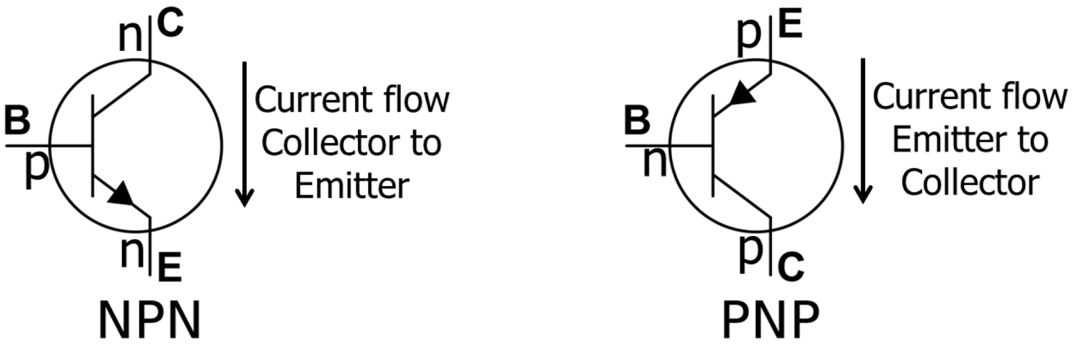


Fig 3.2

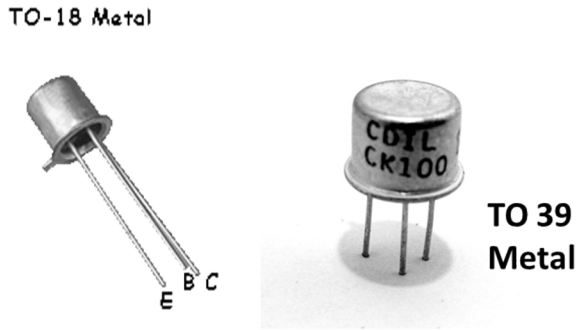


Fig 3.3

In a NPN transistor, the current is flowing out of the emitter and in a PNP transistor, the current is flowing into the emitter. The current flow direction also is indicated in the diagram.

In NPN type the arrow is from p to n. In PNP type the arrow is also from p to n. Therefore remember that the current flow is always from p to n.

Some common metal can packages found in your lab are shown in fig 3.3

3.2 BJT Operation

3.2.1 pn junction operation

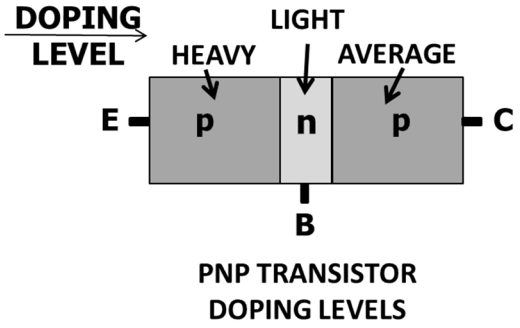


Fig 3.4

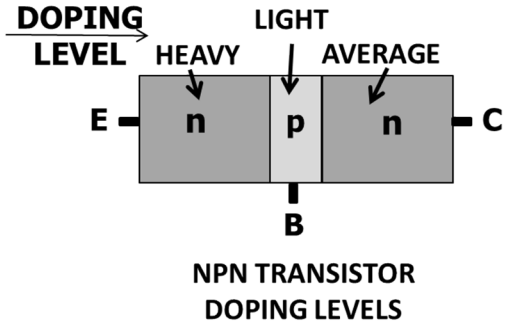


Fig 3.5

Recall the pn junction diffusion process discussed earlier on in section 1.4.1.. The doping levels in emitter, base and collector are shown in fig 3.4 and 3.5

3.2.2 No bias: In the absence of any bias voltage, some electrons move from n region (majority carriers) to p and some holes move from p region (majority carriers) to n. This causes a build up of +ve ions in n region and -ve ions in the p region causing a potential barrier. This barrier prevents further movement of carriers across the junction.

3.2.3 Forward bias (Emitter-Base junction): A npn transistor is shown in fig 3.6. Connect an external battery to the pn junction such that **p is connected to +ve and n is connected to the –ve**

terminal of the battery. Under this condition **the emitter base junction is said to be forward biased.**

When a pn junction is forward biased,

- **Electrons (majority carriers) from n side** are attracted by the +ve potential in the p side and therefore **electrons start crossing the junction and land in p side**.
- **Holes (majority carriers) from p side** are attracted by the -ve potential in the n side and therefore **holes start crossing the junction and land in p side**
- Current flows in the pn junction from p to n under forward bias conditions
- **Current flow is due to majority carriers under forward bias conditions.**

3.2.4 Reverse bias (Collector-Base junction): Connect an external battery to the pn junction such that **p is connected to -ve and n is connected to the +ve terminal of the battery.** Under this condition the **collector base junction is said to be reverse biased.**

Majority carriers

- Electrons (majority carriers) from n side are repelled by the -ve potential in the p side and therefore electrons move away from the junction and remain in n side itself.
- Holes (majority carriers) from p side are repelled by the +ve potential in the n side and therefore holes move away from the junction and remain in p side itself.

Minority carriers

- However, holes (minority carriers) from n side will be attracted by the -ve potential in the p side and therefore **holes start crossing the junction and land in p side.**
- Similarly electrons (minority carriers) from p side will be attracted by the +ve potential in the n side and therefore **electrons start crossing the junction and land in n side**.

Current flow due to majority carriers is not possible under reverse bias conditions but current flow due to minority carriers is a distinct possibility.

3.2.5 Transistor operation: NPN -- The biasing arrangement for a NPN transistor is shown in figure 3.6

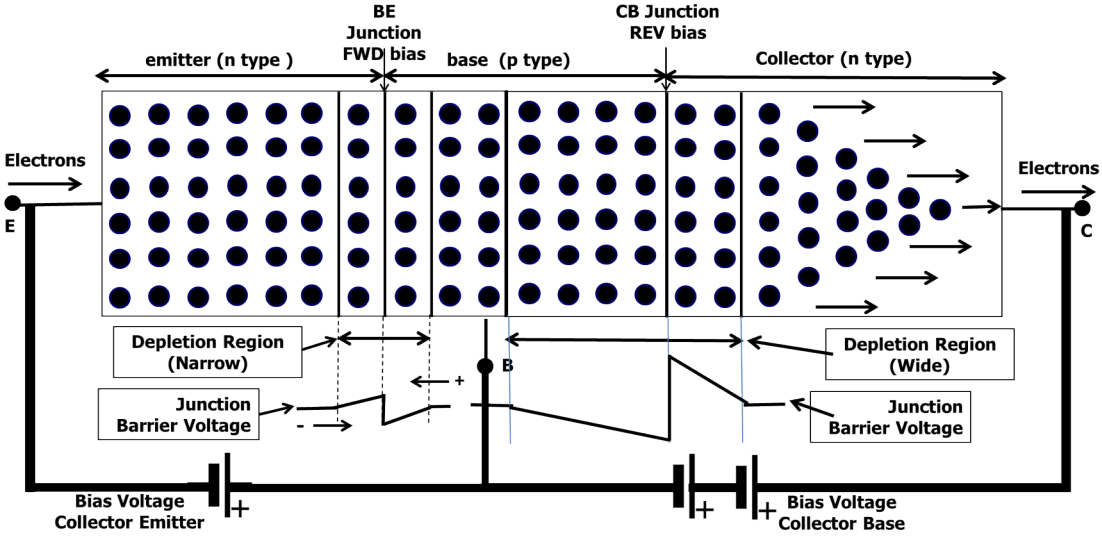
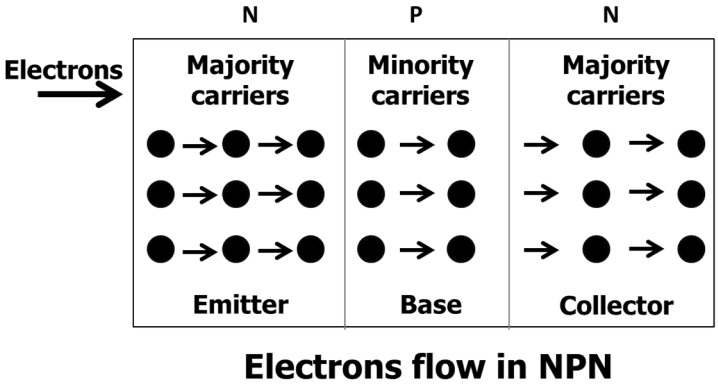


Fig 3.6 Semiconductor Physics of NPN Transistor

Recall:

- Fwd bias junction encourages flow of majority carriers
- Rev bias junction encourages flow of minority carriers
- In a transistor, **emitter and collector are heavily doped and the base is lightly doped. Base region also is very thin.**
- Emitter Base junction is forward biased. Emitter (n) is connected to –ve terminal of the battery and Base (p) is connected to +ve terminal of the battery.
- Current flow due to majority carriers happens. **Electrons from n region are emitted into the base (p) region.**
- This constitutes emitter current (I_E).
- Refer fig 3.7 here.
- **These emitted electrons are now in the base where they are minority carriers.**
- These electrons now see a **reverse bias between base (p) and collector (n). As we saw already, reverse base facilitates minority carrier flow and therefore these electrons are whisked away towards collector.**
- **The base is ultrathin and therefore almost all the electrons which were emitted by the emitter are collected by the collector. There is hardly any loss in the base due to recombination because base is lightly doped.**



- **While the current flow discussion revolves around majority carriers (electrons), the minority carriers (holes) also are involved in the current flow. Therefore these devices are called bipolar junction transistors (BJT).**

Fig 3.7

3.2.6 Carriers flow in Transistors in npn

Refer fig 3.7.

- Electrons are the majority carriers
- Electrons from the emitter cross the Fwd Biased EB into Base.
- This constitutes emitter current (I_E)
- Majority of these Electrons (98 to 99%) transit thro base and thro the rev biased CB into collector. This current is $I_C = 0.98\ I_E$
- That is why base width is kept small (for whisking away)
- Base doping is kept light so that recombination of holes and electrons is less probable. That is why base current is low and
- Very few holes cross from base to emitter

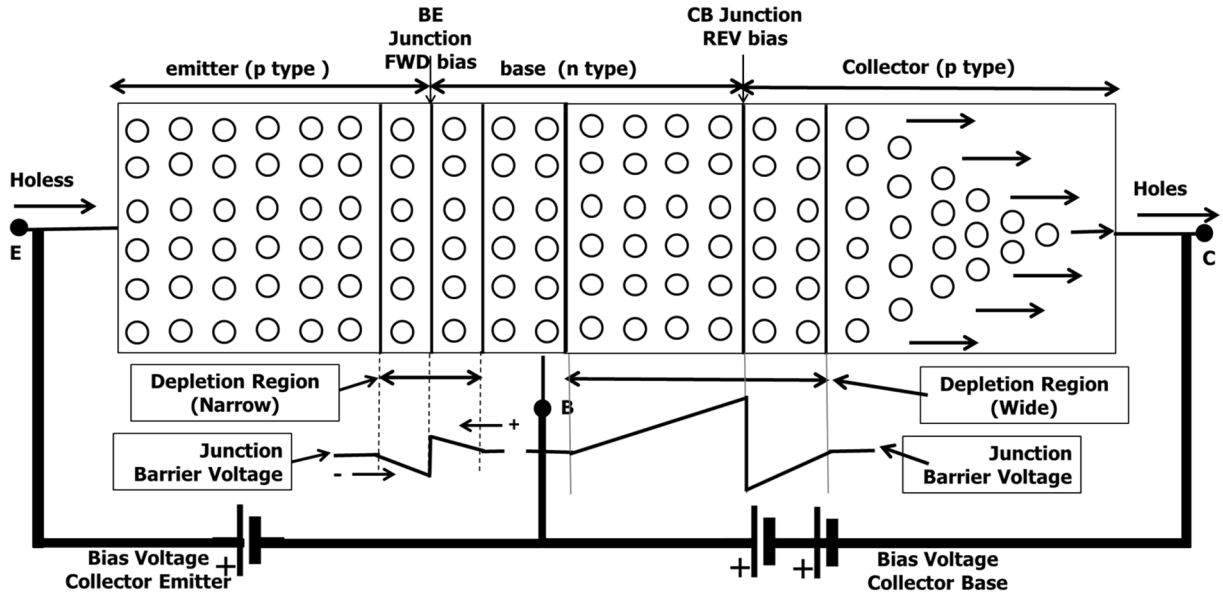
3.2.7 PNP transistor operation

Refer fig 3.8

The biasing arrangement for a NPN transistor is shown in figure

- Emitter Base junction is forward biased. Emitter (p) is connected to +ve terminal of the battery and Base (n) is connected to -ve terminal of the battery.

- Current flow due to majority carriers happens. Holes from p region are e**mitted** into the base (n) region.
- These emitted holes are now in the base where they are minority carriers.
- These holes now see a reverse bias between base (p) and collector (n).
- As we saw already, reverse bias facilitates minority carrier flow and therefore these holes are whisked away towards collector.
- The base is ultrathin and therefore almost all the holes which were emitted by the emitter are collected by the collector.
- There is hardly any loss in the base due to recombination because base is lightly doped.
- While the current flow discussion revolves around majority carriers (holes) the minority
- carriers (electrons) also are involved in the current flow. Therefore these devices are called bipolar junction transistors (BJT).



Semiconductor Physics of PNP Transistor

Fig 3.8

3.2.8 Carriers flow in Transistors in pnp

- Holes are the majority carriers
- Holes from the emitter cross the Fwd Biased EB into Base.
- This constitutes emitter current (I_E)
- Majority of these holes (98 to 99%) transit thro base and thro the rev biased CB into collector. This current is I_C. =0.98 I_E
- That is why base width is kept small (for whisking away)
- Base doping is kept light so that recombination of holes and electrons is less probable. That is why base current is low
- Very few electrons cross from base to emitter

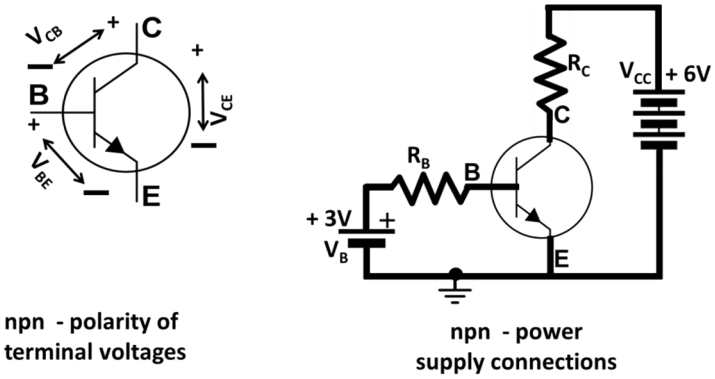
3.3 BJT Voltages and Currents (NPN)

3.3.1 Transistor Voltages:

The biasing arrangements for NPN transistor are shown in the figure 3.9

Base emitter junction : Must be forward biased. Base (p) must be more positive with respect to emitter (n). Note the battery polarity of V_B.

Base Collector junction : Must be reverse biased. Collector (n) must be more positive with respect to base (p) . Note the battery polarity of V_{CC}.



npn - polarity of terminal voltages

npn - power supply connections

Fig 3.9

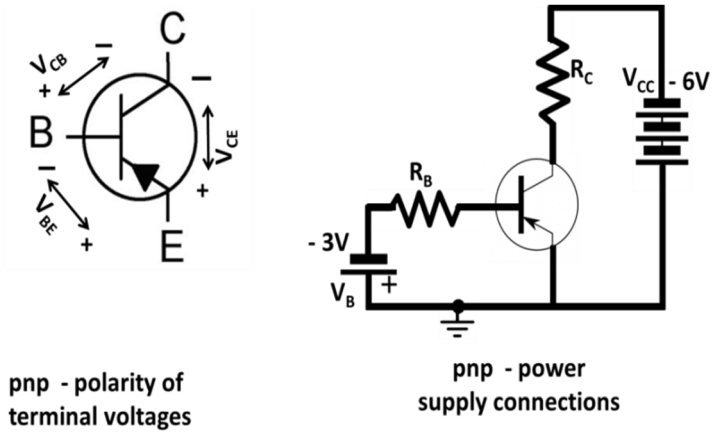
The biasing arrangements for PNP transistor are shown in the figure 3.10.

Base Emitter junction : Must be forward biased. Emitter (p) must be more positive with respect to base (n). Note the battery polarity of V_B.

Base Collector junction : Must be reverse biased. Collector (p) must be more negative with respect to base (n) . Note the battery polarity of V_{CC}

Biasing rules: Collector-base bias (V_{CC}) will always be greater than base bias V_{BB}. This ensures that the CB junction is always reverse biased. In our example, V_B= -3V and V_{cc}= -6V

Current direction: Recall that the arrow indicates emitter and direction of the arrow indicates current flow direction.



pnp - polarity of terminal voltages

pnp - power supply connections

Fig 3.10

.

Resistors R_B and R_C are included in the circuit to limit the base current and collector current to safe limits.

Diode drops: Remember Base - Emitter Diode drop = 0.7V (Si) and 0.3 V (Ge)

3.3.2 Transistor currents:

The figure 3.11 shows the currents that flow in the transistor and the relationship between them. For simplicity, the reverse currents are neglected for this analysis.

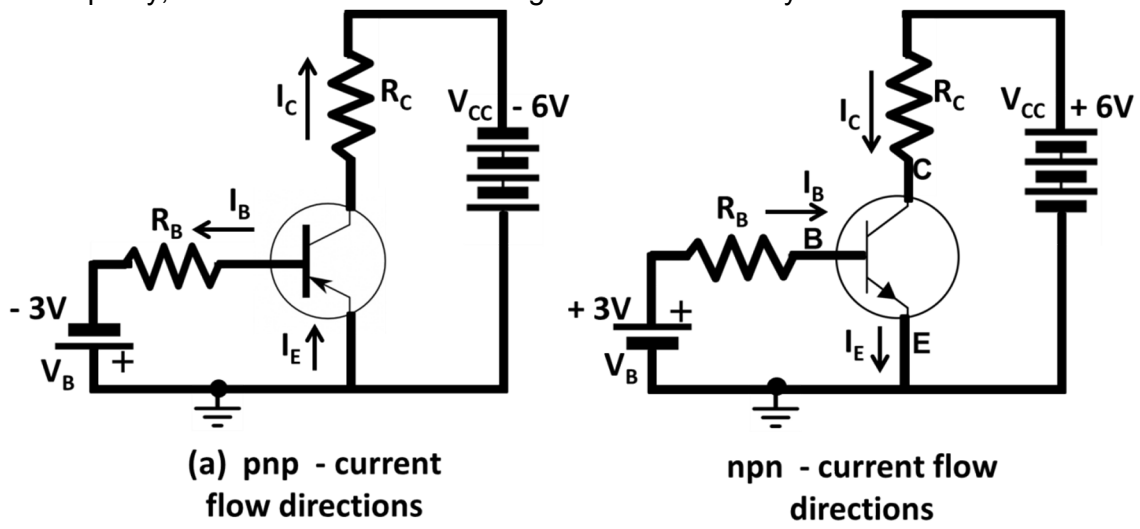


Fig 3.11

What are the different currents in a pnp BJT?

Refer fig 3.11(a). **I_E is the emitter current which flows into the transistor emitter.**
I_B and I_C are the currents that flow out of the transistor.
$I_E = I_B + I_C$
The entire current flow starts from the emitter. We had seen earlier that almost all the holes that originate from emitter reach collector and only a very few holes are lost in the base.

What are the different currents in a npn BJT?

Refer fig 3.11(b). I_C is the collector current which flows into the transistor. I_B is the base current which also flows into the transistor. I_E is the combined current, that flows out of the transistor.

$$I_B + I_C = I_E \qquad 2.5\text{-}1$$

α_{dc} - Emitter to Collector DC current gain

The ratio of the collector current to the emitter current is defined as α. The typical value of α will be between 0.95 to 0.995 (very close to unity)

Emitter to collector DC current gain $= \alpha_{dc} = I_C / I_E$ 2.5-2

or $I_C = \alpha_{dc} I_E$ 2.5-3

α_{dc} is also known as common base current gain

$$I_C = \alpha_{dc} (I_C + I_B) \qquad 2.5\text{-}4$$

Solving, $$I_C = \frac{\alpha_{DC}\ I_B}{(1 - \alpha_{DC})} \qquad 2.5\text{-}5$$

$ß_{dc}$ - Base to Collector DC current gain (h_{FE})

$ß_{dc}$ is another important parameter of transistors. **It is defined as the ratio of collector current to base current. $ß_{dc}$ is also known as h_{FE}**

$$\beta_{dc} = I_C / I_B \qquad 2.5\text{-}6$$

or $$I_C = \beta_{dc} I_B \qquad 2.5\text{-}7$$

Relationship between α_{dc} and $ß_{dc}$

(from 2.5-5) $$I_C = \frac{\alpha_{DC} I_B}{(1-\alpha_{DC})}$$

$$\frac{I_C}{I_B} = \frac{\alpha_{DC}}{(1-\alpha_{DC})}$$

$$\beta_{dc} = \frac{\alpha_{DC}}{(1-\alpha_{DC})} \qquad 2.5\text{-}8$$

or $$\alpha_{dc} = \frac{\beta_{DC}}{(1+\beta_{DC})} \qquad 2.5\text{-}9$$

Problem 3. 1 : A transistor has a α_{dc} of 0.95. The base current is 0.015 mA. Find out I_B, I_C and $ß_{dc}$,

I_B = 0.015 mA = 150 µA. α_{dc} = 0.95

$I_C = \frac{\alpha_{DC} I_B}{(1-\alpha_{DC})} = \frac{0.95\ X\ 150\ \mu A}{1-0.95}$ = 2.85 mA

$I_E = I_C / \alpha_{dc}$ = 2.85 / 0.95 = 3 mA

$\beta_{dc} = \frac{\alpha_{DC}}{(1-\alpha_{DC})} = \frac{0.95}{1-0.95}$ =19

Problem 3. 2: A transistor has a collector current of 10 mA. The base current is 50 µA. Calculate I_E, β_{dc} and α_{dc} of this transistor. If the collector current doubles, what is the new emitter current?

$\beta_{dc} = I_C / I_B$ = 10 mA/ 50 µA = 200

$\alpha_{dc} = \beta_{dc}/(1+\beta_{dc})$ = 200 / (1+200) = 200 / 201 = 0.995

$I_E = I_B + I_C$ = 10 mA + 50 µA = 10 mA + 0.05 mA = 10.05 mA

If collector current doubles, new I_C = 20 mA

New $I_B = I_C / \beta_{dc}$ = 20 mA / 200 = 100 µA

New $I_E = I_B + I_C$ = 20 mA + 100 µA = 20 mA + 0.1 mA = 20.01 mA.

3.4 BJT Amplification

3.4.1 BJT Current Amplification

It is stressed here that the transistor is, a current amplifier.

The **DC current gain $\beta_{dc} = I_C / I_B$** . A small base current produces large collector current. This is a DC parameter. **A small amount of base current variation ΔI_B will produce a large amount of collector current variation as ΔIc.** Therefore

DC Current amplification = $\beta_{dc} = \Delta Ic / \Delta I_B$.

But, amplifiers work on ac mode. Therefore we can **define a new term $\beta_{ac} = I_c / I_b$.**

Convention **: Capital letters for DC parameters and small letters for ac parameters.**

3.4.2 BJT voltage Amplification

In a transistor amplifier,

1. Small variation in base current results in **small variations of base voltage**.
2. However, a small variation in base current results in large variations in collector current.
3. Large variation in collector current leads to **large variations of collector voltage**.

Correlate 1, 2 and 3. **Small variations in base voltage results in large variations in collector voltage. Therefore voltage amplification happens**

Voltage amplification = $\frac{\Delta V_c}{\Delta V_B}$

Conclusions:
Transistor produces current amplification and as a consequence voltage amplification too.

Problem 3.3: What is the voltage amplification of the circuit in fig 3.12?

Base side:
Base voltage variation = ΔV_B = ±30 mV. I_B = 16 µA
From the graph, base current variation = ΔI_B = ± 4 µA variation.
Collector side :
ß =100 (given)
Therefore $I_c = \beta_{dc} \times I_B$ = 100 X 16 µA = 1.6 mA.
The voltage drop across R_c = I_c X R_C
= 1.6 mA X 10K = 16 V
Collector voltage (V_C) = V_{CC} – voltage drop across R_c
= 25 V – 16 V = 9 V
Collector current variation (ΔIc) = ± 4 µA X 100 = ± 400 µA
Collector voltage swing (ΔVc) = ΔIc X R_C
= ± 400 µA X 10000 ohms = ± 4 V
Voltage amplification = $\Delta Vc / \Delta V_B$ = ± 4 V / ± 30 mV = 133.33

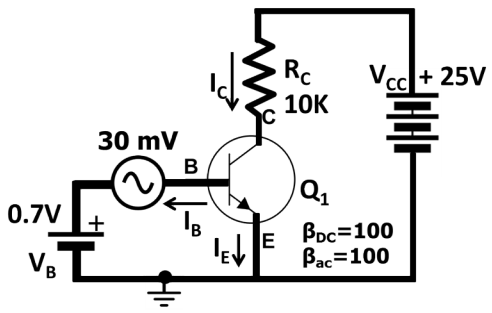
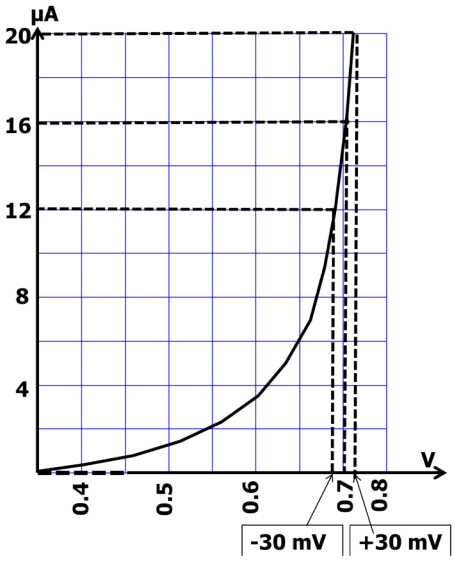


Fig 3.12



Problem 3.4: For the I_B vs V_{BE} characteristics in fig 3.13, what is the voltage gain?

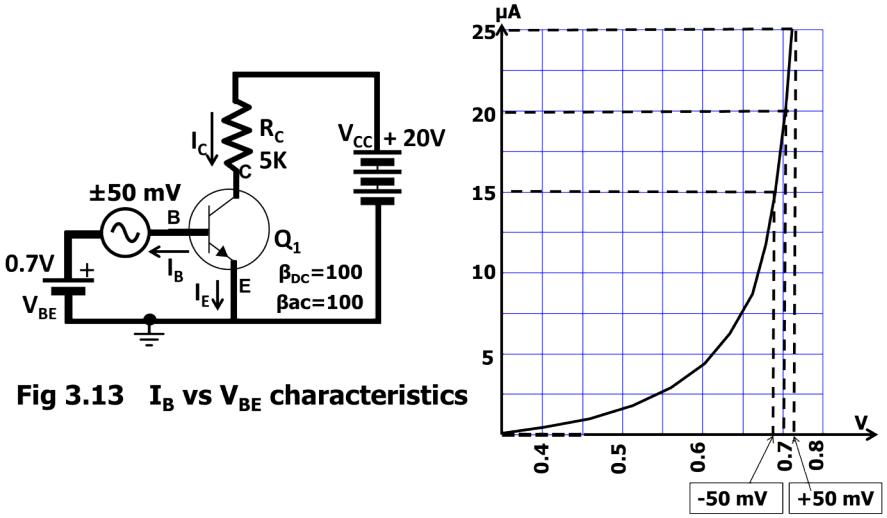


Fig 3.13 I_B vs V_{BE} characteristics

Base side:

Base voltage variation = ΔV_B = ± 50 mV, I_B = 20 μA

From the graph, base current variation = ΔI_B = ± 5 μA variation.

Collector side :

β_{dc} =100 (given), I_B = 20 μA,

Therefore $I_c = \beta_{dc} \times I_B$ = 100 X 20 μA = 2 mA.

The voltage drop across R_c = I_c X R_C
= 2 mA X 5K = 10 V

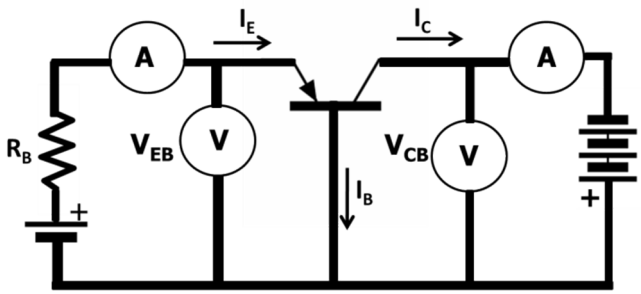
Collector voltage (V_C) = V_{CC} – voltage drop across R_c
= 20 V – 10 V = 10 V

Collector current variation (ΔIc) = ΔI_B X β_{ac}
= ± 5 μA X 100 = ± 500 μA

Collector voltage swing : ΔVc = ΔIc X R_C
= ± 500 μA X 5000 ohms (Since R_C = 5K)
= ± 2.5 V

Voltage amplification = $\Delta Vc / \Delta V_B$ = ± 2.5 V / ± 50 mV = 50

3.5 Common Base Characteristics



Test set up for measurement of Common Base Characteristics

Fig 3.14

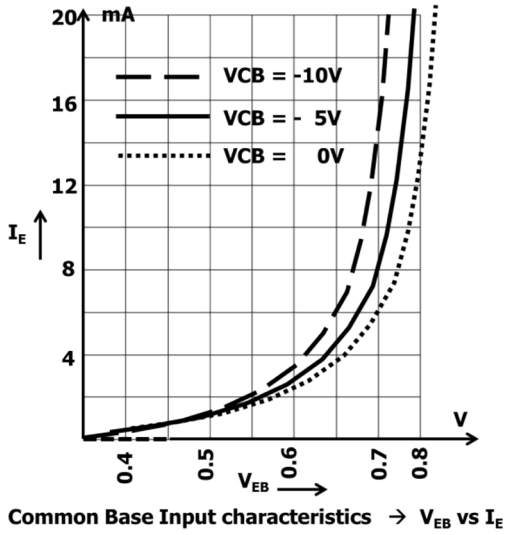
Figure 3.14 shows a pnp transistor in common base configuration. **The base is common to both input and output terminals.**

Common base characteristics deals with two analyses

- Study of input characteristics
- Study of output characteristics

Characteristics	X axis	Y axis	Variable
Input	V_{EB}	I_E	V_{CB}
Output	V_{CB}	I_C	I_E

3.5.1 Common Base Input Characteristics



Common Base Input characteristics → V_{EB} vs I_E

Fig 3.15

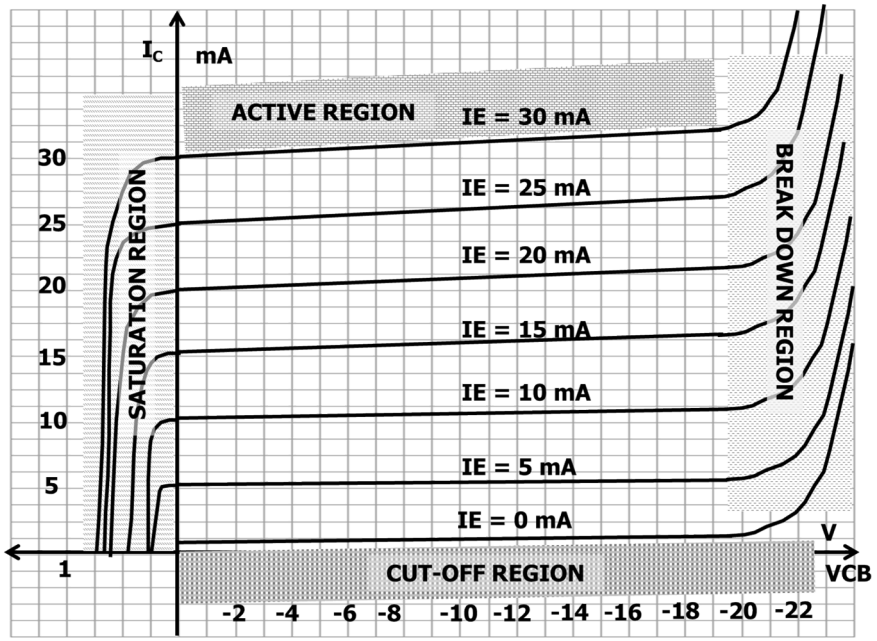
Experiment.

1. Make the connections as per circuit in fig 3.14.
2. Keep V_{CB} at 0 V
3. Vary V_{EB} from 0.3 to 0.75 V & note I_E
4. Ensure V_{CB} does not vary
5. Plot the curve
6. Repeat 2 to 5 for other values of V_{CB}

Input characteristics is a plot of, input voltage (V_{EB}) in X axis and Input current (I_E) in Y axis, for various constant values of collector-base voltages.. It is similar to, a forward-biased diode characteristic.

The curve also shows that as the emitter base voltage is increased, emitter current increases.

3.5.2 Common Base output Characteristics



Common Base Output Characteristics V_{CB} vs I_C

Fig 3.16

Experiment.

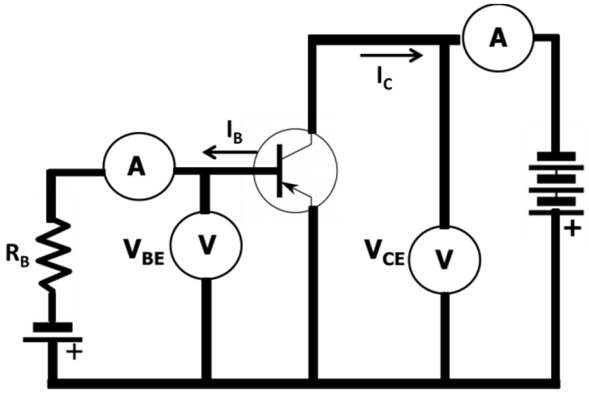
1. Make the connections as per circuit in fig 3.14.
2. Keep I_E at 1 mA.
3. Vary V_{CB} from 0 to -20 V for pnp (0 to +20 V for npn). Measure I_C
4. Ensure I_E does not vary.
5. Plot the curve.
6. Repeat 2 to 5 for other values of I_E.

Output characteristics is a plot of output voltage (V_{CB}) in X axis and output current (I_C) in Y axis, for various constant values of emitter currents.. The graph can be divided into four regions.

1. **Active region:**
   - **E-B junction forward bias. C-B junction reverse bias.**
   - In this region **collector current is almost equal to emitter current.**
   - Output current **(I_C) remains constant for a wide range of output voltage (V_{CB})**
2. **Saturation region:**
   - When output voltage **(V_{CB}) is zero, the output current (I_C) still flows**, mainly due to flow of minority carriers.
   - Output current **(I_C) becomes zero only when Collector base is forward biased**.
3. **Break down region:**
   - When **reverse bias increases beyond maximum permissible voltage, collector base junction breaks down.**
   - This is due to a condition known as **Punch Through** where collector-base depletion region penetrates too far into the base and meets emitter base depletion region.
4. **Cut-off region:**

The region below I_E=0, is known as cut off region. Transistor gets cut off. **Both collector base junction and emitter base junction are reverse biased**

3.6 Common Emitter Characteristics



Test set up for measurement of Common Emitter Characteristics

Fig 3.17

Figure 3.17, shows a pnp transistor in common emitter configuration. The emitter is common to both input and output terminals.

Common emitter characteristics deals with two analyses

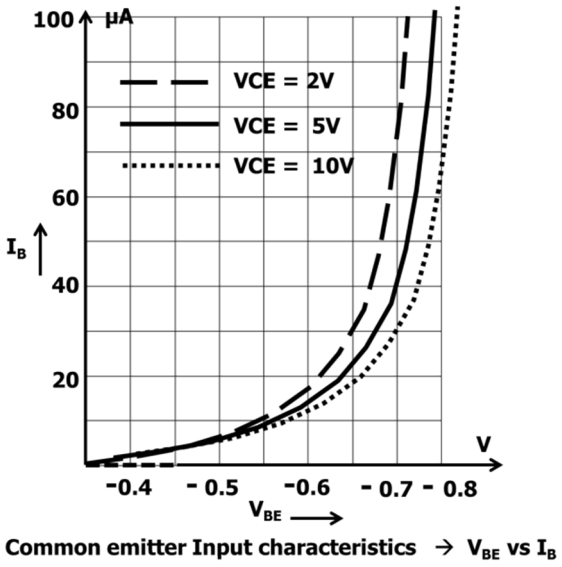
- Study of input characteristics
- Study of output characteristics

Characteristics	X axis	Y axis	Variable
Input	V_{BE}	I_B	V_{CE}
Output	V_{CE}	I_C	I_B

3.6.1 Common Emitter input Characteristics

Experiment.

1. Make the connections as per circuit in fig 3.17.
2. Keep V_{CE} at 2 V
3. Vary V_{BE} from 0.3 to 0.75 V and note I_B
4. Ensure V_{CE} does not vary
5. Plot the curve
6. Repeat 2 to 5 for other values of V_{CE}



Common emitter Input characteristics → V_{BE} vs I_B

Fig 3.18

- Input characteristics (fig 3.18) is a plot of input voltage (V_{BE}) in X axis and Input current (I_B) in Y axis, for various constant values of collector-emitter voltages. It is also similar to a forward-biased diode characteristic
- The curve also shows that as the base emitter voltage is increased, base current increases beyond the knee voltage. **(Knee voltage is 0.7V for silicon and 0.3V for Germanium).**
- I_B reduces as V_{CE} is increased.

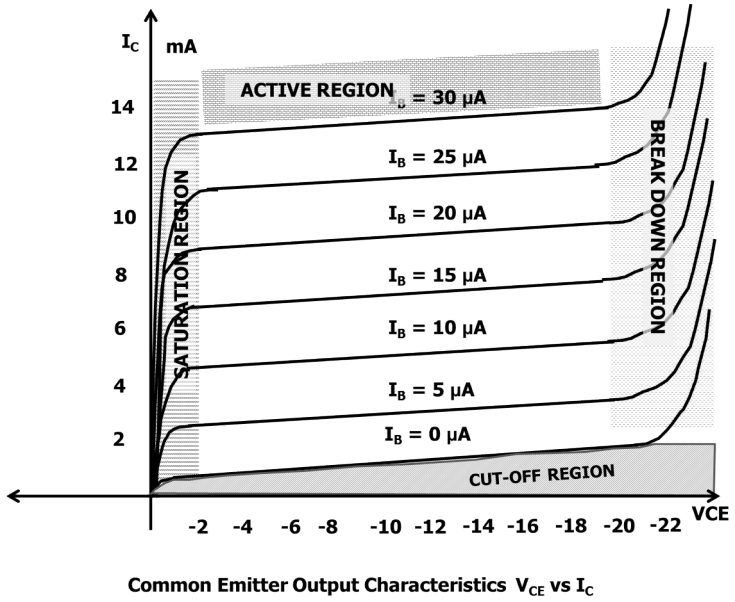
3.6.2 Common Emitter output Characteristics

Experiment.

1. Make the connections as per circuit in fig 3.17.
2. Keep I_B at 0 μA
3. Vary V_{CE} from 0 to -20V for pnp (0 to +20V for npn). Measure I_C
4. Ensure I_B does not vary
5. Plot the curve
6. Repeat 2 to 5 for other values of I_B

Output characteristics (fig 3.19) is a plot of output voltage (V_{CE}) in X axis and output current (I_C) in Y axis. The graph can be divided into four regions

1. **Active region:**
   - **E-B junction forward bias. C-B junction reverse bias.**
   - In this region output current (I_C) increases gradually, as output voltage (V_{CE}) increases.
   - This is the linear region suitable for amplifiers.
2. **Saturation region:**
   - **E-B junction forward bias. C-B junction forward bias.**
   - When output voltage (V_{CE}) is zero, the output current (I_C) is zero.
   - **V_{CE} at saturation is 0.3V for Silicon and 0.1V for Germanium**



Common Emitter Output Characteristics V_{CE} vs I_C

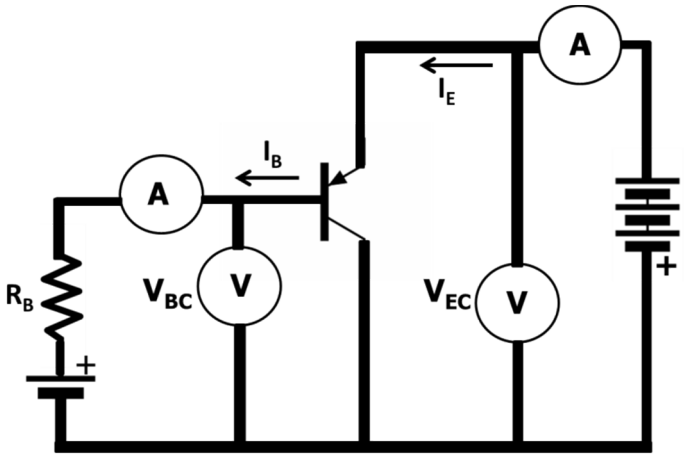
Fig 3.19

3. **Break down region:**
- When reverse bias increases beyond maximum permissible voltage, collector base junction breaks down.
- This is due to a condition known as Punch Through where collector-base depletion region penetrates too far into the base and meets emitter base depletion region.

4. **Cut-off region:**
- The region below I_B=0 is known as cut off region. Transistor gets cut off. **Both collector base junction and emitter base junction are reverse biased**

3.7 Common Collector Characteristics

Common collector amplifier is also known as **emitter follower. Refer fig 3.20**
Difficult to set up this experiment since I_B is very sensitive and keeps changing



Test set up for measurement of Common Collector Characteristics

Fig 3.20

Input characteristics in fig 3.21, is a plot of input voltage (V_{CB}) in X axis and Input current (I_B) in Y axis, for various constant values of collector-emitter voltages.

The characteristic exhibits a different behaviour than CB or CE configuration.

BC Junction (input) is fwd biased and CE Junction (output) is reverse biased.
We can see $\mathbf{V_{CE} = V_{CB} + V_{BE}}$
$\mathbf{V_{CB} = V_{CE} - V_{BE}}$

3.7.1 Common Collector Input Characteristics

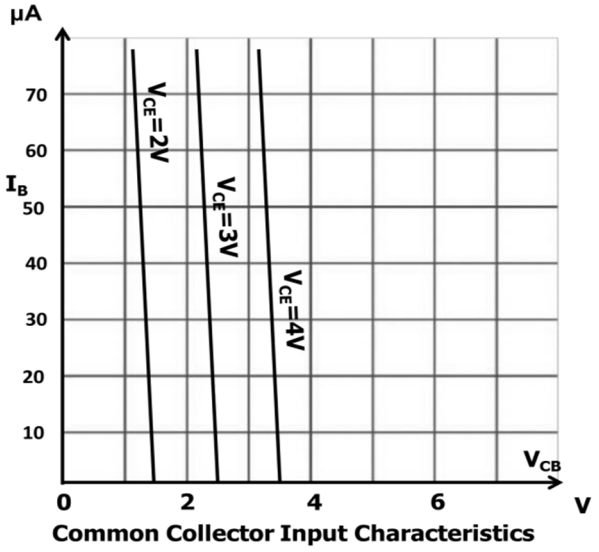


Fig 3.21

3.7.2 Common collector Output characteristics: Refer fig 3.22 . It is very much similar to Common emitter output characteristics in all respects

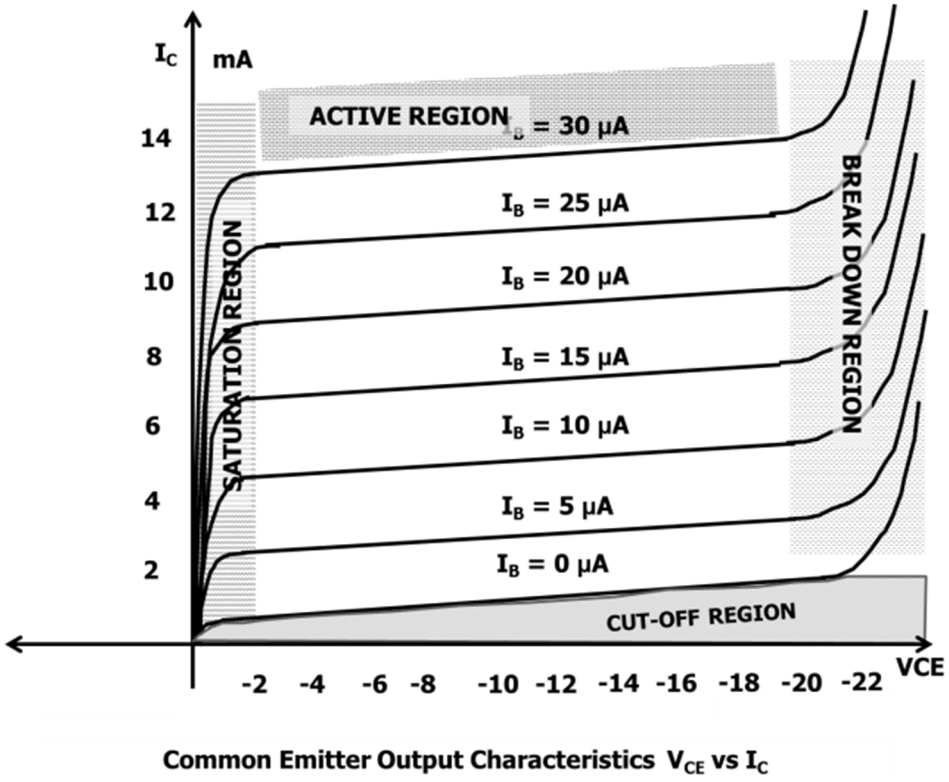


Fig 3.22

Chapter 4: BJT Biasing

Syllabus: BJT Biasing (Text-1) : DC Load line and Bias Point, Base Bias, Voltage divider Bias, Numerical examples as applicable.

4.1 Design Introduction

What are the design issues in transistor biasing?

- DC voltages of C,B and E **should be stable** and constant
- DC currents I_C, I_B and I_E **should be stable** and constant

What is a Q point?

Q point is known as **DC operating point or quiescent point**. It specifies the operating point of a transistor based on its circuit design. It is specified in terms of the value of **I_C and V_{CE}, with no input signal applied.**

- DC operating point or a **Q point always needs to be specified** for a transistor circuit.

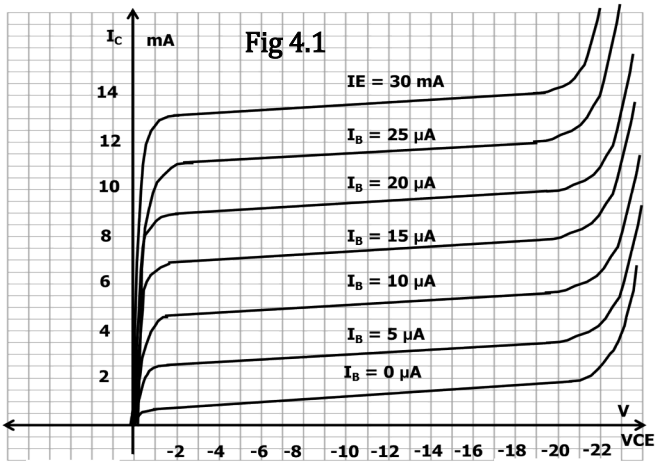
Can a bias voltage or bias current remain constant? No. Why?

- **β (h_{FE}) variations and temp variations result in bias variations**

If the bias voltage can be made stable, Q point can be stabilized and designs can exhibit predictable behavior.

What is a load line?

- **Load line is a straight line drawn on, BJT output characteristics (**Refer fig 4.1**)**
- Recall BJT O/P characteristics is a graph, with **V_{CE} on the x axis and I_C** on the y axis
- **Therefore any point on the load line, has coordinates (V_{CE}, I_C)**



What is a load line for Common Emitter circuit?

It is a graph of **I_C vs V_{CE} (R_C and V_{CC} fixed)**

Why load line?

Load line gives a **complete analysis of all Q points** possible in a transistor circuit.

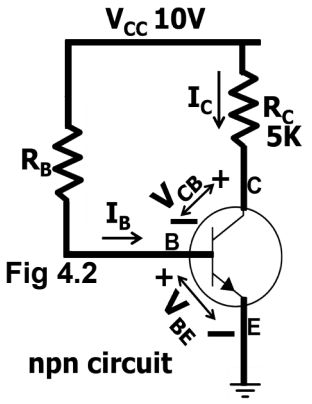


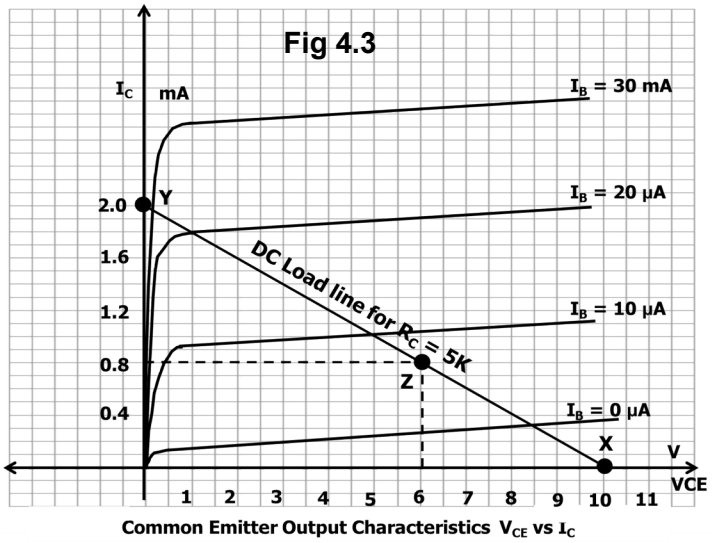
Fig 4.2

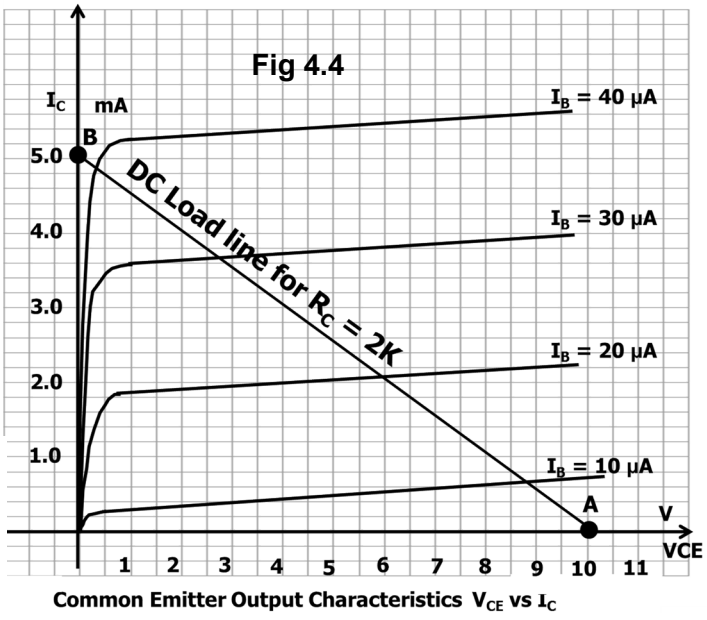
What is biasing and what are the biasing issues?

Look at fig.4.2. In the circuit, BE Junction is

forward biased and CB junction is reverse biased.

- For a transistor to operate as per design, **external DC voltages (V_{CC} Power supply) need to be applied**. The voltages should be of the **correct polarity and permissible magnitude for EB junction and CB junction**. This is known as **biasing**
- Emitter Base junction needs to be forward biased and Collector Base junction needs to be reverse biased. (0.7V for silicon or 0.3 V for gemanium need to be ensured)
- **The operating point of a transistor, has to be preferably at the center ($V_{CE} = V_{CC}/2$),** for maximum voltage swing on either side.
- The bias needs to be stabilised. The bias point should not vary due to temperature variations or β variations or input mains supply variations





What are the basic biasing techniques?

Three popular methods are used. They are**, Base bias, Collector to Base bias and Voltage Divider bias**.

4,2 DC Load line and Bias point

Problem 4.1: Draw a DC load line for the circuit shown in fig 4.2 for a V_{CC} =10 V

$V_{CE} = V_{CC}$ – Voltage drop across R_C

$= V_{CC} – I_C R_C$

When V_{BE} = 0 V,

Transistor does not conduct. $I_C = 0$

V_{CE} = 10 V – (0 mA X 5 K ohm)

= 10 V.

Refer fig 4.3. Mark point X = 10 V on the X axis

When V_{BE} = 0.7 V

Transistor conducts. V_{CE} becomes zero

0 = 10 V – (I_C X 5 K ohm).

I_C = 2 mA. Mark point Y = (0 V, 2 mA) on the Y axis.

Recall, any point on the load line has the coordinates (V_{CE}, I_C). Join XY and this line is the DC load line for this circuit. If any one of these circuit parameters vary, a new load line is to be drawn.

What is the Q point at Z in fig 4.3?

I_C= 0.8 mA and V_{CE} = 6 V

Problem 4.2: Draw the new DC load line for the circuit in fig 4.2, when R_C = 2K

$V_{CE} = V_{CC} – I_C X R_C$

Case1 :

V_{BE} =0, BJT → Not conducting, I_C = 0

V_{CE} = 10 V – 0 mA X 2 K = 10 V

Point A on load line will be (10 V, 0 mA)

Case 2:

V_{CE} = 0 V

0V = 10V – I_C X 2 K $\therefore I_C$ = 5 mA

Point B on load line will be (0V, 5 mA)

Draw AB…….This is the load line **for THIS circuit**.

4.2.1 Q point (quiescent point) of a transistor

What is a Q point of a transistor?

It is the DC Point of the transistor in a given circuit**. It describes its operating point, in terms of (VCE, IC) coordinates.** Ref fig 4.5 which is basically same a s fig 4.4.

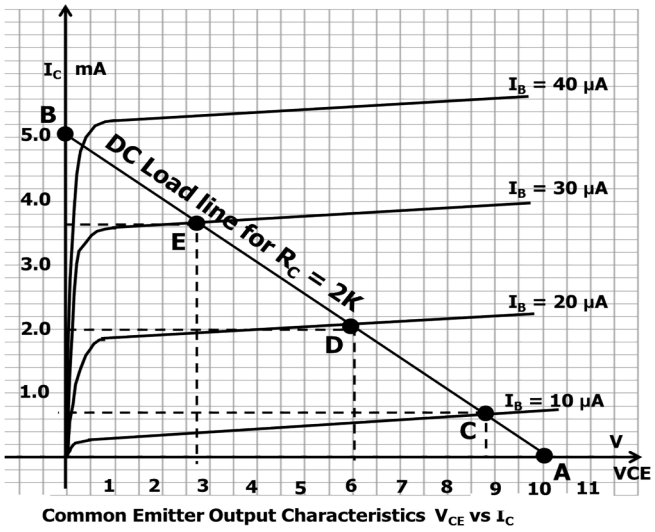


Fig 4.5

Q points analysis			
Q point	**I_B (µA)**	**V_{CE} (V)**	**I_C (mA)**
A	**0**	**10**	**0**
B	**xx**	**0**	**5**
C	**10**	**8.8**	**0.7**
D	**20**	**6.0.**	**2.0.**
E	**30**	**2.7**	**3.6**

Fig 4.6

Graph illustrates the relationship between the various Q points and **how they are related to the important circuit parameters such as I_B, I_C and V_{CE}**

The excel table (fig 4.6) tabulates five Q points (A, B, C, D, E) in the graph, in terms of these parameters.

4.2.2 What are the inferences?

1. When base current varies between 10 µA and 30 µA, V_{CE} varies between 2.7 V and 8.8 V.
2. At extreme points (A and B), the V_{CE} Swings between V_{cc} and 0 V.
3. The best Q point should preferably be, therefore at $V_{CC}/2$
4. The collector current varies between 5.0 mA (saturation) and 0 mA (cut-off).
5. Small variations in base current (10 µA to 30 µA) causes large variations in V_{CE} (2.7 V to 8.8 V)
6. Small variations in base current (10 µA to 30 µA) causes large variations in collector current I_C (0.7 mA to 3.6 mA). **Transistor is a current amplifier**

4.2.3 Q point – 2 conditions

This figure 4.7 illustrates two extremes of the Q point variations and the end points of the DC load line.

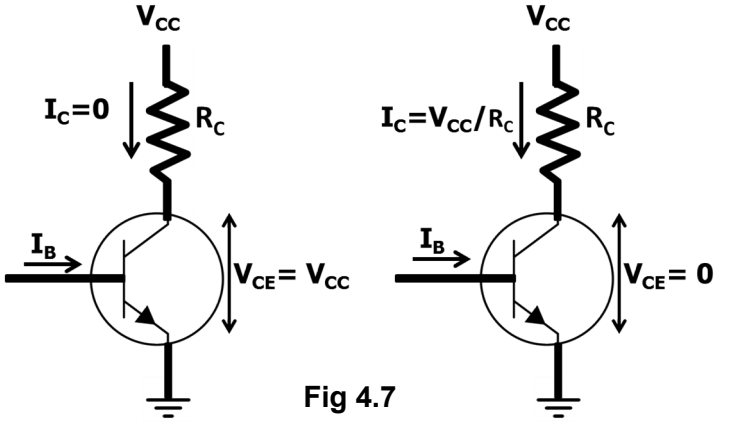


Fig 4.7

Q Point extremes (useful for drawing the load line)
(a) when $I_C=0$, $V_{CE}= V_{CC}$, (b)when $V_{CE}= 0$, $I_C=V_{CC}/R_C$

4.3 Base Bias

Problem 4.3: What is the Q point for this Germanium transistor in fig 4.8 ? Draw the DC load line. (β =100.)
V_{BE} = 0.3V (Germanium)

(a) Find I_B
Apply KVL
$VCC – (I_B X R_2) – V_{BE} = 0$
$10V – (I_B X 470 K) - 0.3 V = 0$
$\therefore I_B = 20.6$ mA

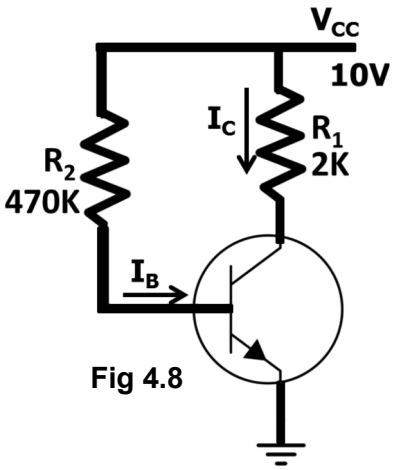


Fig 4.8

base bias

(b) Find I_c

$I_C = \beta \times I_B = 20.6\ mA \times 100 =$ **2.1 mA (Q point: I_C)**

(c) Find collector voltage V_c

$V_{CE} = V_{cc} - (I_C \times R_1)$

$= 10\ V - (2.1\ mA \times 2000\ \Omega)$

= **5.8 V (Q point : VCE)**

Therefore, Q point is **(5.8 V , 2.1 mA)**

(d) How to draw load line?

Point A : When $I_c = 0$, $V_{CE} = V_{CC} = 10V$, **A = (10 , 0)**

Point B : when $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_2} = \frac{10\ V}{2K} = 5$ mA, **B = (0 , 5)**

Draw AB. The load line is shown in fig 4.9. Q point, as calculated = (5.8 V , 2.1 mA)

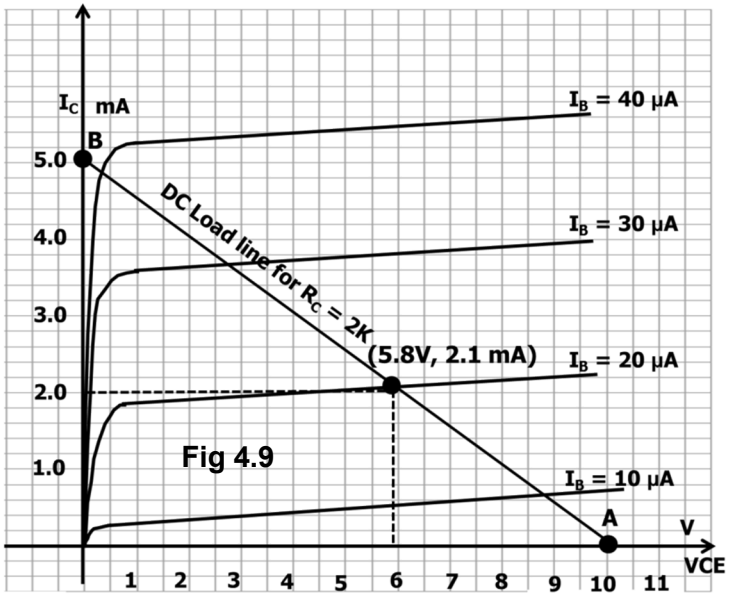


Fig 4.9

Q point (5.8V, 2.1 mA)

Problem 4.4: What is the Q point of this circuit in fig 4.10 and what is the emitter current? Assume silicon transistor.

V_{BE} = 0.7 V (Si)

(a) **Base current**

$V_1 - (I_B \times R1) - 0.7\ V = 0$

$4V - (I_B \times 330\ K) - 0.7 = 0$

$I_B = \frac{3.3\ V}{330\ K}$ = **10 µA**

b) Collector current (I_C)

$I_C = I_B \times \beta = 10\ \mu A \times 200 = 2\ mA$

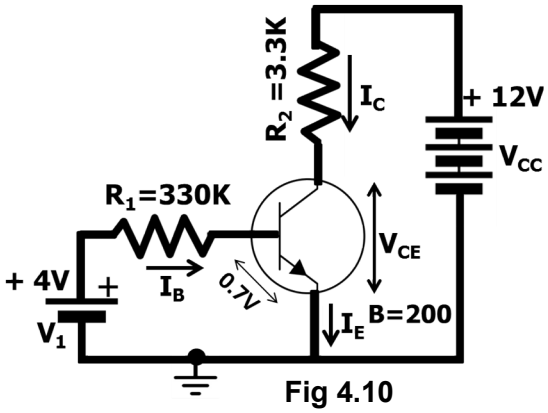


Fig 4.10

(c) V_{CE}

V_{CE} = V_{CC} – I_C X R2

= 12 V –2 mA X 3300 Ω = **5.4 V**

∴Q point = (V_{CE} , I_C) = (5.4 V, 2 mA)

(d) Emitter current

$I_E = I_B + I_C$ = 2 mA + 10 mA = 2.01 mA.

Problem 4.5: Look at the pnp. Silicon transistor in fig 4.11. β=100. Find all the currents and value of R2, given the condition $V_{EC} = \frac{V_{CC}}{2}$

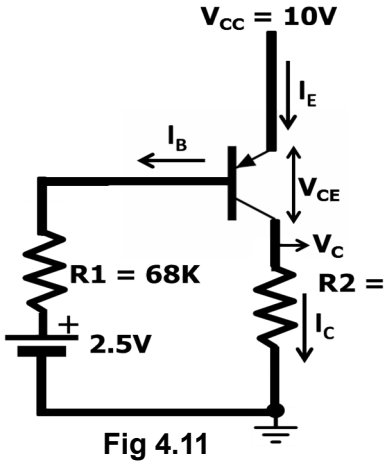


Fig 4.11

(a) Find I_B

V_{EB} = 0.7 V (Silicon)

V_B = V_{CC} – V_{EB} = 10 V - 0.7 V = 9.3 V

Voltage across R1 = 9.3 V – 2.5 V = 6.8 V

$\therefore I_B = \frac{6.8\ V}{68K}$ = 100 μA

(b) Find I_C

I_C = I_B X β

=100 μA X 100 =10 mA.

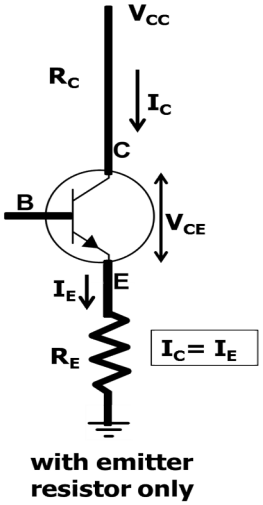
(c) Find R2

V_{CC} = 10 V,

V_{EC} = $\frac{V_{CC}}{2}$ (given) = $\frac{10\ V}{2}$ = 5 V

V_C (at collector) =10 V - 5 V = 5 V

R2 = $\frac{V_C}{I_C}$ = $\frac{5\ V}{10\ mA}$ = 500 Ω



with emitter resistor only

Fig 4.12

d) Emitter current

I_E = I_C + I_B

= 10 mA +100 μA

= 10.1 mA

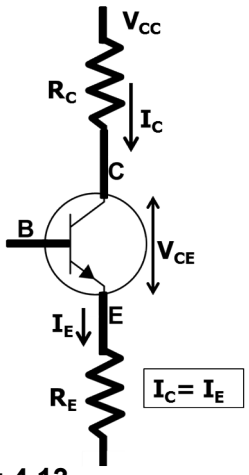


Fig 4.13

4.3.1 Effect of emitter resistor

Look at this circuit. fig 4.12.

There is no resistor in the collector but there is an emitter resistor R_E. **What is the dc load line (R_L), for this circuit ?**

Let I_E be the emitter current

Applying KVL, $V_{CC} - V_{CE} - I_E R_E = 0$

Load line for this circuit

Point B : When V_{CE} =O, **I_E = $\frac{V_{CC}}{R_E}$**

Point A : When I_E =0, $V_{cc} = V_{CE}$
Look at this circuit fig 4.13.

There are two resistors, R_C and R_E .

What will be the dc load line (R_L) for this circuit?
For this circuit, the total dc load resistance = $\mathbf{R_c + R_E}$.
We need to make an assumption that $\mathbf{I_C = I_E}$ **(neglecting base current)**
Applying KVL , $V_{CC} - I_C R_C - V_{CE} - I_c R_E = 0$

Load line for this circuit
Point A : When I_C =0, $V_{CC} = V_{CE}$
Point B : When V_{CE} =0, $I_C = \frac{\mathbf{V_{CC}}}{\mathbf{R_C + R_E}}$

Problem 4.6: Draw DC load line for this circuit in fig 4.14. What is the Q point ? Assume Germanium transistor, and assume β = 99. Find the Q point also.

Apply KVL to base circuit
$V_{CC} - (I_B \text{ X } R_B) - V_{BE} - (I_E \text{ X } R_E) = 0$
$I_E = I_C + I_B = (\beta . I_B) + I_B = I_B (\beta+1)$ (since $I_C = \beta . I_B$)
$\therefore V_{CC} - (I_B \text{ X } R_B) - V_{BE} - (\beta+1)\, I_B . R_E = 0$

$$\mathbf{I_B} = \frac{\mathbf{V_{CC} - V_{BE}}}{\mathbf{R_B + R_E\,(\beta+1)}}$$

$$= \frac{12 - 0.3 \text{ V}}{150\text{K} + (99+1)\ 1\text{K}} = \frac{11.7 \text{ V}}{250 \text{ K}} = 47 \ \mu\text{A}$$

$I_C = \beta \text{ X } I_B = 47\ \mu\text{A X } 99 =$ **4.6 mA (Q point)**

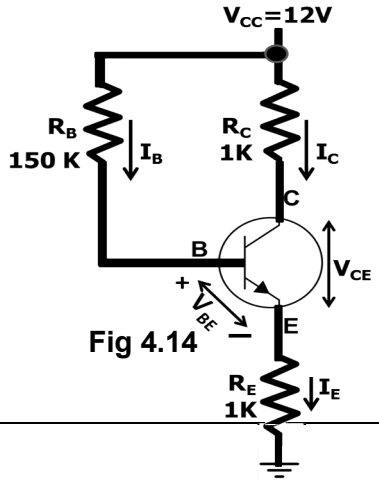


Fig 4.14

$I_E = I_B + I_C = 47\ \mu\text{A} + 4.6 \text{ mA} = 4.65 \text{ mA}$

Apply KVL to collector circuit
$V_{CC} - (I_C \text{ X } R_C) - V_{CE} - (I_E \text{ X } R_E) = 0$
$12 \text{ V} - (4.6 \text{ mA X } 1\text{K}) - V_{CE} - (4.65 \text{ mA X } 1\text{K}) = 0$
V_{CE} = 12 V – 4.6 V – 4.65 V
= **2.75 V (Q Point)**
$\therefore$ **Q point = (2.75 V, 4.6 mA)**

Load line

Point A : When I_c = 0, $V_{CE} = V_{CC}$ = 12 V
Point B: When V_{CE} =0, $I_C = \frac{\mathbf{V_{CC}}}{\mathbf{R_C + R_E}} = \frac{12 \text{ V}}{2\text{K}}$ = 6 mA

4.3.2 Effect of β variations.

Problem 4.7: Calculate two Q points for the base bias circuit shown in fig 4.15, when h_{FE} = 50 and h_{FE} = 100. Assume Silicon transistor. V_{BE} = 0.7 V (Si).

$I_B = \frac{V_{CC} - V_{BE}}{R_1} = \frac{5 - 0.7\ V}{4\ 30K} = 10\ \mu A$

h_{FE} = 50	h_{FE} = 100
$I_C = I_B X\ h_{FE}$ $=10\ \mu A X\ 50 = 0.5\ mA$	$I_C = I_B X\ h_{FE}$ $= 10\ \mu A X\ 100 = 1\ mA$
$V_{CE} = V_{CC} - (I_C X\ R1)$ $= 5\ V - 0.5\ mA X\ 2K$ $= 4\ V$	$V_{CE} = V_{CC} - (I_C X\ R1)$ $= 5\ V - (1\ mA X\ 2K)$ $= 3\ V$
Q Point = (4 V, 0.5 mA)	**Q point (3 V, 1 mA)**

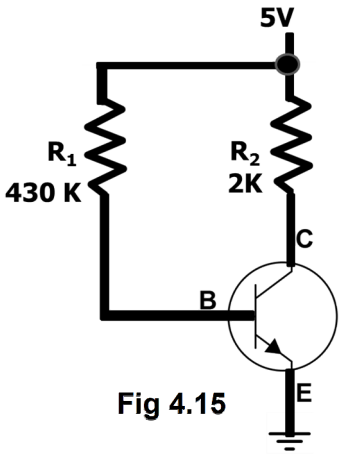


Fig 4.15

4.4 Collector to base bias (npn)

The collector to base bias circuit is shown in fig 4.16.

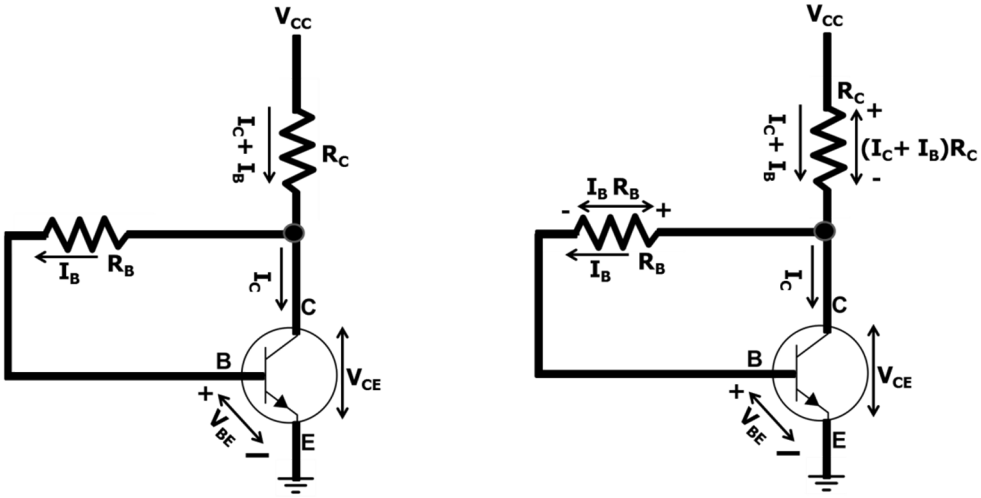


Fig 4.16

From base side

$V_{CE} = I_B R_B + V_{BE}$ 4.4.1

$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ 4.4.2

From collector side

$V_{CE} = V_{CC} - (I_C + I_B) R_C$ 4.4.3

Self-stabilizing action

Collector to base works in a self-correction mode and has good bias stability.

- If I_c increases for some reason, drop across R_C increases
- Therefore V_{CE} drops.
- Because V_{CE} drops, I_B decreases.
- Because I_B decreases, I_C decreases.

Conclusion : If I_C tends to increase, the loop prevents this tendency

Equating both 4.4.1 and 4.4.3,
$I_B R_B + V_{BE} = V_{CC} - (I_C + I_B).R_C$
Substituting $I_C = \beta I_B$
$\therefore I_B R_B + V_{BE} = V_{CC} - [(\beta I_B + I_B).R_C]$

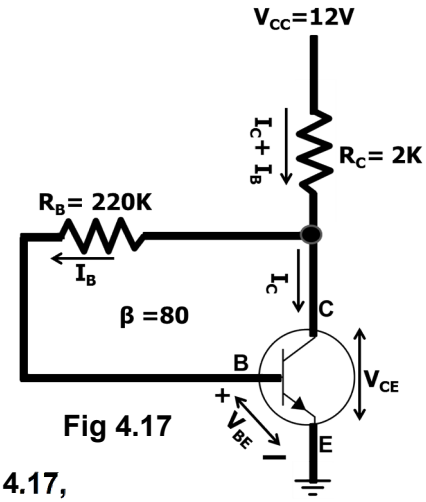


Fig 4.17

$I_B R_B + [\, I_B (\beta + 1) R_C\,] = V_{CC} - V_{BE}$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C(\beta + 1)}$$

Problem 4.8: For the germanium transistor circuit in fig 4.17, with collector-to-base bias, determine I_B, I_C, I_E, V_{CE} and Q point.

V_{BE} = 0.3 V (Ger)

$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C(\beta + 1)} = \frac{12 - 0.3\ V}{220K + 2K\,(80 + 1)}$ = 31 μA

$I_C = \beta I_B$ = 80 X 31 μA = 2.48 mA

$I_E = I_B + I_C$ = 31 μA + 2.48 mA = 2.511 mA **(how?)**

$V_{CE} = V_{CC} - R_C (I_C + I_B)$
= 12 V – 2K (2.48 mA + 31 mA)
= 7.0 V.

Q point = (V_{CE}, I_C) = (7.0 V, 228 mA)

Collector to base bias (PNP) : C to B biasing of pnp is shown in fig 4.18. Reader may analyse the circuit.

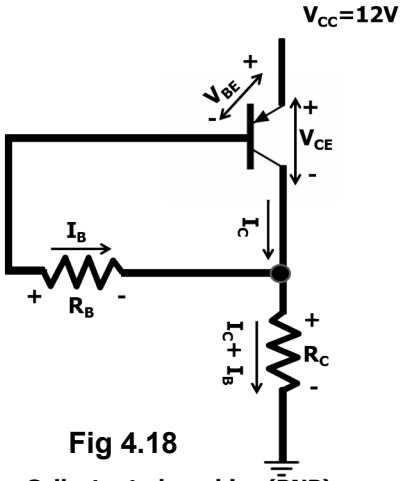


Fig 4.18
Collector to base bias (PNP)

4.5 Voltage divider biasing

It is the **most stable biasing technique**.
Look at the figure 4.19.
Two resistors R1 and R2 are connected in the base circuit, as potential divider. The current and voltage relationships are in the figure 4.19.

1) $V_B = \frac{V_{CC} \times R2}{R_1 + R_2}$ (5 - 7.1)
2) $V_E = V_B - V_{BE}$ (5 - 7.2)
3) $I_E = \frac{V_E}{R_E} = \frac{V_B - V_{BE}}{R_E}$ (5 - 7.3)
Assume $I_E = I_C$ (neglect I_B)
5) $V_C = V_{cc} - I_C R_C$ (5 - 7.4)
4) $I_C = I_E$
6) $V_{CE} = V_C - V_E$ (5 - 7.5)
7) $V_{CE} = V_{cc} - I_C (R_C + R_E)$ (5 - 7.6)

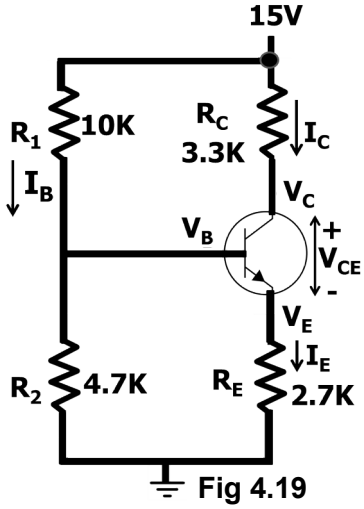


Fig 4.19
Voltage Divider Bias

Circuit analysis –voltage divider bias
Let us analyse the circuit with a numerical example below.

Problem 4.9: Approximate analysis

Analyze this circuit. Neglect I_B. Find V_B, V_C, V_E, I_B, I_C, I_E and V_{CE} (silicon transistor).

1) $V_B = \frac{V_{CC} \text{ X } R2}{R_1 + R_2} = \frac{15V \text{ X } 4.7K}{10K + 4.7K}$ = **4.8 V**

2) $V_E = V_B - V_{BE} = 4.8 - 0.7$ = **4.1 V**

3) $I_E = \frac{V_E}{R_E} = \frac{4.1V}{2{,}7K}$ = **1.5 mA**

Assume $I_E = I_C$ (Neglect I_B)

(4) $\therefore I_C$ = 1.5 mA

(5) $V_C = V_{cc} - I_c R_c = 15\text{ V} - (1.5\text{ mA X } 3.3\text{ K})$ = **10 V**

(6) $V_{CE} = V_C - V_E = 10\text{ V} - 4.1\text{ V}$ = **5.9 V**

Q point = (5.9 V, 1.5 mA)

Thevenin Analysis → precise analysis

How to determine a Thevenin's equivalent circuit ?

Assume $h_{FE} = \beta = 50$

Problem 4.10: Analyze the same circuit precisely, (using Thevenin's equivalent)

$\mathbf{V_{Th}} = \frac{V_{CC} \text{ X } R2}{R_1 + R_2} = \frac{15V \text{ X } 4.7K}{10K + 4.7K}$ = 4.8 V

$\mathbf{R_{Th}}$ = R1 ll R2 $= \frac{R1 \text{ X } R2}{R1 + R2} = \frac{10K \text{ X } 4.7K}{10K + 4.7K}$ = 3.2 K

Look at the modified circuit in fig 4.20.

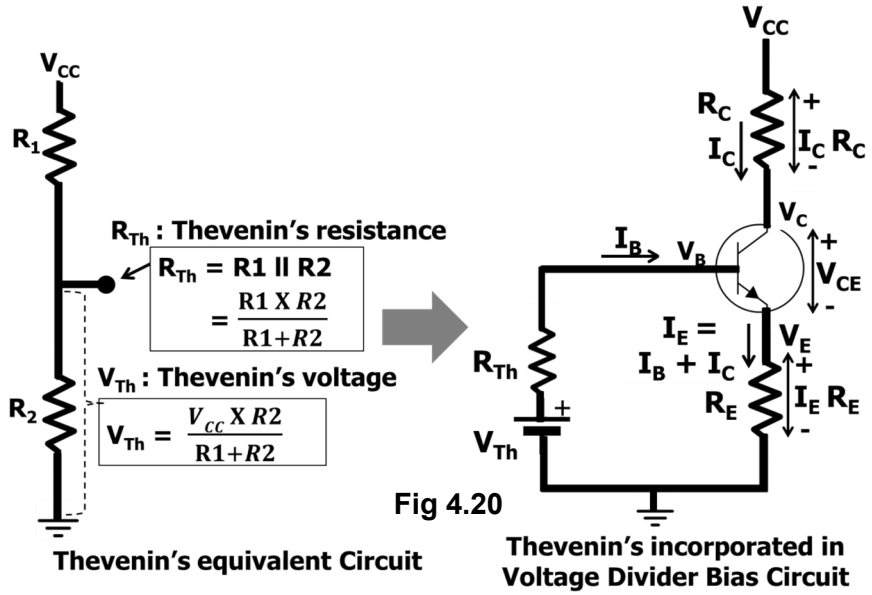


Fig 4.20

Following KVL,

$\mathbf{V_{Th}} = \mathbf{I_B R_{Th} + V_{BE} + R_E (I_B + I_C)}$

$I_C = h_{FE} \text{ X } I_B = \beta . I_B$ (since $h_{FE} = \beta$)

$\therefore V_{Th} = I_B R_{Th} + V_{BE} + R_E I_B (1 + \beta)$

$\therefore I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + R_E(1+\beta)}$

$I_B = \frac{V_{Th}}{R_{Th} + R_E(\beta+1)} = \frac{4.8V - 0.7V}{3.2K + 2.7K(1+50)} =$ **29 µA**.

I_C = h_{FE} X I_B

= 50 X 29 µA = **1.45 mA**

I_E = I_B + I_C

= 29 µA +1.45 mA = **1.479 mA**

V_E = $I_E R_E$ = 1.479 mA X 2.7K = **4.0 V**

V_C = $V_{cc} - I_c R_c$ = 15V – (1.45 mA X 3.3 K) = **10.215V**

V_{CE} = V_C - V_E = 10.215 V - 4.0 V. = **6.215V**

Q point = (6.125 V , 1.45 mA)

4.6 Numerical example

Problem 4.11: Draw a DC load line for problem 4.9.

Point A: When I_C =0, V_{CE} = V_{CC} = **15 V.**

Point B: When V_{CE} = 0, $I_C = \frac{V_{CC}}{R_C + R_E} = \frac{15V}{3K3+2K7}$ = 2.5 mA.

∴Draw a load line with A **(15 V, 0 mA)** and B **(0 V, 2.5 mA)**

Q point from problem 4.10 = (V_{CE} , I_C) = **(6.215 V , 1.45 mA)**

Load line is drawn as shown in fig 4.21

Voltage divider, bias circuit for PNP transistor.

The voltage divider using PNP transistor is shown in fig 4.22. Compare this with NPN circuit. Note, in PNP the emitter and R_E are normally drawn at the top, and the collector and R_C are drawn at the bottom. Biasing resistors R1, and R2 are inverted.

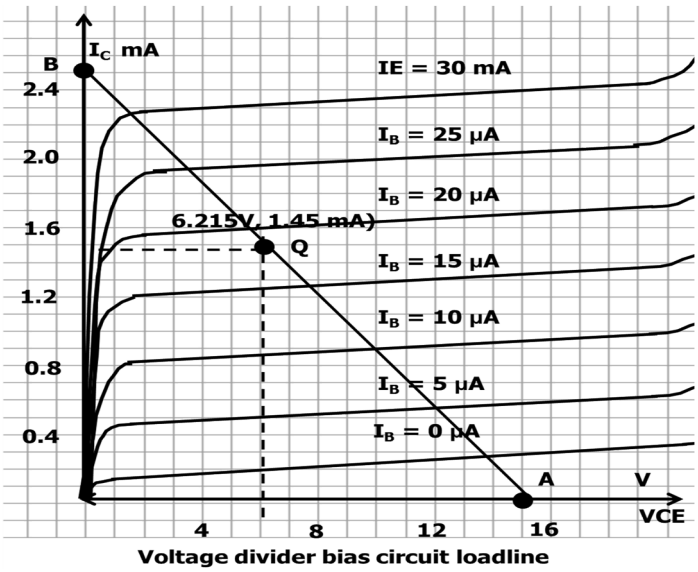


Fig 4.21

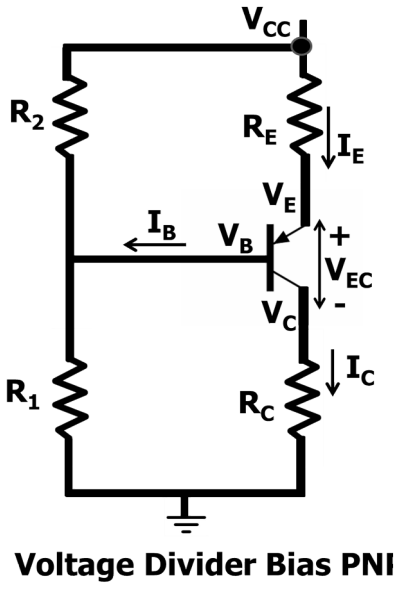


Fig 4.22

Chapter 5: Operational Amplifier (Op-Amp)

Syllabus: Introduction to Operational Amplifiers (Text-2) : Ideal OPAMP, Inverting and Non Inverting OPAMP circuits, OPAMP applications: voltage follower, addition, subtraction, integration, differentiation; Numerical examples as applicable.

5.1 Introduction to operational amplifiers

What is an Operational Amplifier?

- Op-amp is the most important analog component. It has two inputs terminals and one output.
- The input terminals are called **non- inverting (+)** and **inverting (–).**
- It is a **high gain** direct coupled (dc) amplifier.
- The operational amplifier works on a dual supply (V+ and V-). There will be a common ground.
- The op-amp has a **huge gain A** (of the order of 10000).
- **Gain is the ratio of the output and input**.
- The **magnitude of difference between non –inverting and inverting voltage is called differential input V_d**
- Output of op amp = $V_{out} = A \times V_d$
  = $A.(V_{non\text{-}inv} - V_{inv})$

What is the circuit symbol?

Refer Fig 5.1 for circuit symbol.

Abbreviations:

We shall use the following abbreviations in this chapter.

Operational amplifier → op-amp
Inverting → inv
Non- Inverting → non-inv

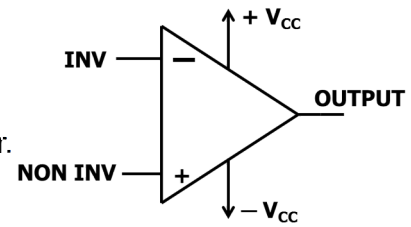


Fig 5.1 Operational Amplifier Circuit symbol

What is an inverting amplifier?

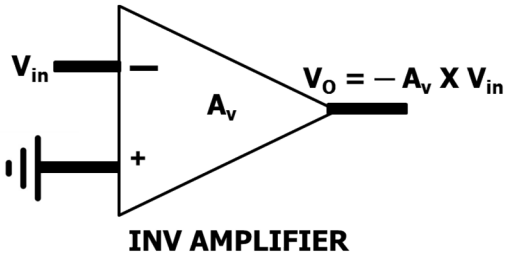


Fig 5.2 (a) Inverting amplifier

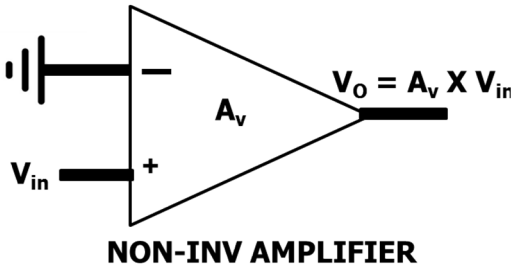


Fig 5.2 (b) Non- Inverting amplifier

In Inverting amplifier, the output waveform is inverted with respect to the input. (Opposite phase). Refer fig 5.2 (a) and 5.3.

- Note that in inverting amplifier configuration, the non-inverting (+) input is grounded.

- Output $V_o = -A_v V_{in}$
- A_v – Gain of the op amp.

What is a non-inverting amplifier?

In the Non-Inverting amplifier, the output waveform is in the same phase with respect to the input. There is no inversion. Refer fig 5.2 (b) and 5.4

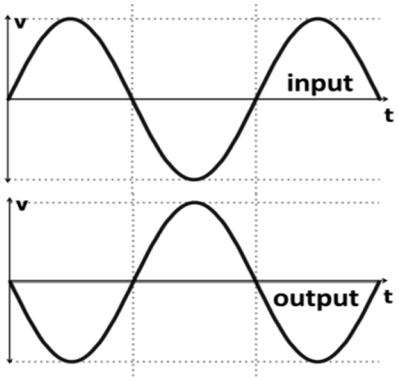


Fig 5.3 Inverting amplifier Input/Output waveforms

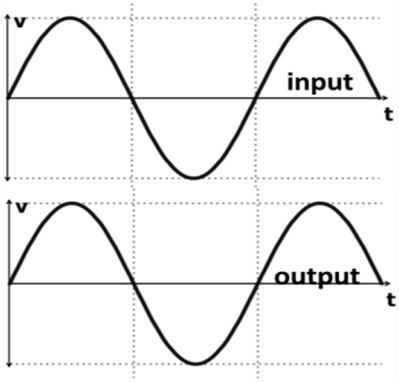


Fig 5.4 non-inverting amplifier Input/Output waveforms

What is the differential input concept?

Refer fig 5.5. The op-amp always amplifies the difference between the inv and non-inv inputs. V_d is the difference between the voltages present at inv and non-inv terminals.

V_d = V2 – V1 (Differential voltage)
Output will be V_d X Gain of the op-amp (A).
$V_o = V_d$ X A.
For an ideal op-amp gain A = ∞.

$$\therefore V_d = V2 - V1 = \frac{V_O}{A} = \frac{V_O}{\infty} = 0$$

∴ There are two interesting conclusions here.

1. **For an op-amp, the <u>differential voltage = 0</u>**
2. **For an op-amp, <u>Inverting and Non-Inverting terminals will be at the same potential. They follow each other</u>**

What is the virtual ground in an op-amp?

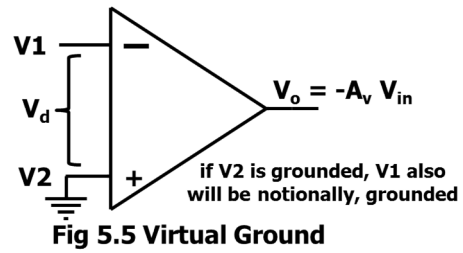


Fig 5.5 Virtual Ground

This is applicable to inverting amplifiers. Virtual ground means that if V2 is grounded, V1 also will be at ground potential (0 V). Therefore **notionally, V1 also is grounded even if there is no physical connection to ground**. V1 is said to be **virtually grounded**.

5.2 Inverting Amplifiers (fig 5.6)

Derive an expression for gain of an inverting amplifier.

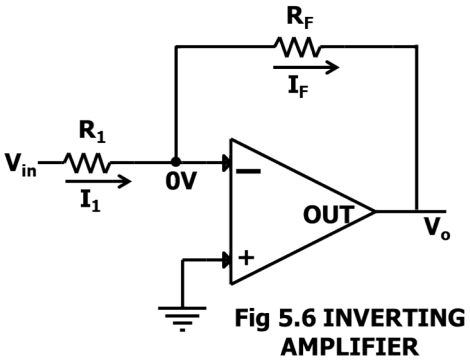


Fig 5.6 INVERTING AMPLIFIER

Input is fed to the Inverting (–) terminal.
Non-inv (+) is grounded.
Therefore, Inv input = 0 V (Virtual ground).
The op-amp input terminals never draw any input current.
Therefore, the entire input current I_1 flows into the feedback circuit as I_F. Therefore $I_1 = I_F$

$$\frac{V_{IN} - 0}{R_1} = \frac{0 - V_O}{R_F} \rightarrow \frac{V_{IN}}{R_1} = \frac{-V_O}{R_F}$$

Therefore, $\frac{V_O}{V_{IN}} = -\frac{R_F}{R_1}$

What are the important aspects to be understood, in op amp circuits ?

Note 1: If non- inverting input is grounded, inverting input also will be at ground potential. This concept is called **virtual ground** (Inv input will be at ground potential without any physical connection to ground).

Note 2: If inverting input is at a potential V1, the non – inverting input also be at V1**. ("Non-inv" will follow "inv").**

Note 3: From both (1) and (2), it can be inferred, that inverting and non – inverting inputs follow each other. The difference between "inv" and "non-inv" inputs is called differential voltage and is denoted by V_d. ($V_d = V_+ - V_-$) **V_d in an op-amp is always zero**.

Note 4: The current drawn by the inverting input terminal or the non- inverting input terminal is zero. Therefore, in op amp analysis **current drawn by V+ pin or V– pin can be neglected**.

Problem 1:The input to the op amp in fig 5.7 is a sinewave of l Volt, l kHz. What is the output?

For non-inverting amplifier, $V_{out} = -V_{in} \frac{R_2}{R_1}$

In this problem, frequency does not matter.

V_{in} = l Volt. **[l V is rms (by default)]**

V_{in} = l V rms = 1 V X $\sqrt{2}$ = 1.4 V peak.(just one peak)

= ± 1.4 V peak (both peaks)

V_{out} = ± 1.4 V X $\frac{100K}{6.8K}$ = ± 11.8 V peak .

Positive peak is 11.8 V and negative peak is - 11.8 V

This is not possible since the op amp has a DC supply of +9 V and –9 V. Therefore the peaks will clip at the power supply voltages.

The input / output waveforms are shown in fig 5.8

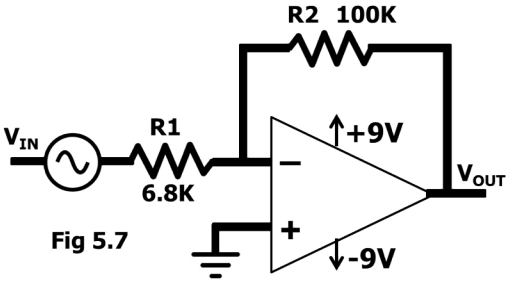
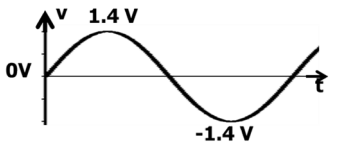


Fig 5.7



INPUT

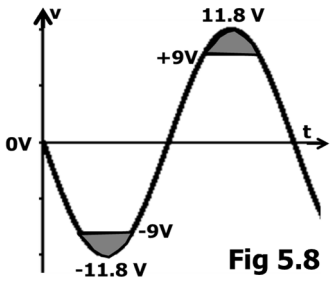


Fig 5.8

OUTPUT

Problem 2: What is the input current and load current for this op-amp shown in fig 5.9?

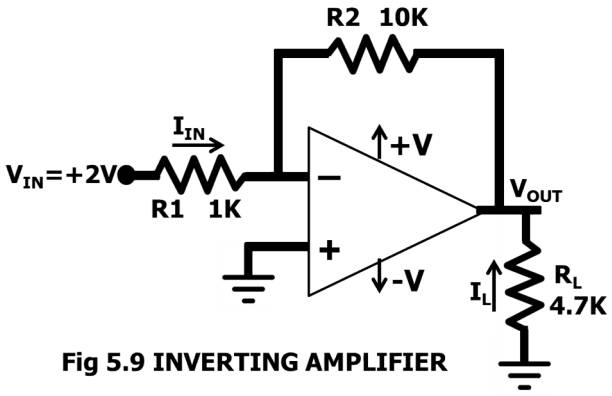


Fig 5.9 INVERTING AMPLIFIER

The inv input terminal is at 0 V **(virtual ground)**.

Input current $= \frac{2\text{ V} - 0\text{ V}}{1\text{K}}$ = 2 mA

$V_{out} = -V_{in}\frac{R2}{R1} = -2 \text{ X } \frac{10\text{K}}{2\text{K}} = -10\text{V}$

Load current $= I_L \frac{V_{out}}{R_L} = \frac{-10\text{ V}}{4.7\text{K}} = -2.5$ mA

I_L is – ve. ∴current flows from ground thro R_L , into the op amp, as shown in the circuit diagram 5.9. The waveform is shown in **fig 5.8**.

Problem 3: What is V_O for the op-amp in fig 5.10?

This is an inverting amplifier.

Therefore $\frac{V_O}{V_{IN}} = -\frac{R_F}{R_1}$

Gain $= -\frac{V_O}{V_{IN}} = -\frac{100\text{K}}{10\text{ K}} = -10$

∴ $V_o = -10 \text{ X } 0.6\text{ V} = -6\text{ V}$

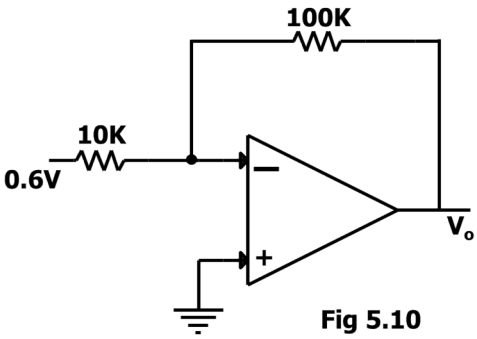


Fig 5.10

5.3 Non-inverting amplifier

Derive an expression for gain of a non-inverting (+) amplifier.

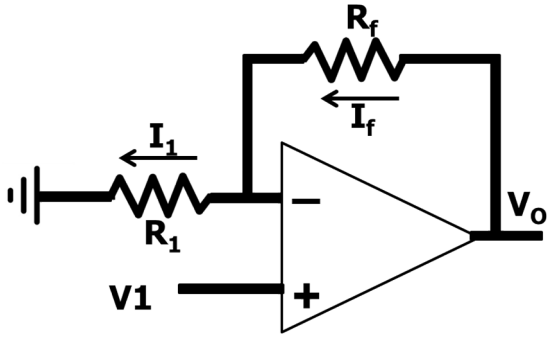


Fig 5.11 NON-INV AMPLIFIER

- Refer **fig 5.11.**
- Note that **the feedback is always between the V_o and Inv terminal**.
- Input is now fed at non-inv (+) terminal.
- **R_1 is grounded**.
- Note that Inv terminal (—) also is **at V_1.** (Both inv and non inv terminals will be at the same potential and **follow each other**)
- No current flows into inv (—) terminal.
- Therefore, the entire current I_F flows into the input resistor as I_1

Therefore $I_1 = I_F$

$$\frac{V_0 - V_1}{R_F} = \frac{V_1 - 0}{R_1}$$

$$\frac{V_O}{R_F} = \frac{V_1}{R_1} + \frac{V_1}{R_F}$$

$$V_O = V_1 \left\{ \frac{R_F}{R_1} + 1 \right\}$$

$$= V_1 \left\{ 1 + \frac{R_F}{R_1} \right\}$$

Therefore, Gain = $\frac{V_O}{V_1} = \{1 + \frac{R_F}{R_1}\}$

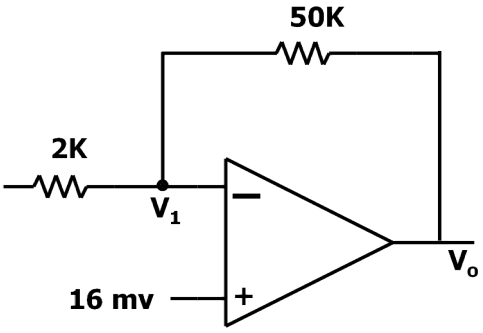


Fig 5.12

Problem 4: For the circuit in fig 5.12, V_o = ? Gain = ?
This is a non-inverting amplifier.

Gain = $\frac{V_O}{V_1} = \{1 + \frac{R_F}{R_1}\}$

= $(1 + \frac{50\ K}{2\ K})$ = 26

V_o = V_{in} $\{1 + \frac{R_F}{R_1}\}$

= 16 X 26 =416 mV

Problem 5: For the circuit in fig 5.13, what is V_O? What is the load current?

First, determine the voltage at B. Note the voltage at B IS NOT 2.2 V but a potential division of 1K and 1.2 K.

$V_B = \frac{2.2\ V\ X\ 1\ K}{1K + 1.2\ K} = 1.0\ V$

V_O = V_B $(1 + \frac{R_F}{R_{in}})$

= 1.0 V $(1 + \frac{22\ K}{2.2\ K})$

= 1.0 V X 11 = +11 V. (Non-Inverting)

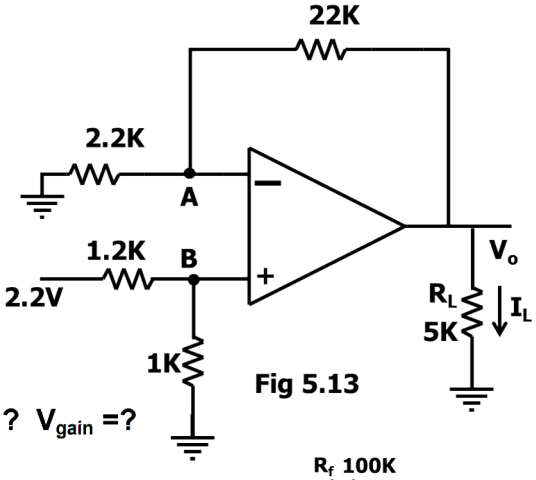


Fig 5.13

Problem 6: In the circuit shown in fig 5.14, V_{out} = ? V_{gain} =?

V_{out} = V_{in} $(1 + \frac{R_f}{R_{in}})$

What is V_{in}? Note V_{in} is NOT 5 V .

It will be the actual voltage **V_{in}** at the non-inverting (+) terminal, after a potential division by R1 and R2.

$\mathbf{V_{in}}$ = 5 V $\frac{R2}{R1 + R2}$ = 5 V X $\frac{33K}{33K + 47K}$ = 2.1 V

$\mathbf{V_{out}}$ = V_{in} $(1 + \frac{R_f}{R_{in}})$ = 2.1 V $(1 + \frac{100K}{22K})$ = 11.65 V

$\mathbf{V_{gain}}$ = $\frac{V_{out}}{V_{in}}$ = $\frac{11.65V}{5V}$ = 2.33

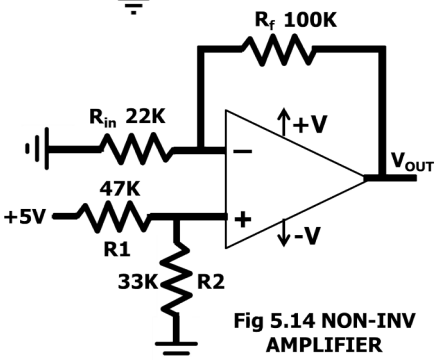


Fig 5.14 NON-INV AMPLIFIER

5.4 Summing Amplifiers

Non inverting summing amplifier (Refer fig 5.15)

It is a non-inverting amplifier . Therefore $V_{out} = V_3 \left(1 + \frac{R_f}{R_{in}}\right)$

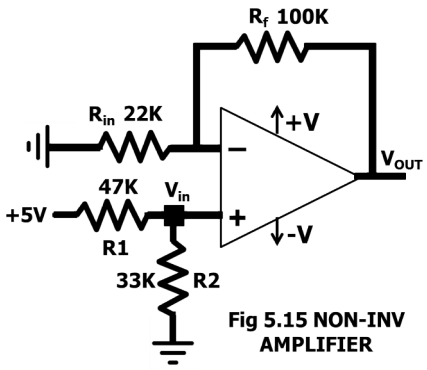


Fig 5.15 NON-INV AMPLIFIER

How to find V_3 ?

At the non-inv terminal, I_1 flows through R1 and I_2 flows through R2,

but the input current I_{in} to the non- inverting (+) terminal = 0

$\therefore I_1 + I_2 = 0$

$\therefore \frac{V_1 - V_3}{R_1} + \frac{V_2 - V_3}{R_2} = 0$

$\frac{V_1}{R_1} + \frac{V_2}{R_2} = \frac{V_3}{R_1} + \frac{V_3}{R_2} = V_3 \left(\frac{1}{R_1} + \frac{1`}{R_2}\right)$

$\frac{V_1 R_2 + V_2 R_1}{R_1 R_2} = V_3 \left(\frac{R_2 + R_1}{R_1 R_2}\right)$

or $V_3 = \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}$

$V_{out} = V3 \left(1 + \frac{R_f}{R_{in}}\right)$ [non–inv op amp]

$= \left(\frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}\right) \left(1 + \frac{R_f}{R_{in}}\right)$

Case 1: Let $R_1 = R_2$, then $V_{out} = \frac{1}{2}(V_1 + V_2)\left(1 + \frac{R_f}{R_{in}}\right)$

Case 2: Also let $R_f = R_{in}$ then $V_{out} = (V_1 + V_2)$ [**This is a SUMMING AMPLIFIER**]

Derive an expression for an inverting, summing amplifier.

Refer fig 5.16. $V_B = 0 \ \therefore V_A = 0$

$I_1 + I_2 = I$

$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1}{R_1}$ (since VA = 0)

$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2}{R_2}$ (since VA = 0)

$I = \frac{V_A - V_0}{R_F} = -\frac{V_0}{R_F}$

$I_1 + I_2 = I$

$\frac{V_1}{R_1} + \frac{V_2}{R_2} = -\frac{V_0}{R_F}$

$\therefore V_O = -\left\{\left(\frac{R_F}{R_1}\right) V_1 + \left(\frac{R_F}{R_2}\right) V_2\right\}$

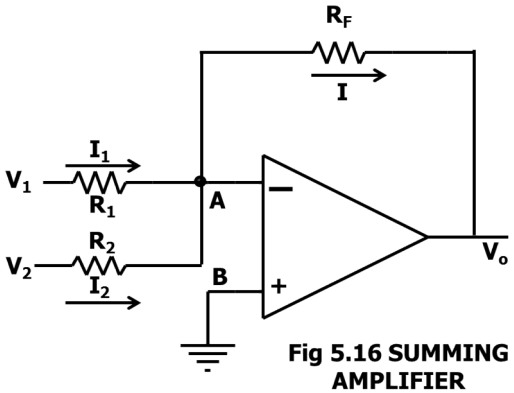


Fig 5.16 SUMMING AMPLIFIER

Case 1: $R_1 = R_2 = R$ $V_O = -\frac{R_F}{R}(V_1 + V_2)$ **(Summing amplifier)**

Case 2: $R_1 = R_2 = R_F = R$ $V_O = -(V_1 + V_2)$ **(Summing amplifier)**

Case 3: $R_1 = R_2 = R$ and $R_F = (R/2)$ $V_o = -\frac{(V_1 + V_2)}{2}$. **(Averaging amplifier.)**

Problem 7: Refer circuit shown in fig 5.17. What is the output?

$V_O = R_F \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$

$= 12K \left(\frac{-2\ V}{2K} + \frac{1.5\ V}{3K} - \frac{0.5\ V}{4K} \right)$

$= -12\ V + 6\ V - 1.5\ V.$

$V_O = -7.5\ V$

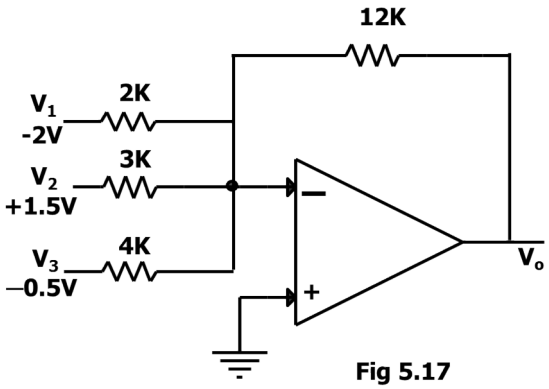


Fig 5.17

Summing circuit (adder) using super position

Problem 8 : What is the output of this circuit if V1 = 2 V, V2 = 3 V and V3 = 5 V

Refer fig 5.18. This can be analysed by using super position theorem.
Superposition principle : When one voltage source is connected all other voltage source should be replaced by short. (in this example, to be replaced by ground) .

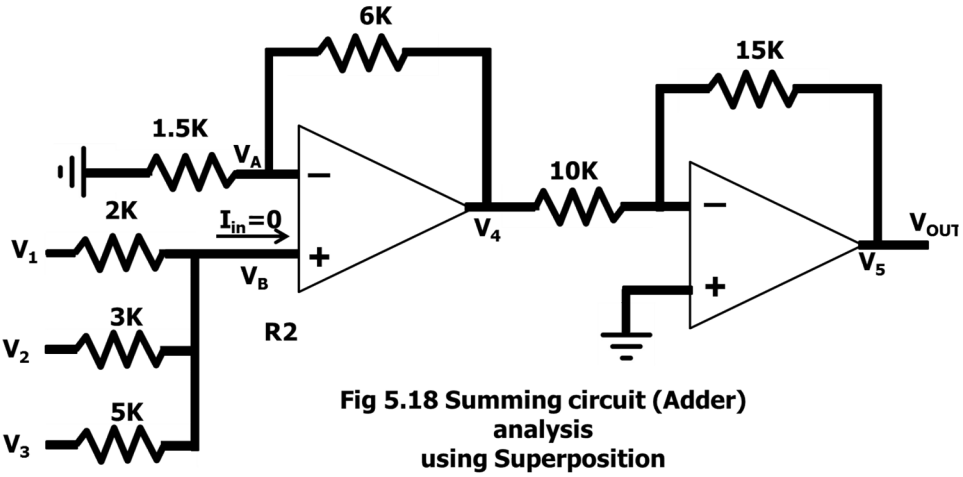


Fig 5.18 Summing circuit (Adder) analysis using Superposition

a) **<u>V1 is connected</u>** **(Refer fig 5.19)**

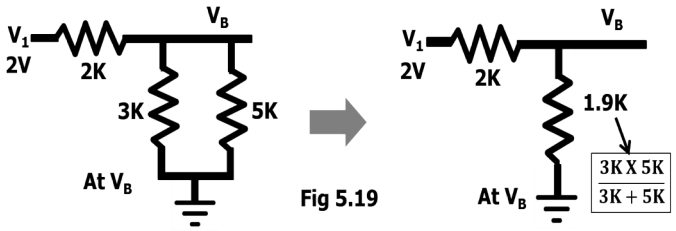


Fig 5.19

$V_B = \frac{V_1 \text{ X } 1.9K}{2K+1.9K} = \frac{2V \text{ X } 1.9K}{3.9K} = 0.97\ V$

$V_{out} = V_B \left(1 + \frac{R_f}{R_{in}}\right) = 0.97\ (1 + \frac{6K}{2K}) = \mathbf{3.9\ V}$

b) V_2 is connected (Refer fig 5.20)

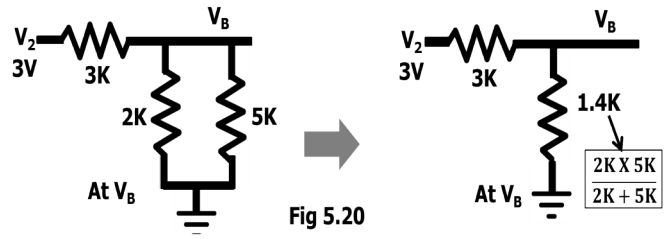


Fig 5.20

$V_B = \frac{V_2 \text{ X } 1.4K}{3K+1.4K} = \frac{3V \text{ X } 1.4K}{4.4K}$ = 0.95 V

$V_{out} = V_B \left(1+\frac{R_f}{R_{in}}\right)$ = 0.95 $(1 + \frac{6K}{2K})$= **3.8 V**

c) V_3 is connected (Refer fig 5.21)

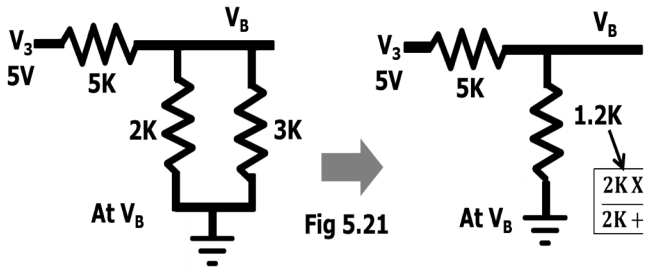


Fig 5.21

$V_B = \frac{V_3 \text{ X } 1.2K}{5K+1.2K} = \frac{5V \text{ X } 1.2K}{6.2K}$ = 0.97 V

$V_{out} = V_B \left(1+\frac{R_f}{R_{in}}\right)$ = 0.97 $(1 + \frac{6K}{2K})$= **3.9 V**

∴the final voltage at adder o/p V_4 =3.9 + 3.8 +3.9 = 11.6V

The output at V_5 = - V_4 X $\frac{15K}{10K}$ = **-**11.6 X1.5 = **-17.4 V**

5.5 Subtractor

Derive an expression for a subtractor.

Subtractor is also called (Difference Amplifier)

At negative terminal,

$$\frac{V_1 - V'}{R_1} = \frac{V' - V_O}{R_2}$$

$$\frac{V_0}{R_2} = \frac{V'}{R_2} + \frac{V'}{R_1} - \frac{V_1}{R_1}$$

$$= V' \left(\frac{1}{R_2} + \frac{1}{R_1}\right) - \frac{V_1}{R_1} \quad \rightarrow \text{(A)}$$

$V' = V'' = \frac{V_2 R_2}{R_1 + R_2}$

Substitute for V' in (A)

$$\frac{V_0}{R_2} = \frac{V_2 R_2}{R_1 + R_2} \left(\frac{R_1 + R_2}{R_1 R_2}\right) - \frac{V_1}{R_1}$$

$$\frac{V_0}{R_2} = \frac{V_2}{R_1} - \frac{V_1}{R_1} = \frac{1}{R_1} (V_2 - V_1)$$

$$V_0 = \frac{R_2}{R_1} (V_2 - V_1)$$

If $R_2 = R_1$, $V_O = (V_2 - V_1)$

This is a subtractor.

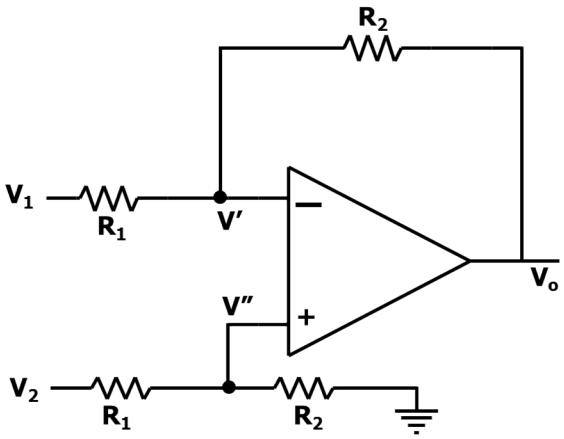


Fig 5.22 SUBTRACTOR

Problem 9: Implement this. $V_O = V_1 - 3V_2 - 2V_4 + 5V_3$. Assume R_F = 30 K.

Refer fig 5.23. Regroup all +ve terms all –ve terms.. $V_O = (V_1 + 5\ V_3) - (3V_2 + 2V_4)$

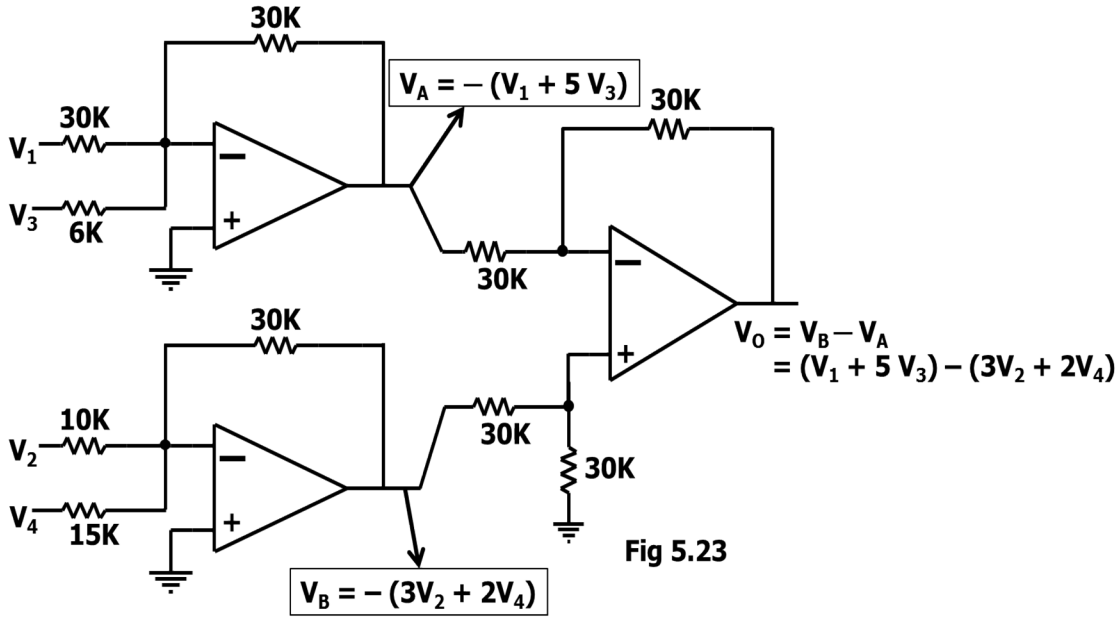


Fig 5.23

Problem 10: This is known as Scaling order. Design a scaling order to give an output $V_O = -(6V_1 - 4V_2 + 3V_3)$. Choose R_F = 120 K. Refer fig 5.24.

Implementation:

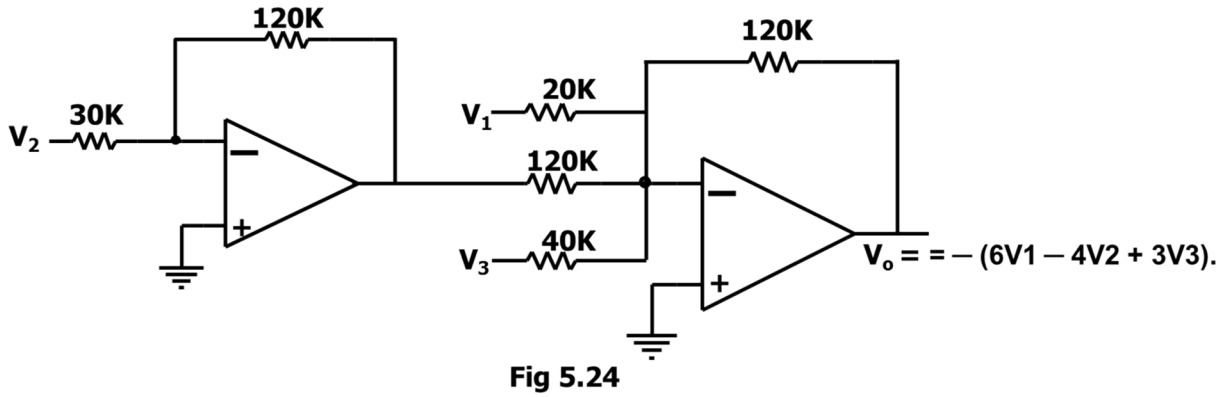


Fig 5.24

5.6 Op-amp applications

5.6.1 Voltage Follower application: (Refer fig 5.25)

Voltage Gain = Unity

$V_B = V_{in}$

$V_A = V_B = V_{in}$

$V_O = V_A = V_B = V_{in}$

$\therefore V_O = V_{in}$

Output follows Input.

Hence the name "**Voltage Follower**"

Voltage Gain = Unity

Large Input impedance

Low output impedance

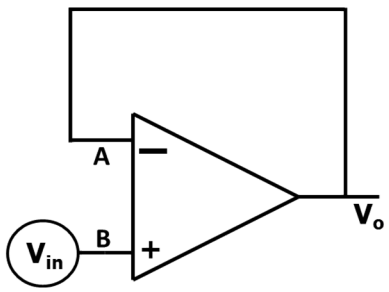


Fig 5.25 VOLTAGE FOLLOWER

5.6.2 Current to Voltage Converter application – Trans-resistance Amplifier: (Refer fig 5.26)

$I_{in} = I_f$

$I_{in} = \frac{0 - V_O}{R_F} = -\frac{V_O}{R_F}$

$\therefore I_{in}$ is proportional to $-V_o$

Input Current is proportional to $-V_O$

Hence Current to Voltage Converter.

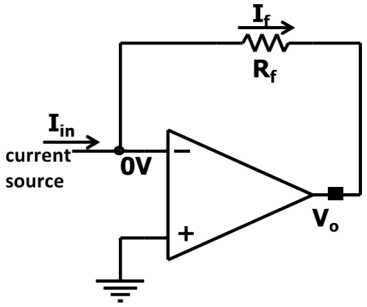


Fig 5.26 CURRENT TO VOLTAGE CONVERTER TRANS RESISITANCE AMPLIFIER

5.6.3 Voltage to current Converter – (Trans-conductance Amplifier) : (Refer fig 5.27)

IS = IL

$\frac{V_S - 0}{R_S} = \frac{0 - V_O}{R_L}$

$\frac{V_S}{R_S} = I_L$

$\therefore V_S$ is proportional to I_L

Hence Voltage to Current converter.

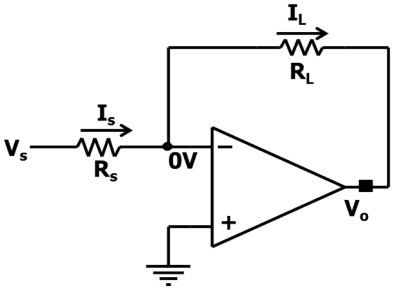


Fig 5.27 VOLTAGE TO CURRENT CONVERTER TRANS CONDUCTANCE AMPLIFIER

5.6.4 Op-Amp Integrator

Refer Fig 5.28. Principle : $I = C\frac{dv}{dt}$

Input side	**output side**
$I = \frac{V_S - 0}{R_S}$	$I = C\frac{d(0 - V_o)}{dt} = -C\frac{dV_o}{dt}$
$\frac{V_S}{R_S}$	$= -C\frac{dV_o}{dt}$

Integrate on both sides

$\int_0^t \frac{V_S}{R_S} dt = -C\int_0^t \frac{dV_o}{dt} dt$

$\therefore \frac{1}{R_S}\int_0^t V_S\, dt = -C\, V_o$

$V_o = \frac{-1}{R_S C}\int_0^t V_S\, dt$ **+ initial conditions**

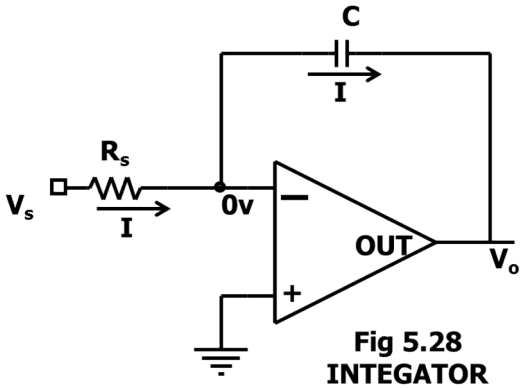


Fig 5.28 INTEGATOR

R_sC is known as time constant

V_{output} is the integration of the input

INPUT	OUT PUT
SIN	– COS
Square wave	Triangular wave

Applications:

- In analog computers, solving differential Equations
- Signal wave shaping circuits

5.6.5 Op-Amp Differentiator: Refer 5.29

Input side **output side**

$I = C \frac{dV_S}{dt}$ $I = \frac{0 - V_o}{R_f}$

$C\frac{dV_S}{dt}$ $= \frac{-V_o}{R_f}$

$V_o = -R_f C \frac{dV_S}{dt}$

Therefore V_{output} is the differentiation of the input

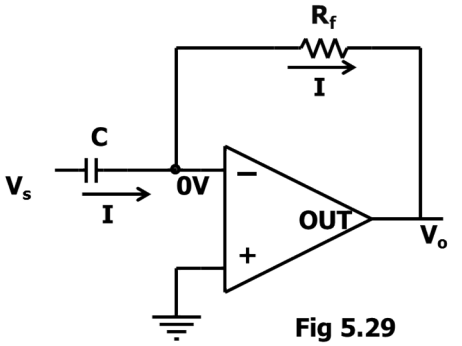


Fig 5.29
DIFFERENTIATOR

INPUT	OUT PUT
COS	- SIN
Triangular wave	Square wave

Applications:

FM demodulators

Signal wave shaping circuits

Problem 11: A sine wave of peak value 6 mv and 2KHz frequency is applied to an op-amp integrator. R_1= 100K, C_f = 1uF. What is the output voltage ?

Solution: For integrator $V_o = V_o = \frac{-1}{R_1 C_f} \int_0^t V_{in}\, dt$ where R_1 = 100K , C_f = 1uf ,

$V_{in} = V_m \sin(\omega t)$, V_m = 6 mV , $\omega = 2\pi f = 2\pi (2000)$

$Vo = \frac{-1}{100K*1uf} \int_0^t 6mv * \sin(2\pi(2000)t)\, dt$

$Vo = -0.06 \left[-\frac{\cos(4000\pi t)}{4\pi * 1000} \right]_0^t$

Vo = 4.77(cos (4000π t) – 1) u volts

Problem 12: In the circuit in fig 5.30, what is the V_0 ?

V1 = - 1 X 10^{-6} A X 10 kΩ = - 0.1 V

V_o = V1 ($1+\frac{R_f}{R_1}$)

= - 0.1 ($1+\frac{100K}{2K}$) = - 5.1 V

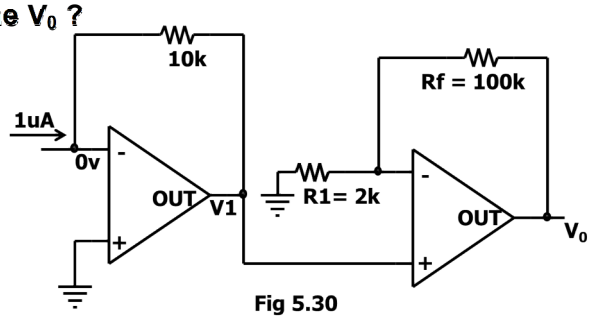


Fig 5.30

Problem 13: In the circuit in fig 5.31,If R_L varies from 1k to 60 k. What is the variation in Vo?

1) RL = 1K then $V_o = 10 (-\frac{1K}{100K}) = -0.1$ V

2) RL = 60K then $V_o = 10 (-\frac{60K}{100K}) = -6.0$ V

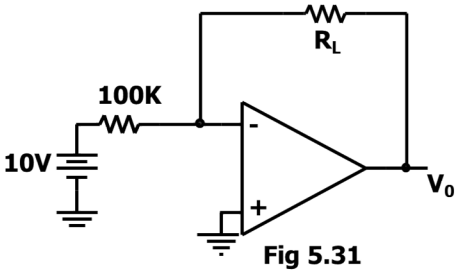


Fig 5.31

5.7 Differential mode and common mode signals:

Preamble: Input to an op-amp, in general, will have two types of signals called, difference signals and common mode signals.

Difference signals are those signals present at V1 and V2 which are different (not same).

Common mode signals are those signals present at V1 and V2 which are exactly same.

What is the differential gain (A_d) ?

Refer fig 5.32

V_d = V1 – V2 (V1 and V2 are different)

$V_o = A_d V_d = A_d (V1 – V2)$

Where A_d = differential gain

and V_d = differential voltage

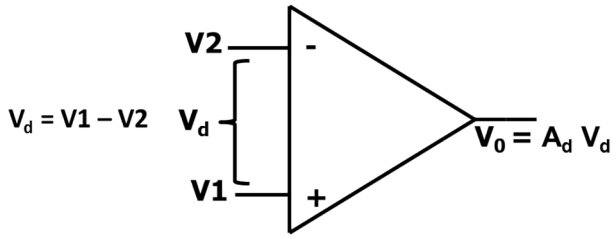


Fig 5.32 Differential Gain

What is a common mode signal ?

Refer fig 5.33. In common mode V1 and V2 are exactly same. Average level of the two input signal V1 and V2 is defined as the common mode signal

$$V_c = \frac{V1 + V2}{2}$$

For a common mode signal also, the op-amp gives an output $V_0 = A_c V_c$

where A_c = common mode gain

V_c = common mode signal

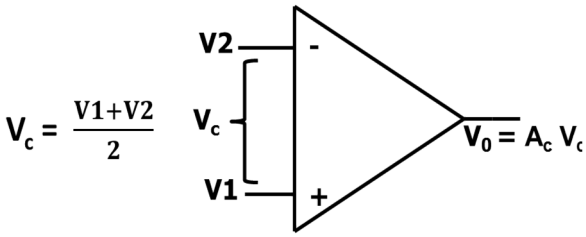


Fig 5.33 Common Mode Gain

Therefore the total output of an Op-amp

V_o = common mode output + differential mode output

$= A_c V_c + A_d V_d$

In an ideal op amp

a) Common mode gain A_c must be Zero
b) Differential mode gain A_d must be infinity

What is common mode rejection ratio (CMRR)?

CMRR is the ability of an op-amp to accept the desired differential signals and reject undesired common mode signals

$$\text{CMRR} = \rho = \left|\frac{A_d}{A_c}\right|$$

for ideal op amp CMRR = ∞ [since $A_d = \infty$ and $A_c = 0$]

Problem 14: In an op-amp, the non-inverting input is 500 μV and the inverting input is 200 μV. Differential gain is 3000 and CMRR = 10^5. Find the common mode gain. What is the output voltage?

CMRR = 10^5 A_d = 3000

$$\text{CMRR} = \left|\frac{A_d}{A_c}\right| = \left|\frac{3000}{A_c}\right|$$

Therefore A_c = 0.03

V_d = 500 - 200 = 300 μV.

$V_c = \frac{500+200}{3}$ = 350 μV

V_o = $A_cV_c + A_dV_d$
= 3000 X 300 µV + 0.03 X 350 µV
= 900.1015 mV

5.8 Ideal Operational amplifier.

What are the characteristics of an op amp?

1. **Infinite open loop voltage gain (A_V):** The ideal OP-amp has a gain of infinity. (However, in practice, A_V will be around 10000)
2. **Infinite bandwidth:** The bandwidth of an op-amp is infinite. It has no low frequency cut –off , nor high frequency cut –off.
3. **Infinite input impedance (R_{in}):** R_{in} = ∞. This means, the op amp does not require any input current and in fact the op-amp does not draw any input current.
4. **Infinite output impedance (R_{out}):** R_{out} = 0. This means, the op-amp output will remain at the same level whether the load R_L = ∞ or R_L = 0. The drive capability of the op-amp is infinite
5. Z**ero offset voltage (V_{IOS}):** If the inputs, V1 = V2 = 0 V, the output will be exactly 0 V.
6. **Infinite Common Mode Rejection Ratio – CMRR (ρ):**
7. CMRR = ∞. If the inputs are equal and identical (V1 =V2), the output will be zero volts. This will ensure, noise signals at the input, will be rejected by the op-amp.
8. **Infinite slew rate (S= ∞) :** If the input is a step voltage, the output also will be a step output. Slew rate is an indication of the rate at which the op-amp output rises. Slew rate S = $\frac{dV_o}{dt}$.
9. **Power supply rejection ratio (PSRR) : Op amp has a good PSRR. Therefore even i**f the power supply voltage fluctuates, the output will still be steady (will not fluctuate)
10. **Temperature stability:** The op amp characteristics will not change due to temperature variations .

Draw a block diagram of an op-amp and explain its operation.

Op amp has 4 stages. Op amp can amplify both ac signals and DC signals

Fig 5.34 Operational Amplifier Basic Block Diagram

1) Input stage :

a) It is a double ended differential amplifier.
b) Two inputs & two outputs. It is a DC amplifier
c) This stage provides maximum gain for the op-amp.
d) Has high input impedance and low output impedance.

2) Single ended differential amplifier :

a) Provides moderate gain. This is also a DC amplifier
b) Two inputs and single output.

3) Emitter follower

a) It is a buffer.

b) Unity gain. DC amplifier, again.

4) Level translator and output stage :

a) All the previous 3 Stages are DC amplifiers. There will be a gradual DC shift in these 3 amplifiers and this DC build up needs to be reset, to ground potential. This stage does this function of level shifting .

b) The o/p stage presents, a low output impedance to the load

c) It can provide large voltage swings, in the output

d) It can source or sink large load currents.

Chapter 6 Digital electronics, Number systems

Module – 3 Part 1 Syllabus : Digital Electronics (Text-2) : Introduction, Switching and Logic Levels, Digital Waveform (Sections 9.1to 9.3).
Number Systems: Decimal Number System, Binary Number System, Converting Decimal to Binary, Hexadecimal Number System: Converting Binary to Hexadecimal, Hexadecimal to Binary, Converting Hexadecimal to Decimal, Converting Decimal to Hexadecimal, Octal Numbers: Binary to Octal Conversion. Complement of Binary Numbers.

6.1 Digital Electronics

6.1.1 Introduction

What is an analog signal? What is a digital signal?
Refer fig 6.1 and 6.2.

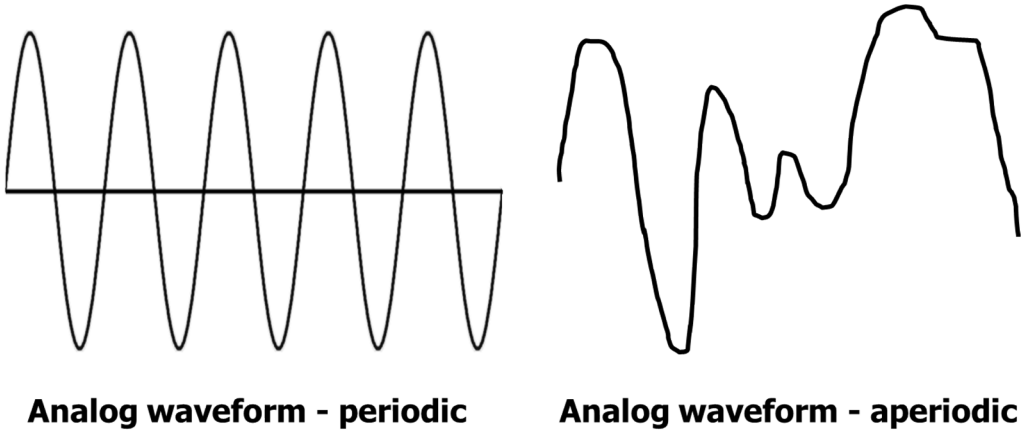


Fig 6.1 Analog waveforms

Analog signal (fig 6.1)

- An analog signal is continuous with respect to time.
- The value of analog function can be continuously defined.
- It can have any instantaneous slope.
- The analog signal can assume any instantaneous value, out of infinite possible values
- May be periodic or not.
- **Example:** All natural phenomenons are analog in nature. Waterfall, light, sound, speech

Digital signal (fig 6.3)

- Also known as discrete signal.
- Not continuous.
- Will have only a few chosen values
- Digital signal is not continuous with respect to time
- The value of a digital signal, cannot be defined at all times.
- May be periodic or not.
- **Example:** Computer data.

6.1.2 Switching and Logic levels: (Refer fig 6.2)

Describe a logic level profile

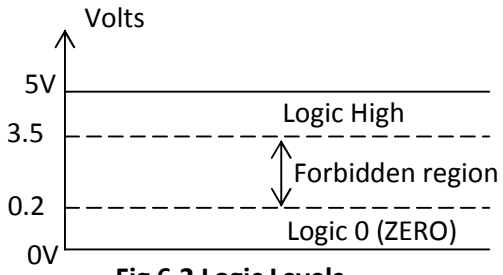


Fig 6.2 Logic Levels

Let us take an example of an inverter gate **operating at 5V supply .**

For logic 1, the output can be anywhere **between 3.5 V and 5.0 V.**

For logic 0, the output can be **between 0 V and 0.2 V.**

The region **between 0.2V and 3.5V** is neither 0 nor 1.

Forbidden region = 3.5 V – 0.2 V = 3.3 V

In this **forbidden** region, the signal is **ambiguous**. It can be recognized **neither as ONE nor as ZERO.**

6.1.3 Digital waveforms

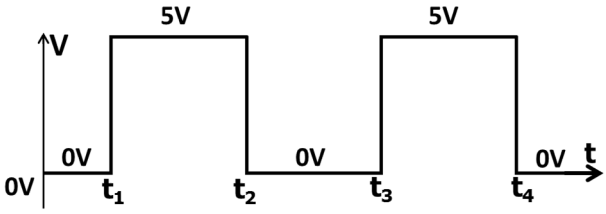


Fig 6.3 Digital waveform

What is Fan out?

It is the number of inputs, a gate output can feed, without its output dropping below 3.5V (into the forbidden region)

What is Fan In?

Fan-in is the number of inputs, a gate can handle.

A digital waveform (a binary TTL logic square wave) is shown in the figure 6.2. **What is the value of this square wave exactly at t_1, t_2, t_3, or t_4? 0 V or 5 V?**

The figure 6.2 shows a digital signal with just two levels 0V and 5V. At these four instances, the value of signal cannot be defined. Digital signals, usually assume only a few discrete levels.

Binary wave form : This is known as a binary signal (Two level signal). Binary (2 levels), Ternary (3 levels), Quaternary (4 levels) and so on…..

Compare analog & digital waveforms

Analog signal	Digital signal
Continuous at all times. Can assume one of the infinite amplitude levels	Discrete and discontinuous. Can assume only a few fixed levels. Binary signals assume only two levels ONE or ZERO
Example : Sine wave, speech, light	Example : Square wave, CDs, Computer data,
Can be affected by noise easily. Suffers a lot, on account of noise	Noise can not affect so easily. Suffers a lot less due to noise.
Analog hardware is fixed and not flexible.	Digital hardware is flexible.
Used in audio and video applications	Used in computer and Internet world
Used in real time applications and occupies less bandwidth	Used in non-real time applications and needs more bandwidth than analog
Storage is complex. Needs analog tapes	Storage is easy in the form of binary bits
Uses resistors, capacitors, inductors, transformers, and operational amplifiers	Uses logic gates, tansistors, Ics, Micro-processors and micro computers

6.2 Number systems:

6.2.1 Introduction:

Binary number systems. (Recall what a Digital signal is → fig 6.4)

Example: Computer data.

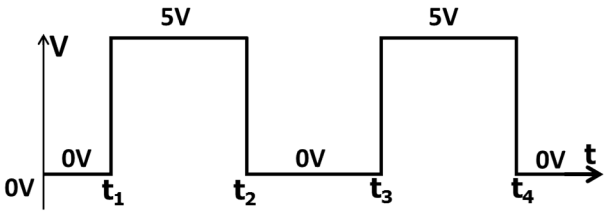


Fig 6.4 Digital waveform

A digital waveform (a binary TTL logic square wave) is shown in the fig 6.4.

A digital signal with just two levels 0V and 5V is a binary signal.

- Binary (2 levels), Ternary (3 levels), Quaternary (4 levels) and so on…..

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6.2.2 Decimal number system

$(5738)_{10} = (5X10^3) + (7X10^2) + (3X10^1) + (8X10^0)$

Thousands Hundreds Tens Units

6.2.3 Binary Number system: This system has a base of 2. Binary and its equivalent decimal values are shown in the table below

Binary	Decimal	Binary	Decimal
0000	0	1000	8
0001	1	1001	9
0010	2	1010	10
0011	3	1011	11
0100	4	1100	12
0101	5	1101	13
0110	6	1110	14
0111	7	1111	15

6.2.4 Binary to Decimal conversion:

Convert $(10101101)_2$ to ($)_{10}$

Note: ($)_{10}$ represents a decimal system (base of ten).

($)_2$ represents a binary system (base of two).

($)_8$ represents an octal system (base of eight).

($)_{16}$ represents a hexa-decimal system (base of sixteen).

Given Binary number	1	0	1	0	1	1	0	1
Multiply by	X	X	X	X	X	X	X	X
Powers of 2	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Decimal Value $= (1X2^7) + (0X2^6) + (1X2^5) + (0X2^4) + (1X2^3) + (1X2^2) + (0X2^1) + (1X2^0)$

$= 128 + 0 + 32 + 0 + 8 + 4 + 0 + 1$

$= \mathbf{(173)_{10}}$

What is a byte? What is a nibble? What is a bit?

Example: $(11001100)_2$

- There are **8 positions** (**digits**) with ones and zeros. Each of these digits is called a **bit.**
- A **nibble** consists of **4 bits.**
- A **byte** consists of **8 bits** (or **2 nibbles**)
- **4 bit string is a nibble, 8 bit string is a byte and 16 bit string is a word**

What is MSB and what is LSB?

- The left most bit in a byte is called MSB (most significant bit)
- The right most bit in a byte is called LSB (least significant bit)

In a byte, MSB will have a higher weigtage ($2^7 = 128$) than LSB ($2^0 = 1$)

What is a binary sequence?

$2^0, 2^1, 2^2, 2^3, 2^4$ …….

What is the decimal equivalent of a binary sequence?

1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, 32768, 65536…….

In fractions, what is the binary sequence and its equivalent decimal sequence?

Binary sequence for fractions : $2^{-1}, 2^{-2}, 2^{-3}, 2^{-4}, 2^{-5}$ …….

Eqvt decimal sequence for fractions : 0.5, 0.25, 0.125, 0.0625, 0.03125……

6.2.5 Decimal to Binary:

Problem 1: Convert $(73)_{10}$ to Binary

Method 1 : using Table.

73 — 64 = 9	**64 = 1000 0000**
9 — 8 = 1	**8 = 0000 1000**
1 — 1 = 0	**1 = 0000 0001**
	73 = 1000 1001

Problem 2: Convert $(61)_{10}$ to binary

2	61	
2	30	1 ↑ END
2	15	0
2	7	1
2	3	1
2	1	1
	1	

START

Decimal to Binary conversion Division Meyhod

The resultant binary number is 111101

Rule: For whole numbers move upwards to compute the binary word

Double Dabble method (Decimal to binary)

Problem 3: Convert $(30.6875)_{10}$ to ($)_2$

2	30		
2	15	-	(0)
2	7	-	(1)
2	3	-	(1)
	(1)	-	(1)

11110

Note: If there is a remainder, read from **the bottom upwards**, to get the answer.

0.6875 X 2 = **(1).**3750

0.3750 X 2 = **(0)**.750

0.750 X 2 = **(1)**.500

0.500 X 2 = **(1)**.000

.1011

Note: If there is a carry, read from the **top downwards,** to get the answer.

∴ The answer is 11110,1011

==========

6.2.6 Binary Addition

Rules:

0 + 0 = 0

0 + 1 = 1

1 + 0 = 1

1 + 1 = 10

Problem 4: Add 101101 and 11001

	1	0	1	1	0	1	$(45)_{10}$
		1	1	0	0	1	$(25)_{10}$
1	1	1			1		Carry
1	**0**	**0**	**0**	**1**	**1**	**0**	**$(70)_{10}$**

Problem 5: Add 11111 and 10111

Digit 1 →	1	1	1	1	1	$(31)_{10}$
Digit 2 →	1	0	1	1	1	$(23)_{10}$
Carry	1	1	1	1	1	
Sum	**1**	**1**	**0**	**1**	**1**	**0**	**$(54)_{10}$**

==========

6.2.7 Binary Subtraction

Rules:

0 - 0 = 0

1 - 0 = 1

1 - 1 = 0

10 - 1 = 1

Problem 6: Subtract 13 from 24

$(24)_{10}$	1	1	0	0	0
$(13)_{10}$	—	1	1	0	1
Borrow		1	1	1	
$(11)_{10}$		**1**	**0**	**1**	**1**

Problem 7: Subtract 21 from 42

$(42)_{10}$	1	0	1	0	1	0
$(21)_{10}$		1	0	1	0	1
	1	0	1	0	1	**$(21)_{10}$**

==========

6.2.8 HEXA-DECIMAL CONVERSION

What is hexa decimal number system?

- Hex means **6.** Decimal is **10**. Therefore Hexa-decimal is **16.**
- Hexa-decimal system is therefore, **a number system with 16 as a base**.
- The digits are **from 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, A, B, C, D, E and F.**
- These 16 digits (0 to F) can be represented by **4 binary bits**.
- Weightage is **powers of 16**
- Hexa-decimal is also also known as, **Alpha-Numeric**

Problem 8: <u>Convert Hex to Decimal</u>

$(F8E)_{16}$ = ( )$_{10}$

$= \mathrm{F} \times 16^2 + 8 \times 16^1 + \mathrm{E} \times 16^0$

$= 15 \times 16^2 + 8 \times 16^1 + 14 \times 16^0$

$= \mathbf{3982}$

Problem 9: Double Dabble conversion

$(49.4)_{10}$ → ( )$_{16}$

16	49		
16	3	-	**(1)**
	0	-	**(3)**

= **$(031)_{16}$**

0.4 X 16 = **6**.4

0.4 X 16 = **6**.4

0.4 X 16 = **6**.4

= $(.666)_{16}$

Therefore $(49.4)_{10}$ → $(031.666^*)_{16}$

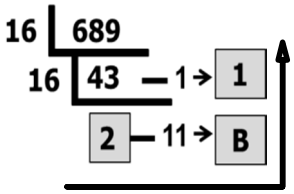
Problem 10: $(972.625)_{10}$ = ( )$_{16}$

8	972			
8	60	- 12	= **(C)**	**0.625 x 16 = 10.0 = A**
	(3)	- 12	= **(C)**	

Therefore, $972.625)_{10}$ = $(3CC.A)_8$

Hexa -Decimal conversion

Problem 11: Convert $(689.985)_{10}$



$(689)_{10}$ = $(2B1)_{16}$

.985 X 16 = **15** . 760
.76 X 16 = **12** . 16
.16 X 16 = **2** . 56
.56 X 16 = **8** . 96

(.985) results in a decimal sequence, top to bottom as **15, 12, 2, 8,** in decimal.
This sequence is equal to **F C 2 8** in Hexa-decimal.
∴(689 . 985) = $(2B1 . FC28)_{16}$

Binary to Hexa Conversion
Problem 12: Convert ($(1011101111010A)_2$ to ($)_{16}$

Rules for Whole numbers
- Start **from LSB and move left towards MSB**
- Group them in **4 bits**
- **Stuff zero or zeros**, **if required on MSB side**.

Rules for Decimal numbers
- Start **from MSB and move right towards LSB**
- Group them **in 4 bits**
- **Stuff zero or zeros in the LSB Side, if needed**

Therefore, $(0010\ 1110\ 1111\ 010A)_2 = (2EF5)_{16}$

Hexa-decimal to Binary conversion
Problem 13: Convert $(FA876)_{16}$ to Binary

Hexa →	F	A	8	7	6
Binary →	1111	1010	1000	0111	0110

Therefore, **$(FA876)_{16}$ =$(1111\ 1010\ 1000\ 0111\ 0110)_2$**

Problem 14: Convert Decimal to Hexa to Binary

$(5\ 7\ 3\ 4\ 5)_{10}$ → ($)_{16}$ → ($)_2$

16	57345						
16	3584	-	1	14	0	0	1
16	224	-	0	(E	0	0	$1)_{16}$
	14	-	0	(1110	0000	0000	$0001)_2$

==========

6.2.9 Octal → Decimal → Octal
What is octal number system?
- A number system with **8 as a base,** is known as octal system.
- The digits are from **0 to 7.**
- These digits (0 to 7) can be represented by **3 binary bits.**
- Weightage is **powers of 8**

Example:
$(1062)_8 = 1 \times 8^3 + 0 \times 8^2 + 6 \times 8^1 + 2 \times 8^0$
= 512 + 0 + 48 + 16 = $(576)_{10}$

Decimal to Octal
$(877)_{10}$ =

8	877		
8	109	-	5
8	13	-	5
	1	-	5

$(1555)_8$

Octal to Binary

$(7565)_8$	Octal →	7	5	6	4
Binary Equivalent →		$(111)_2$	$(101)_2$	$(110)_2$	$(100)_2$
Binary →		$(111101110100)_2$			

Binary to Octal $(1011110101011)_2$

$(\underline{001}\ \underline{011}\ \underline{110}\ \underline{101}\ \underline{011})_2$ ← $(1\quad 3\quad 6\quad 5\quad 3)_8$	Rules for Whole numbers Start from LSB and move left towards MSB Group them in 3 bits Stuff zero or zeros,on MSB side.
Convert the decimal binary $(.1101111000111)_2$ to octal	
$(\underline{.110}\ \underline{111}\ \underline{100}\ \underline{011}\ \underline{100})_2$ → $(.6\quad 7\quad 4\quad 3\quad 4)_8$	Rules for Decimal numbers Start from MSB and move right towards LSB Group them in 3 bits Stuff zero or zeros if required, in the LSB Side, if needed

Double Dabble – Octal to Binary

Problem 15: Convert (642.71)$_8$ to binary.

(6 4 2 . 7 1)$_8$

(110 100 010 . 111 001)$_2$

The equivalent binary is **(110 100 010 . 111 001)$_2$**

What is the weight of a MSB in a 10 bit number?

2^9

Octal Addition

Problem 16: Add $(256)_8$ and $(175)_8$

$(256)_8$	Units digits : 6+5 = $(11)_8$ → carry(1)8 + 3
$(175)_8$	∴carry is 1 addition is 3
$(453)_8$	Tens Digits :) 5 + 7 +1(carry) = $(13)_8$
	$(13)_8$ = (carry1)8 + 5(addition 5)
	Hundreds Digits :) 2 + 1 +1(carry) = $(4)_8$

Hexa-Decimal to Octal

Problem 17: Convert $(3AF)_{16}$ to ( )$_8$

Step (1): Hexa to Binary **(4Bits)**

Step (2): Regroup the binary bits into **groups of 3 bits**

Step (3): Binary to Octal

Follow the same rules for grouping and stuffing of extra bits, as in hexa-decimal to binary conversion.

3	A	F	
0011	1010	1111	← Hex to Binary
001 110	101	111	← Group in 3 bits
(1 6	**5**	**7)$_8$**	

6.2.10 ONE's Complement

What is One's complement ?

In a binary number, if the **ONEs are changed to ZEROs and the ZEROs are changed to ONEs**, the resultant binary number is the ONE's COMPLEMENT of the original binary number.

Example: Ones complement of $(1001110)_2$ is $(0110001)_2$

Problem 18: Find ones Complement of $(39)_{10}$

$(39)_{10}$ = 1 0 0 1 1 1

1's complement = 0 1 1 0 0 0

Problem 19: Find ones complement of $(46.875)_{10}$

$(46.875)_{10}$ = 1 0 1 1 1 0 . 1 1 1

1'scomplement = 0 1 0 0 0 1 . 0 0 0

Sign Convention

$(7)_{10}$ in decimal, is equal to $(111)_2$ in binary.

Now we can add **sign conventions** to this.

For example what is the binary equivalent of $(+7)_{10}$?

For a positive decimal number, a 0 is added as MSB, in its binary equivalent.

$(+7)_{10} = (0111)_2$

For a negative decimal number, a 1 is added as MSB, in its binary equivalent.

$(-7)_{10} = (1111)_2$

Rules: If the **MSB is 0, the number is + ve**

If the **MSB is 1, the number is - ve**

The table below illustrates one's complement and sign conventions clearly

Decimal	Binary equivalent				1's complement				Decimal
+0	0	0	0	0	1	1	1	1	-0
+1	0	0	0	1	1	1	1	0	-1
+2	0	0	1	0	1	1	0	1	-2
+3	0	0	1	1	1	1	0	0	-3
+4	0	1	0	0	1	0	1	1	-4
+5	0	1	0	1	1	0	1	0	-5
+6	0	1	1	0	1	0	0	1	-6
+7	0	1	1	1	1	0	0	0	-7

The number of binary digits is 4 here. Therefore, n = 4.

Max +ve numbers = 7 $= 2^3-1$ $= 2^{4-1}-1$ $= \mathbf{2^{n-1}-1}$

Max -ve numbers = 7 $= 2^3-1$ $= 2^{4-1}-1$ $= \mathbf{2^{n-1}-1}$

In the table above,

all the binary nibbles in the left half have their MSB = 0 and hence they are all +ve digits

all the binary nibbles in the right half have their MSB = 1 and hence they are all –ve digits

and the subsequent bits are in 1's complement form

6.2.11 Two's complement

Problem 20: What is Two's complement?

Take a Binary number $(17)_{10}$ $(10001)_2$
Take 1's Complement (01110)
Add 1 to it 1 +
This is the 2's complement **01111**
Therefore, $(01111)_2$ is the two's complement of $(10001)_2$

Problem 21: Find 2's complement $(39)_{10}$

$(39)_{10}$ = (1 0 0 1 1 1)$_2$
1's complement = (0 1 1 0 0 0)$_2$
Add 1 = 1+
2'scomplement = $(\mathbf{0\,1\,1\,0\,0\,1})_2$

How to verify the answer for 2's complement?

Add the given number and the twos complement computed. The result should be = 2^n
Where n = number of binary digits in the given number.
In the previous example,
Given ' number = (1 0 0 1 1 1)$_2$ **number of bits = n = 6**
2's complement = (0 1 1 0 0 1)$_2$
Add these two = (1 0 0 0 0 0 0) = (64)$_{10}$

(64)$_{10}$ = 2^6 = 2^n (VERIFIED)

The table below illustrates this clearly

Decimal number	Binary equivalent	1's complement	2's complement
0	0 0 0 0	1 1 1 1	1 0 0 0 0
1	0 0 0 1	1 1 1 0	1 1 1 1
2	0 0 1 0	1 1 0 1	1 1 1 0
3	0 0 1 1	1 1 0 0	1 1 0 1
4	0 1 0 0	1 0 1 1	1 1 0 0
5	0 1 0 1	1 0 1 0	1 0 1 1
6	0 1 1 0	1 0 0 1	1 0 1 0
7	0 1 1 1	1 0 0 0	1 0 0 1

Problem 22: Find 2's Complement of $(12.375)_{10}$

$(12.375)_{10}$ = $(1100.011)_2$
There are 4 bits before the decimal. Therefore **n = 4**
What is 2's Complement of 1100.011 = $(12.375)_{10}$
1's Complement = 0011.100
Add 1 1
$\therefore$ 2's Complement = 0011.101 = **$(3.625)_{10}$**

Verification; The answer can be verified, by adding the given number and its 2's complement. Answer should be 2^n where n is number of digits. In this example, n=4 and 2^n =16. .

For example the given number was	12.375	$(1100.011)_2$
2's complement was found to be	3.625	$(0011.010)_2$
Total	**16.000**	**$(10000.000)_2$**

This is equal to $2^4 = 2^n$ where n = 4

Problem 23: Find 2's Complement of $(0.1110100)_2$

1's Complement	=	0.0001011
Add 1	=	1
2's Complement	=	**0.0001100**

How to find 2's Complement ? – the easy way

Problem 24: Find 2's complement of 100111

How many bits are there? 6 Therefore, n = 6

Easy way to find 2's Complement is 2^6 - 100111

= 1000000

− 100111

011001

How to subtract using 2's Complement method?

Problem 25: Subtract 22 − 17

1) 22 is a +ve number. Leave it alone $(22)_{10}$ = 00010110

−17 is –ve. Find 2's compfor the –ve number.

17	=	00010001
1's complement of 17	=	11101110
Add 1	=	1
2's complement	=	11101111

Add to 22 +11101111

SUM 1 00000101

Discard carry if any

RESULT is $(00000101)_2$ → 5

MSB is 0. Therefore the number is +ve

∴ Answer is **+5**

Rules: Flow chart:

1. For +ve numbers, no complementing.
2. For negative numbers, find 2's complement and add to the first number.
3. After adding, in the SUM obtained, discard carry if any and obtain the RESULT.
4. Note, RESULT IS NOT THE FINAL ANSWER.
5. If the MSB is 0 in the RESULT, the answer is the RESULT itself.
6. If the MSB is 1 in the RESULT, the answer is the 2's complement of the RESULT.

==========

6.2.12 More examples on Binary subtraction using 2's complement

Problem 26: Subtract $(55)_{10}$ from $(45)_{10}$

Rules:

1. 55 is to be subtracted. ∴ Take 2's complement of 55

2. Add 45 and 2's complement of 55 and obtain the result.
   The result is not the final answer YET.
3. If there is a carry, the answer is +ve. The result obtained is the answer.
   (IGNORE CARRY)
4. If there is NO carry, the answer is –ve. The result obtained shd undergo 2's complement once again to get the answer.

55 = 110111
2's complement of 55
1's complement = 001000
Add 1 = 1
2's complement = 001001

45 = 101101
2's complement of 55 = 001001
Add = 110110 (RESULT)

No carry. ∴Answer is –ve. ∴RESULT shd undergo 2's complement again

110110 ← Result
001001 ← 1's Complement
1 ← add 1
001010 ← 2's Complement

∴ The Answer is **-10**

Problem 27: Subtract (11 - 3)

11 = 1011
2's complement of 3 = 1101
Add = 11000 (Result)

2's complement of 3
3 = 0011
1's complement = 1100
Add 1 = 1
2's complement = 1101

There is a carry. Ignore it
∴ Answer is +ve
Result is the answer (No more 2's Comp needed)
∴ Answer is **+8**

Problem 28: Substract (4 - 12)

4 = 0100
2's complemented of 12 = 0100
Add = 1000

2's complement of 3
$(12)_{10}$ = 1100
1's complement = 0011
Add 1 = 1
2's complement$(12)_{10}$ = 0100

No carry. ∴ take 2's Complement
Twos complement of $(1000)_2$ = $(1000)_2$ = $(8)_{10}$
No carry ∴Answer = **$-(8)_{10}$**

Binary subtraction using 1's complement method

Problem 29: Subtract 7 from 9, using 1's complement

9 = 1001 ----- A
7 = 0111
1's Complement 0111 → 1000 ----- B
Add A and B 10001
If carry is one, add it back 1
0010 = 2

7 is to be subtracted
∴Take one's complement of 7

Rule : if the carry is 1,
a) The answer is +ve
b) Add the carry, back as illustrated

Carry=1 and therefore, the final answer will be positive.
∴Answer is +ve = **+2**

Problem 30: Subtract 25 – 15, using 1's complement

25 = = 11001

15 = 01111, 1's complement of 15 = 10000

Add 101001

15 is to be subtracted
∴Take 1's complement for 15

Carry 1 ∴add it back 1

Carry 1 ∴Answer is +ve 01010 = 10

Answer is **+10**

Problem 31: Subtract 15 – 25, using 1's complement

25 is to be subtracted. ∴ take 1's complement of 25

25 is to be subtracted
∴Take 1's complement for 25

15 = = 01111

25 = 11001, 1's complement of 25 = 00110

Add both (RESULT) 10101

Rule : if the carry is 0,
c) The answer is -ve
d) Take 1's complement again.

Carry = 0 ∴ Take 1's complement of this RESULT.

Carry = 0 ∴The answer is going to be -ve

1's complement of the RESULT 10101 = 01010 = 10

Since carry =0, the answer is **– 10**

==========

6.2.13 Division and Multiplication: The methods are very similar to decimal division.

Binary Division
(similar to decimal division)
Divide 110110 by 110

```
        1001
110  ) 110110
       110
       ---
       110
       110
       ---
         0
```

$54 \div 6 = (9)_{10}$

$110110 \div 110 = (1001)_2$

Binary Multiplication
(Similar to Decimal Multiplication)
Multiply 1010 X 101

```
  1010
   101
  ----
  1010
 0000
1010
------
110010 = 50   (10 X 5 = 50)
```

==========

6.2.14 Binary coded decimal : In this, the decimal numbers are represented using their binary equivalents

$$(275)_{10} = \left(\frac{\mathbf{0010}}{\mathbf{2}}\ \frac{\mathbf{0111}}{\mathbf{7}}\ \frac{\mathbf{0101}}{\mathbf{5}}\right)_{\boldsymbol{BCD}}$$

Application : Displays
Digital clocks, calculations
Electronic counters

Chapter 7 -- Boolean Algebra and Digital circuits

Module – 3: Part 2 - Syllabus: Boolean Algebra Theorems, De Morgan's theorem.
Digital Circuits: Logic gates, NOT Gate, AND Gate, OR Gate, XOR Gate, NAND Gate, NOR Gate, X-NOR Gate. Algebraic Simplification, NAND and NOR Implementation (Sections 11.7 and 11.8): NAND Implementation, NOR Implementation. Half adder, Full adder. Switching and logic levels

7.1 Digital electronics and Boolean Algebra

7.1.1 What is a Switching circuit? Refer fig 7.1

Figure shows a mechanical switch. When this switch is open, the output will be 5V, (through R). When the switch is closed the output is 0V (grounded). In digital electronics this mechanical switch is replaced by a transistor (an electronic switch).

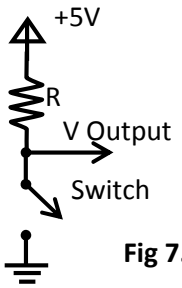


Fig 7.1 Digital switch

Switch	Logic	Output	Boolean	State	Boolean variable
OFF	Low	0V	Zero	False	$\overline{\mathbf{A}}$
ON	High	5V	One	true	**A**

The output may be denoted by different terms which are all listed in the table above.

==========

7.1.2 Logic gates

- A logic gate is a fundamental building block of a digital circuit.
- Logic gates will have one or more inputs and usually one output.
- The inputs can be LOW (ZERO) or HIGH (ONE). The output will be determined by the LOGIC followed by that particular gate.
- There are seven basic logic gates: AND, OR, XOR, NOT, NAND, NOR, and XNOR.

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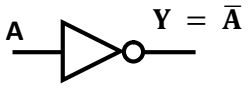
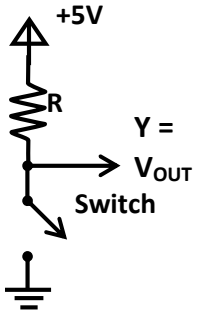
NOT (Inverter) Gate

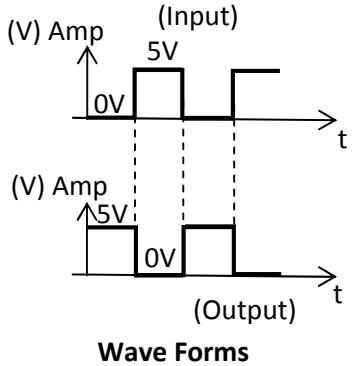


$\boldsymbol{Y = NOT\ A = \overline{A}}$

$\overline{A} = Complement\ of\ A$



A	Y
1	0
0	1

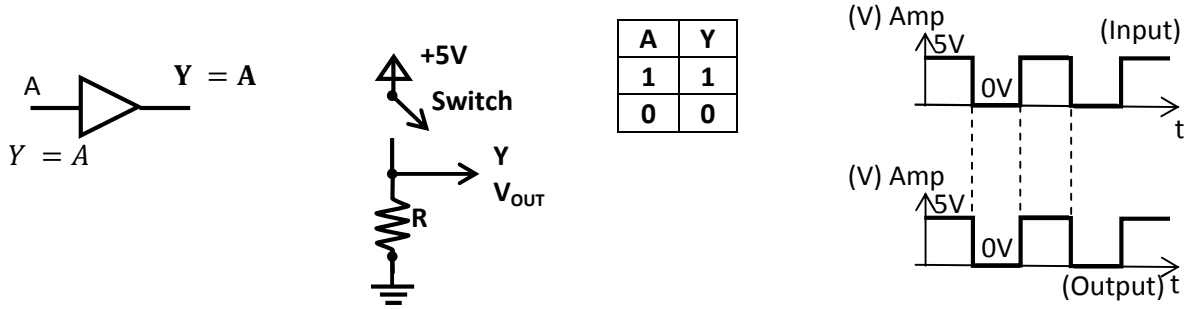


Wave Forms

Fig 7.2 (a, b, c, d) NOT Gate , Equivalent switch, Truth Table

==========

Buffer



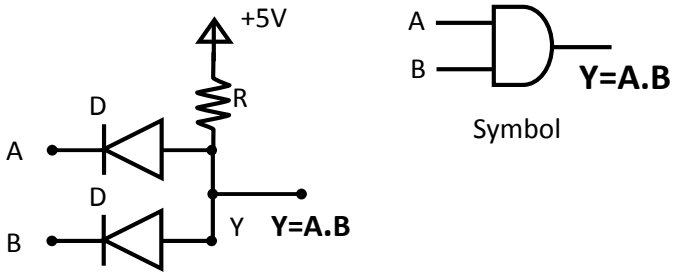
A	Y
1	1
0	0

Fig 7.3 (a, b, c, d) Buffer Gate , Equivalent switch, Truth Table and waveforms

Why buffer? In specific applications, when a single gate output has to be connected to many inputs, the gate output gets overloaded. To avoid this, a buffer is used between this gate and the load (which consists of many inputs). A buffer output can drive many inputs.

==========

AND GATE



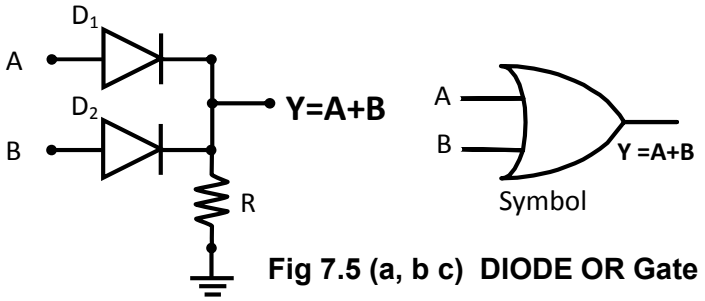
A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

Fig 7.4 (a, b c) DIODE AND Gate , Symbol and Truth Table

It is an **"ALL-ONES"** detector. **In AND, output is ONE if and only if all inputs are one**

A.0 = 0 (B = 0)
A.1 = A (B = 1)
A.A = A (B = A)
When A = 0 or B = 0, the diode is forward biased and hence Y also becomes zero.
When A and B are 1, both diodes are reverse biased and Y becomes +5 V

OR GATE Output will be high if A or B or both are high. Output will be low if and only if all inputs are low. It is an "**ALL-ZEROs**" detector.

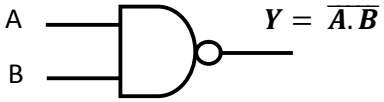


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Fig 7.5 (a, b c) DIODE OR Gate , Symbol and Truth Table

A + 0 = A (B = 0) IF A = 1, D1 becomes forward biased and Y = 1
A + 1 = 1 (B = 1) If B = 1, D2 becomes forward biased and Y = 1.
A + A = A (B = A) Same for A = 1 and B = 1. When A and B are 0, both D1 and D2 are reverse biased and Y becomes 0.

NAND GATE



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Fig 7.6 (a, b) NAND Gate Symbol and Truth Table

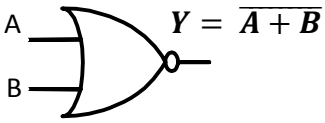
Y = NOT (A AND B)

= $\overline{A.B}$

= Complement of AND **All-ONES** detector (like AND)

==========

NOR GATE



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Fig 7.7 (a, b) NAND Gate Symbol and Truth Table

Y = NOT (A OR B)

= $\overline{A+B}$

= Complement of OR All ZEROs detector (like OR)

==========

Problem 1 : Fill up the truth table and implement with appropriate gates.

XYZ	X.Y.Z	X+Y+Z	$\overline{X.Y.Z}$	$\overline{X+Y+Z}$
000	0	0	1	1
001	0	1	1	0
010	0	1	1	0
011	0	1	1	0
100	0	1	1	0
101	0	1	1	0
110	0	1	1	0
111	1	1	0	0

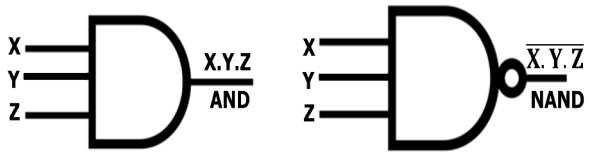
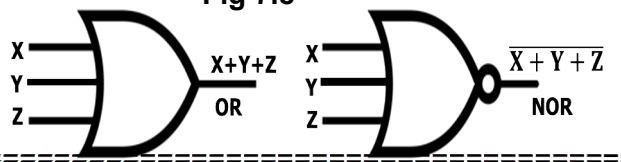


Fig 7.8



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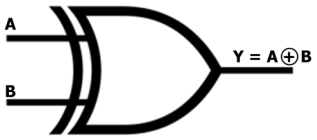
Exclusive OR (Ex-OR)



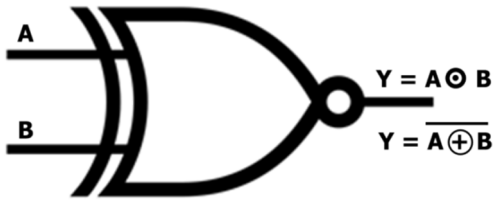
⊕ **Symbol for Exclusive OR**

Output =1 if and only if the inputs are of opposite polarity

Truth Table		
A	**B**	**Y = A⊕B**
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

Fig 7.9 Exclusive OR gate and Truth Table

Exclusive NOR (Ex—NOR) gate: It is also known as Coincidence gate or Equivalence gate.



⊙ Symbol for Exclusive NOR

Output =1 if and only if the inputs are of same polarity

Truth Table		
A	B	Y = A⊙B
0	0	1
0	1	0
1	0	0
1	1	1

Fig 7.10 Exclusive NOR gate and Truth Table

==========

Name a few Digital Technologies

T.T.L (Transistor-Transistor Logic),
CMOS (Complementary Metal Oxide semiconductor)
ECL (Emitter Coupled logic)

==========

Bubbled AND GATE

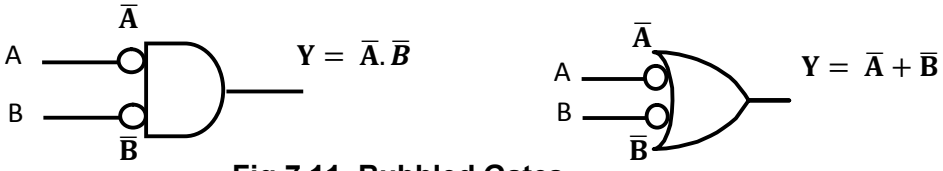


Fig 7.11 Bubbled Gates

Note: $\overline{A} \cdot \overline{B}$ is <u>NOT</u> equal to $\overline{A.B}$

Using Bubbled Gates prove De Morgans Theorem

1) $\overline{A+B} = \overline{A}\,\overline{B}$ **(Law1)** 2) $\overline{AB} = \overline{A} + \overline{B}$ **(Law2)**

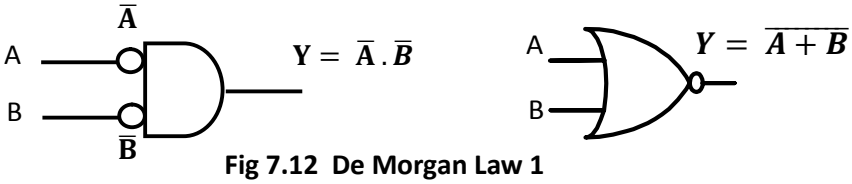


Fig 7.12 De Morgan Law 1

A	B	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$	A+B	$\overline{A+B}$
0	0	1	1	1	0	1
0	1	1	0	0	1	0
1	0	0	1	0	1	0
1	1	0	0	0	1	0

$\overline{A+B} = \overline{A}\,\overline{B}$

Law1 Proved

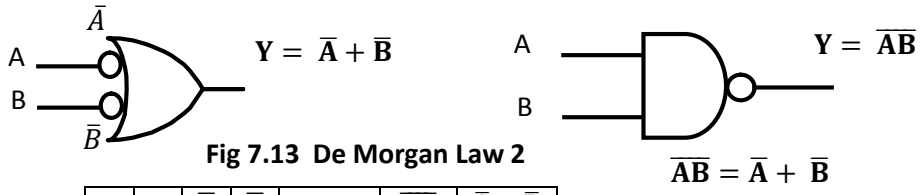


Fig 7.13 De Morgan Law 2

Law2 Proved

A	B	$\bar{A}$	$\bar{B}$	A.B	$\overline{AB}$	$\bar{A} + \bar{B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	1	0	0

Prove NAND is a univerasal gate

What is a universal gate?

A gate using which all logic operations such as AND, OR, Invert, EXOR, NAND, NOR can be implemented. Refer figures 7.14 (a) to (e)

Universal Gate NAND

Inverter gate:

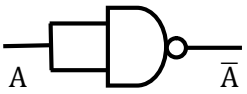


Fig 7.14 (a)

OR Gate:

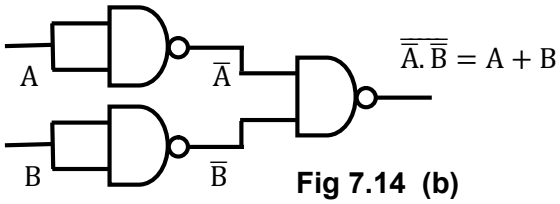


Fig 7.14 (b)

NOR gate:

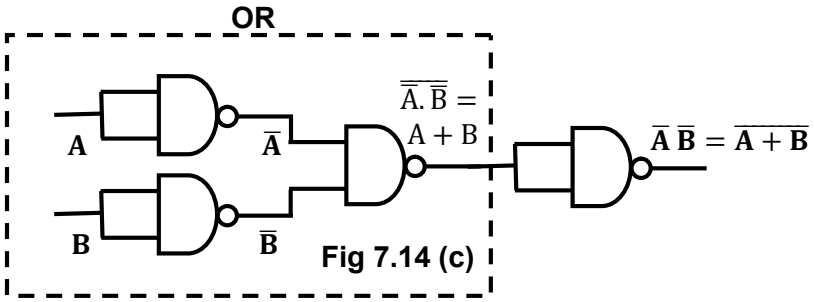


Fig 7.14 (c)

AND gate:

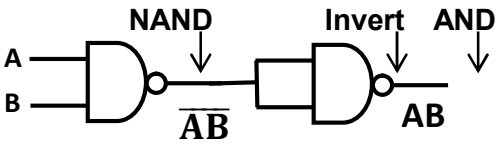


Fig 7.14 (d)

EX-OR Gate

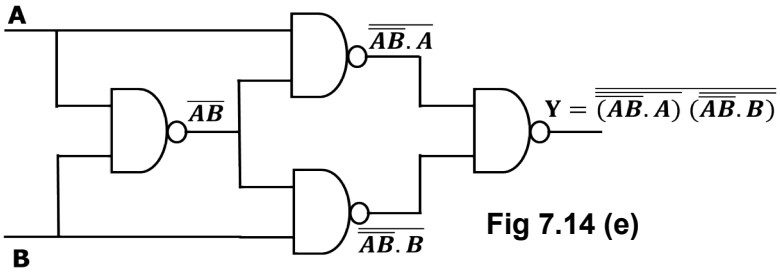


Fig 7.14 (e)

$Y = \overline{\overline{\overline{AB}.A}\ \overline{\overline{AB}.B}}$ $= \overline{AB} \cdot A + \overline{AB} \cdot B$

$= \overline{AB}\,(A + B)$

$= ((\bar{A} + \bar{B})\,(A + B)$

$= \bar{A}B + A\bar{B}$

==========

Prove NOR is a universal gate. Refer figures 7.15 (a) to (e)

NOT

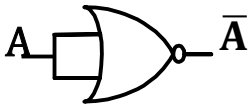


Fig 7.15 (a)

BUFFER

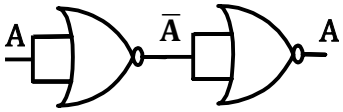


Fig 7.15 (b)

OR

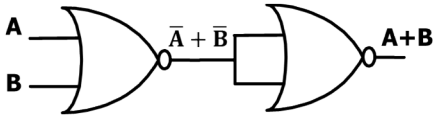
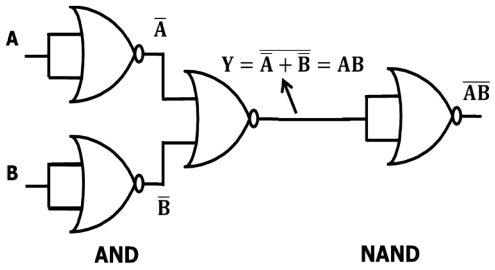
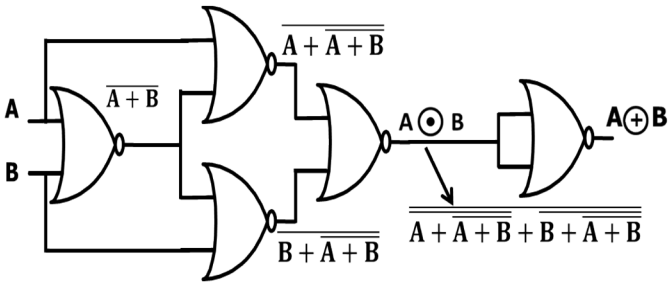


Fig7.15 (c)

AND / NAND



AND / NAND Fig 7.15 (d)



EX-OR Fig 7.15 (e)

Proof : $\overline{\overline{A + \overline{A + B}} + \overline{B + \overline{A + B}}}$ $= (A + \overline{A + B}) \cdot (B + \overline{A + B})$

$= (A + \bar{A}.\bar{B}) \cdot (B + \bar{A}.\bar{B})$

$= AB + A \cdot \bar{A}\,\bar{B} + \bar{A}\,\bar{B}.\mathrm{B} + \bar{A}\,\bar{B} \cdot \bar{A}\,\bar{B}$

$= AB + 0 + 0 + \bar{A}\,\bar{B}$

$= AB + \bar{A}\,\bar{B}$

$= \mathrm{A} \odot \mathrm{B}$

==========

7.1.3 Boolean Algebra:

What is boolean algebra?

Switching and logic levels: In binary digital circuits, the variables can have only two values (ONE or ZERO). These variables are governed by a branch of Algebra, which is known as Boolean algebra. Look at the table below, which describes different kinds of variables.

OR	**AND**
A + A = A	A.A = A
A + $\bar{A}$ = 1	A.$\bar{A}$ = 0
0 + A = A	0.A = 0
1 + A = 1	1.A = A
A + B = B + A (Commutative)	A.B = B.A (Commutative)
A + (B + C) = (A + B) + C (Associative)	A.(B.C) =(A.B).C (Associative)
(A + B).C = (A + B) (A + C) (Distributive)	A.(B + C) = A.B + A.C (Distributive)
$\bar{A} + \bar{B} = \overline{A \cdot B}$ (Demorgan)	$\bar{A}\,\bar{B} = \overline{A + B}$ (Demorgan)

Basic Boolean Algebra rules (Refer fig 7.16 (a) to 7.16 (f)

a. A + A = A

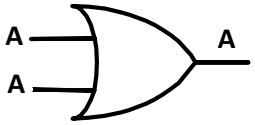


Fig 7.16 (a)

A	A	A
0	0	0
0	1	1

b. $A + \bar{A} = 1$

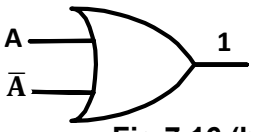


Fig 7.16 (b)

A	$\bar{A}$	A
0	1	1
1	0	1

c. 0 + A = A

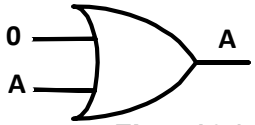


Fig 7.16 (c)

0	A	A
0	0	0
0	1	1

d. 1 + A = 1

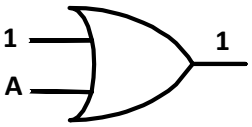


Fig 7.16 (d)

1	A	1
1	0	1
1	1	1

e. A + (B + C) = (A + B) + C

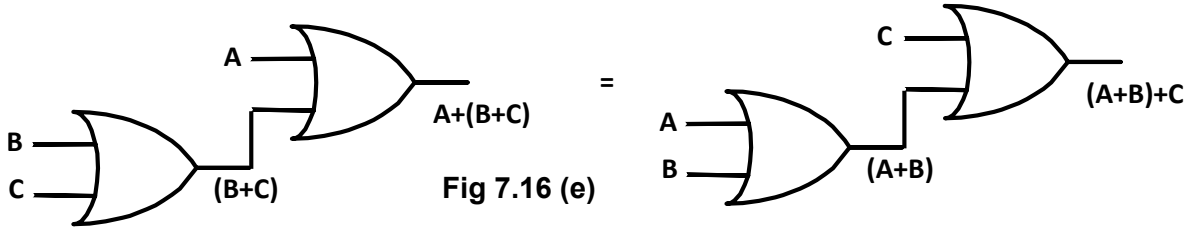


Fig 7.16 (e)

f. **A + (B · C) = (A + B) (A + C)**

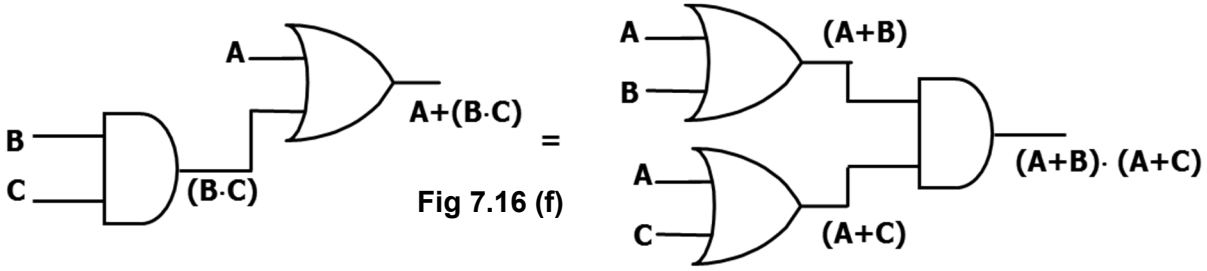


Fig 7.16 (f)

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7.1.4 Demorgan Theorem : $\overline{A} + \overline{B} = \overline{A.B}$

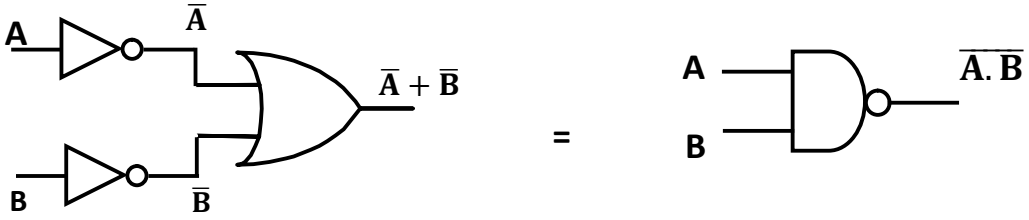


Fig 7.17

Boolean Algebra Problems

Problem 2: Simplify A + $\overline{A}\ \overline{B}$ **+ A C**

= A + A C + $\overline{A}\,\overline{B}$
= A (1 + C) + $\overline{A}\ \overline{B}$
= A + $\overline{A}\ \overline{B}$
= (A + $\overline{A}$) (A + $\overline{B}$) (Distributive)
= **A +** $\overline{B}$

Problem 3: Simplify A + $\overline{A}\ B$ **C +** $\overline{A}$ **B** $\overline{C}$

= A + $\overline{A}$ B (C + $\overline{C}$)
= A + $\overline{A}\ B$
= (A + $\overline{A}$) (A+ B) (Distributive)
= **A +** B (since X + $\overline{X}$ = 1)

Problem 4: Simplify A.B + $\overline{A}$ **C +** $\overline{A}$ **D +** $\overline{B}$ **C +** $\overline{B}$ **D**

= A B + $\overline{A}$ (C + D) + $\overline{B}$ (C + D)
= A B + ($\overline{A}$ + $\overline{B}$) (C + D)
= A B + $\overline{A.B}$ (C + D) (DeMorgan)
= (A B + $\overline{A\,B}$) (A B + C + D) (Distributive)
= **(A B + C + D)** (since X + $\overline{X}$ = 1)

Problem 5: Simplify using DeMorgan's theorem: $\overline{\overline{(a+d)}.\overline{(b+C)}}$.

= $\overline{\overline{(a+d)}}$ + $\overline{\overline{(b+C)}}$.
= (a + d) + (b + c)
= **a + b + c + d**

Problem 6: Simplify using DeMorgan's theorem

Solve: (a) $\overline{ABCD}$ (b) **ABCD** **(c) W + X + Y + Z**

(a) = $\overline{ABCD}$ = $\overline{A} + \overline{B} + \overline{C} + \overline{D}$

(b) = **ABCD** = $\overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$

(c) = **W + X + Y +Z** = $\overline{\overline{W}.\overline{X}.\overline{Y}.\overline{Z}}$

= $\overline{W + X + Y + Z}$ = $W.\overline{X}.\overline{Y}.\overline{Z}$

Problem 7: Solve using D Morgan: $\overline{\overline{A + B\overline{C}} + D(E + \overline{F})}$

= $\overline{\overline{A + B\overline{C}}}$. $\overline{D(E + \overline{F})}$

= **[**$A + B\overline{C}$**]**.[$D(E + \overline{F}$ **)]**

Problem 8: Simplify: P (Q +R) + Q (Q + R) + P Q

= P Q + P R + Q Q + Q R + P Q

= P Q + Q R + P R + Q

= Q (P + R + 1) + P R = **Q + P R**

Problem 9: Simplify: A $\overline{B}$ + A ($\overline{B + C}$) + B $\overline{(B + C)}$

= A $\overline{B}$ + A $\overline{B}.\overline{C}$ + B.$\overline{B}.\overline{C}$

= A $\overline{B}$ (1 + $\overline{C}$) + 0 = **A** $\overline{B}$

Problem 10: Simplify: $\overline{X}$ Y Z + X $\overline{Y}$ $\overline{Z}$ + $\overline{X}$ $\overline{Y}$ $\overline{Z}$ + X $\overline{Y}$ Z + X Y Z

= $\overline{X}$ Y Z + X $\overline{Y}$ $\overline{Z}$ + $\overline{X}$ $\overline{Y}$ $\overline{Z}$ + X $\overline{Y}$ Z + X Y Z+ X Y Z+ X Y Z [A + A = A]

= Y Z ($\overline{X}$ + X) + $\overline{Y}$ $\overline{Z}$ (X + $\overline{X}$) + X Z ($\overline{Y}$ + Y)

= **Y Z +** $\overline{Y}$ $\overline{Z}$ **+ X Z**

Problem 11: Simplify: C [(A $\overline{B}$ + A $\overline{B}$ (C + B D)]

= C [(A $\overline{B}$ + A $\overline{B}$ C +A $\overline{B}$ B D]

= C [A $\overline{\text{B}}$ + A $\overline{\text{B}}$ C]

= A $\overline{\text{B}}$ C + A $\overline{\text{B}}$ C

= **A** $\overline{\textbf{B}}$ **C**

Problem 12: Simplify: (X + $\overline{\text{X}}$ **Z + X Y** $\overline{\text{Z}}$**) (**$\overline{\text{X}}$ $\overline{\text{Z}}$ **+** $\overline{\text{X}}$ **Z)**

= [X (1 + Y $\overline{\text{Z}}$) + $\overline{\text{X}}$ Z] [($\overline{\text{X}}$ +$\overline{\text{Z}}$) + $\overline{\text{X}}$ Z]

= (X + $\overline{\text{X}}$ Z) [$\overline{\text{X}}$ (1 + Z) + $\overline{\text{Z}}$]

= (X + Z) ($\overline{\text{X}}$ + $\overline{\text{Z}}$)

= X $\overline{\text{X}}$ + X $\overline{\text{Z}}$ + $\overline{\text{X}}$ Z + Z $\overline{\text{Z}}$

= **X** $\overline{\textbf{Z}}$ **+** $\overline{\textbf{X}}$ **Z**

==========

Problem 13: What is the boolean for this logic

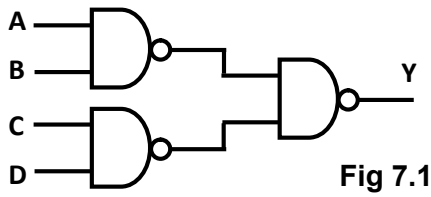


Fig 7.18

$Y = \overline{\overline{AB} \cdot \overline{CD}} = AB + CD$

==========

Problem 14: $\mathbf{AB + \overline{AC} + A\overline{B}C(AB + C)}$

= $AB + (\overline{A} + \overline{C}) + AA\overline{B}BC + A\overline{B}CC$

= $AB + (\overline{A} + \overline{C}) + A\overline{B}C$ $[\therefore B\overline{B} = 0]$

= $(\overline{A} + AB) + \overline{C} + (\overline{A} + A\overline{B}C)$ $[\therefore A + A = A]$

= $(\overline{A} + A)(\overline{A} + B) + \overline{C} + \overline{A} + A\overline{B}C$ [Distributive Law]

= $\overline{A} + B + \overline{C} + \overline{A} + \overline{B}C$ $[\therefore \overline{A} + A\overline{B}C = (\overline{A} + A)(\overline{A} + \overline{B}C)]$

= $\overline{A} + B + \overline{B}C + \overline{C} + \overline{A}$

= $\overline{A} + (B + C) + \overline{C}$

= $\overline{A} + B + 1$

= **1**

Problem 15: $\overline{\overline{A\overline{B}} + \overline{ABC} + A(B + A\overline{B})}$

= $\overline{\overline{A(\overline{B} + BC)} + A(B + A\overline{B})}$

= $\overline{\overline{A(\overline{B} + C)} + A(B + A)}$

= $\overline{\overline{A} + \overline{(\overline{B} + C)} + AB + AA}$

= $\overline{\bar{A} + \overline{(\bar{B} + C)} + AB + A}$

= $\overline{1 + \overline{(\bar{B} + C)} + AB}$ $[\therefore A + \bar{A} = 1]$

= $\bar{1}$ = **0**

==========

Problem 16: Prove $AB + A + AB = A$

$AB + A + AB = A(B + 1 + A)$ = **A**

==========

Problem 17: Simplify $\bar{X}\,\bar{Y}\,\bar{Z} + \bar{X}\,\bar{Y}\,\bar{Z} + \bar{X}\,\bar{Y} + X\,\bar{Y}$

$\bar{X}\,\bar{Y}[\,\bar{Z} + \bar{Z} + 1] + X\,\bar{Y}$

$\bar{X}\,\bar{Y} + X\,\bar{Y} = \bar{Y}\,(\bar{X} + X) = \bar{Y}$

==========

Problem 18: $A\,B\,C + A\,B\,\bar{C} + \bar{A}\,B\,C$

= $A\,B\,(C + \bar{C}) + \bar{A}\,B\,C$

= $A\,B + \bar{A}\,B\,C$ = $B\,(A + \bar{A}\,C)$

= $B\,(A + \bar{A})(A + C)$ = $B\,(A + C)$

= $AB + AC$

==========

Problem 19: $\overline{\overline{X\,Y + X\,Y\,Z} + X\,(Y + X\,\bar{Y})}$

= $\overline{\overline{X\,Y + X\,Y\,Z}} \cdot \overline{X\,(Y + X\,\bar{Y})}$

= $(X\,Y + X\,Y\,Z) \cdot \left(\bar{X} + \overline{Y + X\bar{Y}}\right)$

= $[X\,Y\,(1 + Z)] \cdot [\bar{X} + \overline{Y + X}]$

= $(X\,Y)\,(\bar{X} + \bar{Y}\,\bar{X})$

= $X\,\bar{X}\,Y + X\,Y\,\bar{Y}\,\bar{X}$

= **0**

==========

7.1.5 Logic Implementation

Problem 20: Implement the logic Y = $\overline{\overline{A}B} + \overline{A+B}$ without simplifying & after simplifying.

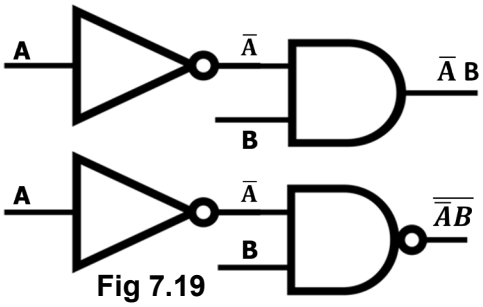


Fig 7.19

WITHOUT SIMPLIFICATION:

How to implement $\bar{A}$ B

Refer fig 7.19

Start with A. Get $\bar{A}$ out of A using an inverter.

Get $\bar{A}$ B thro an AND gate.

How to implement $\overline{\bar{A}B}$

Refer fig 7.19

Get $\overline{\bar{A}B}$ by making AND as NAND

How to get $\overline{A+B}$?

Refer fig 7.20

First get $A + B$**.** It is an OR function.

Then get $\overline{A+B}$ by converting OR into NOR.

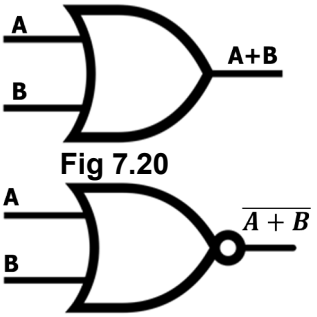


Fig 7.20

Combine both to realize $\overline{\bar{A}B} + \overline{A+B}$

Refer fig 7.21

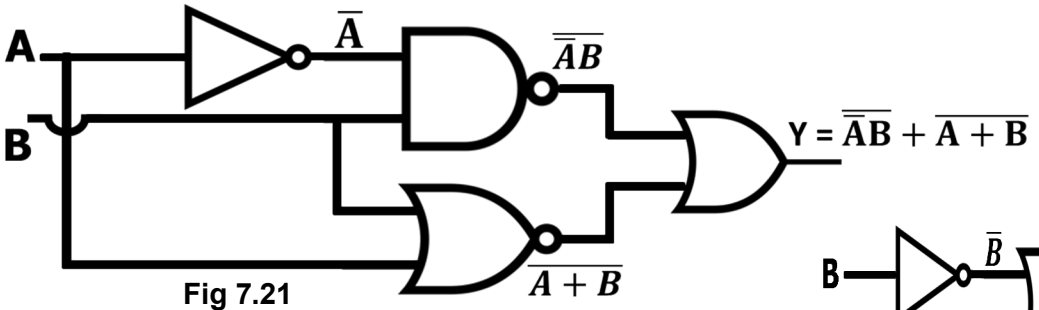


Fig 7.21

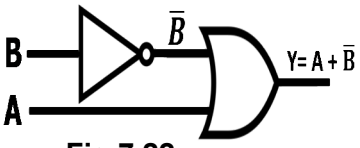


Fig 7.22

Problem 21: Simplify Y = $\overline{\bar{A}B} + \overline{A+B}$

= (A + $\bar{B}$) + ($\bar{A}$ $\bar{B}$)

= A + $\bar{B}$ (1 + $\bar{A}$)

Y = A + $\bar{B}$

(It means that output Y = 1 when input A = 1 or input B = 0). Refer fig 7.22

TRUTH TABLE		
A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

==========

7.1.6 Product of sums (POS) ➔ NOR-NOR

Problem 22: Implement Y = (A + B) (B + C) (C + A), using NOR gates

We want NOR. ∴Let us invert Y as $\bar{Y}$

$\overline{Y}$ = $\overline{(A+B)(B+C)(C+A)}$

= $\overline{(A+B)}$ + $\overline{(B+C)}$ + $\overline{(C+A)}$

NOR OR NOR OR NOR

Y = $\overline{\overline{(A+B)}+\overline{(B+C)}+\overline{(C+A)}}$

∴ **Y = (A + B) (B + C) (C + A).**

= (Sum) X (Sum) X (Sum)

This is in the form of "Product of sums " (POS)

Refer fig 7.23. This is an "**ALL-NOR"** implementation now.

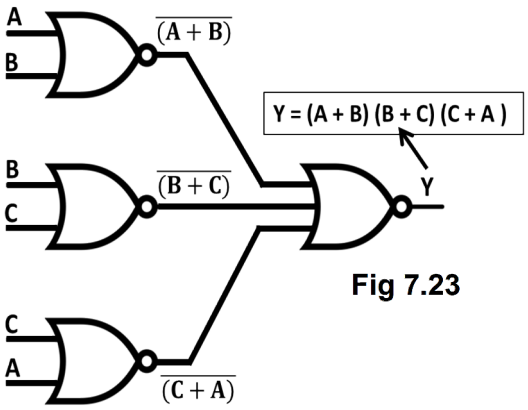


Fig 7.23

NOR - NOR Implementation

We can implement, a given Boolean function, using only NOR gates. This is known as **NOR - NOR** implementation.

Problem 23: Take this expression Y = (A + B) (B + C) D

Y = (A + B) (B + C) D

= (SUM) X (SUM) X (SUM) ➔ **Product Of Sums**

How to implement this using NOR –NOR. Refer fig 7.24

Rule 1: Implement using OR gates followed by AND gates.
Rule 2: Level 1 OR gates to be replaced by NOR gates.
Rule 3: Level 2 AND gates to be replaced by NOR gates.
Rule 4: If in level 1, there is a lone input, connect that input also through a 2input NOR.

Problem 24:Let us solve Y = (A +B) (B+C) D

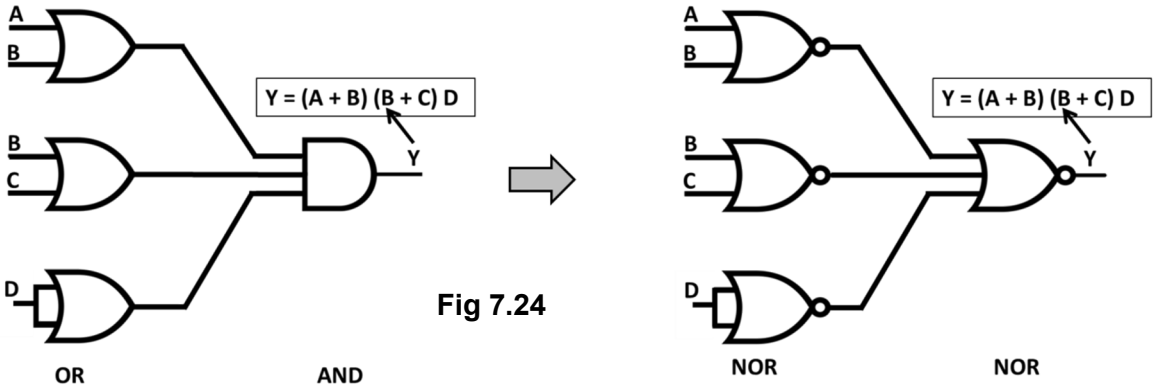


Fig 7.24

Problem 25: Simplify M = X $\overline{Y}$ Z + $\overline{X}$ Y $\overline{Z}$ using simple gates and also NOR -NOR gates.

NOR - NOR →POS.

M = X $\overline{Y}$ Z + $\overline{X}$ Y $\overline{Z}$

M = $\overline{\overline{X}+Y+\overline{Z}}+\overline{X+\overline{Y}+Z}$

= $\overline{(\overline{X}+Y+\overline{Z})(X+\overline{Y}+Z)}$

Thro simple gates Refer fig 7.25.

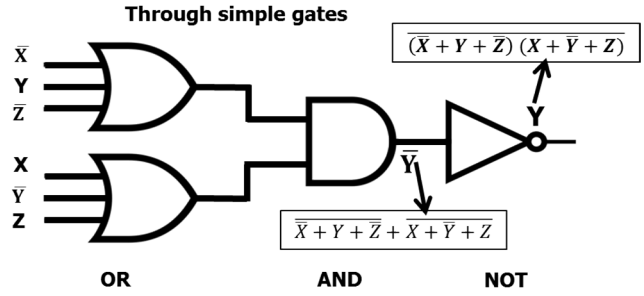


Fig 7.25

Using NOR – NOR Refer fig 7.26

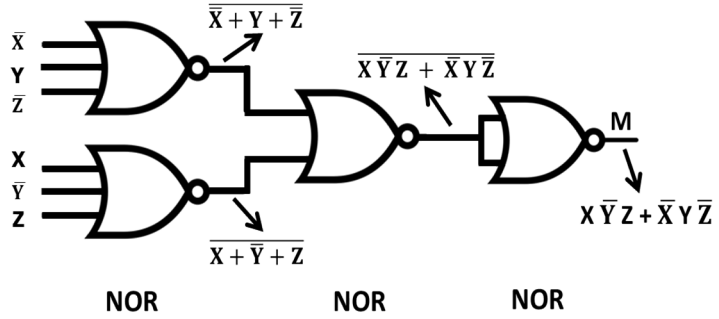


Fig 7.26

Problem 26: Implement using NOR - NOR gates, after simplification

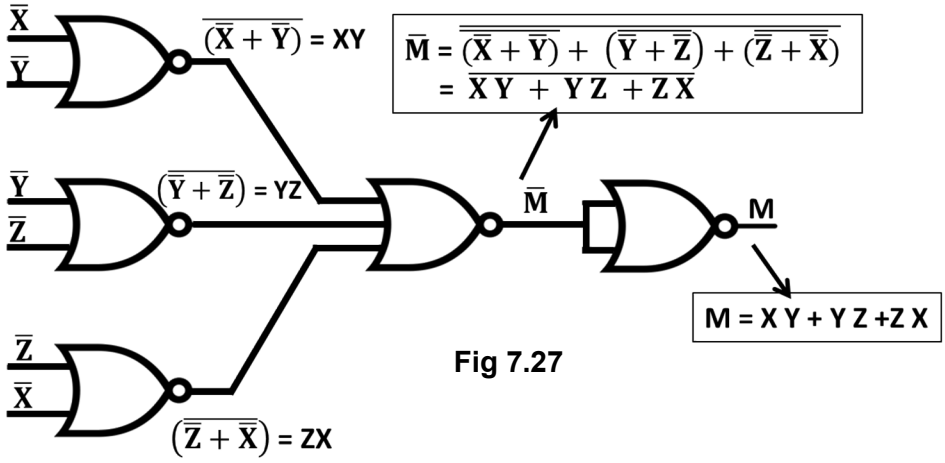


Fig 7.27

M = $\bar{X}$ Y Z + X $\bar{Y}$ Z + X Y $\bar{Z}$ + X Y Z.

After simplification as per **example 37 below**

M = X Y + Y Z + Z X . This is in SOP (sum of products) form.

We want NOR – NOR. Hence this has to be converted to POS (Product of Sum) Form.

M = X Y + Y Z +Z X

= $\overline{(\overline{XY})(\overline{YZ})(\overline{ZX})}$

There is a whole bar on top. This is not convenient for a 2 level NOR NOR implementation.

Therefore implement $\bar{M}$ first and then M

$\overline{M}$ = $\overline{X\,Y\ +\ Y\,Z\ +\ Z\,X}$

= $(\overline{XY})(\overline{YZ})(\overline{ZX})$ = $(\overline{X}+\overline{Y})(\overline{Y}+\overline{Z})(\overline{Z}+\overline{X})$

= $\overline{(\overline{\overline{X}+\overline{Y}})+(\overline{\overline{Y}+\overline{Z}})+(\overline{\overline{Z}+\overline{X}})}$

This can be implemented by NOR NOR combiImplementation. Refer fig 6.31

The output is still $\overline{M}$. Using a simple NOR inverter obtain M

==========

7.1.7 Sum of Products (SOP) - NAND NAND Implementation.

Let us see whether a given Boolean expression, can be implemented using only NAND gates. This is known as, **NAND –NAND** implementation

Problem 27: Take the expression Y = $\overline{X}$ Y Z + X $\overline{Y}$ Z + X Y $\overline{Z}$ + X Y Z

Simplify first

Y = $\overline{X}$ Y Z + X $\overline{Y}$ Z + X Y $\overline{Z}$ + X Y Z + X Y Z + X Y Z

= Y Z ($\overline{X}$ + X) + X Z ($\overline{Y}$ + Y) + X Y ($\overline{Z}$ + Z)

= Y Z + X Z + X Y

= X Y + Y Z + Z X

(Product) + (Product) + (Product).

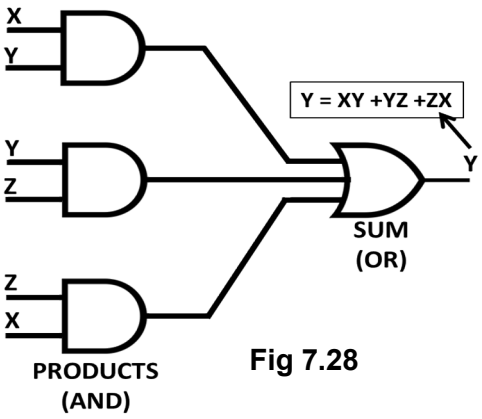


Fig 7.28

This is in the form of **Sum Of Products (SOP).**

Products X Y, Y Z and Z X are summed.

Refer fig 7.28

Implement Y = XY + YZ + ZX using basic gates.

This does not use NAND gates, but just **basic gates.**

How to convert this to NAND NAND form?

Rule 1: Implement using AND gates followed by OR gates.

Rule 2: The level 1 AND gates to be replaced by NAND gates

Rule 3: The level 2 OR gates to be replaced by NAND gates

∴ Fig 7.28 gets modified as fig 7.29.

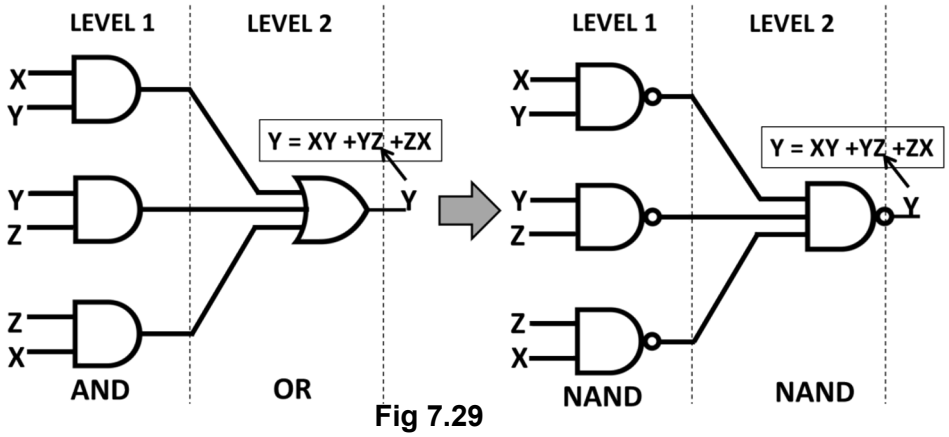


Fig 7.29

Rule 4:

Note : If in level 1there is a lone input, connect that input also through a 2 input NAND.

Problem 28: Simplify Y= A+ BCD using basic gates and NAND NAND gates. Refer fig 6.34

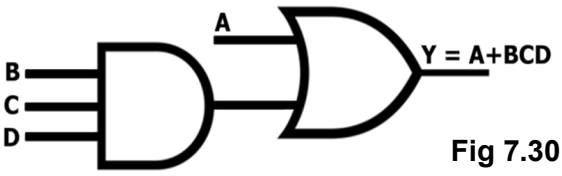
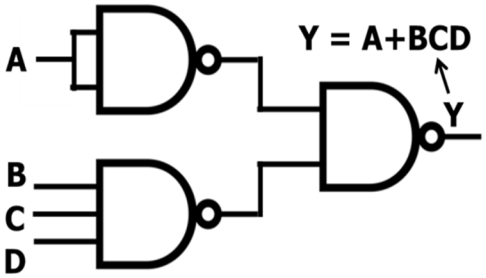


Fig 7.30



Problem 29: Implement Y = $\bar{P}$ Q + $\bar{Q}$ R + $\bar{R}$ S + T using NAND ---NAND gates, NAND- NAND → SOP Refer fig 7.31

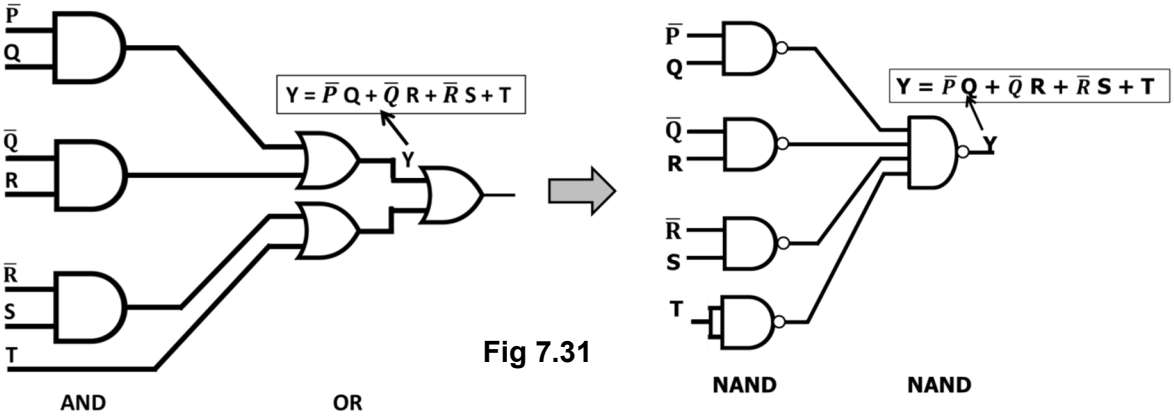


Fig 7.31

Problem 30: Implement through NAND – NAND Y = (L,M,N) = Σ m (1, 3, 2, 7)
NAND - NAND →SOP

Using Karnaugh Map the function is reduced to Y = $\bar{A}$ C + $\bar{A}$ B + B C
Refer fig 7.32 for implementation

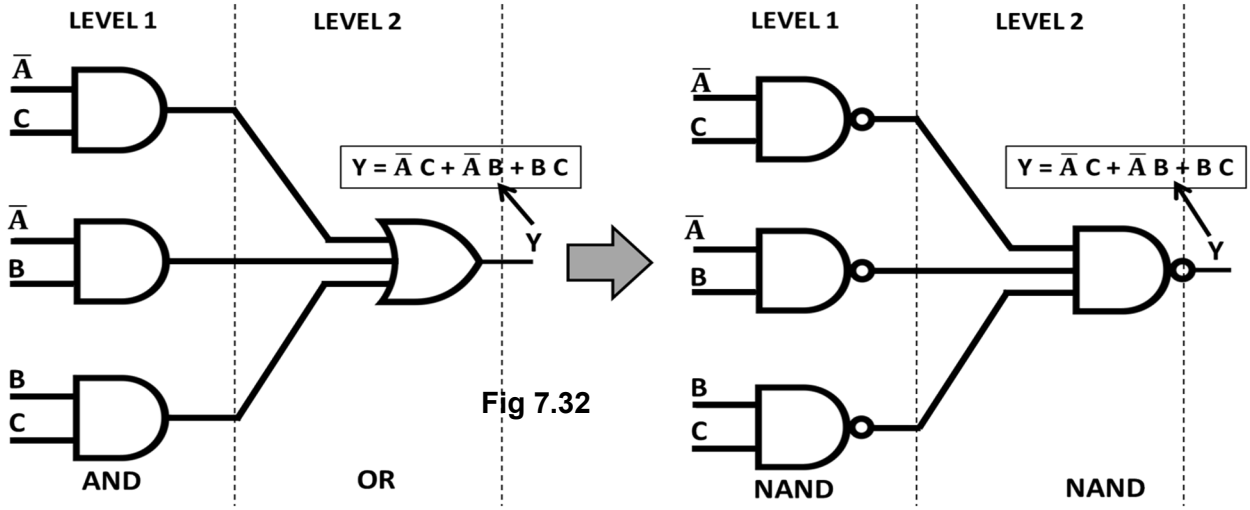


Fig 7.32

Implement the following using AND – OR gates and also NAND –NAND gates.

1) Exclusive - OR

2) Exclusive - NOR

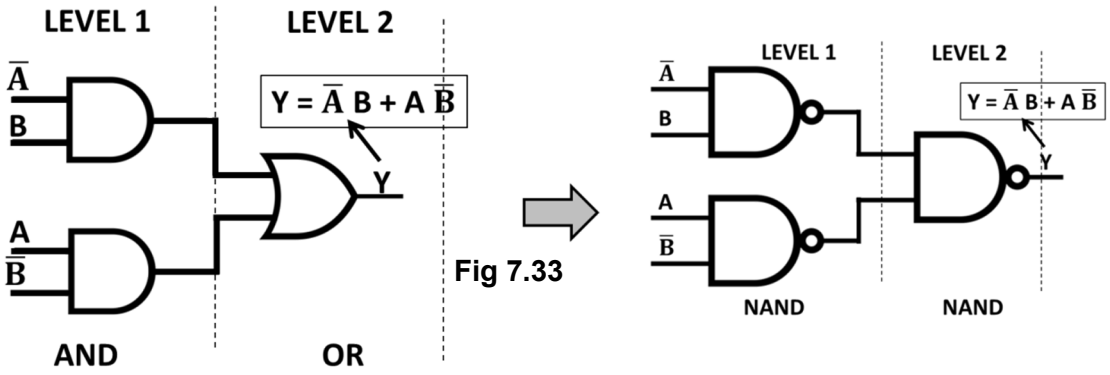


Fig 7.33

NAND – NAND → SOP

Refer fig 7.33 and fig 7.34

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1) Exclusive - OR Y = $\bar{A}$ B + A $\bar{B}$

2) Exclusive NOR Y = $\bar{A}$ $\bar{B}$ + A B

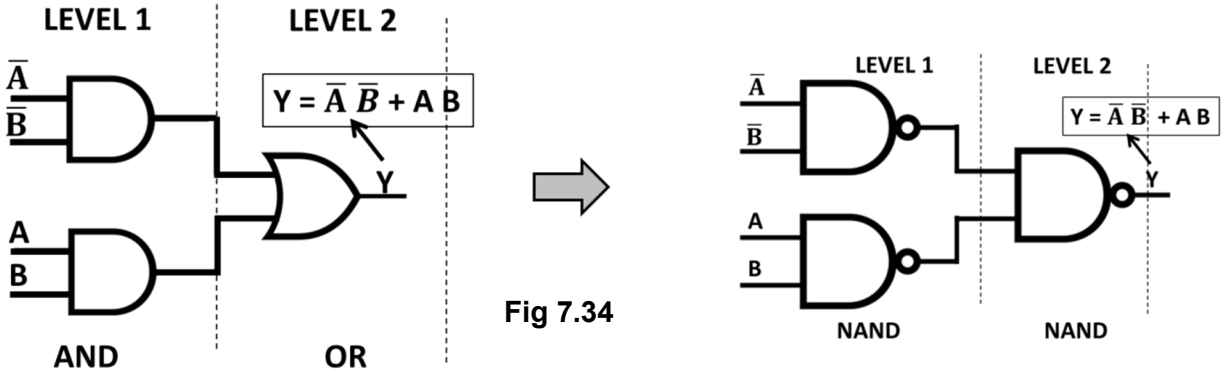

Fig 7.34

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7.2 Half adder:

Let us go back to the Boolean addition.
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 10

The last one, 1 + 1 = 10, produces a carry output.
These operations can be implemented through a logic circuit, known as half adder.

- Adder is a combinational logic circuit. Half adder adds two binary numbers
- A typical half adder produces a sum (S) and a carry (C) as the output, as shown above.
- The half adder will have two inputs viz **augend and addend** bits. It provides **two outputs. (sum and carry).**

Block diagram:

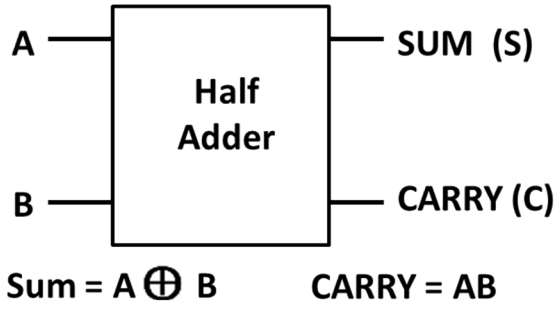


Fig 7.35

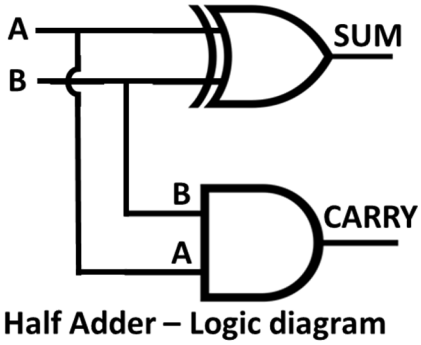
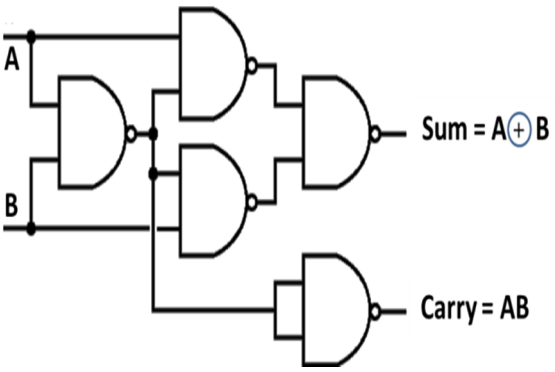


Fig 7.36

Truth Table for Half adder:

Truth Table			
Input A	**Input B**	**Carry**	**Sum**
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



Implementation of Half Adder using NAND gates

Fig 7.37

Boolean expressions for Half adder:

Sum = S = A $\bar{B}$ + $\bar{A}$ B = A exclusive-or B
Carry = C = A B

7.3 Full adder (FA)

Full adder adds three inputs, unlike half adder which handles only two inputs.

What are these three inputs?

1. Input A
2. Input B
3. Carry Output from a previous addition.

e.g. Add $(11)_2 + (01)_2$

Input 1		1	1
Input 2		0	1
Carry In from previous addition	1	1	
Sum		0	0
Carry Out	1		

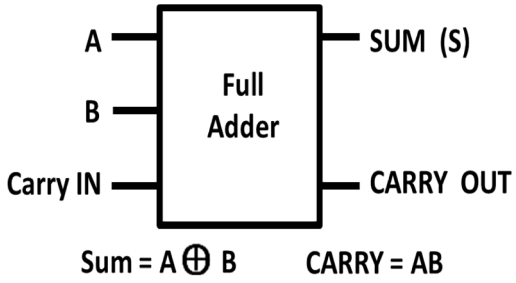


Fig 7.38

The addition is shown in the form of a table. Note that intermediate additions may result in "carry in" outputs which are added to the input bits in the next column. C_{out} is the final carry bit.

Truth Table for Full adder:

Truth Table				
Input A	**Input B**	**Carry In C_{in}**	**Carry Out C_{out}**	**Sum**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**1**
0	**1**	**0**	**0**	**1**
0	**1**	**1**	**1**	**0**
1	**0**	**0**	**0**	**1**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**1**	**1**

Boolean expressions for Full adder:

Carry Out $= \overline{A}\,B\,C + A\,\overline{B}\,C + A\,B\,\overline{C} + A\,B\,C$

$= \overline{A}\,B\,C + A\,\overline{B}\,C + A\,B\,\overline{C} + A\,B\,C + A\,B\,C + A\,B\,C$ (since A + A + A = A)

$= BC\,(\overline{A} + A) + AC\,(\overline{B} + B) + AB\,(\overline{C} + C)$

$= AB + BC + CA$

Sum $= \overline{A}\,\overline{B}\,C + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C} + A\,B\,C$

$= C\,(\overline{A}\,\overline{B} + A\,B) + \overline{C}\,(\overline{A}\,B + A\,\overline{B})$

$= C\,(\overline{A \oplus B}) + \overline{C}\,(A \oplus B)$

$= A \oplus B \oplus C$

7.3.1 Full adder implementation using two half adders

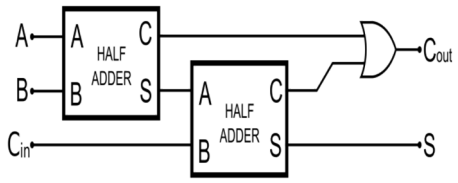


Fig 7.39 Block diagram of full adder using two half adders

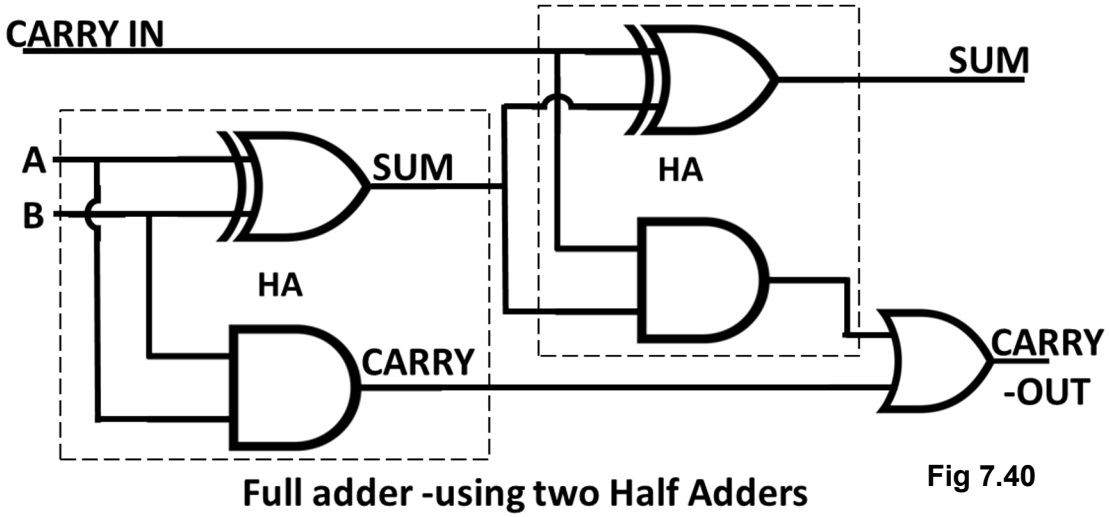


Fig 7.40

Chapter 8 Flip-Flops

Module – 4 Syllabus:
Flip-Flops (Text-2)**:** Introduction to Flip-Flops (Section 12.1), NAND Gate Latch/ NOR Gate Latch, RS Flip-Flop, Gated Flip-Flops:Clocked RS Flip-Flop (Sections 12.3 to 12.5).

Microcontrollers (Ref.1)**:** Introduction to Microcontrollers, 8051 Microcontroller Architecture and an example of Microcontroller based stepper motor control system (only Block Diagram approach).

8.1 Introduction to flip-flops

Explain a flip-flop.

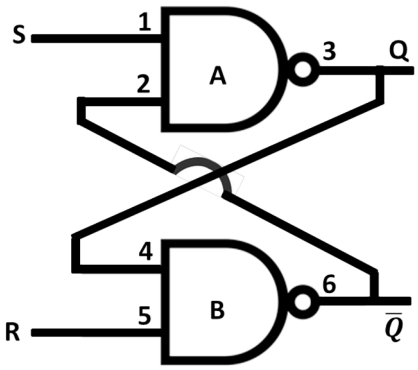
- Flip-flop, is the fundamental building block, in electronic circuits.
- There are two outputs in a flip-flop, called **Q and $\overline{Q}$**
- Q and $\overline{Q}$ will always remain, in **opposite states**.
- If **Q is in ONE, $\overline{Q}$ will be ZERO** and vice versa.
- Each of these two outputs, can remain in a **stable state** (Logic 1 or Logic 0).
- **The flip-flop can be made to change (toggle) from its present state, by applying a logic signal to one of its control inputs.**
- There are many such control inputs such as, **Clock, Set, Reset, J, K, S, R, T** and so on.
- For example, a Q output can change from 1 to 0 or 0 to 1, if a square wave is applied to its clock input. This is called **toggling**.
- It is a basic storage element in sequential (one after the other) circuits.
- The name flip-flop comes about due to the nature of the circuit. The outputs Q and $\overline{Q}$, flip and flop based on control inputs. When **Q flips, $\overline{Q}$ flops**.

Types of flip-flops

a. **D** flip-flop
b. **J-K** flip-flop
c. **Set-Reset** flip-flop
d. **T** flip-flop

Latches

- They can be used, as memory devices.
- They can store one bit of information (1 or 0) indefinitely, as long as the device is powered.
- The latch will change from its present state, if and only if, a logic signal is applied to, one of its control inputs.
- They **"latch on"** to information and hold it



SIMPLE NAND S-R LATCH

Fig 8.1

8.2 NAND gate SR latch (also called RS Latch)

Explain a simple latch operation using NAND gates. (SR latch)

The circuit diagram for a SR latch, using two NAND gates, is shown in fig 8.1

Latch in SET state:

a. Let S = 0 and R = 1
b. In gate A, when S = 0, **Q**= 1
c. In gate B, Pin 5 = 1 since R = 1 and Pin 4 =1 since **Q** = 1.
   Therefore, in gate B, both inputs are 1 and output (Pin 6) = 0.
   $\therefore \overline{Q} = 0$.

Therefore, in SET mode, $\therefore$Q = 1 and $\overline{Q} = 0$.

Latch in RESET state:

a. Let S = 1 and R = 0
b. In gate B, when R = 0, $\overline{Q}$ = 1
c. In gate A, Pin 1 = 1 since S = 1 and Pin 2 =1 since $\overline{Q}$ = 1.
   Therefore, in gate A, both inputs are one and output (Pin 3) = 0. **$\therefore$Q = 0.**

Therefore, in RESET mode, $\therefore$Q = 0 and $\overline{Q} = 1$.

The truth table of a simple SR latch using NAND gates is shown.

S	R	Q	$\overline{Q}$	Remarks
0	0	Meta state		Illegal
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q	$\overline{Q}$	No Change (Latched)

Latch in latched state

a) Happens when S = 1 and R = 1.

For a NAND gate, a logic one is a 'don't-care' condition.
Therefore, when S = 1 and R = 1, these two inputs, cannot influence the output.
Q will remain in its previous state and $\overline{Q}$ also, will remain in its previous state.
In other words, $Q_{n+1} = Q_n$ and $\overline{Q_{n+1}} = \overline{Q_n}$. No change happens in the latch outputs.
Latch remains in its previous sate (**latch remains latched**)

Metastable state

Metastability in electronics, is the ability of an electronic circuit, to persist in an unstable equilibrium, forever. (Remain confused forever!). In latches, this happens when **S = 0 and R = 0 (for NAND) and S = 1 and R = 1 (for NOR).**

In NAND latch, when S = 0 and R = 0, gate A output is being asked to make itself 1 as well as 0, by two contradictory commands, from S and R respectively.
Same confusion exists at Gate B output, as well.
This results in, what is known as a "race condition" in the latch.
If the gates are exactly identical, the war between Gate A and Gate B will go on indefinitely and the output states of **Q** and $\overline{Q}$ can never be predicted.

Designers, therefore ensure that such input conditions are never presented to the latch. **Therefore S = 0 and R = 0 (for NAND) and S = 1 and R = 1 (for NOR) are generally called illegal.**

8.3 NOR Gate RS latch (also called SR Latch)

Explain a simple latch operation using NOR gates.

Refer fig 8.2. Note **R and S inputs are inter-changed** in NOR latch

Set State: (S = 1 and R= 0)

1. In gate B, when S = 1, output = 0. $\therefore \overline{Q} = 0$
2. In gate A, both inputs are 0 (Since R = 0 and $\overline{Q}$ = 0).
3. Therefore, gate A output is 1. $\therefore$ **Q = 1.**

Therefore, in SET mode, $\therefore$Q = 1 and $\overline{Q}$ = 0.

Reset State: (S = 0 and R= 1)

1. In gate A, when R = 1, output = 0. $\therefore$**Q = 0**
2. In gate B, both inputs are 0 (Since S = 0 and Q = 0).
3. Therefore, gate B output is 1. $\therefore$ $\overline{Q}$ **= 1.**

Therefore, in RESET mode, $\therefore$Q = 0 and $\overline{Q}$ = 1.

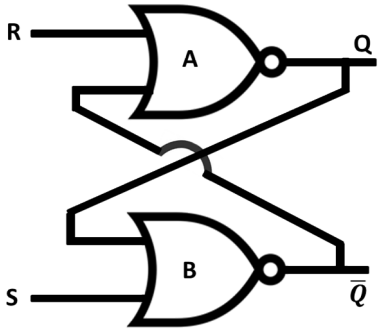


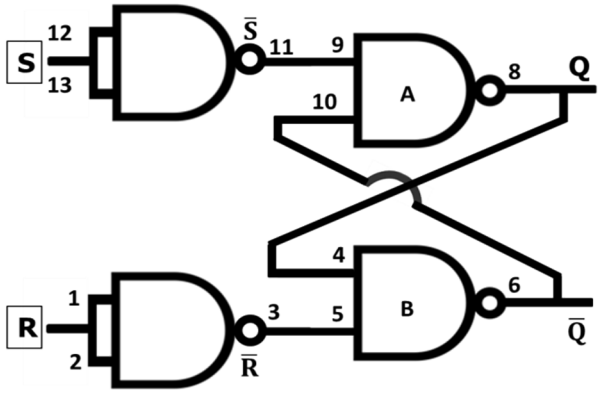
Fig 8.2 SIMPLE NOR S-R LATCH

Metastate: As seen earlier, this happens when S = 1 and R = 1 in NOR gate.

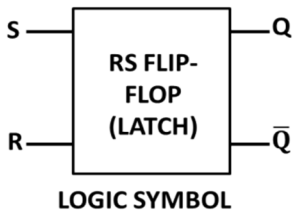
S	R	Q	$\overline{Q}$	Remarks
0	0	Latched		No Change
0	1	0	1	Reset
1	0	1	0	Set
1	1	Meta state		Illegal

8.4 A typical RS latch (NAND)

Explain a SR latch (also called RS latch) operation, using NAND gates. Refer fig 8.3



A TYPICAL NAND S-R LATCH



LOGIC SYMBOL

Fig 8.3

Latch in SET mode

a. Let S = 1 and R = 0
b. Since S = 1, $\overline{S}$ = 0 and Pin 9 of gate A = 0.
   $\therefore$ Pin 8 of gate A = 1. $\therefore$**Q = 1**

c. Since R = 0, $\overline{R}$ = 1, both inputs of gate B (Pins 4 and 5) are 1. Therefore Pin 6 of gate B = 0. **$\therefore \overline{Q}$ = 0.**

Therefore, in SET mode, $\therefore$Q = 1 and $\overline{Q}$ = 0.

Latch in RESET mode

a. Let S = 0 and R = 1
b. Since R = 1, $\overline{R}$ = 0 and Pin 5 of B =0.
   Pin 6 of gate B = 1. **$\therefore \overline{Q}$ = 1**
c. Since S = 0, $\overline{S}$ = 1, both inputs of gate A (Pins 9 and 10) are 1. Therefore Pin 8 of gate A = 0. **$\therefore$Q = 0.**

Therefore, in RESET mode, $\therefore$Q = 0 and $\overline{Q}$ = 1.

Latch in NO CHANGE mode

- Let S = 0 and R = 0
- Therefore, $\overline{S}$ = 1, $\overline{R}$ = 1
- A logic 1 input to a NAND gate is a 'don't-care' condition. Therefore the outputs will remain in their respective previous states. Next state will be the same as previous state. In other words, **$Q_{n+1} = Q_n$** and **$\overline{Q_{n+1}} = \overline{Q_n}$** .

Latch in Metastate condition

When S =1 and R = 1, $\overline{S}$ = 0 and $\overline{R}$ = 0
This condition will make both Q = 1 and $\overline{Q}$ = 1
Most of the circuits never use this condition. It is an illegal mode.

The logic symbol of SR latch is shown in fig 8.3.
The truth table of SR latch using NAND gates is shown.

S	R	Q	$\overline{Q}$	Remarks
0	0	Latched		No Change
0	1	0	1	Reset
1	0	1	0	Set
1	1	Meta state		Illegal

Note: This truth table has changed with respect to the simple latch discussed in the previous section. This is because of the extra gate (inverter) at the front end in this circuit.

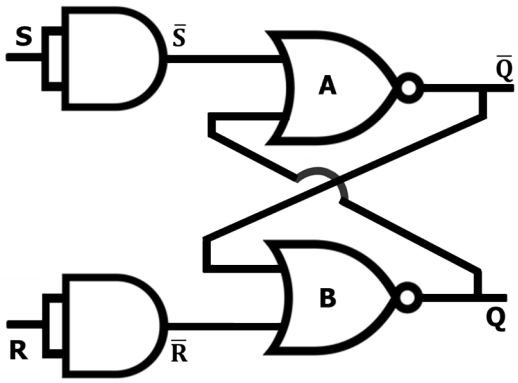


Fig 8.4 TYPICAL NOR S-R LATCH

8.5 A typical SR latch (NOR)

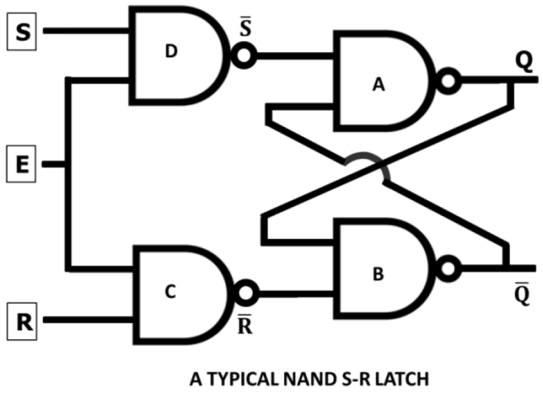
Explain a SR latch operation, using NOR gates.
Refer fig 8.4. In the NOR implementation note
a) Input gates are AND
b) Q and $\overline{Q}$ are interchanged.
Truth table changes for S =1 and R = 1

The truth table of SR latch using NOR gates is shown

S	R	Q	$\bar{Q}$	Remarks
0	0	Q	$\bar{Q}$	No Change
0	1	0	1	Reset
1	0	1	0	Set
1	1	**0**	**0**	Illegal

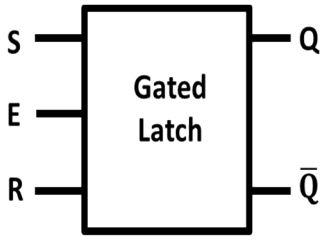
Gated SR latches

Refer fig 8.5.



A TYPICAL NAND S-R LATCH

Fig 8.5



Gated SR Flip-Flop / Latch - Logic Symbol

Fig 8.6

- The circuit is almost same, except that there is an enable input (E) added.
- When Enable = 1, the circuit explanation also is, exactly same, as in previous section.
- When Enable = 0, both $\bar{S}$ and $\bar{R}$ will be in 1. S input and R input become redundant ("don't-care").
- Therefore the outputs will remain in their respective previous states. Next state will be the same as previous state. In other words, $Q_{n+1} = Q_n$ and $\overline{Q_{n+1}} = \overline{Q_n}$

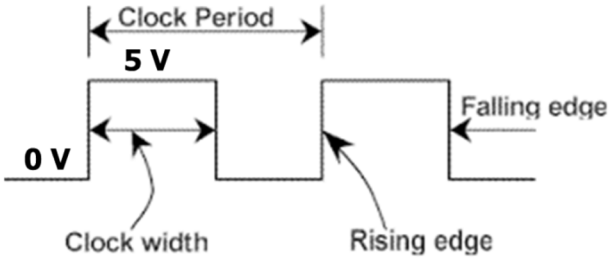
The logic symbol of a gated SR latch is shown in fig 8.6. The truth table of a gated SR latch is shown

Enable	S	R	$Q_n \rightarrow Q_{n+1}$	Remarks
1	0	0	0 → 0 1 → 1	No change
1	0	1	0 → 0 1 → 0	Reset
1	1	0	0 → 1 1 → 1	Set
1	1	1	0 → 1 1 → 1	Metastable (Illegal)
0	X	X	0 → 0 1 → 1	No change

Clock pulses:

What is a clock?

Refer fig 8.7.It is a square wave with logic levels. A TTL (transistor-transistor-logic) clock is shown (0 to 5 V).



A clock will have a rising edge (+ve edge) and a falling edge (-ve edge).

A flip-flop will use only one type of edge and ignore the other edge.

Some flip-flops are +ve edge triggered and some flip-flops are -ve edge triggered

Fig 8.7

Difference between a Latch and a Flip-flop.

Very often latches and flip-flops are used interchangeably, by mistake. There are definite differences in their operating modes as follows.

Latches	Flip-Flops
Based on the enable input function	Based on the clock input function
Level sensitive. Respond to ONE or ZERO levels. (Specific voltage levels)	Edge sensitive. Respond to +ve edge or –ve edge of a clock input.
Sensitive to the entire duration of the input.	Sensitive during only the transition edges. (rising edge or falling edge)
Can transfer data, during the entire duration of the input.	Can transfer data, only at a single instant during clock transitions. Data cannot change till the next clock transition happens.

8.6 CLOCKED RS FLIP-FLOP (NAND)

Explain a clocked RS flip-flop using NAND gates

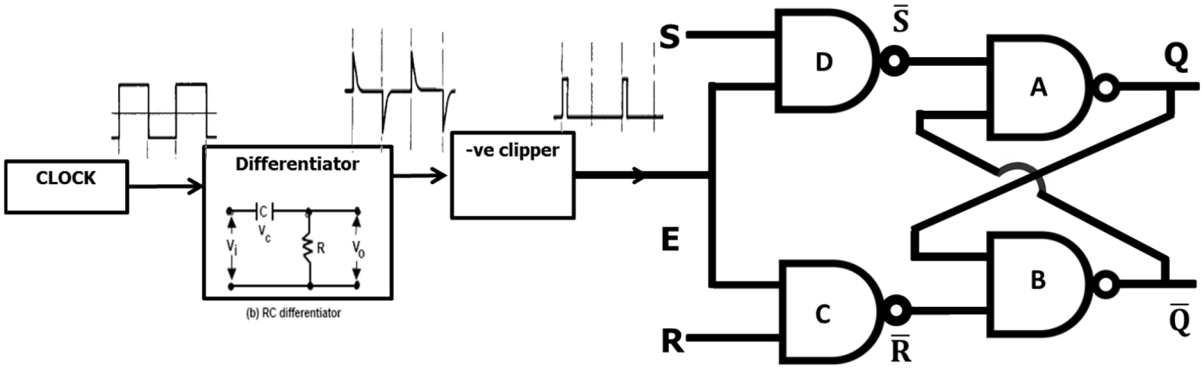
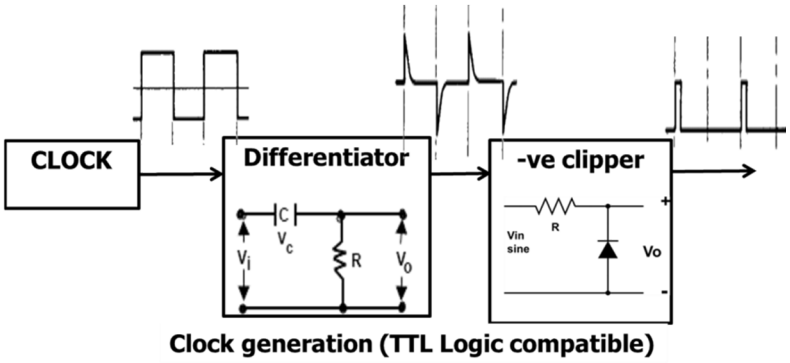


Fig 8.8

Refer fig Fig 8.8. This is a clocked RS flip-flop. The enable signal in the previous section, is replaced by a positive pulse stream.

Differentiator and – ve clippers

Refer diagram 8.9. The differentiator produces spikes, every time the clock goes through a transition. The differentiator produces a positive spike during the rising edge of the input clock and



the differentiator produces a negative spike during the falling edge of the input clock. The negative clipper, clips all –ve spikes and only +ve spikes appear, at the output.

Fig 8.9

Clocked SR flip-flop

Clock	S	R	$Q_n \rightarrow Q_{n+1}$	Remarks
↑	0	0	0 → 0 1 → 1	No change
↑	0	1	0 → 0 1 → 0	Reset
↑	1	0	0 → 1 1 → 1	Set
↑	1	1	0 → 1 1 → 1	Metastable (Illegal)
0	X	X	0 → 0 1 → 1	No change

When the clock pulse is +ve the flip flop is enabled. The set input or the reset input can propagate through and can perform a flip-flop operation.

When the clock is absent, the clock input remains at zero. The Set and Reset inputs are inhibited.

Therefore, the circuit responds to S or R, only when clock pulses are present.
The flip-flop action (operation) is same as that of SR latch with Enable input, in fig 8.5

8.7 CLOCKED RS FLIP-FLOP (NOR)

Explain a clocked SR flip-flop using NOR gates

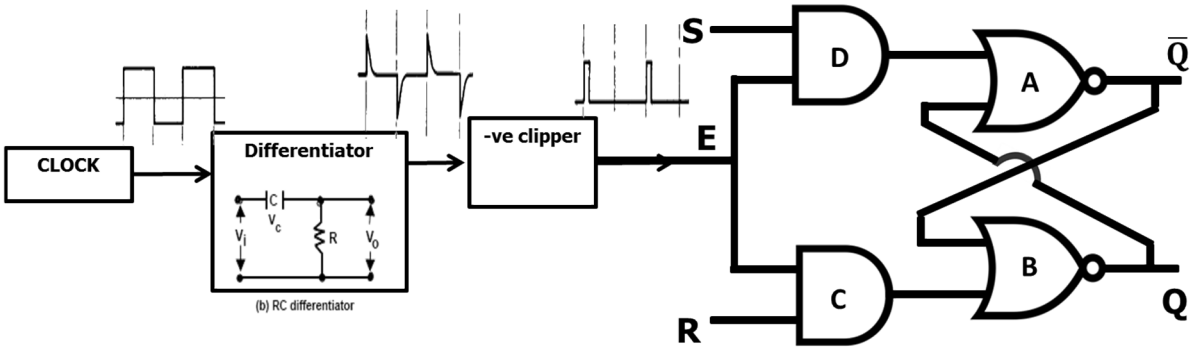
Refer fig 8.10. Circuit explanation is similar to previous section, using NAND gates.

In the NOR implementation note

a) Input gates are AND

b) Q and $\overline{Q}$ are interchanged.

Truth table changes for S =1 and R = 1. Both Q and $\overline{Q}$ go to 0



A TYPICAL NOR S-R LATCH

Fig 8.10

Clock	S	R	$Q_n \rightarrow Q_{n+1}$	Remarks
↑	0	0	0 → 0 1 → 1	No change
↑	0	1	0 → 0 1 → 0	Reset
↑	1	0	0 → 1 1 → 1	Set
↑	1	1	0 → 0 1 → 0	Metastable (Illegal)
0	X	X	0 → 0 1 → 1	No change

Chapter 9: 8085 Microprocessor and 8051 Microcontroller

What is a microprocessor?

- A microprocessor is basically, a processor.
- It is a **Central Processing Unit (CPU**), on a single chip.
- A µP has a **program written into it**, by the user.
- Program contains a **series of instructions**, on the various operations **to be performed sequentially (one by one).**
- Programs are stored in the **memory.**
- Based on the program, the **digital data input is processed**, to provide results as output.
- It has a **few registers to assist** the µP, to perform different kinds of operations.
- Each µP has a fixed set of instructions coded in binary.
    - µP **accepts binary data**.
    - µP circuit **reads binary instructions** from memory.
    - **Translates** (decodes) the instructions.
    - **Processes** data as per instructions.
    - **Executes** what is decoded.
    - **Provides** results as output.

Features of 8085

- **8 bit machine.**
- **Single chip. NMOS.**
- **40 pin IC. 6200 transistors.**
- **Single supply, 5V.**
- **Crystal clock – 3 MHz to 5 MHz.**
- **Address bus : 16 bit address. A0 to A15.**
- **A0 to A7** :
    - Will handle address bits (Lower **A0 to A7 bits**), to access memory
    - Will **also handle data** at times
    - Since it handles address and data it is a **multiplexed bus**.
- **A8 to A15**:
    - Will **handle only address**, to access memory

What is a Program?

Look at this example. A musical instrument can produce only notes. Only a good musician can **create music thro proper programming** (through a musical sheet)

Microprocessor – Basic structure

A µP has three major blocks

1. ALU
2. Registers
    a. Accumulator
    b. Instruction register
    c. General Purpose Registers
    d. Program counter
    e. Status register
3. Control Unit

Bus: Refer fig 9.1. Contains three types of BUS.

1) **Data Bus 2) Address Bus 3) Control bus**

Communication between memory, I/O devices, Registers etc happen thro common communication paths called BUS.

In µP, **the bus handles 8 bits (data or address**) in a **parallel mode**.

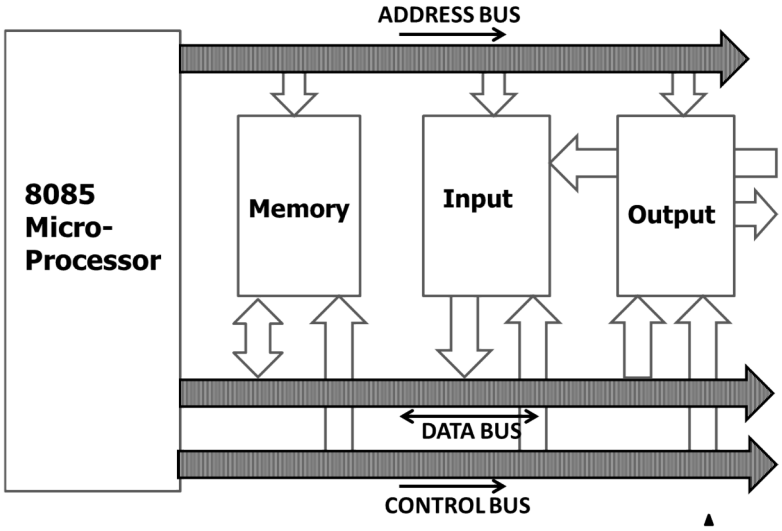


Fig 9.1 Microprocessor BUS structure

Memory: Stores binary instructions and data..

Provides the **required information to µP,** on demand.

Stores **results** sent by µP

ROM - (Read Only Memory):

- Stores programs **permanently.**
- **Cannot be erased** easily
- **Can only be read** from.
- **Cannot be over-written** into.
- Even after power is switched off, the **ROM retains its content**

RAM – Random Access Memory:

- Stores Data, which is **not permanent** in nature.
- Information in RAM **can be erased, by overwriting** into it.
- After power is switched off, the **RAM loses its content**.

8085 Architecture Refer fig 9.2

1. ALU (Arithmetic Logic Unit)

Performs Arithmetic and Logic operations.

Arithmetic **:** +, - etc

Logic **:** AND, OR, Ex-OR, Complement, Shift Right, Shift left.

2. Registers

- 8 bit **accumulator.**
- **Flag register** (Status Register).

- 6 general purpose registers (**B, C, D, E, H, L**).
- Gen purpose registers can be combined for **16 bit operation (B,C), (D,E), (H,L).**
- Two 16 bit registers (**Program counter and Stack Pointer**).
- Temp **w & Z** registers (not for users).
- **Data exchange is faster with general purpose registers than with memory.**
- Good programmers will use general purpose registers maximum.

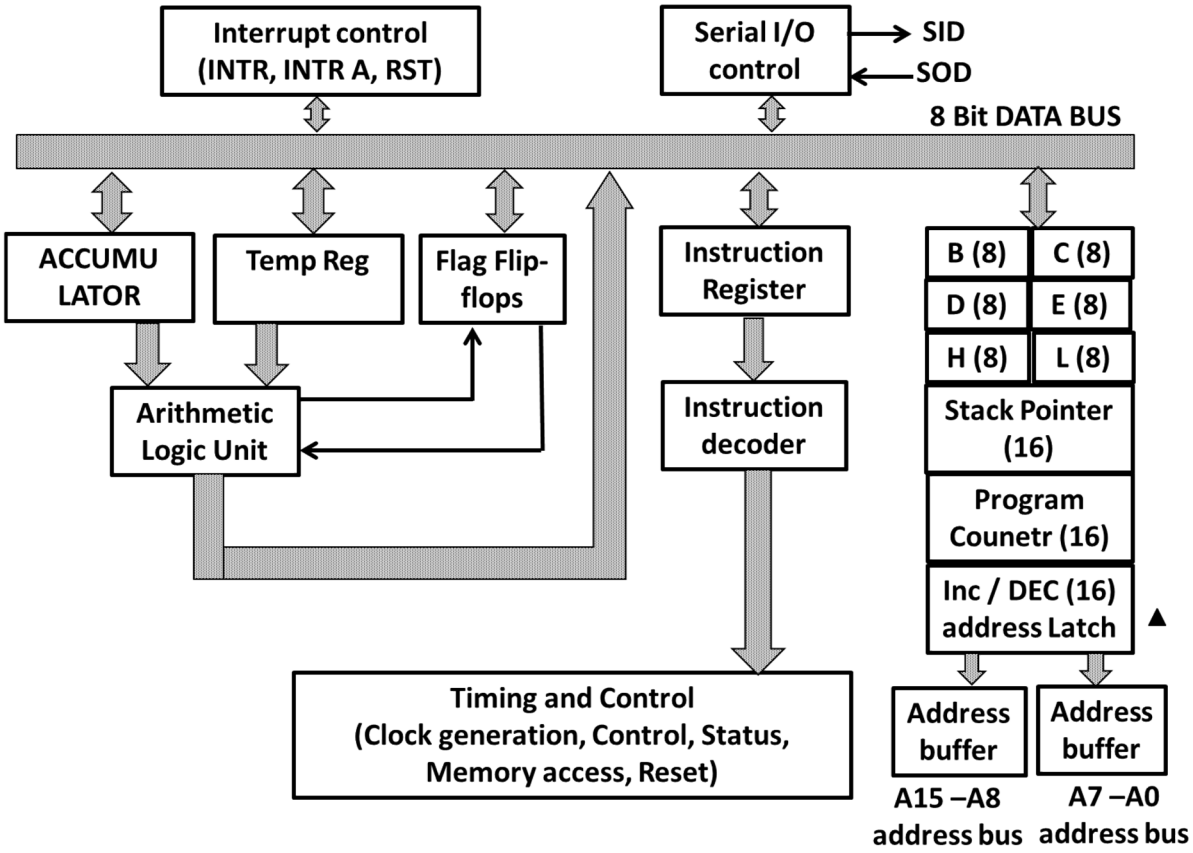


Fig 9.2 8085 Microprocessor architecture

a) <u>A register – Accumulator (8 bit):</u>

- **The Accumulator, an 8 bit register**, is the most **versatile** register. As its name implies, it is used to accumulate the results of a large number of instructions.
- Used for Arithmetic / Logic operations (**Add, Subtract, Multiply and Divide**).
- Contains **one operand.** The other operand is parked in a **temporary register.**
- Provides **data to ALU**.
- Result from ALU is sent back to A, to replace the original data.

c) <u>General Purpose register (8 bit):</u>

- µP has several registers such as **B, C, D, E, H, L** which can be **judiciously used** to execute complex programs.

Special purpose registers

e) Status register (8bit)

- Also known as **flag register**.
- Part of ALU.
- Has 5 flip-flops which are set or reset based on an operation by the accumulator.
- **The flags are Zero (Z) Carry (CY), Sign (S), Parity (P), and Auxiliary (AC).**

Instruction register

- **Program contains a series of instructions**.
- Each instruction is read **from memory**.
- It is **loaded into instruction register**.
- It is then **sent to instruction decoder**.
- Instruction decoder decodes the instruction.
- **CPU selects one of the 256 alternatives** at its disposal, to set up the appropriate action plan. Decoded signal is **sent to CPU** for further action.

Program counter (16 bit).

- PC is a **2-byte address** which informs the µP, as to **where the next instruction, to be executed, will be found in memory.**
- When the µP is initialized, PC will always start at 0000h. PC will be incremented (maybe 1, 2 or 3 bytes) each time, after an instruction is executed.
- The value of PC **can never be altered**, through any instruction.
- **PC increments automatically,** after every instruction.

Stack and Stack pointer (8 bit):

Refer fig 9.3.

- Stacks are typically used for **temporary storage of data**.
- Analogous to a stack of papers or a stack of cards.
- When you **push a value** onto the stack, the 8051 first **increments the value of SP** and **then stores the value** at the stack pointer memory location.
- The Stack Pointer is used to indicate where **the next value to be 'removed from' or 'stored into' the stack**, should be taken from.

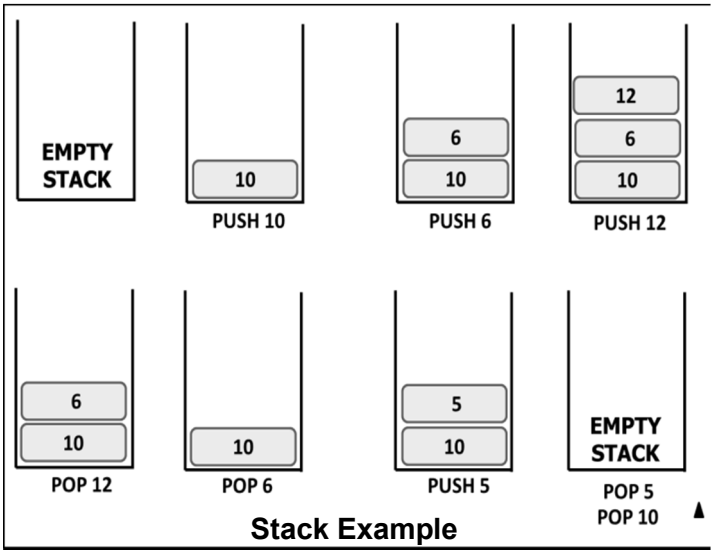


Fig 9.3 Stack Operation and Data flow

SP is modified directly by the 8051 by six instructions: **PUSH, POP, ACALL, LCALL, RET, and RETI**

Some rules:

- **Push :** Place cards on the top of the stack
- **Pop :** Remove cards from the top of the stack

- **LIFO : ** Last In is the First Out

3) Control Unit (8 bit).

- Responsible for **all functions of µP**.
- Maintains **Synchronization** of all parts of µP
- **Receives inputs** from Instruction decoder
- **Generates all control signals** needed, to carry out the particular task contained in that instruction
- In essence, CPU **opens (enables)** some parts of µP and **closes (disables)** some other parts of µP to execute that task.

What is an Interrupt?

- Interrupt is a process, where an **external device can get the attention of the microprocessor**.
- An interrupt is considered to be **an emergency signal that may be serviced.**
- When the Microprocessor receives an interrupt signal, it **suspends the current program** currently being executed and jumps **to an Interrupt Service Routine**.
- **5 HW Interrupts**.
- **TRAP, RST 7.5, RST 6.5, RST 5.5, INTR.**
- Can handle serial Input / Output (I/O) communication.

Serial I/O control

- 2 Lines SOD and SID
- **SOD :** Serial output data
- **SID : ** Serial Input Data

Instruction execution and Data flow in 8085.

Refer fig 9.4

What is an Opcode?

- µP converts the **instruction into suitable machine language**, so that the **CPU can understand the operation,** to be performed and execute it.
- Opcode is **the machine language instruction** which conveys to the µP, about **what operation should be performed** on the specific data.

Consider MVI A, 18H. (Move into the accumulator a specific value 18 in Hex)

1. µP **gets the opcode** for MVI A (The first byte of the instruction).
2. Opcode for MVI A is 3EH.
3. µP first **reads this opcode** (3EH), from the instruction.
4. Let us assume that the above instruction is stored in a specific address (Memory location) say 5500H and the data 18H is stored at the next location 5501H. In other words, 5500H contains 3EH and 5501 contains 18H.
5. **µP sends the address 5500H, in the address bus**, to the memory. (asks the memory location 5500H to send its contents)
6. **Memory 5500H places the opcode** byte (3EH), on the data bus.
7. µP knows that the first byte that has just been received (3EH) is always **an opcode (and not data).**
8. **µP** sends the **opcode to the instruction decoder**.

9. **Instruction decoder** decodes the opcode (3EH) and **identifies it as MVI A** instruction.
10. As soon as this information is obtained, **µP starts looking for the data** on which this operation should be performed
11. The **program counter is increased by 1**. So the **address bus** moves from 5500H to 5501H.
12. **µP also knows that the second byte to be received is a data byte and not an opcode.**
13. **µP then sends the address 5501H** (in PC), in the **data bus.**
    .
14. **Memory 5501H places the data** byte (18H), on to the **data bus**.

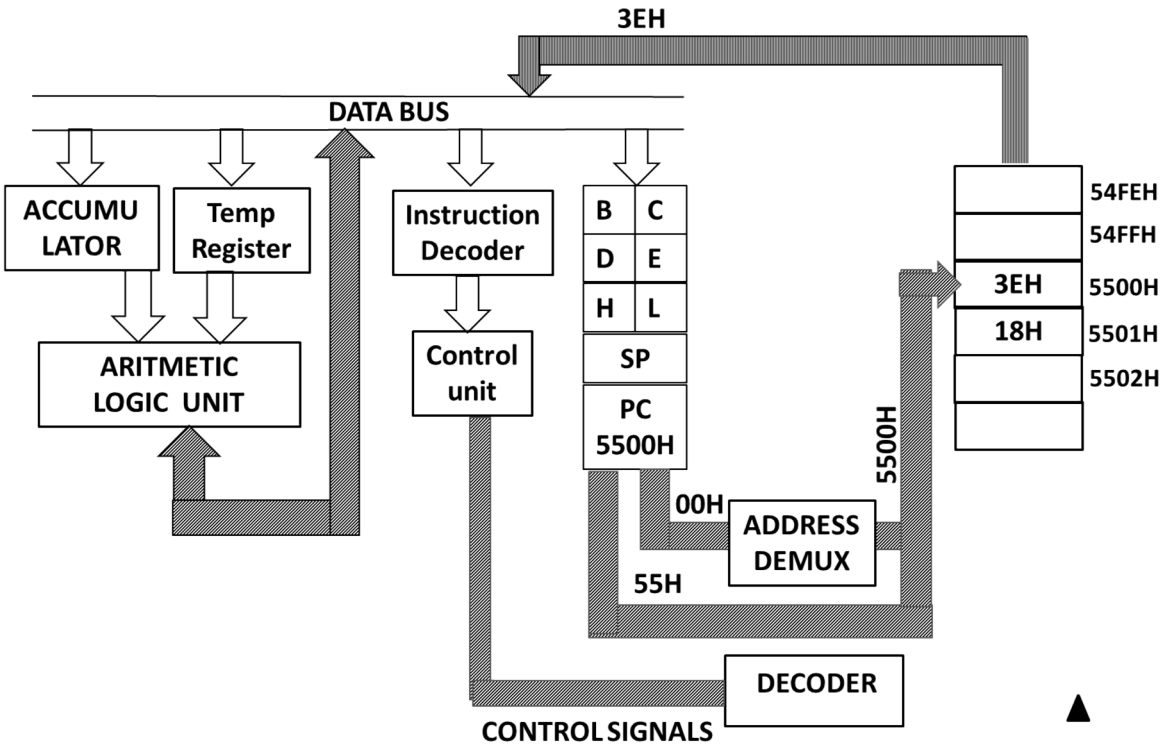


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Fig 9.4 Instruction execution and Data flow in 8085

15. µP knows this 18H is **not an opcode**.
16. The data 18H, is **moved to the accumulator**.
17. Thus the MVI A **operation is performed on the data** 18H and the **result is sent to accumulator.**

Compare a Microprocessor and a Microcontroller

The terms microprocessor and microcontroller have always been confused with each other. Both are meant for, real time applications.
Both have a lot of common features and lot of differences.

Microprocessors (µP)	Microcontrollers (Micon)
Microprocessor cannot be used as a stand-alone device.	Micons are invariably, stand- alone, mini computers
µP is an IC which has only a CPU, ALU and a few registers. It has only processing capability.	Micon is an IC which has a CPU, and also an in-built RAM, ROM. It has good computing capability.
They need external RAM, ROM, buffer, I/O ports. Therefore a system designed around µP is quite costly.	Micon has its own RAM, ROM, Peripherals, I/O ports etc. This in turn, reduces the size and the cost.
Microprocessor finds applications where tasks are unspecific. The relationship between input and output is not defined.	Microcontrollers are designed to perform specific tasks. The relationship of input and output is clearly defined
Examples: Games software, websites, Photo editing, creation of documents …….	Example: Keyboards, washing machine, digital cameras, pen drive, microwave, automobiles, toys, mobiles etc.
Clock speed: Very high. (1GHz and above)	Clock speed: Very low.(1 MHz to 50 MHz)
Instructions will have one or two bytes	Instructions will have many bytes
Slow devices. Access time is more	Fast devices. Access time is less.
Flexible design	Single objective design. Rigid.

8051 Microcontrollers

Introduction to micro-controllers

A micro-controller is a compact IC which can be called, a **mini stand-alone computer**.

- ⊗ It is versatile, **capable of executing, pre-programmed tasks**.
- ⊗ It can also **interact with other hardware devices**.
- ⊗ We can find a microcontroller **in every machine these days**, right from toys, washing machines, small telephone exchanges and so on.

What are the salient features of 8051?

- ⊗ **4K bytes** of on chip Read Only Memory **(ROM),** for storing program
- ⊗ **64KB** of, **external ROM** (Program)
- ⊗ **128 Bytes** On-Chip Random Access Memory **(RAM),** for storing data
- ⊗ **64 KB of external RAM** (Data)
- ⊗ **4 register banks**
- ⊗ **128 flags**
- ⊗ **4 Ports (8 bits) – Parallel (I/P and O/P)**
- ⊗ **High speed serial port**
- ⊗ Binary and Decimal arithmetic
- ⊗ **5 Interrupts**

Explain 8051 Architecture

Refer fig 9.5. The block diagram of 8051 Micro-Controller is given. It consists of.

- ⊗ A Processor (**CPU**),
- ⊗ Two types of memory (**ROM for Program and RAM for Data**),
- ⊗ **4** input,/,output (**I/O**) ports,
- ⊗ **128 Special function registers** (80h through FFh),
- ⊗ **Serial port**,
- ⊗ Interrupts (**5 vectored interrupts**).

CPU:

- ⊗ Arithmetic Logic Unit - **ALU** (8 bit),
- ⊗ Registers **A,B, PSW, SP, PC, DPTR,**
- ⊗ Special function registers **(SFRs)**.

A - Accumulator (8 bit):

The **Accumulator, an 8 bit register**, is the most versatile register.

As its name implies, it is used to accumulate the results of, a large number of instructions.

- ⊗ Receives results of all Arithmetic operations of **ALU** (Arithmetic Logic Unit), such as Add, Subtract, Multiply and Divide.
- ⊗ **Special functions : Rotate, Parity computation, Testing for zero etc**

Register- B (8 bit):

Very similar to the Accumulator.

- ⊗ Used mainly for hardware **multiplication and Division.**
- ⊗ The "B" register responds to, only two 8051 instructions: **MUL AB and DIV AB**.

⊗ For executing multiplication or division of two numbers, Accumulator stores one number in A and another number in "B".

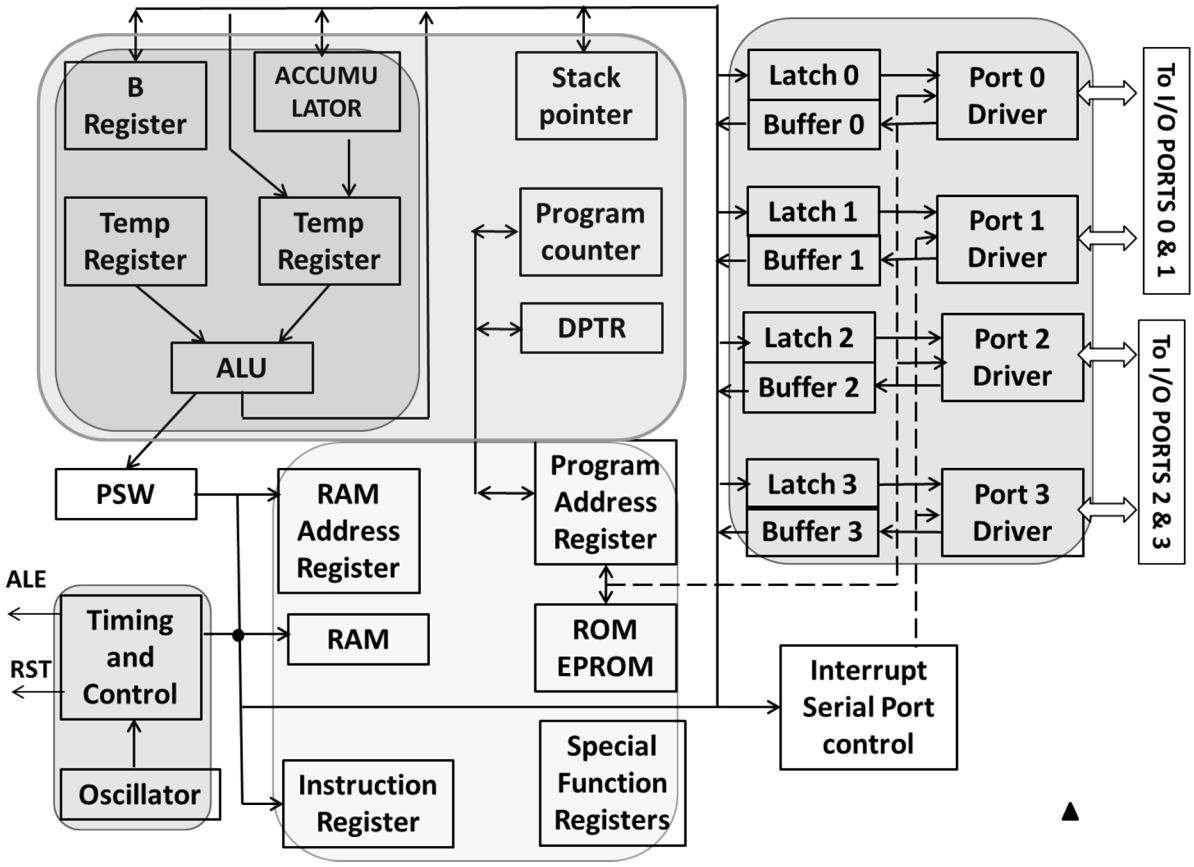


Fig 9.5 8051 Micro-Controller Block diagram

DPTR (Data Pointer)

⊗ It is a **16 bit (2 byte) register.**

⊗ DPTR, as the name suggests**, is used to point to, where the data is stored**, **in the external memory**.

⊗ DPTR is a 2 byte register whereas, Accumulator, "R" registers, and "B" register are all 1-byte values.

PC (Program Counter)

⊗ PC is a **2-byte address**, which informs 8051, as to **where the next instruction, to be executed, will be found** in memory.

⊗ When the 8051 is initialized, PC will always start at 0000h. PC will be incremented (maybe 1, 2 or 3 bytes) each time, after an instruction is executed.

⊗ PC **increments automatically,** after every instruction

⊗ The value of PC can never be altered, through any instruction.

8051 Flag bits and PSW register

PSW: Processor Status Word (Program status word):
Refer fig 9.6.

PSW is a special purpose register. It contains an 8 bit word which carries information on the status of the CPU.
It contains indicators or flags to use conditional statements in the program, to make decisions. The details are shown in the Table below

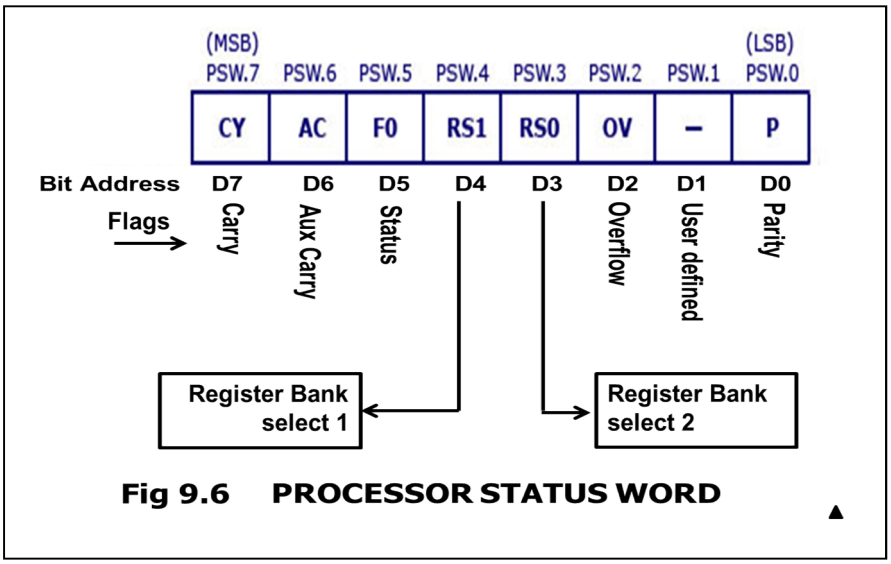


Fig 9.6 PROCESSOR STATUS WORD

Bit No	Bit Symbol	Direct Address	Name	Function
0	P	D0	Parity	This bit will be set, if ACC has odd number of 1's after an operation. If not, bit will remain cleared.
1	-	D1		User definable bit
2	0 V	D2	Overflow	0 V flag is set, if there is a carry from bit 6 (but not from bit 7), of an Arithmetic operation.
3	RS0	D3	Register Bank select bit 0	LSB of the register bank select bit.. Registers are grouped into 4 groups (banks)
4	RS1	D4	Register Bank select bit 1	MSB of the register bank select bits. RST 00- Bank 1; RST 01- Bank2 and so on
5	F0	D5	Flag 0	User defined flag
6	AC	D6	Auxiliary carry	This bit is set, if during an Arithmetic operation, data is overflowing, from bit 3 to bit 4 of Accumulator.
7	CY	D7	Carry	Is set, if during an Arithmetic operation, data is overflowing, out of bit 7 of Accumulator.

Fig 9.7 Program Status Word

Memories:

Refer figure 9.8 on RAM structure.

⊗ 8051 has **128 bytes of RAM space,** for SFRs. The address span for the RAM is, **00h to 7Fh**.

⊗ In addition, there are **128 bytes for Special function registers (80 h to FFh)** (see diagram 9.8)

⊗ There are four functional areas,

First 128 bytes:

- ⊗ **00h to 1Fh:** Register Banks 0 to 4 (Can be manipulated as 8 bit registers, **byte by byte**)
- ⊗ **20h to 2Fh:** Bit Addressable RAM (Can be manipulated **bit by bit**)
- ⊗ **30 to 7Fh:** General Purpose RAM

Next 128 bytes:

- ⊗ **80h to FFh:** Special Function Registers

RAM address	Purpose								Details
0	R0	R1	R2	R3	R4	R5	R6	R7	Register Bank 0
8	R0	R1	R2	R3	R4	R5	R6	R7	Register Bank 1
10	R0	R1	R2	R3	R4	R5	R6	R7	Register Bank 2
18	R0	R1	R2	R3	R4	R5	R6	R7	Register Bank 3
20	0	8	10	18	20	28	30	38	Bit addressable 00h to 3Fh (64 bits)
28	40	48	50	58	60	68	70	7F	Bit addressable 40h to 7Fh (64 bits)
30	General Purpose RAM space								User RAM for genearl usage and stack space. 30h to 7Fh (Total 80 bytes)
7F									
80	SFRs								Special Function registers 80h to 7Fh (total 128 bytes)
FF									

Fig 9.8 RAM structure

Special Function registers- SFR (128 bytes)

- ⊗ Special function registers occupy the upper part of RAM (80 h to FFh). 128 bytes.
- ⊗ Handles all **4 I/O (input / output) ports**.
- ⊗ Handles **Timer control, Interrupt control, Serial Communications, and CPU registers**
- ⊗ **21 such registers** are available

Input / Output ports

- ⊗ Used for interfacing with external devices such as **printers, memories** etc
- ⊗ There are 4 I/O ports each 8 bits wide. (**PO and P2 for external memory, P1 and P3 for I/O**)

ROM:

Refer figure on ROM structure.

On-Chip Memory : **4K bytes internal ROM** is available in 8051 (0000 H to 0FFF H).

External **: 60K Bytes external** memory is possible (1000 H to FFFF H).

This is often in the form of, an external EPROM.

Stack and Stack pointer (8 bit):

Refer fig 9.9.

- ⊗ Stacks are typically used for, **temporary storage of data**
- ⊗ Analogous to a stack of papers or a stack of cards
- ⊗ When you push a value onto the stack, the 8051 first increments the value of SP and then stores the value, at the stack pointer memory location.

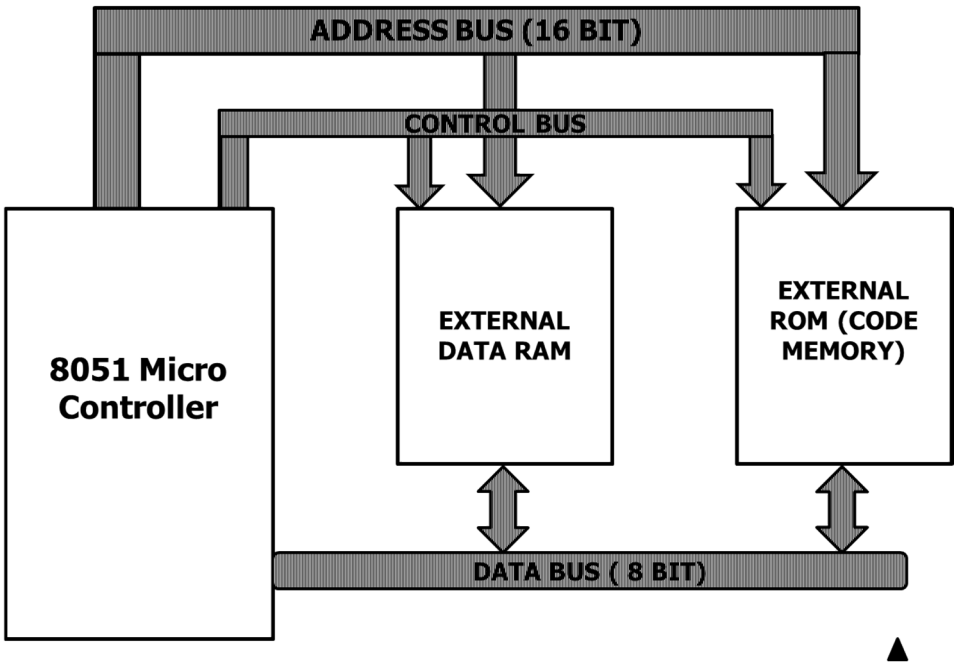


Fig 9.9 ROM structure

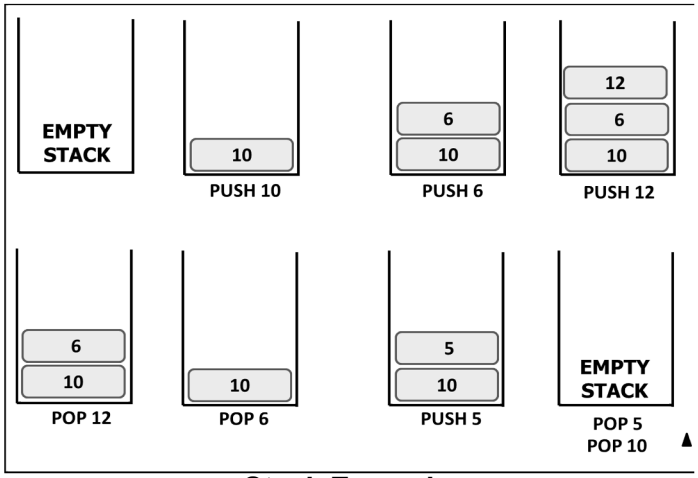
- ⊗ The Stack Pointer is used to indicate, **where the next value to be 'removed from' or 'stored into' the stack,** should be taken from.
- ⊗ SP is modified directly by the 8051 by six instructions: **PUSH, POP, ACALL, LCALL, RET, and RETI**

Some rules:

Push: Place cards, on the top of the stack

Pop: Remove cards, from the top of the stack

LIFO: Last In is the First Out



Stack Example

Fig 9.10 Stack Operation and Data flow

An example of microcontroller based stepper motor control system (only Block Diagram approach).

What is a Stepper Motor?

We know that DC motors run continuously in a smooth fashion, when power is applied. The DC power input is continuous and the consequent rotation also is continuous.

On the other hand a stepper motor runs only in discrete steps. Current pulses (on/off) are applied to the motor, and the motor shaft rotates in a discrete fashion (start/stop). Unlike DC motor, it has no brushes. Stepper motor is a digital motor.

Each input current pulse rotates the rotor by specified degrees (18degrees or 36 degrees, for example). These pulses are called "steps" and hence the name "stepper motor". Each rotation (360degrees) is divided into a number of steps. The number of pulses applied to the input can move and hold the rotor at a proportionate number of steps.
Broadly there are two types of stepper motors, namely Permanent-magnet (PM) stepper motor and Variable-reluctance (VR) stepper motor

Brief principle of operation

- A stepper motor consists of stators, a rotor with a shaft, and coil windings.
- The stators remains stationary
- The rotor is a central shaft within the motor which rotates (spins) during use.
- Refer Figure 9.11(a) and 1(b).

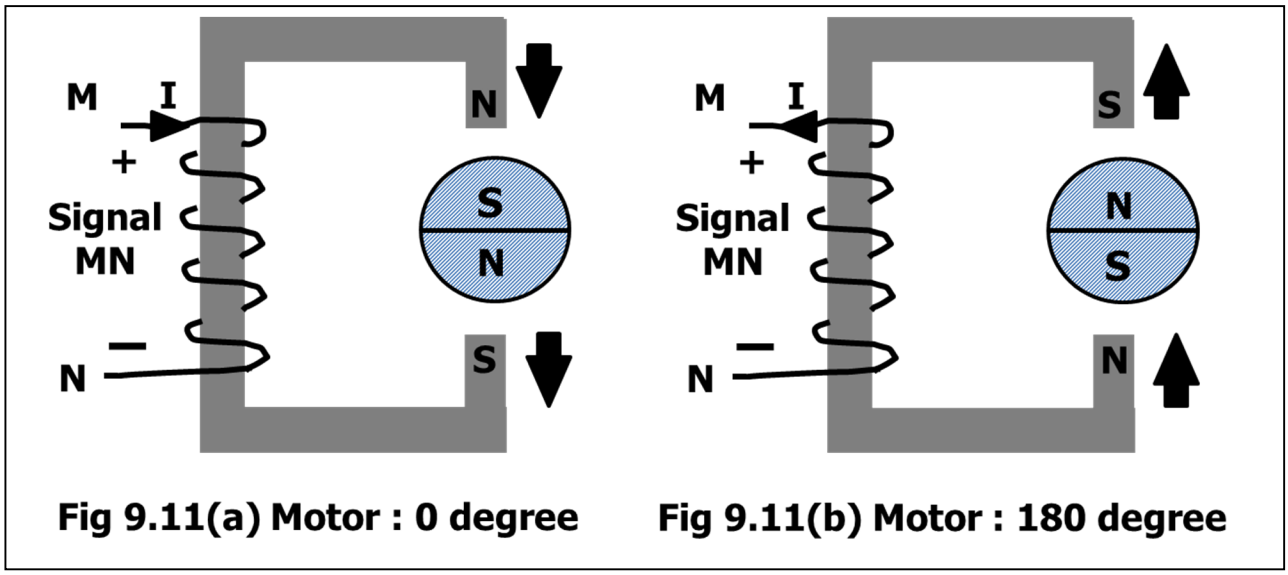


Fig 9.11(a) Motor : 0 degree **Fig 9.11(b) Motor : 180 degree**

- The rotor is actually a permanent-magnet. It is in the shape of a disk attached to a rotor shaft. It is a magnetic disk consisting of north and south magnetic poles interlaced together as shown.
- The number of poles can be many but in our example let us discuss a rotor with just two poles on the disk.

- The stator usually has a minimum of two or more coil windings. In fig 9.11, a stator with a coil winding is shown. When electrical current flows from top to bottom, through the coil as shown, a magnetic field is generated within the coil.

- A magnetic field is created due to this current flow such that a north pole is at the top and a south pole at the bottom. This is shown in figure (N at the top and S at the bottom).

- We know opposite poles attract and like poles repel. Therefore, the rotor which is permanent magnet will undergo attraction/repulsion.

In the present example

- The south pole of the rotor disc will get attracted to the north pole of the stator on top and
- The north pole of the rotor disc will get attracted to the south pole of the stator in the bottom.

If we now reverse the current in the coil, the stator exhibits an S at the top and N at the bottom.

Now the rotor undergoes different forces.

- The south pole of the rotor disc will get attracted to the north pole of the stator at the bottom.
- The north pole of the rotor disc will get attracted to the south pole of the stator at the top.

The rotor has moved 180 degrees due to the current phase reversal in the stator.

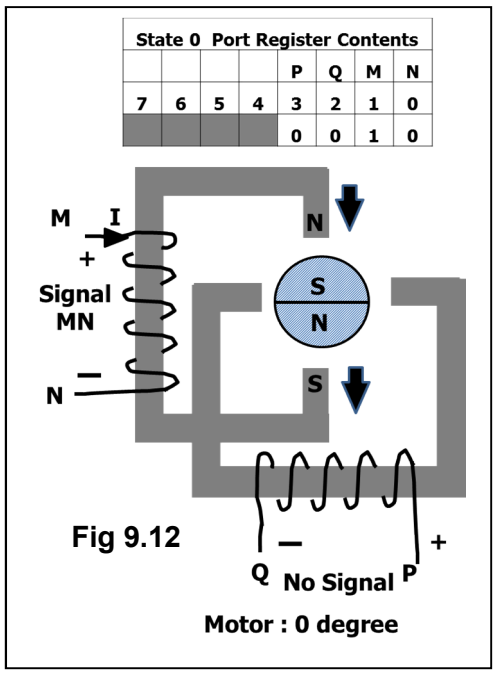


Fig 9.12

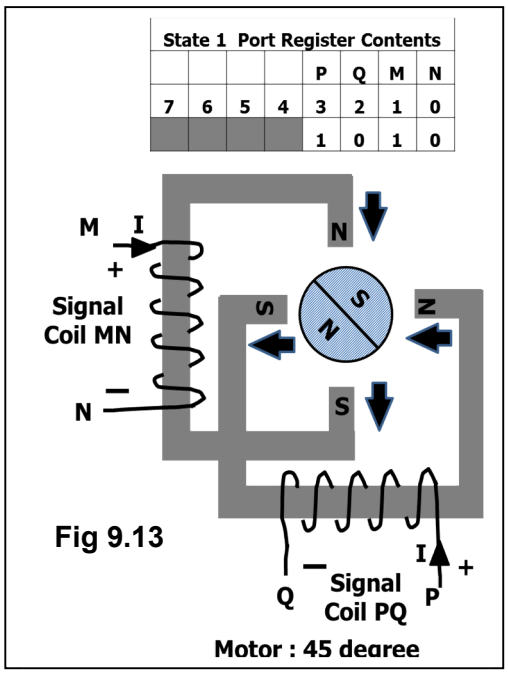


Fig 9.13

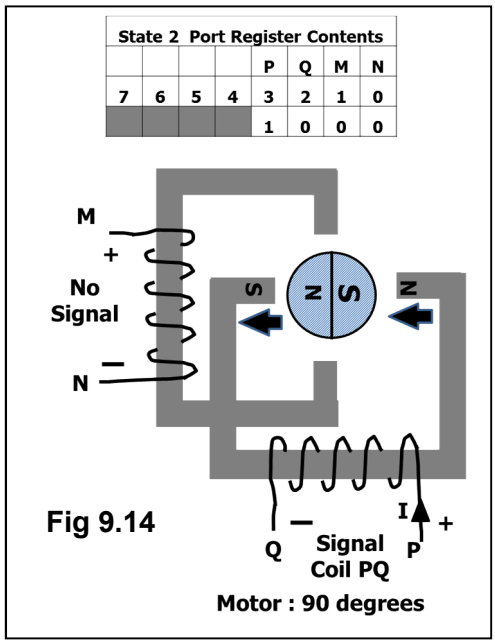


Fig 9.14

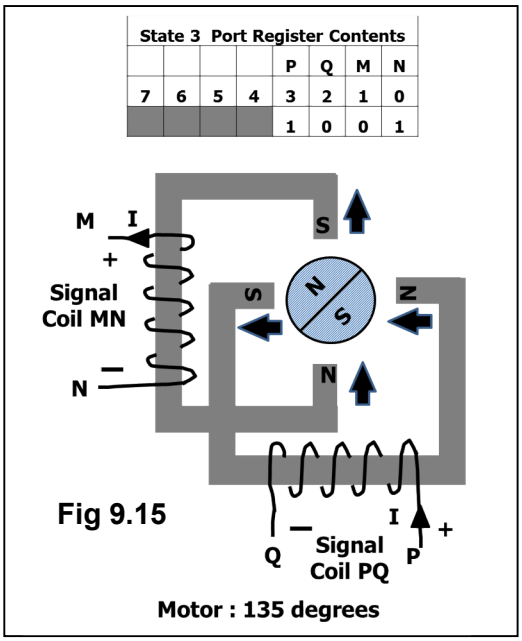


Fig 9.15

The practical stepper motors work with at least 2 coils perpendicular to each other as shown in figures 9.12, 9.13, 9.14 and 9.15.

The diagrams are self-explanatory. This stepper motor moves in 45 degrees step.

Pls note if the rotor disc sees two north poles of the stator at 90 degrees to each other, the rotor's South pole will settle exactly halfway through (at 45 degrees).

Step angle:

- Step angle is defined as the minimum degree of rotation with a single step.
- No of steps per revolution = 360° /step angle
- Example: step angle = 2°
- No of steps per revolution = 180
- Steps per second = (rpm x steps per revolution) /60

Switching Sequence of Motor:

Refer Table below

Rotation (in degrees)	P	Q	M	N
0	0	0	1	0
45	1	0	1	0
90	1	0	0	0
135	1	0	0	1
180	0	0	0	1
225	0	1	0	1
270	0	1	0	0
315	0	1	1	0
360	0	0	1	0

- From the discussion, it is evident that the stator coils need to be energized in sequence, for the rotation. This can be done by sending appropriate “bits sequence” to the stator coils.
- For the example the Table shows the bits sequence vs rotation angles.
- The bit sequence (codes) sent determines the step angle. The rate at which these codes are sent determines the speed of rotation (rpm)
- With 4 bits output from the microcontroller, 8 steps are possible, 45 degrees each. This arrangement needs two windings as shown.
- With 8 bits output from the microcontroller, 16 steps are possible, 22.5 degrees each. This arrangement needs four windings.

Note: There are many arrangements of windings and different kinds of inputs possible. The example discussed above is purely for illustrative purposes and by no means exhaustive

Figure 9.16 shows a block diagram of a stepper motor operation using 8051 micro controller
The program must ensure appropriate binary codes are generated in sequence, and fed as inputs to the stepper motor.

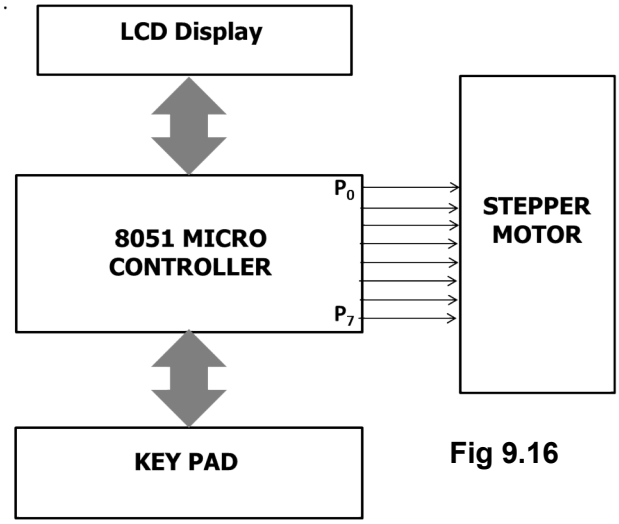


Fig 9.16

Block Diagram of a Stepper Motor Operation using 8051 Micro Controller

For example the codes to be generated in our example for 45 deg rotation are as per the table above.

Chapter 10 Communication Systems

Communication Systems: Introduction, Elements of Communication, Systems, Modulation: Amplitude Modulation, Spectrum Power, AM Detection (Demodulation), Frequency and Phase Modulation. Amplitude and Frequency Modulation: A comparison.

Introduction

What is the role of communication?

A “hello how are you” from one person, from one location, needs to be conveyed effectively and clearly **without noise**, to another person in another location.

A picture sent to someone far away, should be received **without any distortion**.

A file transferred from one location to another location, should be received **without errors**

Communication engineering is a process by which, connection (link) is established between two points, for information exchange maximising customer delight.

Then, what is telecommunications?

Telecommunication implies, communication between two points, separated by a distance. “Tele” means “at a distance”. It takes into account that something may be and will be lost in the process; hence the term 'telecommunication' includes all kinds of distances and all kinds of techniques such as radio, telegraphy, television, telephony, data communication and computer networking

We can define telecommunication as, communicating information such as data, text, pictures, voice, audio, video, feelings, thoughts…… over long distance. The medium for such signal transmission can be thro electrical wire or cable (also known as "copper"), optical fibre or ether etc.

- If the communication is through the free-space by means of electromagnetic waves, then it is called wireless.
- The Internet is the largest example of a typical data communication network.
- Few other forms of Telecom networks, can be Corporate and academic wide-area networks (WANs)
- Different technologies have evolved, to bring out newer applications. Broadband and mobile communication have instantly become popular.
- Some of the technologies in vogue are

  Digital Telephone networks
  WIMAX, WIFI, BLUETOOTH
  Police wireless (Walkie talkie)
  GSM / CDMA / UMTS / LTE / Wireless LAN
  Facebook, Twitter, Linked in, WhatsApp ……..

Distance does not matter anymore. Communication has to happen anytime, anywhere, at any place, through any medium, at any speed, through any device,…….

Elements of communication

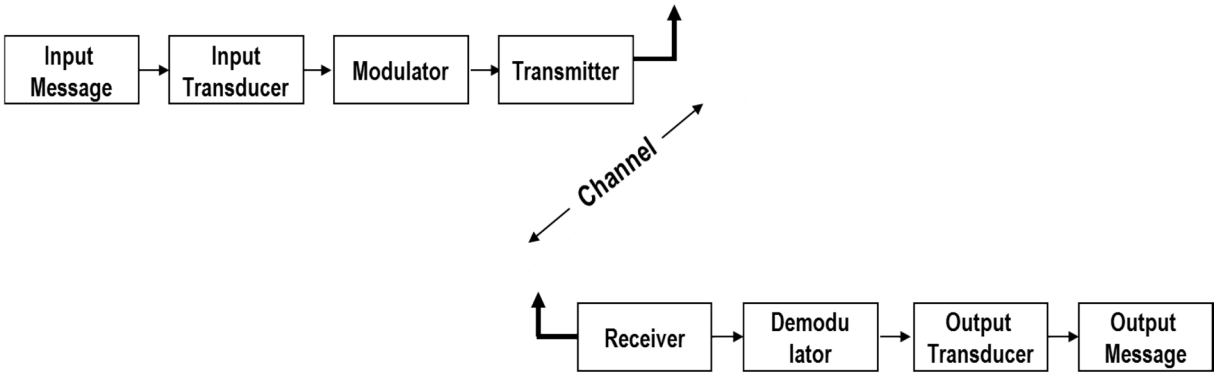


Fig 10.1 Block Diagram of a Communication System

The basic elements of a communication system are shown in the elementary block diagram.

Objectives: Minimum bandwidth, Maximum quality **(Signal to Ratio),** Minimum Bit Error Rate **(BER),** Maximum speed, Economy, Reliability, Mobility …….

Messages: Message can be voice, music, Data, Video, Temperature, Light, Pressure etc

Input transducer: The input can be in any energy form (temperature, pressure, light…….) but for transmission purposes this **needs to be converted to electrical energy**. Transducer does this.

Modulator: Translates the input signal to a higher frequency spectrum and also modulates **(camouflages)** the signal to **combat noise** (Amplitude Modulation, Freq Modulation, Phase Modulation, PCM, Delta Modulation, ASK, FSK, PSK, QPSK, QAM, GMSK ….etc). The output can be **analog or digital** (thro A/D converters).

Transmitter: Converts info into a signal suitable for transmission over a medium. Transmitter **increases the power** of the signal thro power amplifiers and also **provides interfaces to match the transmission medium**, such as antenna interface, fibre interface and so on.

Antenna: If it is a wireless communication, antenna **propagates (radiates)** the signal thro ether (atmosphere)

Channel:

It is the **medium between the Transmitter and Receiver**. It can be Copper wires, fibre, Coaxial, Twisted pair, Ether (atmosphere), Ionosphere and so on; Channel adds noise to the signal. Channel attenuates (reduces the power of) the signal

Noise:

Noise is **the challenge for communication engineers**. It is random and unpredictable in nature.

Noise is the **undesirable electric energy** that enters the communication system and interferes with the desired signal.

Noise is **produced at the transmitter, channel and also at the receiver. Everywhere**.

It can be man-made and natural.

Natural noise: Lightning, Solar radiation, Thermal

Man-made: Welding, Sparking, Motors, Car ignition, Tube lights, Electronic fan regulators etc

Receiver:

- Receives the **signal (desired) with noise (undesired).**
- Recovers the original signal **in spite of the noise**.
- Consists of **amplifiers, filters, mixers, oscillators, demodulators, transducers**.
- Receiver consists of a similar sequence of block diagrams.
- Whatever was **done** in the transmitter will be **undone** in the receiver.
- For example, modulation in TX will be matched by Demodulation in RX, A to D in TX will be undone by D to A in receiver and so on.

Introduction to modulation

Communication is a process of exchanging information.

For example a conversation between friends is a communication which does not have many of the blocks we saw earlier on.

There is no modulator or an antenna, for example. What is conveyed is speech, in its original form as nature intended it to be..

A base band signal is defined as original frequency range of a transmission signal before it is converted, or modulated, to a different frequency range.

Some of the base band signals are Telephone Speech in the local loop, audio music, video picture, computer data in a LAN, USB to PC communication, PC to printer communication and so on.

What are the limitations of baseband communication?

The frequency band of the base band signals will be very less. Therefore, the signals can be sent over very short distances only. Even the best of shouts cannot be heard beyond 100 meters perhaps. The transmission losses (attenuation) will be very high.

Hence, in order to send these signals over long distances, further signal processing is necessary. Essentially the base band **has to be pushed up to occupy a higher frequency range. This process is called modulation.**

What is modulation?

If we want to travel from Bangalore to Chennai, we do not walk all the way. If we do walk it will be like baseband transmission.

We prefer to travel by car, bus, train, plane etc. In other words we **prefer a carrier** to reach faster.

Similarly, in communication systems also, for long distance communications we prefer a **carrier. (A higher freq signal that can carry the baseband signal).**

Higher frequency signals can be carried over longer distances without losses.

Baseband signal is translated into a higher frequency band, using a carrier.

The process by which the base band signal modifies the carrier is called modulation

The resultant signal is called the **modulated signal**

Modulation is employed at the transmitter end. (**Demodulation** is employed at the receiver end)

What is demodulation?

Deployed at the receiver end.

Reverse of modulation.

The process by which the original modulating (input) signal is recovered from the incoming modulated signal is called demodulation

Why modulation?

1) Base band signals are incompatible for long distance communication. Base band signal is prone to rapid attenuation (losses) because of its lower frequency spectrum. Therefore **for long distance communication,** the freq spectrum of base band signals need to be shifted up through modulation

2) Modulation (higher frequencies) **reduces the size and height of the antenna**. Antennae propagate efficiently if their height is around λ/4
   λ = Wavelength of the signal being transmitted.
   λ is given by the relation, **λ = c / f**.
   C= velocity of light ($3X10^8$ m/sec) and f= freq of transmission.
   Therefore if f is high, height of the antenna (λ/4) comes down.

3) **Modulation avoids mixing of signals** from different users (applications) and **allows multiplexing.** Multiplexing means transmission of two or more signals from different users, simultaneously without any mutual interference.
   Examples: A number of FM stations within Bangalore, Many TV channels in a single cable in your home TV).
   In one such multiplexing technique, each one of the many users is allotted a unique carrier frequency and their signals are combined at the transmitter end.
   At the receiver, by employing filters (or tuned circuits) the signals can be separated (demultiplexed or decombined) and sent to the intended recipients.

4) **Improved quality of reception:** Better modulation techniques such as **Frequency modulation, Pulse code modulation** etc **can ignore most of the noise by virtue of their coding techniques** and therefore enhance the quality of communication

Modulation techniques

What are the different types of modulation techniques?

Analog Modulation and Pulse modulation

Refer figure 10.2.

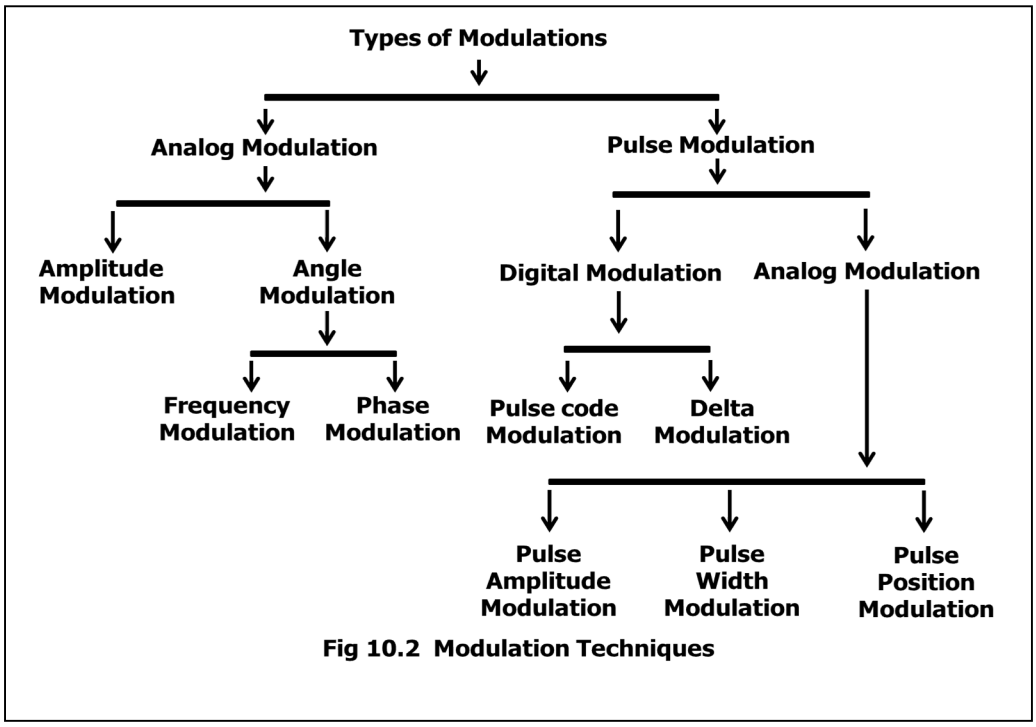


Fig 10.2 Modulation Techniques

What are the analog modulations? Define them

Amplitude modulation: The **Amplitude of the carrier** signal is varied proportional to (in accordance with) the **Amplitude of the input** modulating signal

Angle modulation: There are two types

> **Frequency modulation:** The **Frequency of the carrier** signal is varied proportional to (in accordance with) the **Amplitude of the input** modulating signal
>
> **Phase modulation:** The **Phase of the carrier** signal is varied proportional to (in accordance with) the **Amplitude of the input** modulating signal

What are the pulse modulations?

Some of them are Pulse Code modulation, Pulse Amplitude modulation, Pulse duration modulation and Pulse Position modulation. These will not be discussed in this book further.

What are angle modulation techniques?

FM and PM are known as **angle modulations.**

AMPLITUDE MODULATION

Explain amplitude modulation in detail

Refer fig 10.3 for AM waveforms.

Definition of AM:

Amplitude modulation: The **amplitude of the carrier** signal is varied proportional to (in accordance with) the a**mplitude of the input** modulating signal

In AM, there is a modulating signal. This is also called input signal or base band signal. (Speech for example). This is a low frequency signal as we have seen earlier.

There is another **high frequency signal called carrier.**

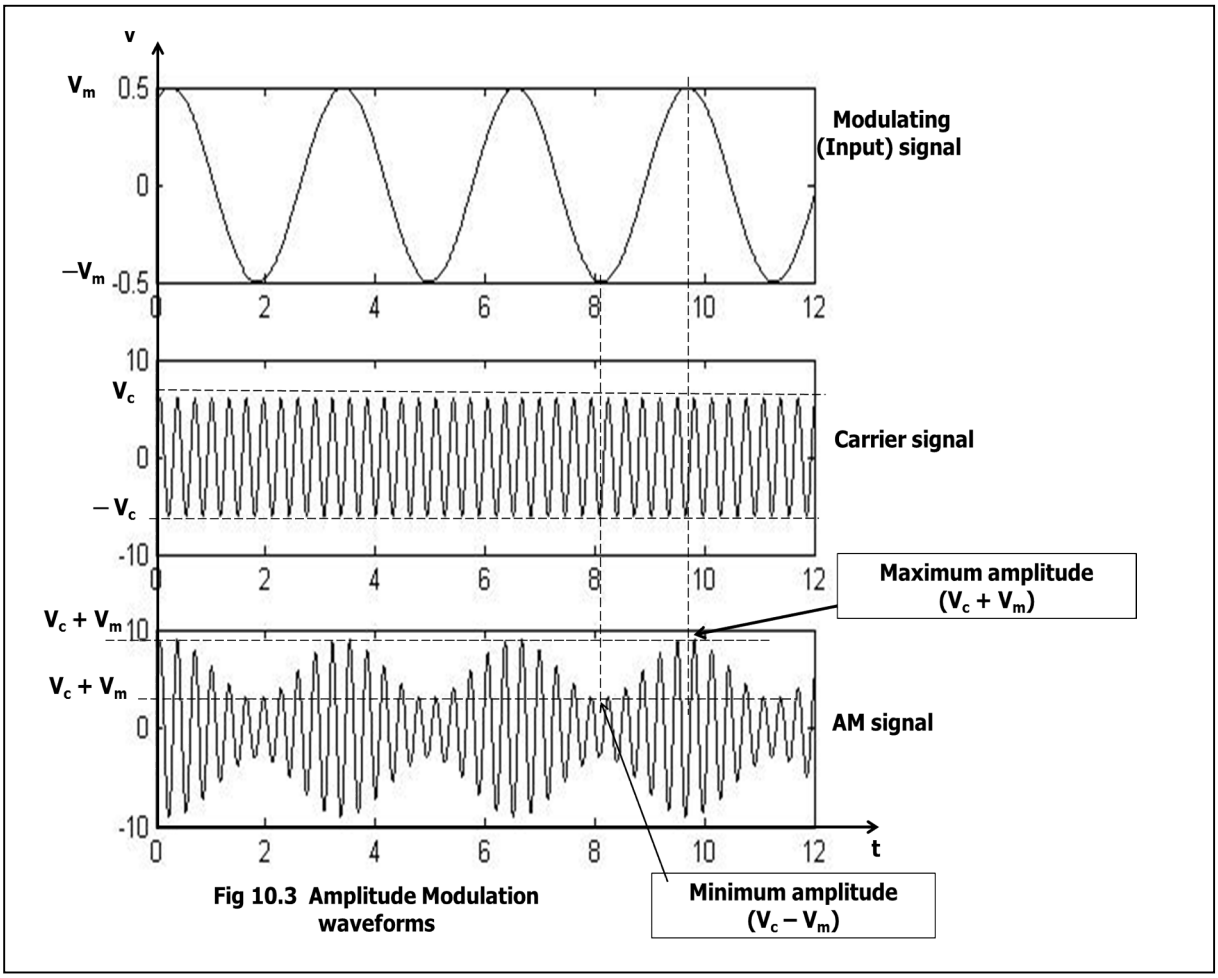


Fig 10.3 Amplitude Modulation waveforms

The purpose of AM is to translate the low frequency base band signal to a higher freq signal using the carrier. As discussed earlier, high frequency signals can be propagated over longer distances than lower frequency signals.

Derive AM equations:

Refer Fig 10.4 for AM waveform Mathematical analysis

Modulating signal (Input signal)

Look at figure 10.4

$v_m = V_m \sin \omega_m t$

where v_m is the instantaneous value and V_m is the maximum value of the modulating (input) signal.

f_m is the freq of the modulating (input) signal and $\omega_m = 2\pi f_m$

Carrier signal

$v_c = V_c \sin \omega_c t$

where v_c is the instantaneous value and V_c is the maximum value of the carrier signal. f_c is the freq of the carrier signal and $\omega_c = 2\pi f_c$

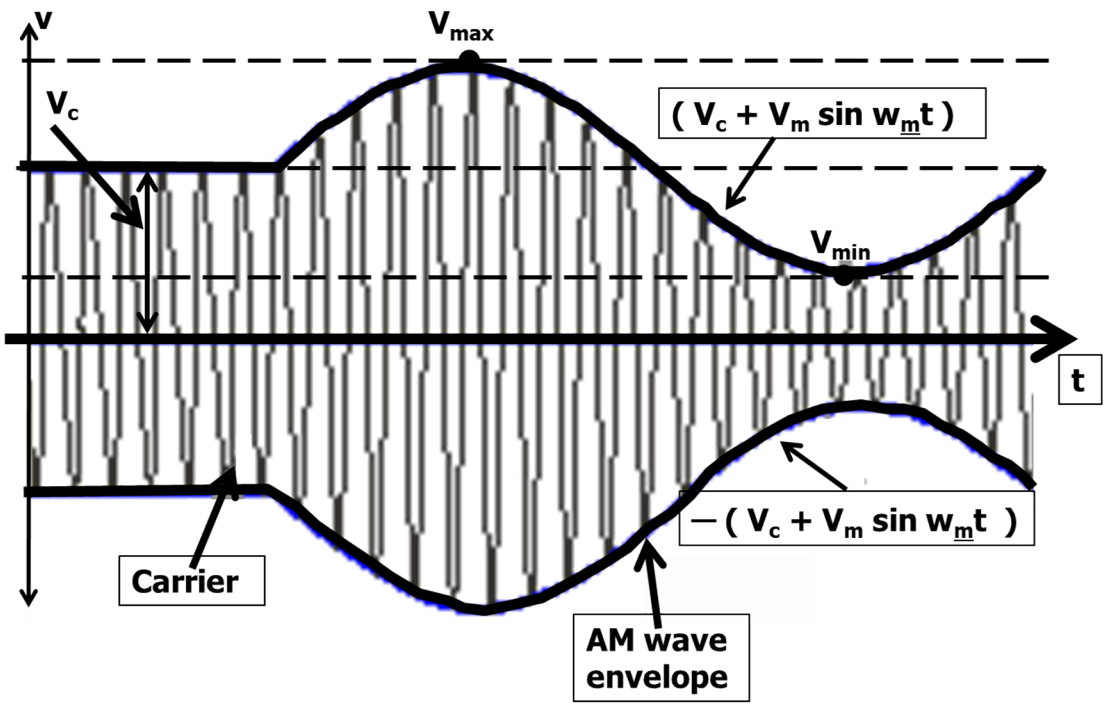


Fig 10.4 AM waveform -- Analysis

Amplitude Modulated signal derivation

Refer fig 10.4

$V_{AM} = V_c + v_m$

$= V_c + V_m \sin \omega_m t$ 10 - 1

$v_{AM} = V_{AM} \sin \theta$

$= V_{AM} \sin \omega_c t$

$= (Vc + V_m \sin \omega_m t) \sin \omega_c t$

$= Vc\ (1+m \sin \omega_m t) \sin \omega_c t$ where m is given by $m = \frac{V_m}{V_c}$ 10 - 2

What is Modulation Index?

Modulation Index is defined as the ratio of the amplitude of the modulating signal and the amplitude of the carrier signal. It is denoted by m

Modulation Index = m = m = $\frac{V_m}{V_c}$ 10 - 3

Modulation Index is also known as **Modulation factor, Modulation coefficient or degree of modulation**

"m" shall have a value **between 0 and 1**.

"m" when expressed as a percentage is called % modulation.

Look at figure 10.4

$V_m = \frac{Vmax - Vmin}{2}$ 10 - 4

V_c = Vmax – Vm

$V_c = V_{max} - \left(\frac{Vmax - Vmin}{2}\right) = \left(\frac{Vmax + Vmin}{2}\right)$ 10 - 5

$\therefore m = \frac{V_m}{V_c} = \frac{(Vmax - Vmin)}{(Vmax + Vmin)}$ 10 - 6

Critical modulation: Look at the Figure 10.5.

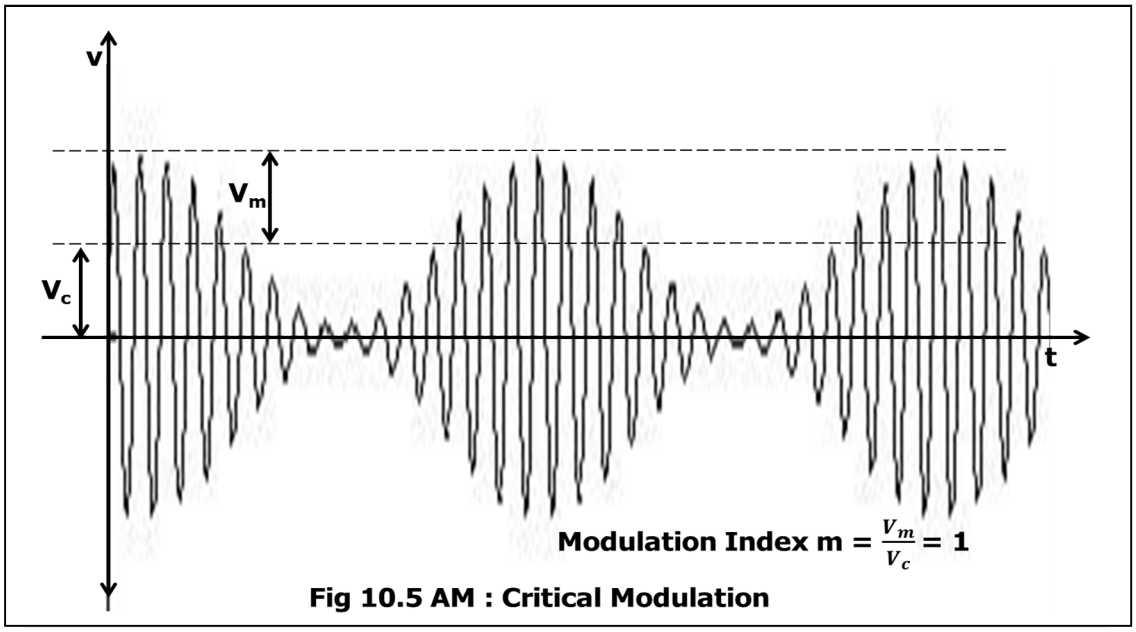


Fig 10.5 AM : Critical Modulation

Happens when modulation Index (m) =1. Note, during critical modulation V_{min} =0

m = $\frac{V_m}{V_c} = \frac{(Vmax - Vmin)}{(Vmax + Vmin)} = \frac{(Vmax)}{(Vmax} = 1$

a. Substitute V_{min} =0. Therefore at critical modulation **$m = V_m / V_c$** ,
b. Substitute m = 1. Therefore at critical modulation **$V_m = V_c$**

What is over modulation?

Look at figure 10.6. Happens when m>1

That is $(V_m / V_c) > 1$. Therefore $V_m > V_c$. In other words the modulating signal is greater than the carrier signal.

What are the sidebands of AM?

The AM signal will generate new signals called side bands, at frequencies other than f_c or f_m.

We know from 10 - 2 that $v_{AM} = (V_c + m V_m \sin \omega_m t) \sin \omega_c t$

We also know from 10 - 3 that $m = V_m / V_c$. Therefore $V_m = m.V_c$

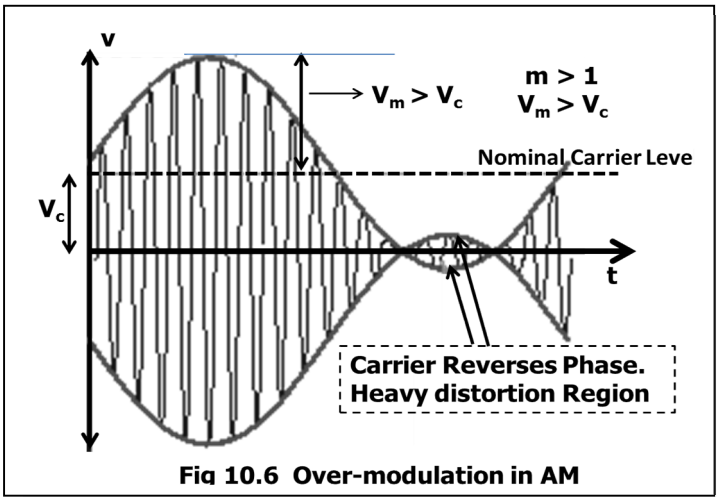


Fig 10.6 Over-modulation in AM

Therefore

Case 1: Both input signal and carrier signal are sine waves.

$v_{AM} = (V_c + m V_c \sin \omega_m t) \sin \omega_c t$ 10.7

$= V_c \sin \omega_c t + m V_c \sin \omega_m t \,.\, \text{Sin}\, \omega_c t$

Recall sin A sin B

$$= \frac{1}{2} [\cos (A - B) - \cos (A + B)]$$

Therefore $v_{AM} = V_c \sin \omega_c t + [\frac{mV_c}{2} \cos (\omega_c - w_m)t] - [\frac{mV_c}{2} \cos (\omega_c + w_m)t]$ 10.8

(Carrier) (Lower side band) (Upper side band)

Therefore AM signal has three frequency components, Carrier, Upper Sideband and Lower Side Band

Case 2: Both input signal and carrier signal are cos waves.

$v_{AM} = (V_c + m V_c \cos \omega_m t) \cos \omega_c t$

$= V_c \cos \omega_c t + mV_c \cos \omega_m t. \cos \omega_c t$

Recall Cos A Cos B $= \frac{1}{2} [\cos (A - B) + \cos (A + B)]$

Therefore $v_{AM} = V_c \cos \omega_c t + [\frac{mV_c}{2} \cos (\omega_c - w_m)t] + [\frac{mV_c}{2} \cos (\omega_c + w_m)t]$ 10.9

(Carrier) (Lower side band) (Upper side band)

Therefore AM signal has three frequency components, Carrier, Upper Sideband and Lower Side Band

What are the frequency components of AM? (or) **Draw the Frequency Spectrum of AM**

Refer fig 10.7.

What is the bandwidth of AM?

The bandwidth of a complex signal like AM, is the difference between its highest and lowest frequency components, and is expressed in Hertz (Hz).

Bandwidth deals with only frequencies.

As shown in the figure 10.7

Bandwidth = $(f_c - f_m) - (f_c + f_m) = 2 f_m$ 10 - 10

Power levels in carrier and side bands

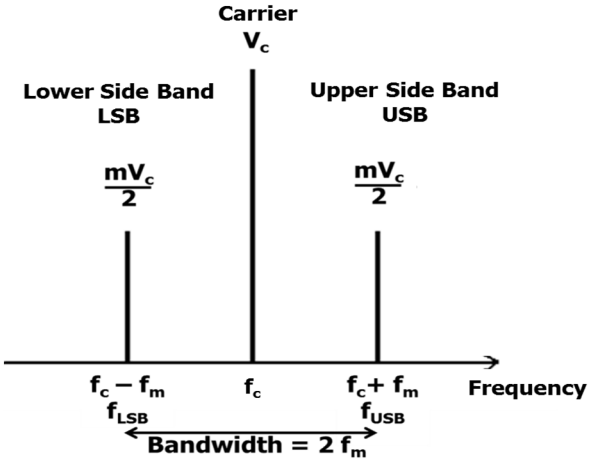


Fig 10.7 AM Side Bands

What are the power relations in AM wave?

There are three components in AM wave.

Unmodulated carrier, USB and LSB.

Total Power of AM is = Power in the Unmodulated carrier + Power in USB + Power in LSB

If R is the load, then Power in AM = $\frac{V_c^2}{R} + \frac{V_{LSB}^2}{R} + \frac{V_{USB}^2}{R}$ 10 - 11

Carrier Power

Peak carrier Power = $\frac{V_c^2}{R}$ 10 - 12

Peak Voltage = V_c ∴RMS voltage = $\frac{V_c}{\sqrt{2}}$

RMS carrier power = $\frac{1}{R}\left[\frac{V_c}{\sqrt{2}}\right]^2 = \frac{V_c^2}{2R}$ 10 - 13

RMS Power in side bands

$P_{LSB} = P_{USB} = \frac{V_{SB}^2}{R} = \frac{1}{R} \times \left[\frac{mV_c/2}{\sqrt{2}}\right]^2$

$= \frac{m^2 (V_c)^2}{8R} = \frac{m^2}{4} X \frac{V_c^2}{2R}$ 10 – 14

	Carrier power	Upper side band	Lower sideband
Peak value	Vc	$\frac{\mathbf{mV_c}}{\mathbf{2}}$	$\frac{\mathbf{mV_c}}{\mathbf{2}}$
RMS Value	$\frac{\mathbf{V_c}}{\sqrt{\mathbf{2}}}$	$\frac{mV_c/_2}{\sqrt{2}} = \frac{mV_c}{2\sqrt{2}}$	$\frac{mV_c/_2}{\sqrt{2}} = \frac{mV_c}{2\sqrt{2}}$
Power (RMS)	$\frac{1}{R}\left[\frac{V_c}{\sqrt{2}}\right]^2$ $= \frac{V_c^2}{2R}$	$\frac{1}{R}$ X $\left[\frac{mV_c/_2}{\sqrt{2}}\right]^2$ $= \frac{m^2V_c^2}{8R}$	$\frac{1}{R}$ X $\left[\frac{mV_c/_2}{\sqrt{2}}\right]^2$ $= \frac{m^2V_c^2}{8R}$

We know $\frac{V_c^2}{2R} = P_c$

Therefore $P_{LSB} = \frac{m^2}{4}$ X P_c 10 - 15

Total Power $= \frac{V_c^2}{2R} + \frac{m^2V_c^2}{8R} + \frac{m^2V_c^2}{8R}$

$= \frac{V_c^2}{2R}$ [1 + (m^2/4) + (m^2/4)] 10 - 16

$= P_c$[1 + (m^2/4) + (m^2/4)]

$\mathbf{P_{Total} = P_c\left[1 + \frac{m^2}{2}\right]}$ 10 - 17

Modulation Index in terms of Total Power (P_{Total}) and Carrier Power (P_c)

$P_{Total} = P_c\left[1+\frac{m^2}{2}\right]$

$\frac{P_{Total}}{P_c} = \left[1 + \frac{m^2}{2}\right]$

$\frac{m^2}{2} = \frac{P_{Total}}{P_c} - 1$

$\mathbf{m = \sqrt{2\left(\frac{P_{Total}}{P_c} - 1\right)}}$

Transmission efficiency

In AM there are three power components P_c, P_{LSB} and P_{USB}

Out of these P_c is an unmodulated carrier. It **is wasteful** as it carries **no information at all.**

The two sidebands carry, all the useful information and therefore useful power is spent only in sidebands.

Definition of efficiency (η) :

Ratio of transmitted power which contains the useful information (P_{LSB} + P_{USB}) to the total transmitted power.

Transmission efficiency = (P_{LSB} + P_{USB}) / (P_{Total})

$$\eta = P_c \left[\frac{m^2}{4} + \frac{m^2}{4} \right] / P_c \left[1 + \frac{m^2}{2} \right]$$

$$= \frac{\mathbf{m^2}}{(\mathbf{2+m^2})}$$

$$\eta\ (\%) = \frac{\mathbf{m^2}}{(\mathbf{2+m^2})} \mathbf{X100}$$

AM Detection

Inverse of modulator.

Demodulator: It recovers (decodes) the original signal (what was the modulating signal at the transmitter end) from the received AM signal.

Envelop detector: Refer Fig 10.8.

AM is a simple wave. Detector is a demodulator. It recovers the original signal (what was the modulating signal at the transmitter end) from the received AM signal.

Detector consists of a simple half wave rectifier which rectifies the received AM signal

This is followed by a low pass filter which removes (by passes) the high frequency carrier wave from the received signal

The resultant output of the low pass filter will be the original input (modulating) signal.

Look at the figure 10.8

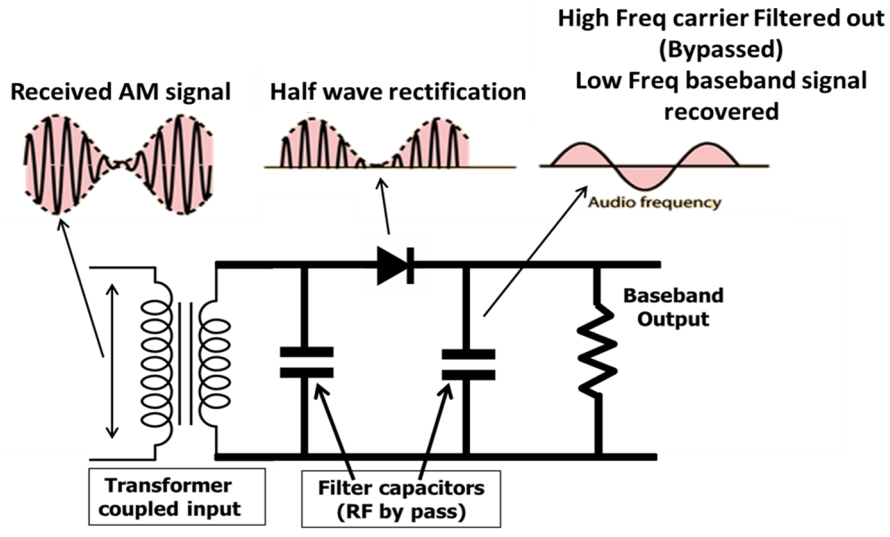


Fig 10.8 AM Demodulator (detector)

The incoming AM signal is transformer coupled

HW rectifier conducts during positive cycles of AM and cuts off negative cycles of AM

Filter capacitor C filters (by passes) the high frequency carrier (f_c) and allows only the lower frequency (f_m)

Thus, the filter output is the original input (modulating) signal.

Problem 1: Calculate modulation index and percentage modulation when modulating signal is 60 Sin $\omega_m t$ and carrier signal 80 Sin $\omega_c t$.

Modulation Index : $\frac{V_m}{V_c} = \frac{60}{80}$ = 0.75.

Percentage modulation = 75 %

Problem 2: In an AM system, the maximum amplitude of the AM wave is 90 V. The modulation Index is 0.5.

What is the minimum amplitude of the AM wave form? What is the amplitude of the carrier?

What is the magnitudes of the side bands? Draw the waveforms.

V_{max} = 90 V, m= 0.5 V_{min} = ? V_c= ? Magnitude of Sidebands = ?

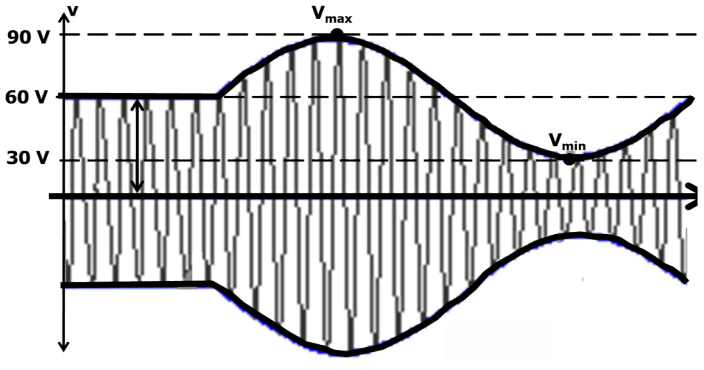
$$\mathbf{m = \frac{V_m}{V_c} = \frac{(Vmax - Vmin)}{(Vmax + Vmin)}}$$

$$0.5 = \frac{(90 - Vmin)}{(90 + Vmin)}$$

On calculating, V_{min} = 30 V

$$V_c = \left(\frac{Vmax + Vmin}{2}\right) = \frac{90 + 30}{2} = 60 \text{ V}$$

Magnitude of Sidebands = $\frac{mV_c}{2}$ = 0.5 X 60 / 2 =15 V



10.9 AM waveform

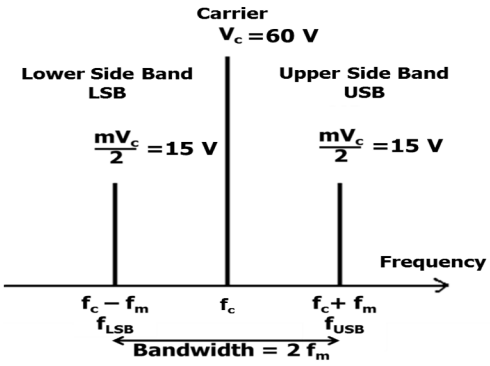


Fig 10.10 AM Side Bands

Problem 3: An AM system has the following specifications. Carrier = 100 sin 100000 πt.

Input audio signal = 30 Sin 2000 πt.

What is the (a) Modulating frequency, (b) Carrier frequency, (c) modulation Index, (d) Side Band frequencies and Bandwidth (e) Amplitude of the sidebands, (f) Carrier Power, (g) Each Sideband Power, (h) Total Power delivered to a load of 50 ohms and (j) Transmission efficiency?

a) Modulating Frequency

Input audio signal = 30 Sin 2000 πt. = $V_m \sin \omega_m t = V_m \sin 2 \pi f_m t$

∴ V_m = 30 V and f_m = 1000 Hz = **1 KHz**

b) Carrier Frequency

Carrier signal = 100 Sin 100000 πt. = $V_c \sin \omega_c t = V_c \sin 2 \pi f_c t$

∴ V_c = 100 V and f_c = 50000 Hz = **50 KHz**

c) Modulation Index : $\frac{V_m}{V_c}$ = $\frac{3\ 0}{100}$ = **0.3. = 30%**

d) Side Band frequencies and Bandwidth

Upper side band frequency: f_{USB} = ($f_c + f_m$) = 50 KHz + 1 KHz = **51 KHz**

Lower sideband frequency : f_{LSB} = ($f_c - f_m$) = 50 KHz ─ 1 KHz = **49 KHz**

Bandwidth = $f_{USB} – f_{LSB}$ = 51 KHz – 49 KHz = **2 KHz**

(e) Amplitude of the sidebands = = $\frac{mV_c}{2}$ = 0.3 X 100 V/2 = **15 V.**

(f) Carrier Power = P_c = $\frac{V_c^2}{2R}$ = $\frac{100\ X\ 100}{2\ X\ 5\ 0}$ = **100 watts**

(g) Each Sideband Power = $\frac{m^2 V_c^2}{8R}$ = $\frac{(0.3)^2\ X\ 100\ X\ 100}{8\ X\ 5\ 0}$ = 0.09 X 25 = **2.25 W**

(h) Total Power delivered to a load of 50 ohms = P_{Total} = $P_c \left[1 + \frac{m^2}{2}\right]$

= 100 watts $\left[1 + \frac{(0.3)^2}{2}\right]$ =100 X 1.045 = **104.5 watts**

(j) Transmission efficiency = $\frac{m^2}{(2+m^2)}$ = $\frac{0.3^2}{(2+0.3^2)}$ = $\frac{0.09}{2.09}$ = 0.043 = **4.3%**

Frequency Modulation

Frequency modulation: The **Frequency of the carrier** signal is varied proportional to (in accordance with) the **Amplitude of the input** modulating signal

Explain Frequency modulation with a diagram

Refer figure 10.9. The input is a single tone sinewave. The carrier and the FM waveform also are shown.

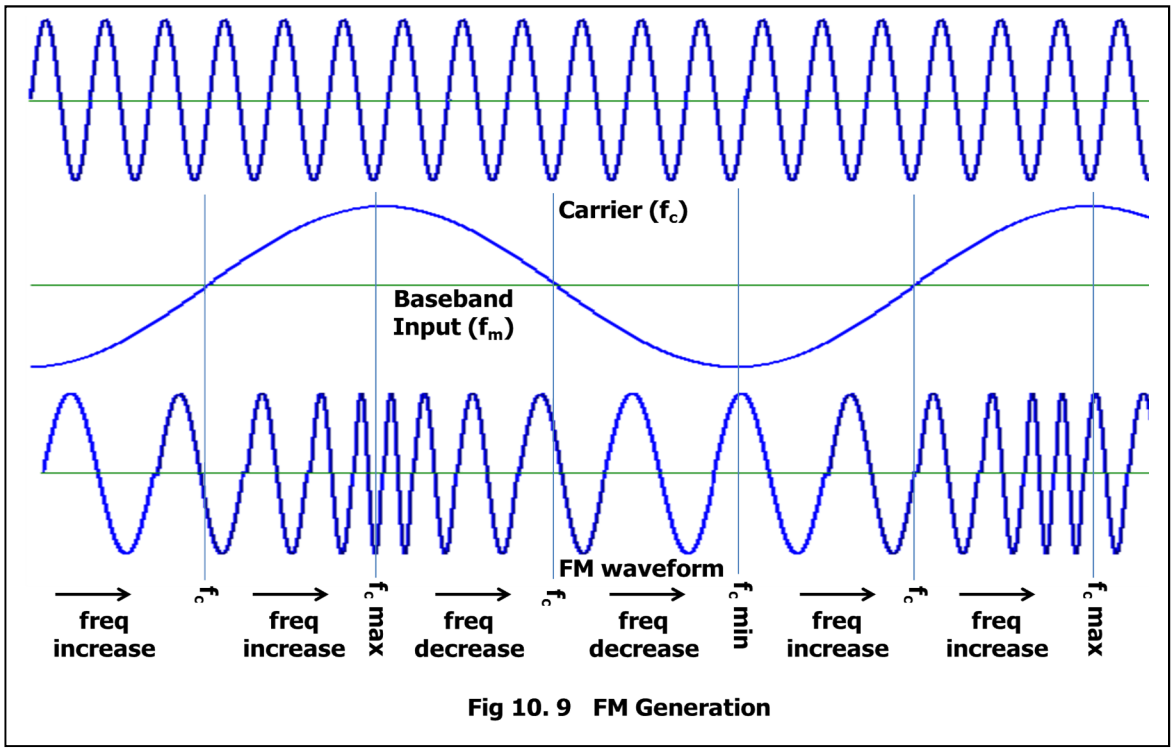


Fig 10. 9 FM Generation

Frequency Modulation explanation:

Refer fig 10.9. The frequency of a carrier (f_c) will increase as the amplitude of modulating (input) signal increases. **The carrier frequency will be maximum (f_c max) when the input signal is at its peak**. The carrier **deviates maximum** from its normal value

The frequency of a carrier will decrease as the amplitude of modulating (input) signal decreases. **The carrier frequency will be minimum (f_c min) when the input signal is at its lowest.** The carrier **deviates minimum** from its normal value

The frequency of the carrier will be at its normal value (free running) f_c when the input signal value is 0V. There is **no deviation** in the carrier.

Fig 10.9 shows the frequency of the FM wave when the input is at its max, 0V and at its min.

What is frequency deviation? Give an example

The Carrier frequency **swings between f_{max} and f_{min}** as the input varies in its amplitude.

The difference between f_{max} and f_c is known as frequency deviation. $f_d = f_{max} - f_c$

Similarly, **the difference between f_c and f_{min} also is known as frequency deviation. $f_d = f_c - f_{min}$**

It is denoted by Δf. Therefore $\Delta \mathbf{f} = f_{max} - f_c = f_c - f_{min}$

It is denoted by f_d. Therefore $\mathbf{f_d} = f_{max} - f_c = f_c - f_{min}$

Modulating signal Amplitude	Frequency of Carrier	Deviation
0 V	100 MHz	Nil (Center frequency)
+2 V	105 MHz	+ 5 MHz
– 2 V	95 MHz	- 5 MHz

Freq deviation = 105 -100 = 5 MHz (or) Freq deviation = 100 - 95 = 5 MHz

The amount of change in the carrier frequency produced, by the amplitude of the input modulating signal, is called frequency deviation

FM equation:

$v = A \sin [w_c t + (\Delta f / f_m) \sin w_m t]$

$= A \sin [w_c t + m_f \sin w_m t]$

A = Amplitude of FM signal. Δf = Frequency deviation

m_f = Modulation Index of FM

$\mathbf{m_f = \frac{\Delta f}{f_m}}$ $\mathbf{m_f}$ is called the modulation index of frequency modulation.

$w_m = 2\pi f_m$ $w_c = 2\pi f_c$

What is modulation Index of Frequency Modulation?

Modulation index of FM is defined as the ratio of the frequency deviation of the carrier to the frequency of the modulating signal

m_f = Modulation Index of FM = $\mathbf{\frac{\Delta f}{f_m}}$

Problem 4: Find the modulation index of this FM signal. Carrier frequency = 0.2 GHz. Modulating frequency = 20 kHz. The carrier is designed to deviate by 15% due to FM.

f_c = 0.2 GHz = 0.2 X10^9 = 200 MHz. f_m = 20 kHz. Δf = 15% of f_c = 15% of 200 kHz = 30 kHz.

m_f = Modulation Index of FM = $\mathbf{\frac{\Delta f}{f_m}}$ = 30 kHz / 20 kHz = 1.5

Problem 5: In a freq modulation system, the carrier frequency deviates 10 kHz for every 1 Volt increase in the modulating signal amplitude (10 kHz/V). If the input signal peak amplitude is 2.5V and its frequency is 3.4 kHz what is the peak deviation and the modulation index

Input voltage = 2.5 V peak.

Frequency deviation = 10 kHz for every 1V of input. Therefore Freq deviation (Δf) = 10 kHz X 2.5 V

Δf = 25 kHz, f_m = 3.4 KHz,

$\therefore m_f$ = Modulation Index of FM = $\mathbf{\frac{\Delta f}{f_m}}$ = 25 KHz / 3.4 KHz = 7.35

Problem 6: Identify the peak voltage, RMS voltage, Modulation Index, Carrier frequency and the modulating frequency if a FM signal is described as v = 6.5 sin(2X10^7 + 10 sin 3400t).

Compare this eqn with the standard form v = A sin [$w_c t + \frac{\Delta f}{f_m} \sin w_m t$]

Peak voltage (A) = 6.5 V RMS voltage = 6.5 / $\sqrt{2}$ = 4.6 V

$\omega_c = 2X10^7$ $\therefore f_c = \frac{\omega_c}{2\pi} = \frac{2\ X\ 10^7}{2\pi}$ = 3.2 MHz

$\omega_m = 3400$ $\therefore f_m = \frac{\omega_m}{2\pi} = \frac{3\ 400}{2\pi}$ = 541 Hz

Modulation Index = 10

Problem 7: For the above example find the frequency deviation

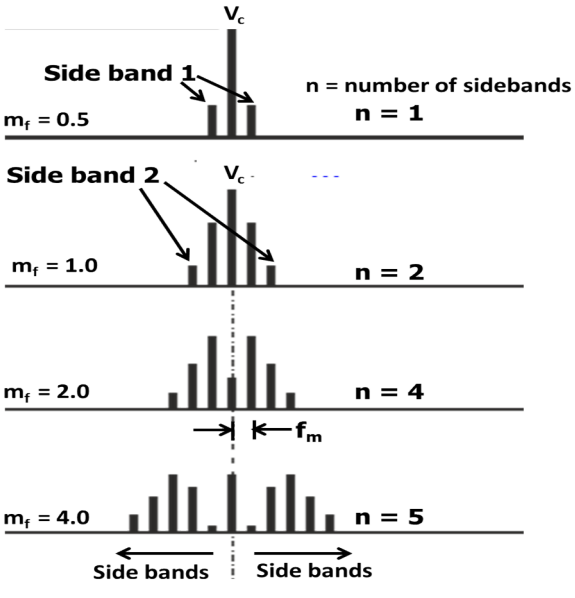
A = 6.5, f_c = 3.2 MHz f_m= 541 Hz

$m_f = 10 = \frac{\Delta f}{f_m}$ $\therefore \Delta f = m_f X\ f_m$ = 10 X 541 Hz = 5410 Hz

Bandwidth of Frequency Modulation signal

Recall, the bandwidth of a complex signal like FM, is the difference between its highest and lowest frequency components, and is expressed in Hertz (Hz). Bandwidth deals with only frequencies.

AM has only two side bands (USB and LSB) and the bandwidth was found to be 2 f_m.



10.10 Frequency Modulation : Sidebands

In FM it is not so simple. FM signal spectrum is quite complex and **will have infinite number of sidebands as shown in figure 10.10**. This figure gives an idea, how the spectrum expands as the modulation index increases.

Sidebands are separated from carrier by $f_c \pm f_m$, $f_c \pm 2f_m$, $f_c \pm 3f_m$ and so on……

Only the first few sidebands will contain the major share of the power (98% of the total power) and therefore only these few bands are considered to be significant sidebands

As a rule of thumb, often termed as Carson's Rule, 98% of the signal power in FM is contained within a bandwidth equal to the deviation frequency, plus the modulation frequency doubled:

Carson's rule: Bandwidth of FM BW_{FM} $= 2 [\Delta f + f_m]$.

$= 2 f_m [m_f + 1]$

FM is known as Constant bandwidth system. Why?

Example:

$\Delta f = 75$ KHz $f_m = 500$ Hz $BW_{FM} = 2 [75 + (500/1000)]$ KHz $= 151.0$ KHz

$\Delta f = 75$ KHz $f_m = 5000$ Hz $BW_{FM} = 2 [75 + (5000/1000)]$ KHz $= 160.0$ KHz

$\Delta f = 75$ KHz $f_m = 10000$ Hz $BW_{FM} = 2 [75 + (10000/1000)]$ KHz $= 170.0$ KHz

Although modulating freq increased 20 times (50 Hz to 5000 Hz), deviation increased only marginally (151 KHz to 170 KHz). Hence FM is known as constant bandwidth system

Commercial FM (Carson's rule.**)**

Max freq deviation = 75 KHz

Max Modulating freq = 15 KHz

$BW_{FM} = 2 [75 + 15]$ = 180.0 KHz

Compare AM and FM

Frequency Modulation	Amplitude modulation
Equation for FM : $v = A \sin [w_c t + \frac{\Delta f}{f_m} \sin w_m t]$ $= A \sin [w_c t + m_f \sin w_m t]$	Equation for AM = $V_c (1 + m \sin \omega_m t) \sin \omega_c t$ where m is given by $m = V_m / V_c$
Modulation Index can have any value greater than 1 or less than one	Modulation Index will be between 0 and 1
In FM, carrier amplitude is constant. Therefore transmitted power is constant. Transmitted power does not depend on modulation index	Transmitted power depends on modulation index $P_{Total} = P_c [1 + (m^2/2)]$
Number of significant side bands in FM is large.	Only two sidebands in AM
Bandwidth of FM depends on the modulation index of FM	Bandwidth does not depend on modulation index of AM. Always 2 side bands. BW of AM is $2 f_m$

FM has better noise immunity. FM is rugged / robust against noise. The quality of FM will be good even in the presence of noise	In AM, quality is affected seriously by noise
Bandwidth required by FM is quite high. FM bandwidth = 2 [$\Delta f + f_m$].	Banwdwidth required by AM is less (2 f_m)
Circuits for FM transmitter and receiver are very complex and very expensive	Circuits for AM transmitter and receiver are simple and less expensive

Phase Modulation

Phase modulation: The **Phase of the carrier** (ϕ) signal is varied proportional to (in accordance with) the **Amplitude of the input** modulating signal

PM equation:

$v = A \sin [w_c t + \phi]$

$v = A \sin [w_c t + m_p \sin w_m t]$

A = Amplitude of PM signal. m_p = Modulation Index of PM

$w_m = 2\pi f_m$ $w_c = 2\pi f_c$

The carrier phase deviation will be more if the input signal amplitude increases and vice versa.

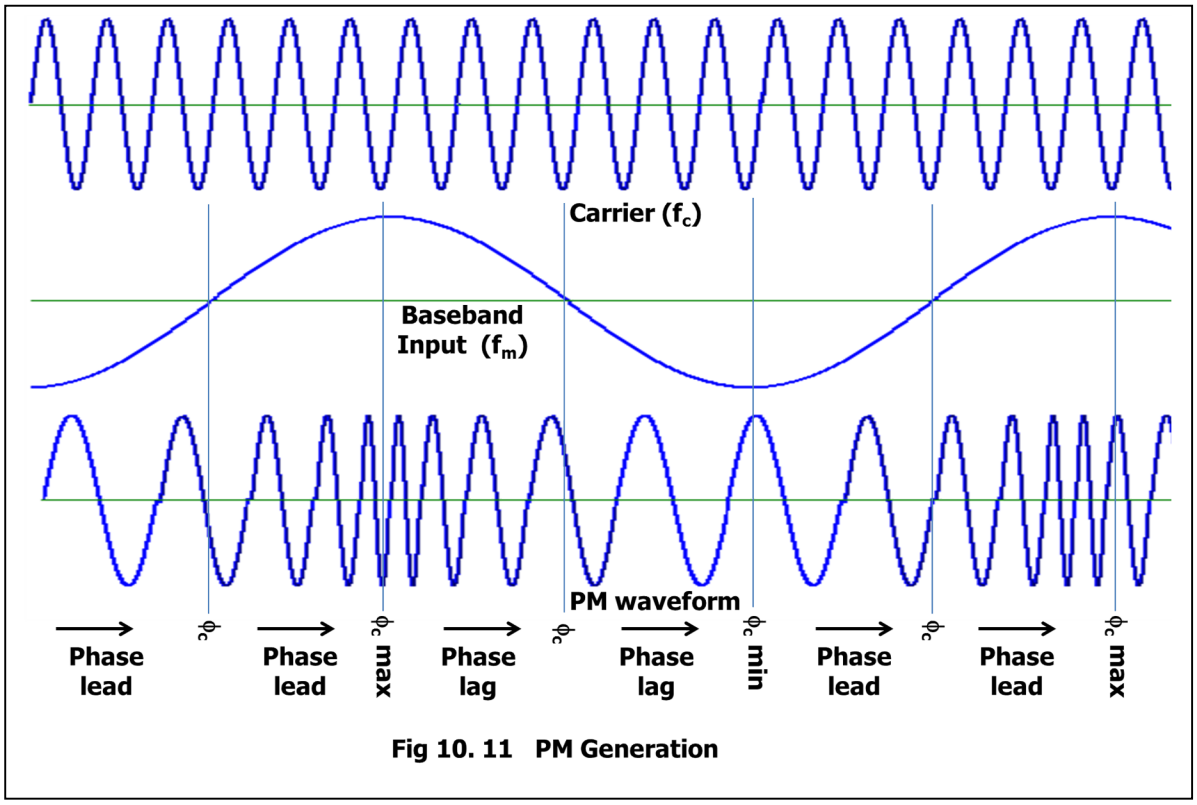


Fig 10. 11 PM Generation

Figure 10.11 shows phase modulation. In this example,

When the input amplitude increases (+ve slope) the carrier undergoes phase lead.

When the input amplitude decreases (-ve slope) the carrier undergoes phase lag.

Therefore as the input amplitude increases, the magnitude of the phase lead also goes on increasing from instant to instant. For example if the phase lead was 30 degrees at t =1 sec, the phase lead increases to 35 degrees at t = 1.1 sec and so on. **Increase in phase lead is equivalent to increase of frequency.**

Similarly, as the input amplitude decreases, the magnitude of the phase lag also goes on increasing from instant to instant. For example if the phase lag was 30 degrees at t =1 sec, the phase lag increases to 35 degrees at t = 1.1 sec and so on**. Increase in phase lag is equivalent to decrease of frequency.**

Therefore PM waveform will be similar to FM waveform in all aspects.

Chapter 11 Transducers

Module 5 Syllabus: Transducers (Text-2): Introduction, Passive Electrical Transducers, Resistive Transducers, Resistance Thermometers, Thermistor. Linear Variable Differential Transformer (LVDT). Active Electrical Transducers, Piezoelectric Transducer, Photoelectric Transducer

11.1 Introduction

What is a transducer?

- **A transducer is a device that converts one type of energy, to another type**. The output energy maybe of any form (need not necessarily be electrical)
- **Example:** A speaker is a transducer. It converts electrical signal, to pressure waves (sound).
- Transducer is a device that **converts variations in one form of energy, such as, pressure, temperature, displacement, force, sound or brightness, into another form of energy or vice versa.**

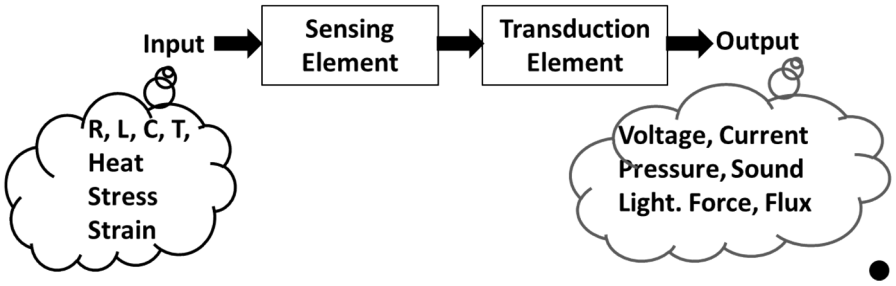


Fig 11.1 Transducer Block Diagram

A transducer will have basically two main components. They are

1. Sensing Element (Sensor)

Sensor senses an input physical quantity or its rate of change, and converted it as an output. This output will be fed to a transduction element. The figure gives examples of, the types of inputs to the sensor.

2. Transduction Element

The output of the sensing element (sensor) is, the input to the transduction element. This element converts the **non-electrical signals into, a proportional electrical signal**. The figure gives examples of, the types of outputs of the transduction element.

What is an electrical transducer?

- An electrical **transducer** is a device which **converts any input physical quantity, into a proportional electrical quantity, such as voltage or electric current**. **The output is always in electrical form** and is equivalent to the measured quantity.
- Examples: A temperature transducer will convert temperature, to an equivalent electrical potential. A potentiometer, will convert the change in displacement, into change in the resistance

What are the classifications of transducers?

The transducers can be classified in several ways such as

1. Active and passive transducers.
2. Primary and secondary transducer
3. Analog and digital transducers.
4. On the basis of transduction principle used.
5. Transducers and inverse transducers.

Let us look at just 1 and 2.

11.2 Passive Transducers:

What is a passive transducer? Classify passive transducers.

- **Passive transducers** are those which convert one form of energy, to another form, **without the use of any external energy.**
- A passive sensor **has no power supply** and all the energy it delivers to the next stage, is **drawn from the input (measurand)**.
- Passive sensors are also known as, **self-generating sensors**.
- Passive transducers convert physical quantities like, temperature, pressure, and speed etc., into equivalent electrical energy. They **do not need any external power supplies**, to perform this action.

Three major classifications are possible

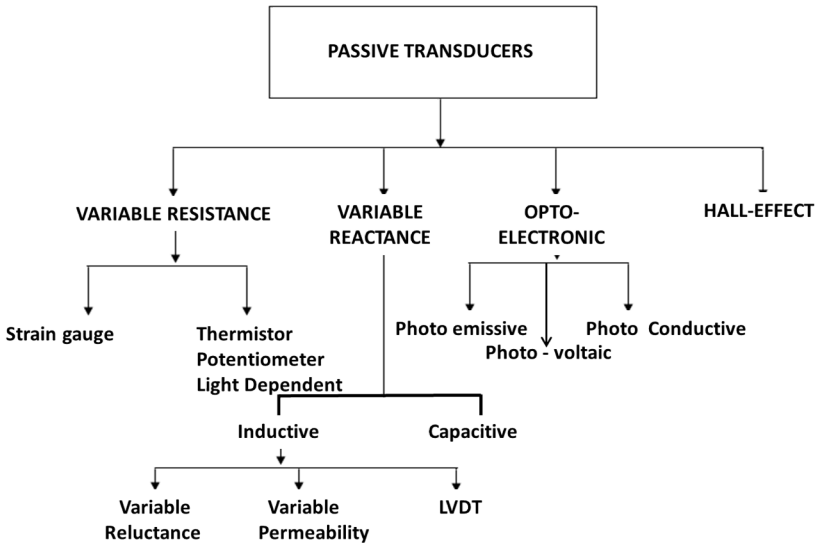


Fig 11.2 PASSIVE TRANSDUCER CLASSIFICATION

Variable resistance:

A resistance is a transducer. Its resistance value will change, due to an applied **mechanical motion (slider) or due to input temperature, input light etc.**

This **change of resistance** value can be measured, at the output as **voltage or current**.

Examples: Photoconductors, Sliding Potentiometers, Strain Gauges, LDRs, Thermistors

What is a Strain Gauge?

- It is **a sensor**, **whose resistance varies, with applied force**; It converts **force, pressure, tension, weight, etc., into a change in electrical resistance** which can then be measured and displayed appropriately.
- If a wire is stretched, the wire becomes thin and area of cross section **(a) of the wire reduces**. Resistance increases.
- If the wire is compressed, wire becomes thick and area of cross section **(a) of the wire increases**. Resistance decreases. This principle is used in strain gauges

Variable reactance:

The reactance of an **inductor or capacitor, varies due to motion which in turn may be, due to Pressure, temperature etc**.

Example 1. Capacitive Transducer:-

In a secondary transducer, the **capacitance value changes, when the distance between two plates is varied** (by using a primary transducer). It is also possible, to **vary overlapping areas of the plates, by moving them around**, to vary the capacitance value.

Example 2: A varactor diode varies its capacitance when reverse bias across it varies.

11.3 Photo electric Transducers

Opto-electronics:

Mainly three types. **Photo voltaic, photo conductive and photo emissive**.

a) Photo Voltaic transducer

The photovoltaic effect is, the **creation of voltage or electric current in a material, upon exposure to light.**

Photovoltaic cells are made from single crystal silicon PN junctions. They are very similar to photodiodes, with a very large light sensitive region.

When illuminated, the light energy causes electrons to flow through the PN junction. For example, an individual **solar cell** can generate an open circuit voltage of about 0.58v (580mV).

Example: Solar Panel.

b) Photo conductive: It is the property of certain materials, which **increase their electrical conductivity, when exposed to light of sufficient energy**. Example **: LDR**- Light dependent resistor. It is a photo resistor. **The resistance of a photo-resistor decreases, with increasing incident light intensity and vice versa**. One popular material for LDR, is cadmium sulphide (CdS)

c) Photo emissive Transducers

Photoemission is the **emission of electrons from a surface, caused by the action of light striking it.**

Photo emissive transducers are **also known as Photo electric transducers**.

Phototube: Has a photocathode coated with alkali metals. Light input, to be measured, will be incident on this cathode. As a result photons are released. Radiation photons with sufficient energy, cause electrons to jump from cathode to anode.

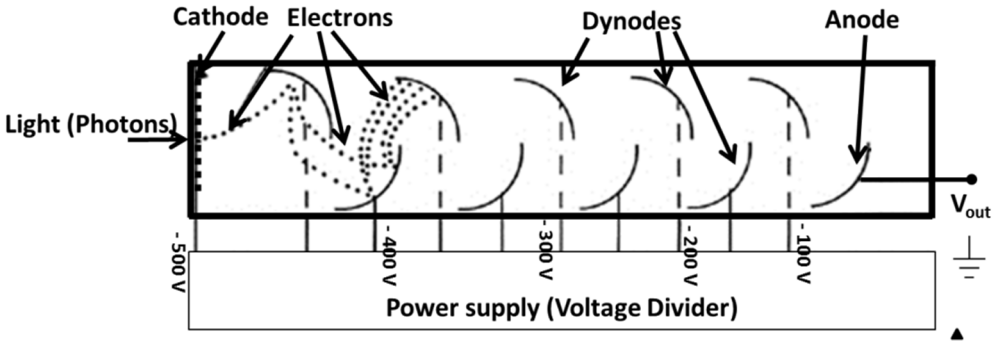


Fig 11.3 Photo emissive (Photo electric) Transducer

Photomultiplier: An incoming photon strikes the photocathode. It liberates an electron. This electron is accelerated toward the first dynode, which is 100 V more positive than the cathode. Due to its impact, this **single electron liberates several electrons, by what is called secondary emission**. This **multiplication process continues** at every successive dynode, until it reaches the anode, where currents of about 1 mA flow through R_L.

11.4 Active Transducers:

What is an active transducer? Classify active transducers.

- **Active transducers** are those which **definitely require an external source** of energy to operate. Energy has to be supplied to these transducers, **through a separate Power supply** source.
- An active sensor is a modulator. It **can deliver more energy to the output**, than it takes from the input (measurand)..
- Example: **Piezoelectric Type** – When an **external force is applied on to a quartz crystal, there will be a proportionate change in the voltage generated across its surface.** This change is measured and correlated to the input force applied. They need an external power supply, to perform this action.

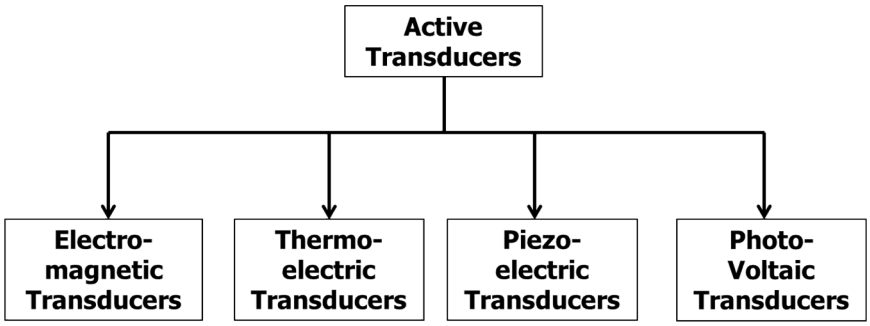


Fig 11.4 Active Transducers Classification

Four major classifications are possible.

1. **Electromagnetic:** Example: Antennae convert input electrical signals into, electromagnetic waves
2. **Thermo-electric:** The **thermoelectric effect** is the **direct conversion of temperature differences, to electric voltage** and vice versa. Example: Take iron and copper wires and join at both ends. Heat one junction, while the other junction is at room temperature. A current will flow from cold junction to hot.

3. **Piezo electric:** It is the ability of certain materials, **to generate an electric charge, in response to applied mechanical stress**. Example: Quartz crystal used in clocks and wrist watches.
4. **Photo voltaic:** The **photovoltaic effect** is the **creation of voltage or electric current, in a material upon exposure to light**. Example: Solar Cell.

Compare passive and active transducers:

Active transducers	Passive transducers
External power source is not needed They generate their own outputs and hence are known as self-generating transducers.	External power source is a must. They depend on an external power source, to produce outputs and hence are not self-generating.
They usually produce outputs such as voltage, current and so on…..	They produce changes in their basic parametric values such as resistance, inductance, capacitance…..
Exa mples: Thermocouple, Solar cells, Piezo electric crystals…….	Examples: LDR, Thermistor, Varactor diode, LVDT……

11.5 Resistive Transducers

Explain the principle of a resistive type of transducer.

The transducer here is a resistor.

As we know, the resistance of any conductor = $R = \frac{\rho l}{a}$

Where, ρ — resistivity of the conductor, in ohms-meter.
l — length of the conductor in meters.
a — area of the conductor in $(meter)^2$.

1) **When length (l) of a conductor is varied, resistance value changes**. This principle is used in slide potentiometers and rotary potentiometers

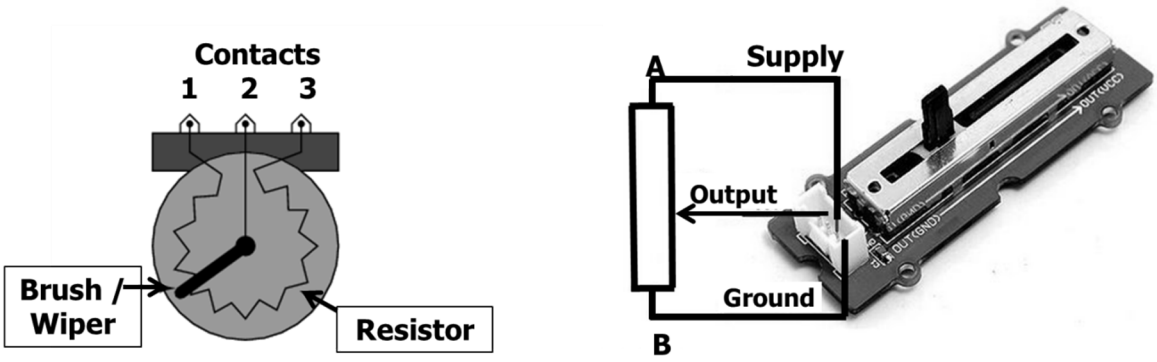


Fig 11.5 Resistive Transducers

2) If the wire is stretched, wire becomes thin **and area of cross section (a) of the wire reduces. Resistance increases.**
3) If the wire is compressed, wire becomes thick and area of cross section **(a) of the wire increases. Resistance decreases.** This principle is used in **strain gauges.**
4) **Resistivity (ρ), changes with temperature**,. This property is used in temperature measurements.

Change in any of these parameters, (ρ, l or a) causes change in resistance value. This resistor is connected to a power supply.
Value changes in R will result in value changes in current, through the circuit. The change of current can be measured and displayed as proportionate change in temperature, displacement, stress, strain torque etc.

Resistance transducer for displacement.

- Input is fed to a primary transducer (not shown).
- The output of the primary transducer is in the form of a linear motion, which is used to move the slider arm of a potentiometer.
- The wiper attached to the potentiometer moves left or right, causing a variation in the resistance value. This causes a change in the circuit current I. The ammeter reading varies accordingly.
- The change of current can be displayed, as proportionate change of the input temperature, displacement, stress, strain torque etc.
- Thus, the input is converted into a proportional output current.

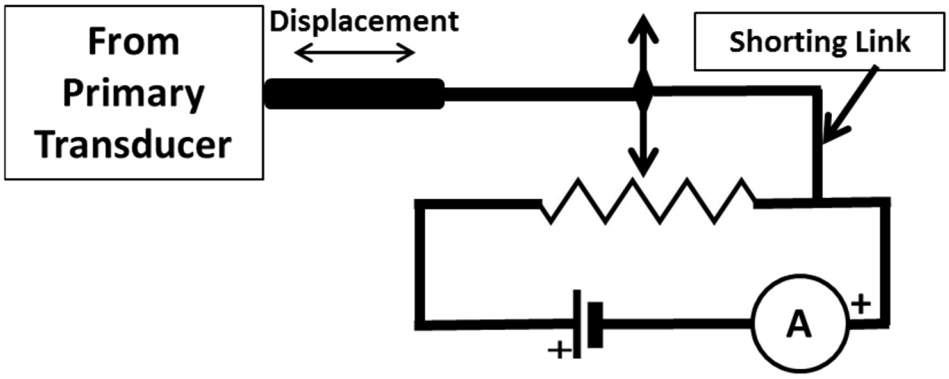


Fig 11.6 Resistance transducer for displacement.

11.6 Resistance Thermometers

Explain the principle and operation of a thermometer.

- Resistance thermometer is also known as, **resistance temperature detectors. (RTDs).**
- **Principle:** If **temperature of a resistor increases or decreases, the resistance increases or decreases respectively**. It is a positive temperature coefficient characteristic. Resistance variation with respect to temperature, is given by $\mathbf{R_t = R_0\ [\ 1 + \alpha_t\ ]}$.
- R_t and R_0 are resistances at temperatures t˚C and 0˚C.
- α = temperature coefficient of the resistance.
- RTDs use a **wheat-stone bridge** as shown.

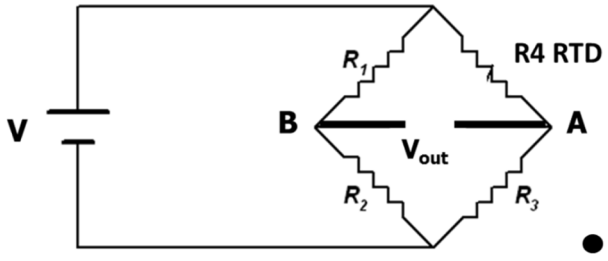
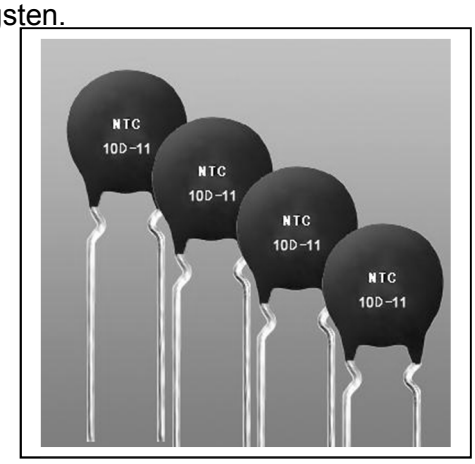


Fig 11.7 Resistance Thermometers

As we know, in Wheatstone bridge, the voltage across AB will be zero if $\frac{R_1}{R_2} = \frac{R_4}{R_3}$

The RTD transducer resistor is connected as R_4. The temperature to be measured, heats up R_4. The resistance R_4 varies, proportionate to the temperature. The **imbalance in the bridge, will show up as an error voltage,** which can be measured and displayed appropriately.
The popular materials for RTDs are copper, Nickel and Tungsten.



11.7 Thermistor

Explain the principle and operation of a thermistor.
Principle of Thermistor:

- It is a thermal resistor.
- Its **resistance varies significantly with temperature**.
- Thermistor resistance **(R) decreases with increasing temperature (T).** (For metals, R increases with T)
- Thermistor therefore, is a **negative temperature coefficient device**.
- Thermistor equation: $\mathbf{R_T = R \exp \beta(\frac{1}{T_1} - \frac{1}{T_2})}$

All the temperatures **are in Kelvin**
R → Resistance at a known temperature (T_1)
R_T → Resistance at the unknown temperature, to be measured. (T_2)
B → Thermistor constant.

The same RTD circuit shown earlier can be used for thermistors also. RTD has to be replaced by thermistor.
Thermistors are made of metal oxides of copper, manganese or nickel.

Advantages: Low cost and compact. Resistance variation is large, with temperature.
Disadvantages: Resistance variation with temperature is not linear. Requires a complex circuit such as wheatstone bridge.

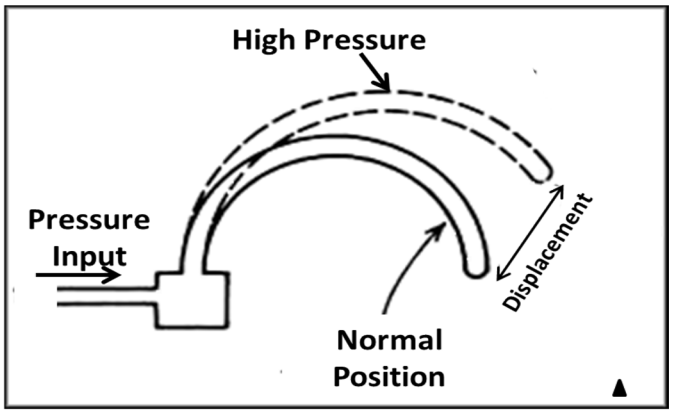
11.8 PRIMARY AND SECONDARY TRANSDUCERS

What is a Primary transducer?
Primary transducer: A sensing device, which **converts the physical quantity to be measured, into a mechanical signal.** These transducers **do not need electrical power supply**. Primary transducer output is **always fed to, a secondary transducer**.
Secondary transducer: The Electrical device, which **converts this mechanical signal to the electrical signal.**
Example: Microphone. The speech energy (air-pressure) goes and impinges on the diaphragm of the microphone. The diaphragm moves and converts the pressure, to mechanical energy. Diaphragm is the primary transducer.
The mechanical movement of the diaphragm is converted into electrical energy, through a coil and magnet assembly. This assembly is the secondary transducer.

Bourdon tube

- A Bourdon tube is a device using which, pressure can be measured. **Pressure is converted into, a proportionate mechanical motion.**

- A Bourdon tube is a metal tube, which is **curled up**.
- The base-end is held rigid and cannot move.
- The tip-end is, free to move.
- When **pressure is applied, the tube tends to uncurl and eventually straighten out**. More pressure will uncurl (unwind) the tube and less pressure will curl (wind) the tube.



Example of a primary transducer. Pressure to Displacement

Fig 11.8 Bourdon Tube

- This means, the **tip moves proportional to the pressure applied, at the input**. This is an example of a primary transducer.
- For example, **the movement of the tip, can be used to move a core (iron or ferrite), inside a coil, up or down, depending upon the quantum of input pressure. As a result, the voltage induced in the coil will increase or decrease. This assembly is the secondary transducer**.

11.9 LVDT (Linear Variable Differential Transducer)

Explain the principle and operation of a LVDT (Linear Variable Differential Transducer). LVDT is a secondary transducer. **For LVDT to function, it depends on a primary transducer**. In LVDT, **mutual inductance (M) is varied between a primary winding and two secondary windings**. The **variation of M, is dependent on displacement of a core (armature), caused by a primary transducer.**

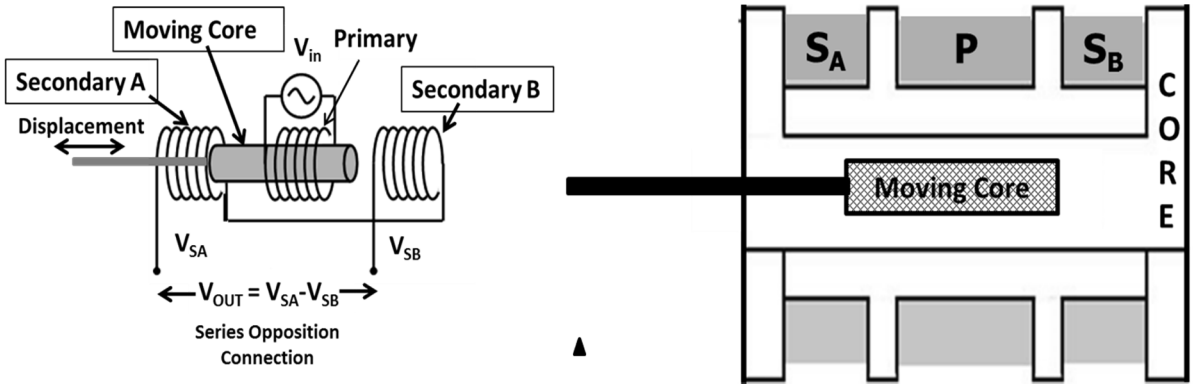


Fig 11.9 LVDT Construction

- LVDT consists of one primary winding (P) and two secondary windings S_A and S_B. Refer fig 11.9.
- All these three windings are symmetrically wound around a hollow, tube.

- A movable magnetic core is placed, inside this hollow tube, concentrically.
- This core, made of some good magnetic material such as ferrite, gets magnetically linked (flux linkage) to all the three windings (P, S_A and S_B).
- An input is applied at the primary. Due to this, **voltages V_{SA} and V_{SB} are induced**, in the secondary windings.
- **The two secondaries S_A and S_B are connected in such a way, the induced voltages oppose each other**.
- **The net output will be the difference, between V_{SA} and V_{SB}.**

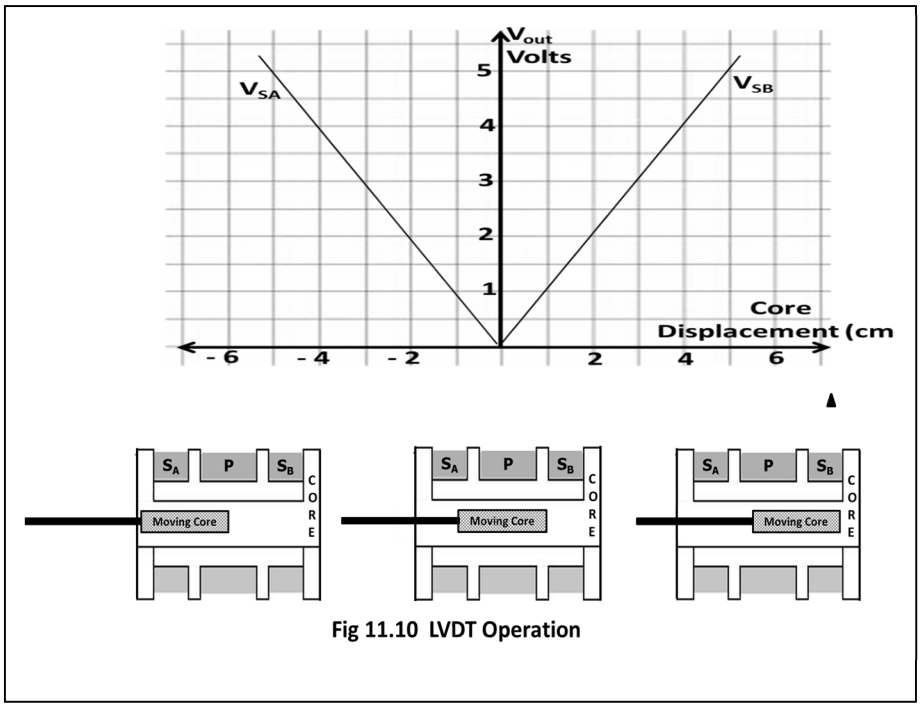


Fig 11.10 LVDT Operation

A. If the core is **at center position**, flux linkage will be equal, and therefore induced **voltages V_{SA} and V_{SB}, will be equal to each other**. Net output = 0 V.

B. If the core is **moved off center, for example towards left side in the diagram, the induced voltage V_{SA} is more than V_{SB}.**

C. If the core is **moved off center, for example towards right side in the diagram, the induced voltage V_{SB} is more than V_{SA}.**

<u>LVDT is a transducer.</u>

Refer fig 11.9

- **An input, for example, is applied to a Primary transducer (not shown in figure). The pressure is converted into a linear displacement motion, by this transducer**.
- The linear displacement motion from the **primary transducer** is linked, to the core in the **secondary transducer LVDT**.
- As **the pressure increases, the core moves towards right and V_{SB} increases. The differential output V_{SA} - V_{SB}, will be net negative**.
- As the **pressure decreases, the core moves towards left and V_{SA} increases. The differential output V_{SA} - V_{SB}, will be net positive**.

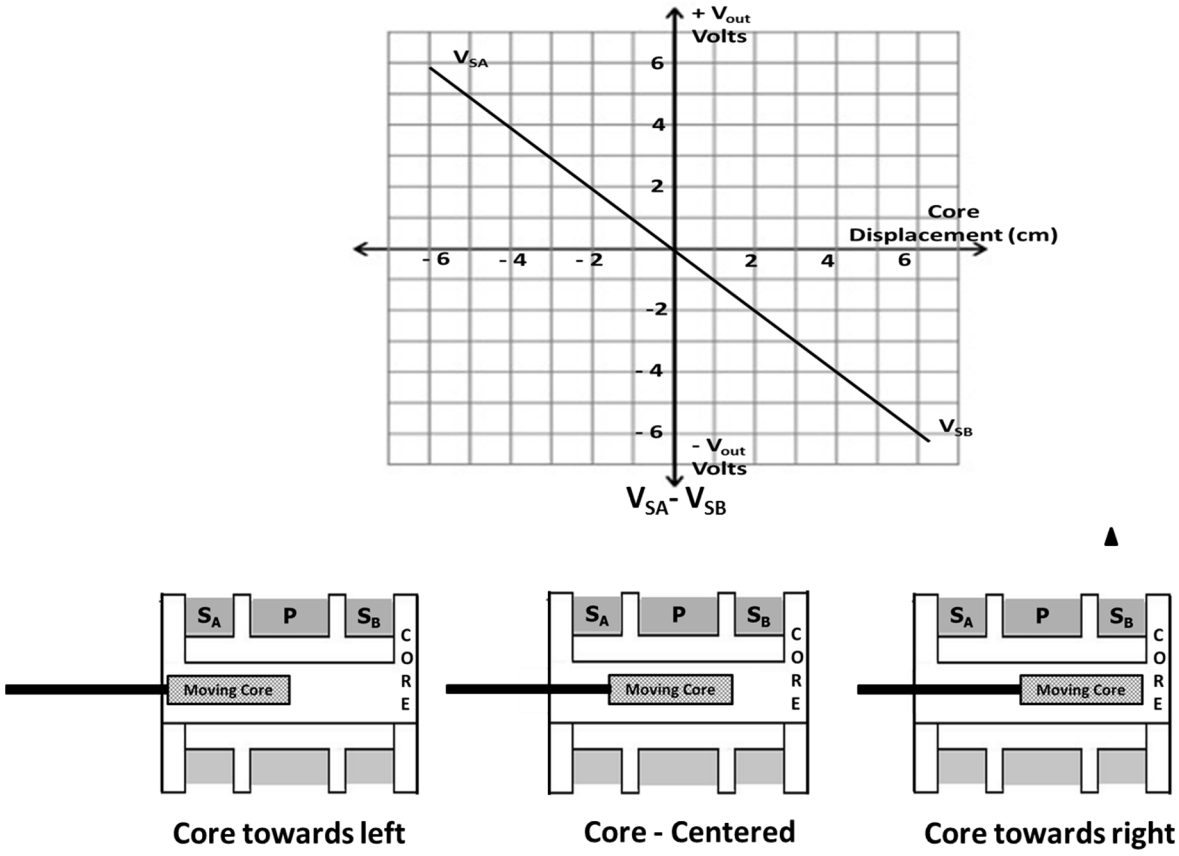


Fig 11.9 LVDT Performance -- Output versus Input

- Thus the pressure variation results in voltage variations