Digital Basics
—part I

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Digital electronics has hit amateur radio—and hobby electronics in general—in a big way! This field of electronic endeavor was once the province of a few freaky computerniks, military electronics technicians, and industrial electronics types, but today, *none* of us can safely ignore digital electronics.

Digital electronics is, in a way, actually simpler than conventional analog electronics because the digital logic devices recognize only two states, i.e., ON and OFF. This fact makes digital circuits similar to relays and mechanical switches. Simple, huh? In fact, some digital circuits are little more than high-frequency electronic versions of simple switches. It is my opinion that anyone who can understand simple relay and switch circuits also can understand the basics of digital electronics! Certainly anyone who can understand the vagaries of single-sideband and FM communications equipment will be able to understand digital electronics.

In this three-part series, we will explore the various forms of IC logic elements: gates, flip-flops, and multivibrators. In this first installment, I am going to give some basic definitions, introduce you to the popular IC-device families, and explore the principal forms of logic gates.

Logic States

I have mentioned that digital circuits respond only to two different input states—ON and OFF—which can be called 1 and 0 (after the two permissible digits of the *binary*, i.e., base 2, number system), HIGH and LOW, or (in older textbooks) "true" and "false." These designations are used to refer to two different voltage levels. In this article, I will stick to the HIGH/LOW designation because it will graphically describe what is actually going on in the circuit.

Transistor-transistor logic (TTL) responds to 0 and +5 volts for the two logic levels. If any other voltage levels are used, then the TTL device will either (1) fail to work, (2) work unpredictably, or (3) burn out (ZZZAPPP!).

Fig. 1 shows the TTL logic levels.

Positive and Negative Logic

You may sometimes hear the terms positive logic and negative logic. These terms sometimes tend to confuse the newcomer; they mean nothing more than how the HIGH and LOW *logic states* are related to *voltage levels*. In *positive logic*, the HIGH is logical 1 and will be a positive voltage (e.g., +5 volts in the case of TTL). The LOW, logical 0, is the 0-volts condition (e.g., in TTL). Logical 0 may be a negative voltage in some CMOS circuits. In *negative logic* these designations are reversed (i.e., HIGH = logical 0 and LOW = logical 1). In the vast majority of uses, positive logic is specified. In fact, the descriptive names given to digital IC devices reflect a bias toward positive logic. This potential confusion is why I prefer HIGH/LOW designations. The 1/0 designation

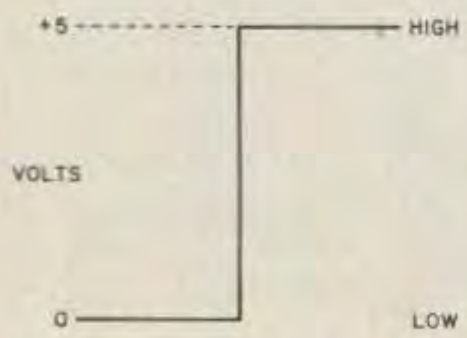

Fig. 1. TTL logic levels: 0 volts is LOW, 5 volts is HIGH.

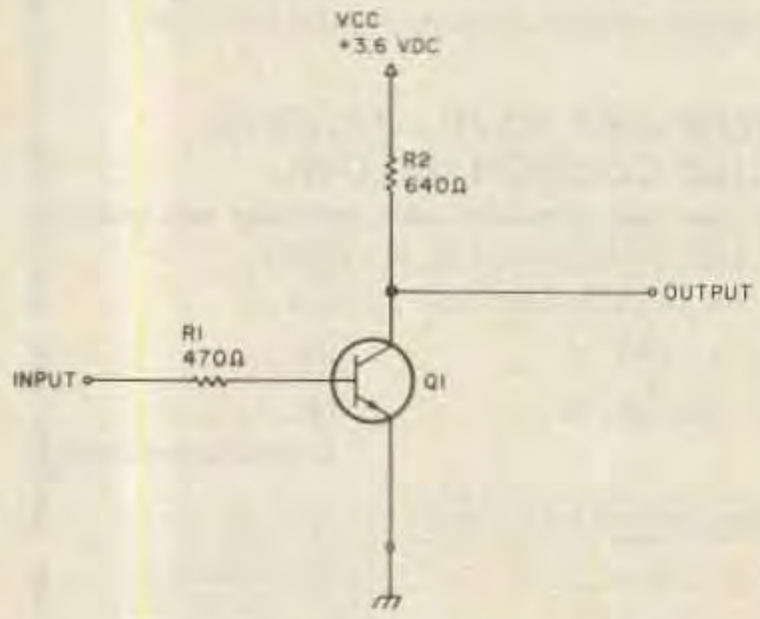

Fig. 2. This typical RTL (resistor-transistor logic) inverter circuit produces a LOW output when the input is HIGH. A LOW input is accompanied by a HIGH output. For RTL, 0 volts is LOW and 3.6 volts is HIGH.

will be reserved for the illustrations and truth tables... but keep in mind that *positive logic* is used unless otherwise noted.

Logic Families

A *logic family* is a series of IC devices that may easily be interconnected and which use similar technology in their construction. All of the devices within a given family will have the same input and output circuits, so that direct interconnection is possible.

The only major consideration is whether an output can supply sufficient current to drive all of the inputs that are connected to it. But in any given logic family, output voltage and current levels and input voltage and current requirements are fixed by agreement. They are defined in terms of units of *fan-in* and *fan-out*. This unit is the current requirement of a single standard input at the fixed voltage level. Such an input has a fan-in of *one unit*. If an IC is said to have a fan-out of, say, five, it will *drive five standard inputs*. The device, therefore, can supply sufficient current to drive all five inputs satisfactorily. The total fan-in of all devices connected to any output must be equal to, or less than, the rated fan-out of the output.

The logic families which we will consider are: RTL, DTL, TTL, HTL, ECL, and CMOS. Of these families, CMOS and TTL are the most popular today; RTL and DTL are obsolete and no longer used in new designs. Plenty of older equipment still in use, however, contains RTL and DTL devices.

Speed vs. Power

The principal factors governing the speed (i.e., maximum operating frequency) of a digital IC are the internal resistances and capacitances. If resistances are increased so that power consumption drops, then the RC time constant of the device is longer. Long RC time constants mean slower operating speeds. As a general rule, higher-speed logic families require greater power consumption. CMOS devices, which require very little current (hence are low power), operate well only to 4 or 5 megahertz (MHz), with some devices tooting along to 10 MHz. TTL devices, on the other hand, usually work to 18 or 20 MHz, with some devices operating to well over 80 MHz.

RTL Devices

Resistor-transistor logic (RTL) is an obsolete logic family that was popular in the early to mid-60s. Fig. 2 shows a typical RTL inverter circuit, i.e., a circuit that produces a LOW output when the input is HIGH and a HIGH output when the input is LOW.

RTL logic IC devices used 0 volts for logical 0 and +3.6 volts for logical 1. If the input of the RTL inverter is grounded (i.e., placed LOW), then the output voltage will be HIGH, which in this case means +3.6 volts. But, if the input voltage is +3.6 volts, then the output will be 0 volts.

RTL devices usually carry type numbers in the uL900 range (mostly 8- and 10-pin metal cans) and MC700 series (mostly 14-pin DIPs).

DTL Devices

The next popular IC logic family was the diode-transistor logic (DTL) family. These devices operated at speeds greater than most RTL devices. Fig. 3 shows a typical DTL inverter.

When the DTL input is HIGH, diode D1 is reverse-biased. In that condition, R1 will forward-bias transistor Q1, which in turn forward-biases D2 and Q2. Voltage levels in most digital circuits are selected to *saturate* the transistors, so when Q2 is turned on, it is turned on to full saturation.

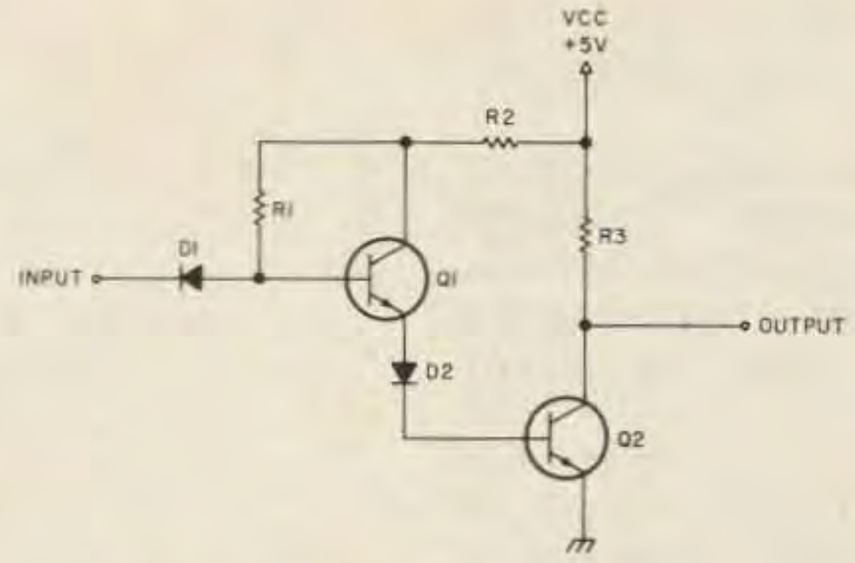

Fig. 3. DTL (diode-transistor logic) offers better speed than RTL. A typical DTL inverter is shown here.

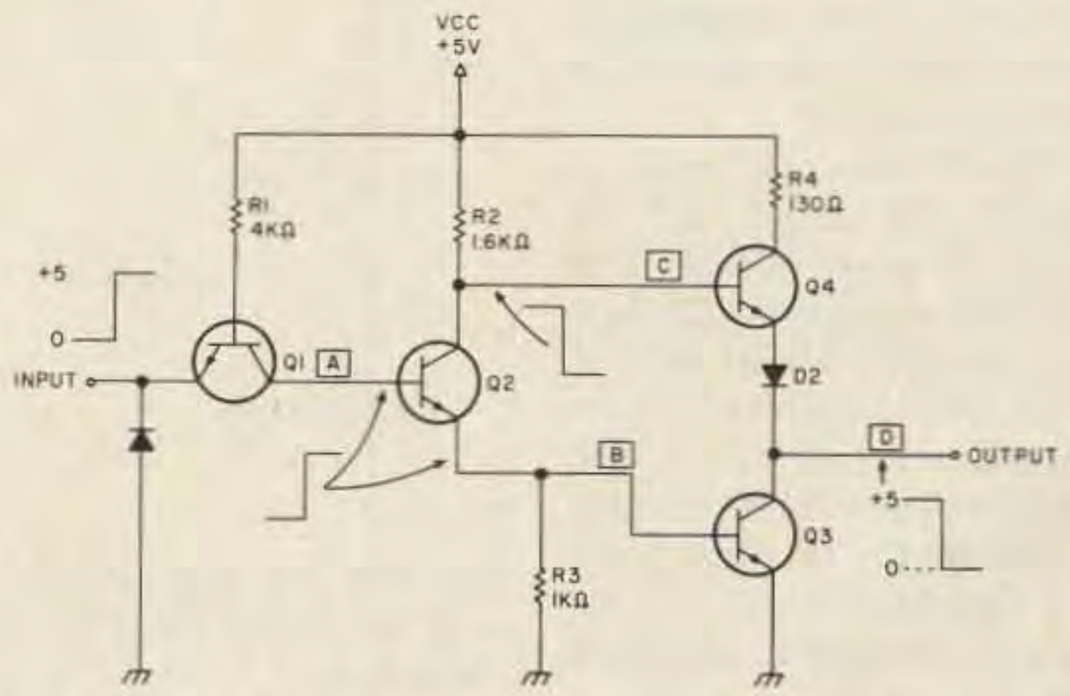

Fig. 4(a). The TTL (transistor-transistor logic) family has LOW values ranging from 0 to 0.8 volts. HIGH is 2.4 to 5.0 volts. An inverter is shown here.

This condition means that the output of the inverter, which is the collector terminal of Q2, goes nearly to ground. The actual voltage $V_{ce(sat)}$ of the transistor is on the order of a few tenths of a volt at most.

When the input is LOW, the cathode of D1 is grounded. Since D1 is now forward-biased, the base of Q1 is essentially grounded. Under this condition, Q1, D1, and Q2 are reverse-biased. With Q2 cut off, then, the output voltage rises to that of Vcc (+). Most DTL devices carry part numbers in the MC800 and MC900 ranges (Motorola designation).

TTL Devices

Probably the most widely used digital IC logic family is the transistor-transistor logic (TTL) family. When most people speak of digital ICs, it is the TTL family of devices to which they refer. Most TTL devices carry type numbers in the 7400 range. (Those devices in the 5400 range are military equivalents to the 7400-series, i.e., a 5447 is a 7447 in uniform. The principal difference between the 5400 and 7400 devices is in the operating temperature range—0 to 80° C for com-

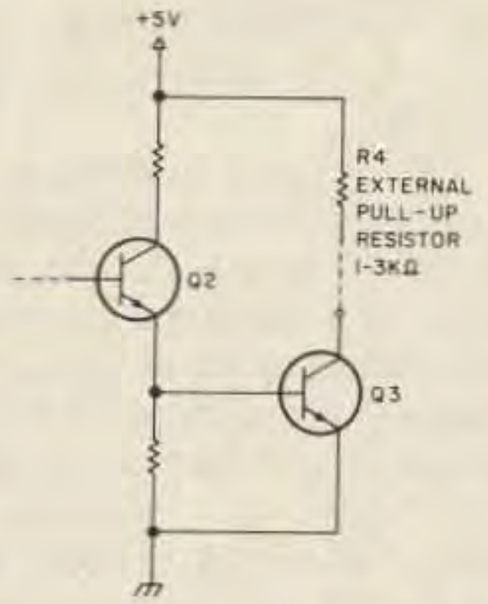

Fig. 4(b). An open-collector TTL circuit results when the output circuit is simplified. An external resistor is needed between the output and +5 volts.

mercial devices and −55 to +125° C for military devices.)

Fig. 4(a) shows the circuit for a typical TTL inverter IC. Like the DTL device, the TTL input acts as a *current source* while the output acts as a *current sink*. The typical TTL input will source 1.8 mA and will be LOW if the voltage is 0 to 0.8 volts and HIGH if 2.4 to 5.0 volts are applied. Performance at values of input potentials between 0.8 and 2.4 volts is not defined, so operation of the devices is unpredictable.

When the TTL input is HIGH, Q1 is cut off, so point A goes HIGH. This condition turns on Q2, forcing point B HIGH and C LOW. We find, then, Q3 is turned on and Q4 is off. This forces the output LOW. Again, the transistors are operated either totally cut-off or totally saturated-on.

If the input is LOW, then exactly the opposite situation occurs: Q1 is turned on (forcing point A LOW), Q3 is off, and Q4 is turned on, i.e., it is connected to Vcc(+).

TTL devices must have a regulated dc power supply of +4.75 to +5.25 volts. In fact, there are some circuits of combinations of devices that require a more limited range of voltages nearer to +5 volts dc. Voltages greater than +5.25 volts often result in a high failure rate of TTL devices.

Some TTL devices are described as being *open-collector* devices. These are essentially the same as regular TTL devices except that the output circuit is modified, i.e., Q4 and D2 are missing. An example of an open-collector circuit is shown in Fig. 4(b). These devices require an external 1k- to 2k-Ohm resistor between the output terminal and the 5-volt dc power-supply line.

Open-collector devices can be useful if you need to tie the outputs of two or more gates together or if you are driving something other than TTL.

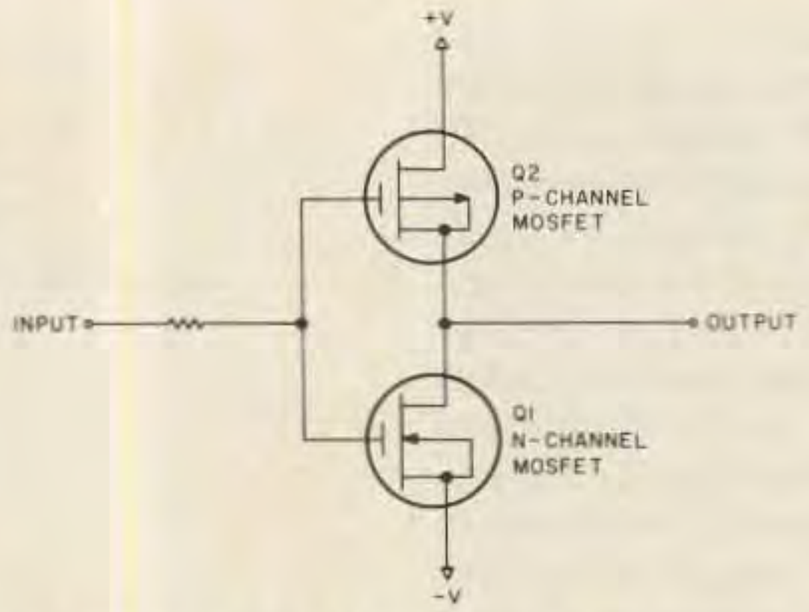

Fig. 5(a). A typical CMOS inverter circuit.

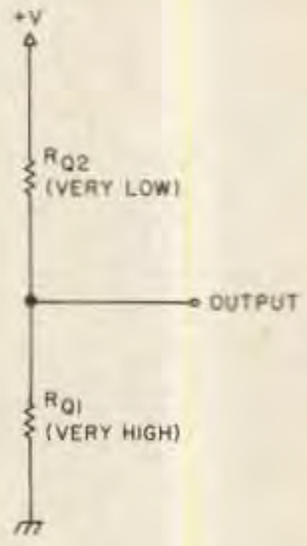

Fig. 5(b). An equivalent circuit for LOW input, HIGH output.

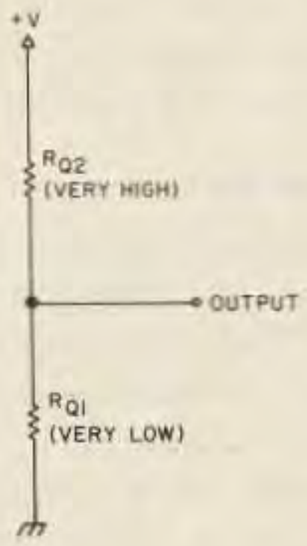

Fig. 5(c). An equivalent circuit for HIGH input, LOW output.

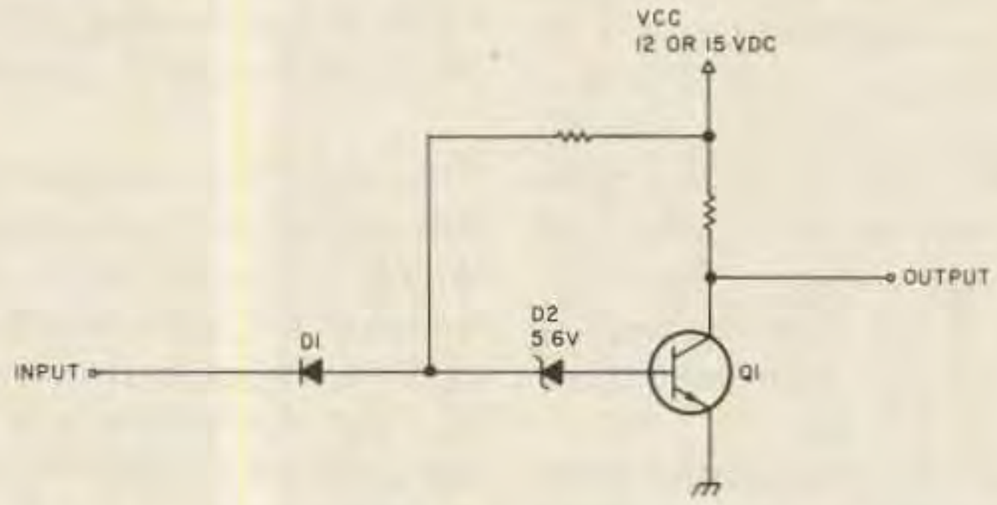

Fig. 6. HTL (high-threshold logic) is useful in applications where noise pulses may be a problem.

CMOS Devices

CMOS IC devices use MOSFET transistors instead of the PNP or NPN bipolar transistors that are used in other logic families. CMOS inputs, therefore, offer a very high impedance. Fig. 5(a) shows a typical CMOS inverter circuit. Note that this family is called *complementary* because the output circuit consists of a complementary pair of MOSFET transistors, i.e., an n-channel and a p-channel in series.

CMOS circuits work over a wide range of voltages, with most devices using a LOW of 0 to 1 volt and a HIGH between 3 and 15 volts. The optimum power supply and HIGH value is usually between 9 and 12 volts. In some instances, a bipolar supply may be used.

CMOS outputs are not directly TTL-compatible, although some specific ICs in the CMOS line are designed to have a TTL-output stage (e.g., the 4049 and 4050 devices). These TTL-compatible devices are often used to directly interface CMOS and TTL devices.

Figs. 5(b) and 5(c) show the equivalent circuits for a CMOS inverter in both possible input conditions, i.e., input HIGH and input LOW. Recall that a p-channel MOSFET turns on when the gate is LOW, while the n-channel device turns on when the gate is HIGH.

Fig. 5(b) shows the situation in which the input is LOW. Transistor Q1 will have a very low (e.g., 200 Ohms) channel resistance. In this case, the output is equivalent to a 200-Ohm resistor to the V+ power-supply line.

In Fig. 5(c), we see the situation in which the input is HIGH. Transistor Q2 now has a very high channel resistance, and Q1 has a very low channel resistance (again, about 200 Ohms). In this case, the output looks like a 200-Ohm resistance to ground, so the output is LOW.

The CMOS ouput stage always looks like a high and low resistor in series across the power supply—see Figs. 5(b) and 5(c). The overall current drain, therefore, is very small.

But CMOS devices do have a problem: They contain MOSFETs, so they are sensitive to static electricity. All A-series CMOS devices (e.g., the 4001A) have this problem, but it is less severe in B-series (e.g., the 4001B) devices. The B-series have built-in diode gate-protection to bypass high static potentials around the sensitive gate structure. Even so, they should be handled with care.

HTL Devices

Noise pulses often are seen by logic circuits as valid input pulses. This problem is especially bothersome in high-speed TTL devices that are normally able to pass high-frequency, short-duration pulses. The solution in noisy environ-

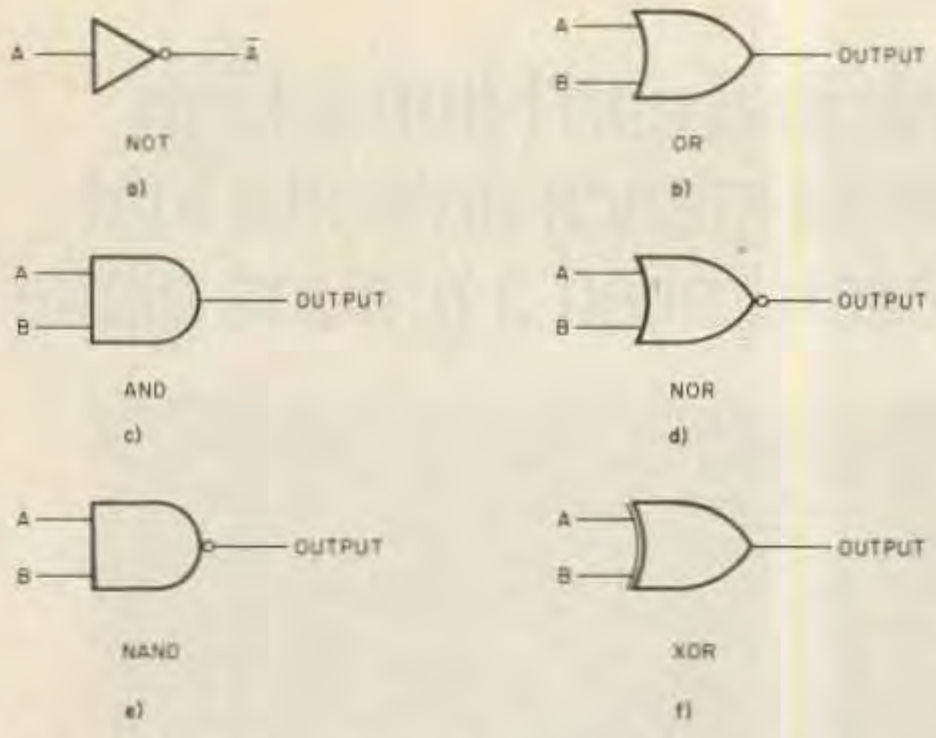

Fig. 7. You can determine the function of a TTL gate by looking at its schematic symbol.

ments is to use a digital IC logic family that requires a high input voltage to trigger. CMOS devices operated at high V− and V+ values meet this requirement, but the older bipolar *high-threshold logic* (HTL) may also be used (Fig. 6).

HTL (also sometimes called *high-noise-immunity logic*, or HNIL) uses V+ values of 12 or 15 volts depending upon the series. As a result, the logic levels also are high, so it requires a bigger noise pulse to cause trouble.

Emitter-Coupled Logic

Up until now we have been talking about *saturated* logic families, i.e., the transistors in the ICs are either all the way on or all the way off (cut off or saturated). *Emitter-coupled logic* (ECL) is called an ac logic family because the transistors are operated in a nonsaturated mode. As a consequence, ECL devices are capable of very fast operation. Most commonplace ECL devices operate to 80 or 120 MHz, while some costly special devices operate to over 1 GHz (that's 1000 MHz!). The usual *prescaler* for a digital frequency counter is nothing more than an ECL frequency divider that divides the 500-MHz input signal down to 50 MHz.

Note that it is necessary to use VHF/UHF circuit design and layout techniques when working with ECL devices. The very high frequencies used are, after all, in the UHF range.

Gates

A digital electronic *gate* is a circuit whose output is HIGH or LOW depending on the input. Gates operate under a set of well-defined rules. The basic forms of digital electronic gates are: NOT, OR, AND, NOR, NAND, and XOR (Exclusive-OR). In the paragraphs to follow, we will discuss all of these basic gates.

NOT Gates

NOT gates, also called *inverters*, produce an output that is the opposite of the input signal. Recall that digital circuits respond only to HIGH and LOW voltage levels. In an inverter circuit, therefore, the output will be HIGH when the input is LOW and LOW when the input is HIGH.

The circuit symbol for the inverter is shown in Fig. 7(a), while the truth table is given in Fig. 8(a). Note that any digital symbol with a *circle* on the output produces an *inverted* output. Similarly, if one or more inputs has a circle on it, then that input is inverted. The rules for the operation of the inverter are:

1) A HIGH on the input produces a LOW output.

2) A LOW on the input produces a HIGH output.

OR Gates

An OR gate will be HIGH if any of its input is HIGH. The symbol for an OR gate is shown in Fig. 7(b), while the truth table is given in Fig. 8(b). The truth table shows the rules of operation for the two-input OR gate, and these are summarized below:

1) If both inputs A and B are LOW, then the output is LOW.

2) If either input A or B is HIGH, then the output is HIGH.

3) If both inputs A and B are HIGH, then the output is HIGH.

AND Gates

The AND gate is the opposite of the OR gate. The AND gate produces a HIGH output only when *all* inputs also are HIGH. The circuit symbol for the AND gate is given in Fig. 7(c), and the truth table is shown in Fig. 8(c). The rules for the operation of the two-input AND gate are:

1) If both inputs A and B are LOW, then the output is LOW.

2) If either input A or B is LOW, then the output is LOW.

3) If both inputs A and B are HIGH, then the output is HIGH.

NOR Gates

The NOR gate is a combination of a NOT gate (inverter) and an OR gate, hence the designation NOR, which means NOT/OR. It is, therefore, an OR gate with an inverted output. The NOR gate is, in fact, sometimes represented in textbooks as an OR gate with an inverter following. The NOR gate symbol, shown in Fig. 7(d), is an OR gate symbol with the circle denoting inversion at the output. The truth table for the two-input NOR gate is shown in Fig. 8(d), and the rules for its operation are summarized below:

1) If both A and B inputs are LOW, then the output is HIGH.

2) If either input A or B is HIGH, then the output is LOW.

3) If both inputs A and B are HIGH, then the output is LOW.

NAND Gates

The NAND gate is a NOT/AND gate, i.e., an AND gate followed by an inverter. The symbol for the NAND

(a) NOT

Input	Output
1	0
0	1

(b) OR

Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	1

(c) AND

Input A	Input B	Output
0	0	0
0	1	0
1	0	0
1	1	1

(d) NOR

Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	0

(e) NAND

Input A	Input B	Output
0	0	1
0	1	1
1	0	1
1	1	0

(f) XOR

Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0

Fig. 8. Understanding a truth table is the key to using logic devices. The 1 designates a HIGH state and the 0 designates a LOW one.

gate is shown in Fig. 7(e). This symbol is the AND gate symbol with the circle at the output to denote inversion. The truth table for the two-input NAND gate is shown in Fig. 8(e), and the rules are presented in summary below:

1) If both A and B inputs are LOW, then the output is HIGH.

2) If either input A or B is LOW, then the output is HIGH.

3) If both A and B are HIGH, then the output is LOW.

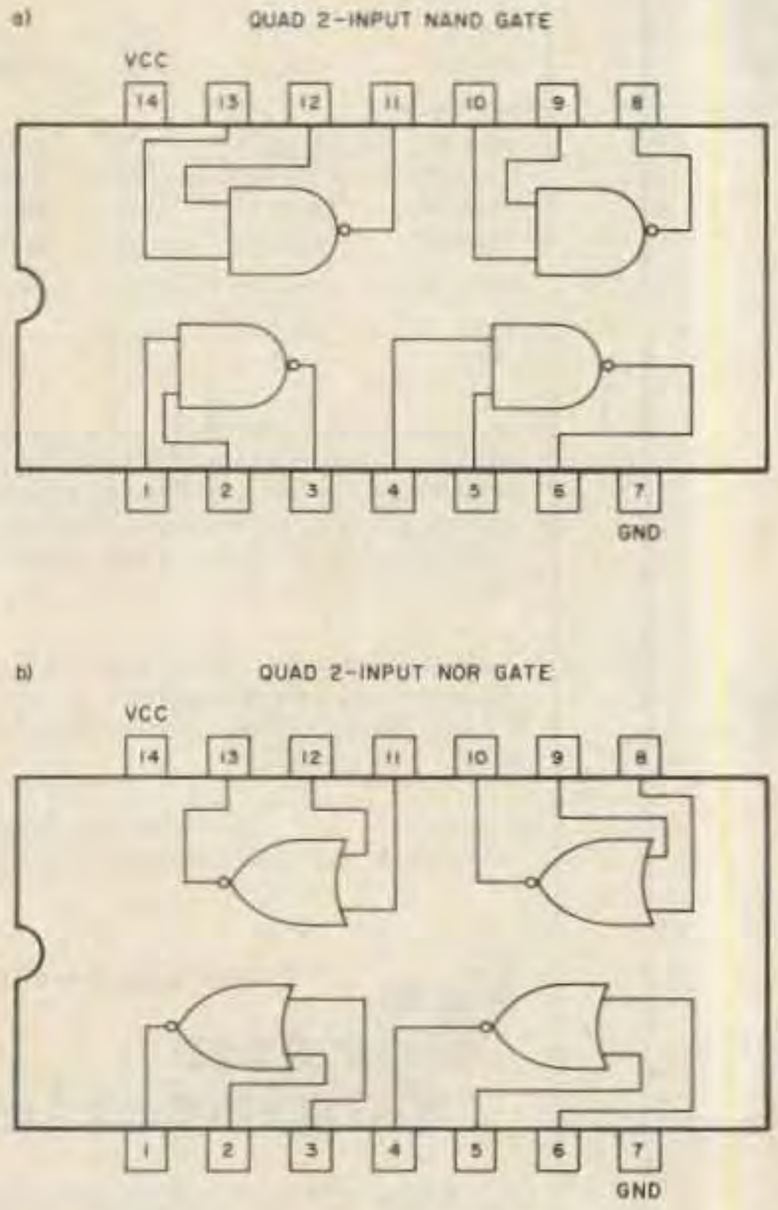

Fig. 9. A chip may contain as many as six individual gates.

XOR Gates

An Exclusive-OR (XOR) gate is like the OR gate discussed earlier except that it will have a LOW output if more than one of its inputs is HIGH. For a HIGH output, there must be one exclusive HIGH input. The XOR gate symbol, shown in Fig. 7(f), is a modified OR gate symbol. The XOR operation is summarized by the truth table in Fig. 8(f) and the rules below:

1) If A and B are both LOW, then the output is LOW.

2) If A is HIGH and B is LOW, then the output is HIGH.

3) If B is HIGH and A is LOW, then the output is HIGH.

4) If A and B are both HIGH, then the output is LOW.

TTL and CMOS Examples

Earlier in this article, I introduced you to several different families of IC digital-logic devices. Of these, several are considered obsolete, so they will not be discussed further. The TTL and CMOS families, however, are very much alive and form the basis of most digital projects today.

TTL/CMOS NAND Gates

In the TTL IC logic family, the most popular NAND gate (and probably the most popular IC) is the 7400 (see Fig. 9). This device contains four two-input NAND gates and usually sells for less than 25¢—or around six cents per gate. Each of the four NAND gates in the 7400 package is an independent entity, but shares the common power supply and ground connections (pins 14 and 7, respectively).

The 7401 and 7403 are similar to the 7400 except that they are open-collector devices. This means that pull-up resistors are needed, i.e., one 2k- to 4k-Ohm resistor from each output to the +5 volt line.

The 7430 is an eight-input NAND gate (one per 14-pin DIP package). The 7430 device, therefore, has eight distinct inputs . . . and all eight must be HIGH before the output drops LOW. If any one of the eight inputs remains LOW, then the output stays HIGH. Since most microcomputers today are eight-bit machines, the 7430 is often used as an address, or I/O port, decoder.

The 7410 and 7420 are three- and four-input TTL NAND gates, respectively.

In the CMOS line, we also have several different types of NAND gates. The 4011 is a quad two-input NAND gate that is reminiscent of the 7400. The 4012 device is a dual four-input NAND gate. All four inputs of either gate must be HIGH for the respective output to be LOW. The 4023 device is a triple three-input NAND gate, while the 4068 is an eight-input NAND gate.

TTL/CMOS NOR Gates

The 7402 TTL NOR gate is by far the most common example from the TTL line and is almost as popular as the 7400 device. The pinouts for the 7402 are shown in Fig. 9(b)—see 9(a) for pinouts for the 7400, for comparison. Note that the pinouts of the 7400 and 7402 are different, as are their logical responses.

And Now . . .

We have just gotten our toes wet in the study of digital electronics. In part II, we will progress a little further: We will be up to our ankles in flip-flops. For now, however, you have sufficient information to begin experimenting with flip-flops. ■